Shew Juan, Kok

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Professional Summary

Experienced ASIC Design Engineer with expertise in SoC architecture, front-end design flows, and functional verification. Proven track record in HDL coding, code coverage analysis, constraint-random verification, synthesis, DFT implementation and early back-end design explorations. Currently exploring the integration of AI agents, AI workflows, Model Context Protocol (MCP), and Retrieval-Augmented Generation (RAG) to develop fully automated workflow systems for chip design. Eager to apply extensive hardware experience to pioneering roles in AI-integrated ASIC development, focusing on leveraging AI agents and advanced automation to accelerate the future of chip design.

Work Experience

ASIC DESIGN ENGINEER | AION SILICON | READING, UK | *SEP,2023-PRESENT*

- Automated front-end design flows using Python, TCL, and Shell scripting, significantly reducing manual effort and improving design cycle efficiency
- Led front-end design initiatives using SystemVerilog for complex IP and SoC projects, driving development from architectural specification through to implementation.
- Executed comprehensive functional verification plans using constrained-random methodologies and assertions to ensure designs met rigorous specification requirements.
- Managed DFT implementation for large-scale, ASIL-B compliant SoCs, developing and debugging ATPG patterns with Synopsys TestMax to achieve over 90% test coverage.
- Established and integrated a company-wide linting methodology using Synopsys and Siemens tools, enhancing code quality and consistency across all design teams.
- Performed early-stage design exploration for critical subsystems using Synopsys RTL-Architect, optimizing for performance and area to "shift left" the design process with early global placement and routing.
- Designed and architected system-level solutions, including the integration of third-party and in-house IP for advanced SoC implementations.

Education

MASTER OF ENGINEERING (MENG) IN ELECTRICAL AND ELECTRONICS ENGINEERING | 2023 | UNIVERSITY OF SOUTHAMPTON

Skills

HARDWARE DESIGN & VERIFICATION:

- SystemVerilog – RTL coding, constrained random verification, functional verification.
- HDL Design Patterns - Pipelined architectures, FSM implementation, parameterizable IP blocks, consistent RTL coding practices, ECC and redundancy checks for safety-critical implementations.
- IP Design - Created in-house IP and integrated external IP for various SoC design
- Industry Protocols - AMBA AXI/AHB protocols, PCIe, DDR interfaces

EDA TOOLS:

- DFT Tools - Synopsys TestMax for DFT ATPG pattern development and debugging at SoCs level

- Front-end Tools - Synopsys Design Compiler, RTL-Architect, Platform Architect for synthesis and exploration
- Static Formal Tools - Questa Static Formal / VC Spyglass, code quality check and best practices
- Verification Tools - Verdi, VCS, coverage analysis tools and waveform analysis
- Open Source Tools – Verible, Slang, Verilator for self -exploration

SCRIPTING & LANGUAGES:

- Scripting – Python, TCL, Bash
- SystemC - TLM modeling, high-level synthesis
- Rust (Learning)
- Documentation – Markdown

VERSION CONTROL:

- Git and SVN (subversion) for proper team collaboration.

Professional Interests

- Integrating AI agents and RAG-based systems into chip design pipelines for enhanced automation.
- Developing AI-driven specifications and methodologies for advanced chip design workflows
- Building web-based tools and applications for personal productivity and design automation
- Machine learning hardware optimization and neural network implementation architectures
- System-level hardware-software co-optimization for AI-centric applications.
- Exploring advanced verification methodologies and AI-driven automated verification techniques for advanced node technologies

Additional Information

- Requires skilled worker visa sponsorship in the UK
- Strong collaborative and communication skills
- Excellent problem solving skills and proactive learner
- Continuous learning mindset with focus on AI/ML hardware trends