OHO_DY1

USER'S MANUAL

V 1.2

OHO-Elektronik
www.oho-elektronik.de

Author: M.Randelzhofer

OHO-Elektronik

Michael Randelzhofer

Rudolf-Diesel-Str. 8
85221 Dachau
Germany

WEB: www.oho-elektronik.de
EMAIL: info@oho-elektronik.de

Phone: +49 8131 339230
FAX: +49 8131 339294

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1. Table of contents:

2. Introduction

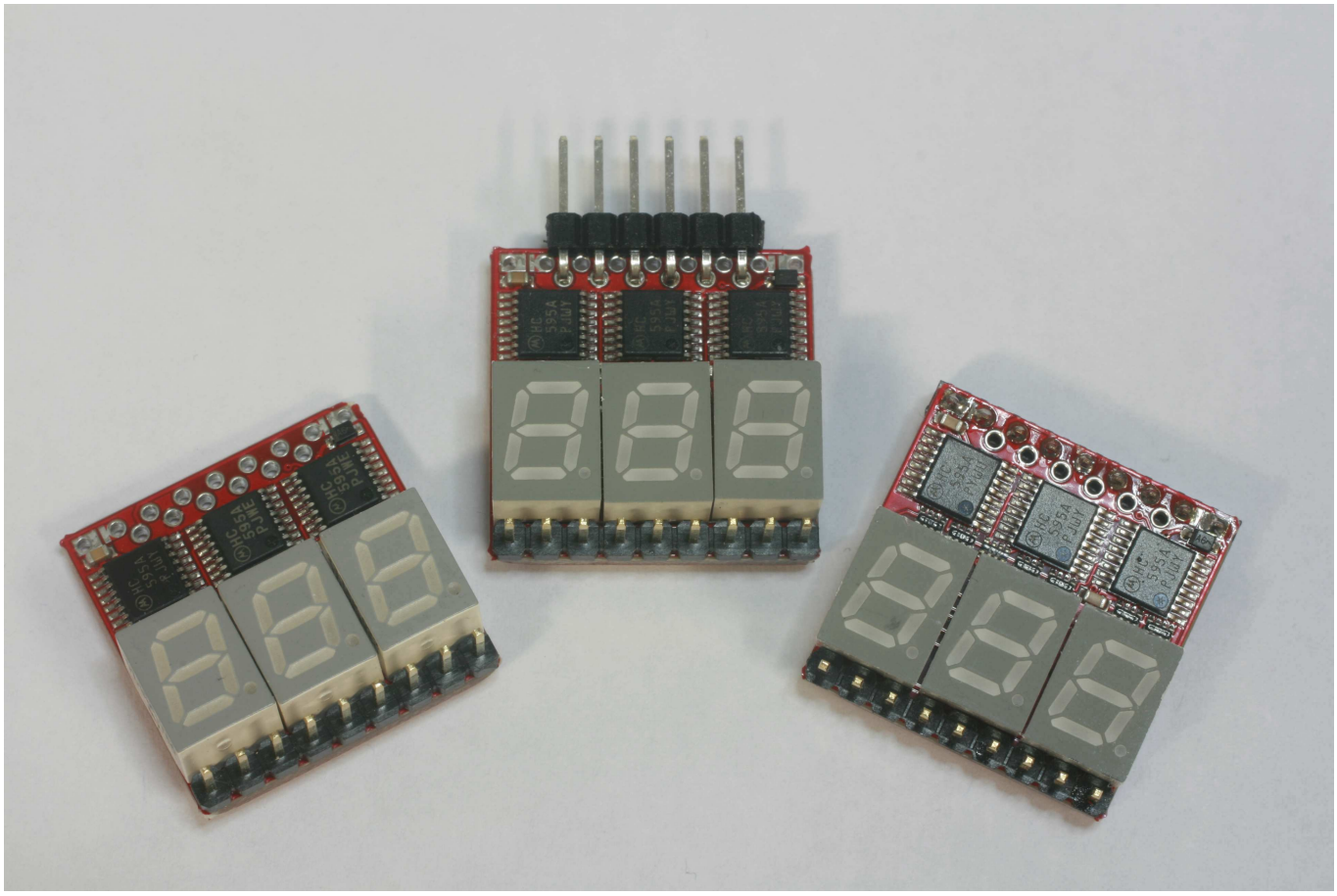
The OHO_DY1 module is a small 23mm x 23mm (0.9” x 0.9”) 7 segment display unit for displaying 3 digits of hex numbers (12 bits) or arbitrary segment combinations including their associated decimal points.
It is primarily intended for debugging or educational use.
The modules can be stacked to extend the number of digits.

A VHDL core is available, to directly display hex numbers on up to 5 stacked OHO-DY1 modules.
Alternatively the modules can be connected to any microcontroller or DSP using only 3 GPIOs.

2.1. OHO_DY1 Features:

- small 3 digit 7 segment display module
- up to 5 stackable modules on the same connector
- 9 pin OHO or 6 pin Digilent compatible interface connector, 3 I/O´s needed
- 9 pin connector can be reduced to 7 pins for use with OHO CPLD modules
- simple SPI like interface
- 3,3V and 5V modules available
- red, green and blue (only on 5V) modules available
- brightness controllable (PWM)
- VHDL core available
- OHO_DY1 modules can be also used on most microcontrollers
- reverse voltage protection

2.2. OHO_DY1 Board Pictures



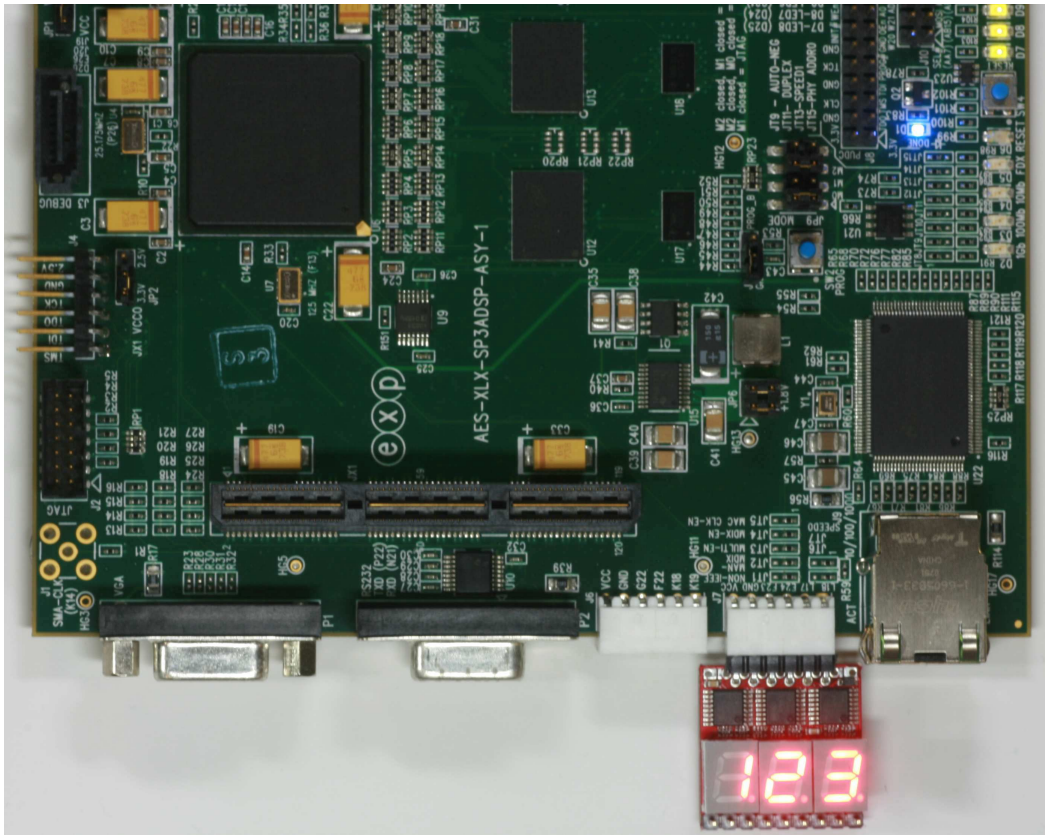
The picture show the three possible connector configurations of the OHO_DY1.
The module in the middle is soldered with a 6 pin connector which fits into the Xilinx Spartan3E and Spartan3A/3AN/3ADSP Starterkits.

On the right side a 9 pin jack is soldered on the bottom side of the display module.
This one can be plugged into the test connector of an OHO CPLD or FPGA module, or stacked into the 9 pin connector under the led display modules of any already plugged OHO_DY1 module.
A maximum of 2 stacked modules is recommended for debugging purposes because of mechanical issues, however 5 modules (max. 15 digits) are supported by the VHDL display core.

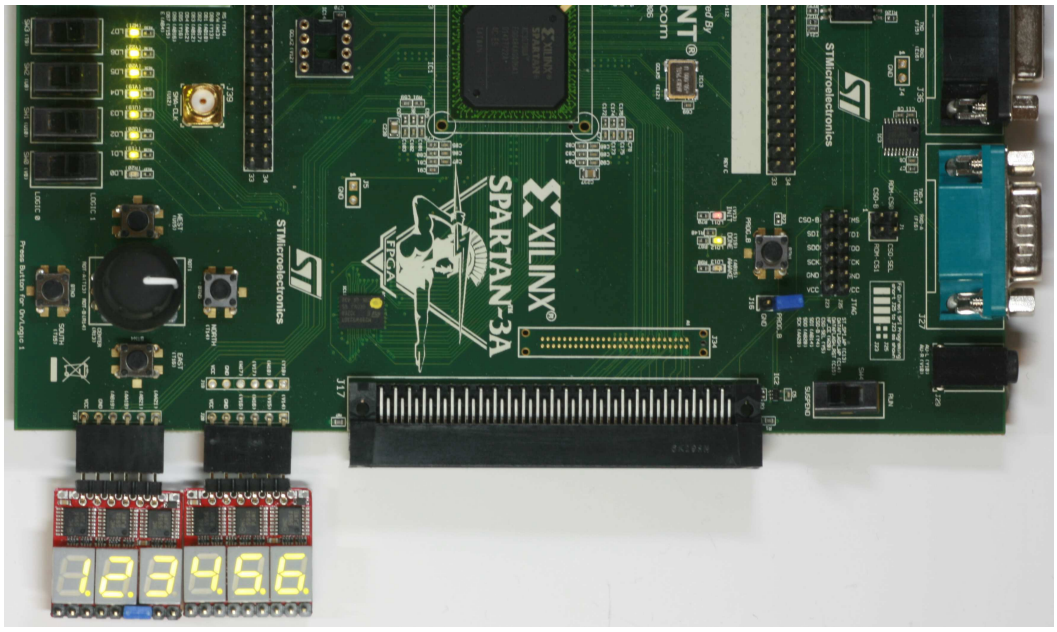
A version without connector, shown on the left side in the picture above, is available for customers who want to use their own hardware.
On the left side, an unsoldered version can be delivered, where the customer can decide which connector he (or she) wants to use.

Please note:
There are modules for 3,3V power supply – normally used in Xilinx Starter Kits, and 5V modules, used for the OHO FPGA and CPLD modules.

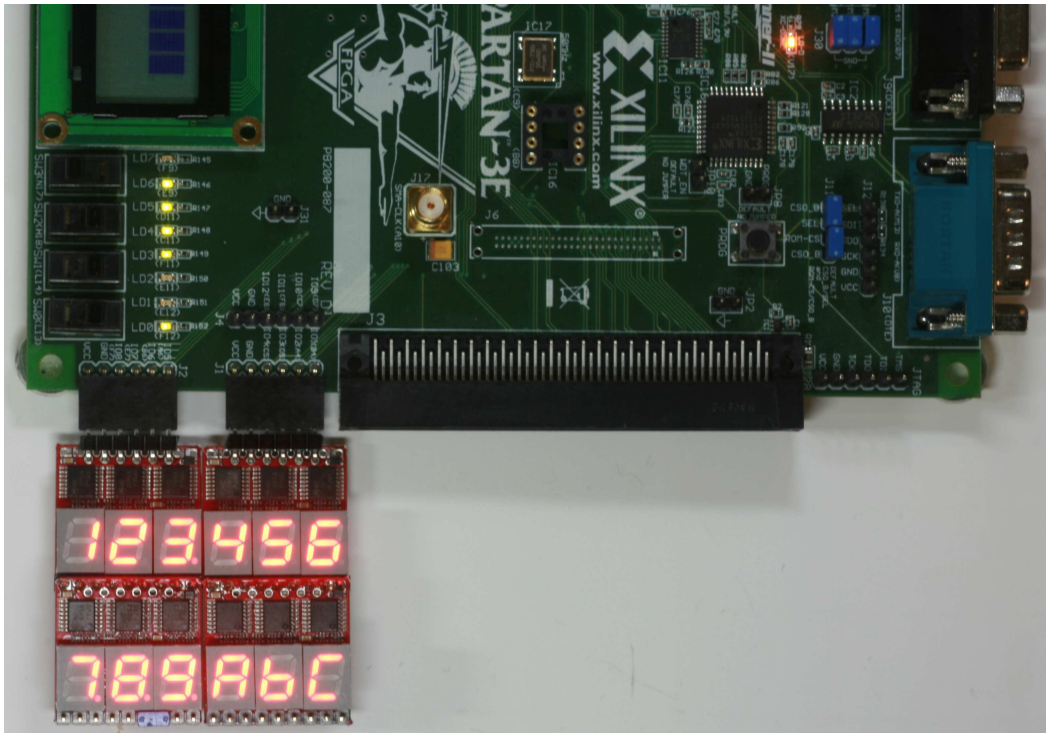
2.3. One OHO_DY1 module on a Xilinx Spartan 3ADSP Starter Kit.



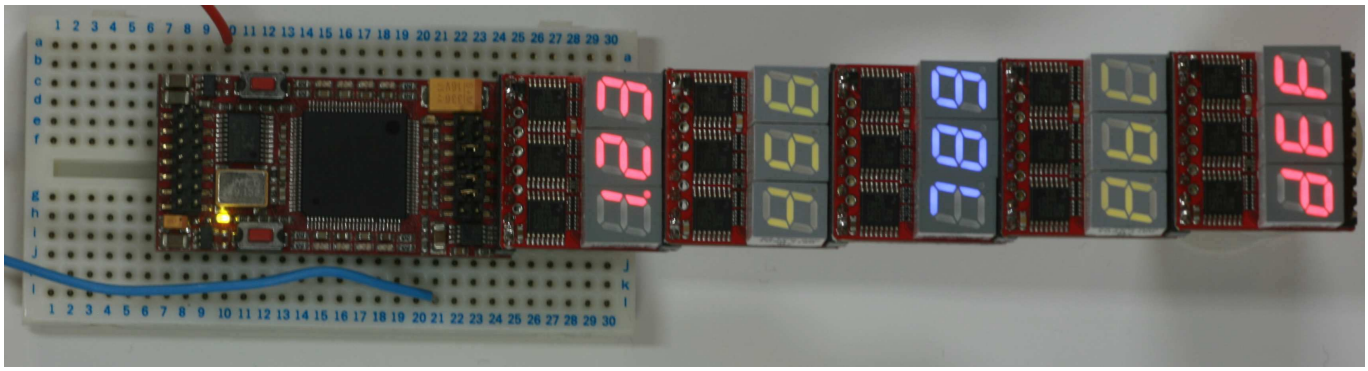
2.4. Two OHO_DY1 modules on a Xilinx Spartan 3A Starter Kit.



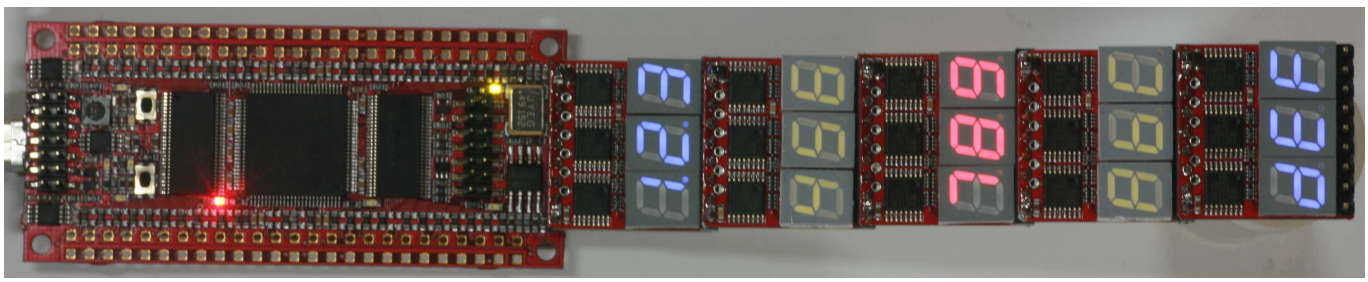
2.5. Four OHO_DY1 modules on a Xilinx Spartan 3E Starter Kit.



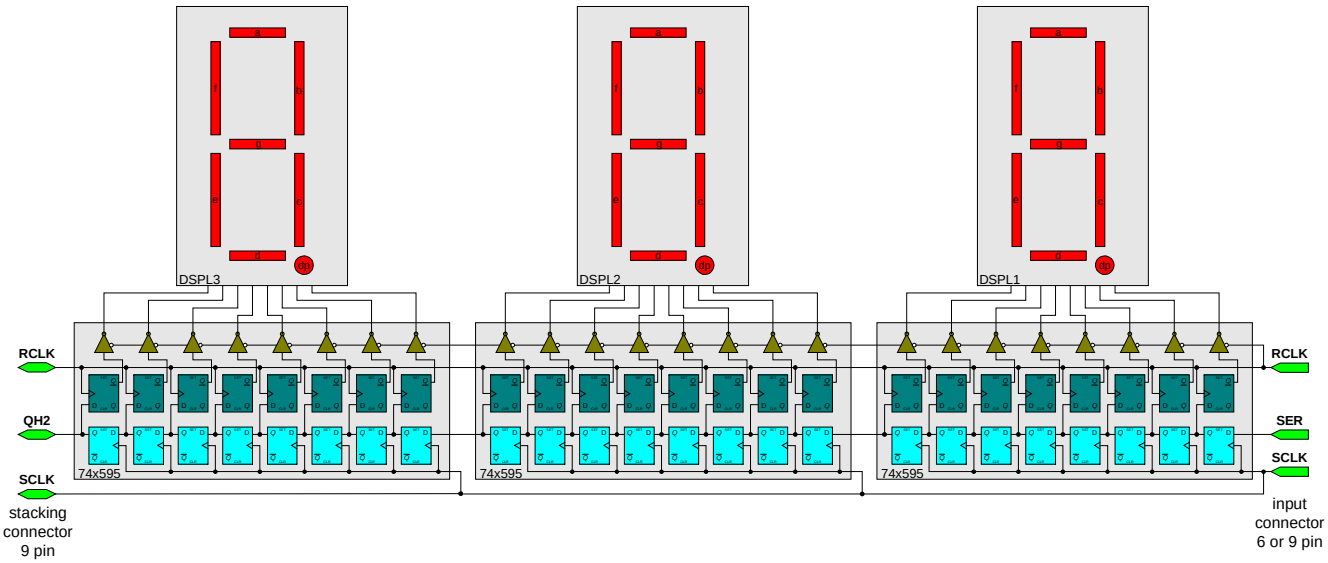
2.6. Five OHO_DY1 modules on an OHO GOP_XC3S200 module.



2.7. Five OHO_DY1 modules on an OHO GODIL48 module.



3. OHO_DY1 Block Diagram



4. OHO_DY1 circuit description

One basic display unit – one digit – consists of a 7 segment led display with a common anode, connected to a 74x595 like shift register with output catch registers. The current limiting series resistor arrays are not shown in the overview (but in schematics of course).
An OHO_DY1 module consists of three digits interconnected as shown in the block diagram.

The shift register parts of the 74x595s are all clocked by SCLK with input data SER on the rising edge of SCLK. SCLK and SER as well as RCLK are routed from the 6 or 9 pin input connector. The 74x595s are chained from right to left, forming a 24 bit shift register. The output of the first 74x595 on the right side is fed to the middle 74x595, which feeds its output to the left 74x595, which offers its output QH2 on the 9 pin stacking connector on pin6.

Since the 7 segment displays uses a common anode, a ´0´ on the input data is needed to light up a segment (input data on SER has to be inverted) .

The module SCLK clock and the SER input data can be seen as the module SPI clock with its data input clocked on the rising edge. A microcontroller SPI peripheral can be used to drive these signals.

However also software bit banging is reasonable; SCLK can be as high as about 10 MHz on 3,3V modules or about 15 MHz on 5V modules, thus no software delays should be necessary for the display update function loop. See datasheets of 74HC595 for 3,3V and 74AHCT595 for 5V modules, but consider that the clock and data signals are not terminated on the modules itself, so frequencies have to be derated. Please note that these frequecies must be derated again for stacked modules.

The common catch register clock of the 74x595s (RCLK) is connected to the output enables of all 74x595s, thus display update is coupled with display enable. This allows for brightness control by pulse width modulation (PWM) with a reduced pin count.
The display is updated by a rising edge on RCLK.
The display is enabled by a logical ´0´ and disabled by a logical ´1´ on RCLK.

The signals RCLK, SCLK and QH2 are connected to the 9 pin stacking connector, so with adding another module, the block diagram is effectively extended to the left with n x 3 digits, where n is the number of stacked modules.

The 3,3V version of the OHO_DY1 module uses a 74HC595 device with appropriate series resistors for the LED 7 segment displays.
It can be used for Xilinx Starter Kits with a 6 pin Digilent compatible connector, or with OHO CPLD and FPGA modules with a 9 pin connector running from 3,3V-3.5V.
Any microcontroller or other device with 3,3V levels can also be used, the connector used is up to the user´s choice. The module must be powered from 3,3V.

The 5V version of the OHO_DY1 module uses a 74AHCT595 device with appropriate series resistors for the LED 7 segment displays. The 74AHCT595, yet powered from 5V accepts 3,3V and 5V logic levels.
It can be used for OHO CPLD and FPGA modules with a 9 pin connector running from 5V.
Any microcontroller or other device with 3,3V or 5V levels can also be used, the connector used is up to the user´s choice. The module must be powered from 5V.

Table of orderable configurations/options:

Label code	**Suitable for**	**Comment**
5ggg0	OHO 5V FPGA and CPLD modules	A 5V display module with 3 green led display digits
5ggg1		Schottky diode PMEG2020EJ assembled
5ooo1		A 5V display module with 3 orange led display digits
5bbb0		A 5V display module with 3 blue led display digits
3rrr0	Xilinx Starterkits	A 3,3V display module with 3 red led display digits
3rrr1		Schottky diode BAT54HTG1 assembled
3ggg1		A 3,3V display module with 3 green led display digits

The label code consists of 3 parts:

- the first digit is 3 or 5 for the supply voltage 3,3V or 5V
- the next 3 digits show a colour code for every digit from left to right
- the last digit is an internal manufacturing version code for reference

5. OHO_DY1 Vhdl core

5.1. OHO_DY1 core interface signals:

Signal name	Direction	Length	Function
dy_clock	input	1	core clock, 10-125MHz recommended
dy_rst_n	input	1	core reset, negative active
dy_data	input	array 15 x 9	user defined array data type, 15 digits x std_logic_vector(8 downto 0) dy_data(0) is first (right) digit of first module, dy_data(1) is second (middle) digit of first module, dy_data(2) is third (left) digit of first module, dy_data(3) is first digit of second module, dy_data(4) is second digit of second module, dy_data(5) is third digit of second module, dy_data(6) is first digit of third module, dy_data(7) is second digit of third module, dy_data(8) is third digit of third module, dy_data(9) is first digit of fourth module, dy_data(10) is second digit of fourth module, dy_data(11) is third digit of fourth module, dy_data(12) is first digit of fifth module, dy_data(13) is second digit of fifth module, dy_data(14) is third digit of fifth module, one 9bit word is defined in the next table
dy_update	input	1	display update, ‘1’ updates display continuously, and allows PWM brightness control a single clock pulse ‘1’ or longer pulses updates the display only for one or DupVal (see ohopack.vhd) times, max brightness only
dy_frame	output	1	pulse nearly as long as display frame, indicates frame start
dy_frameend	output	1	continuous ‘1’ indicates display frame end
dy_frameend_c	output	1	single clock ‘1’ indicates display frame end
dy_pwm	input	4	“1111” sets max intensity, “0000” lowest, only if dy_update is always set to ‘1’
dy_counter	output	16(32)	main free running binary counter as state machine substitution for display control only the first 16 lower significant bits are used all 32 bits can be used externally as divided clock outputs
dy_sclk	output	1	display module SCLK as described above
dy_ser	output	1	display module SER as described above
dy_rclk	output	1	display module RCLK as described above

5.2. OHO_DY1 core usage

The core can be used quite easily, to display hex numbers only the signals dy_clock, dy_rst_n and dy_data must be provided, see the core examples.
Since the display uses a non multiplexed approach, users may want to update the display after an input data (dy_data) change only.
To do so, a single clock pulse trigger on dy_update starts the display frame update from the actual dy_data array.
Frame end is indicated by the core via dy_frameend and frameend_c.
Please note, that the input data dy_data must be stable up to the end of the display frame.
Even easier is to update the display continuously by setting dy_update to '1', which also allows for PWM brightness control.

5.3. OHO_DY1 core input signal "dy_data" format

One dy_data word is defined as a VHDL std_logic_vector(8 downto 0), so its a 9 bit vector.

The vector can contain an 8 bit raw segment word with all the seven segments of one display digit and an additional decimal point segment.

Alternatively the vector can contain 5 bits, consisting of one 4 bit hex number which will be decoded by the core, plus the decimal point.

dy_data vector part	**polarity**	**Function**
std_logic_vector(8) std_logic_vector(7 downto 0)	'0' inverted data	"raw" display format including decimal point display segments, defined in "ohopack.vhd"
std_logic_vector(8) std_logic_vector(7) std_logic_vector(6 downto 4) std_logic_vector(3 downto 0)	'1' '1' is on, '0' is off - hex code X"x"	"hex" display format decimal point not used display decoded hex number

5.4. OHO_DY1 core examples

There are some example .zip files for the following hardware which demonstrates easily how to use the OHO_DY1 display core:

- Xilinx Spartan 3E Starter Kit
- Xilinx Spartan 3A/3AN Starter Kit
- Xilinx Spartan 3A DSP S3D1800A Starter Platform
- OHO GOP_XC3S200 module
- OHO GODIL48 module

Please note:
Some demos need a jumper from pin6 to pin7 at the stacking connector of the OHO_DY1 module.

5.5. Brief OHO_DY1 core description

The core sends display data to the OHO_DY1 modules in display frames, containing data for 16 display digits (however only 15 digits can be user defined).
One display frame starts with 8x16 = 128 SCLK cycles with its associated display data on SER, and finishes with a pulse containing a rising and falling edge on RCLK.

The main timing generator of the OHO_DY1 core is a simple free running 32 bit binary up counter clocked by the system clock e.g. 50MHz, and is named displaycounter (dy_counter).
The counter is defined as a std_logic_vector as displaycounter(31 downto 0).
Only the lower 16 bits are used by the core to buid a display frame, the upper 16 bits can be used by the user, or is optimized away by the post processing tools.
A display frame starts when all 16 lower displaycounter bits are zero.
A display frame only stops if dy_update is reset to low, and if the internal display update counter decremented to zero.

SCLK is derived from displaycounter (8), system clock divided by 256, about 195kHz @ 50MHz.
In other words, one SCLK low time takes 256 system clocks which corresponds to more than 5us Setup, and one SCLK high time also takes 256 system clocks which corresponds to more than 5us Hold time @50MHz for the interconnected 74x595.

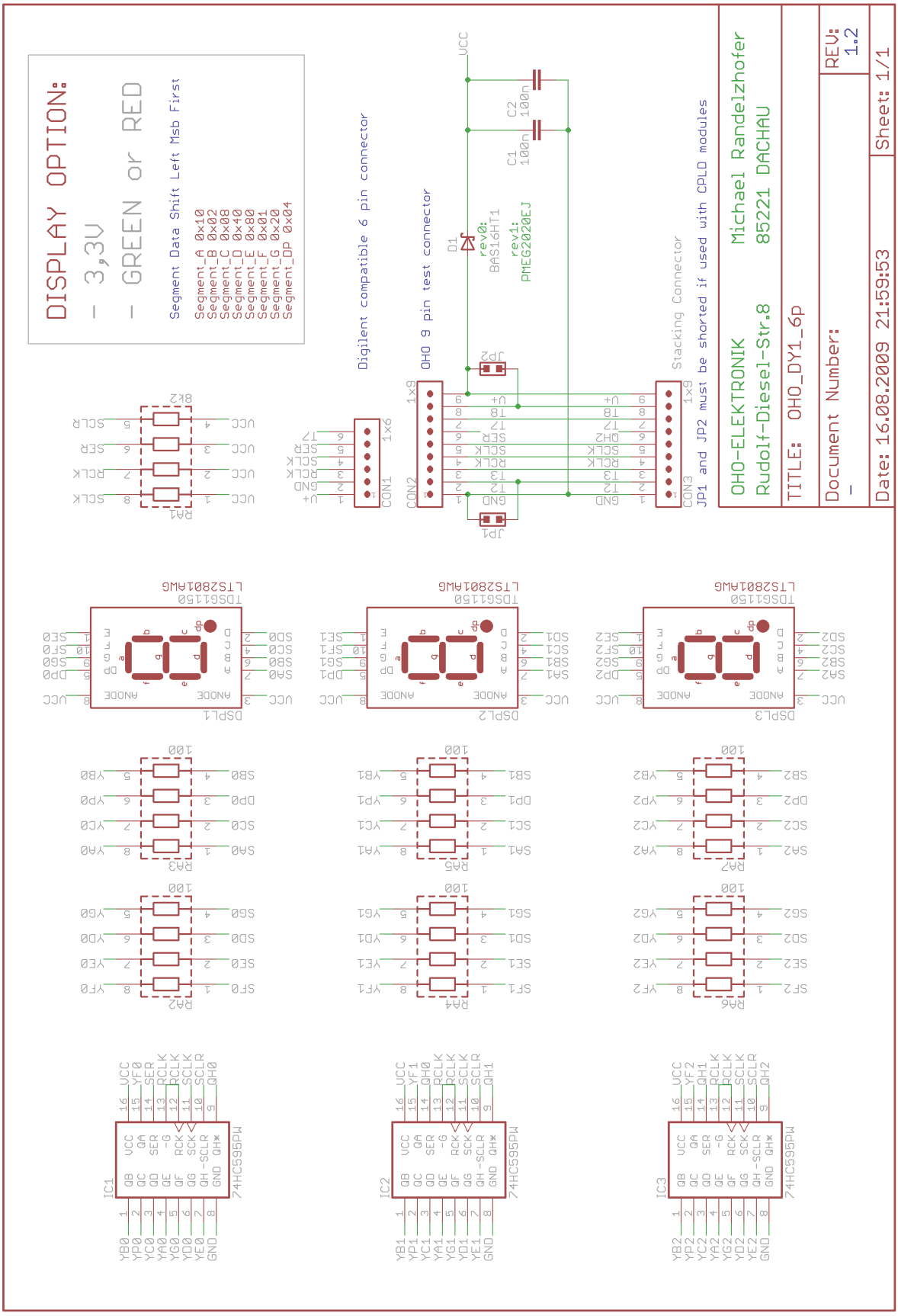
Display data on SER is generated by the function SerialHexDecode in 8 SCLK packets, one packet represents one display digit, 16 packets are sent for 16 digits in one whole display frame.
SerialHexDecode uses 2 input parameters, one is the display data to serialize, the signal actualdigit.
The other parameter is the timing source for the serialisation, the 3 bit signal displaycounter (11 downto 9).

A 16 to 1 multiplexer sources actualdigit from all 15 input values of the display core input signal digits.
The multiplexer select input is driven by displaycounter (15 downto 12).

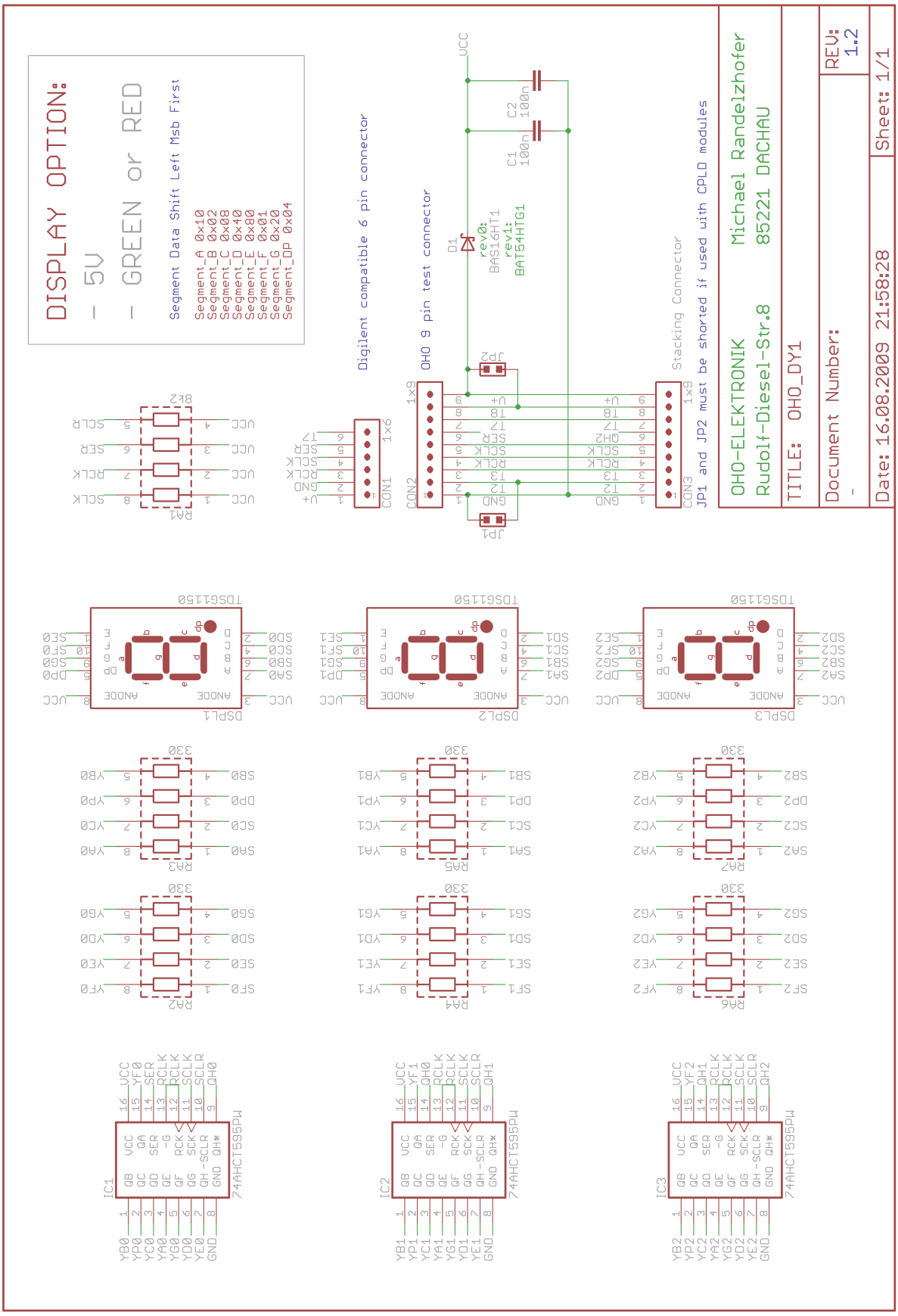
When the least significant 16 bits of the displaycounter rolls over to X”0000” (thus incrementing the most significant 16 bits of the counter), RCLK is set to ‘1’ to generate a rising edge, which transfers the shift register content to the 74x595 output latch to display the transferred display frame.
In a single display frame update, RCLK needs to be reset (on the next rising SCLK) to switch on the LED displays.

During continuous display update in the next display frame, RCLK needs to be reset again to enable a further display update.
That RCLK reset is also derived from displaycounter (15 downto 12) dependent on dy_pwm, which forms a pulse width modulated output enable (also connected to RCLK) for display brightness.

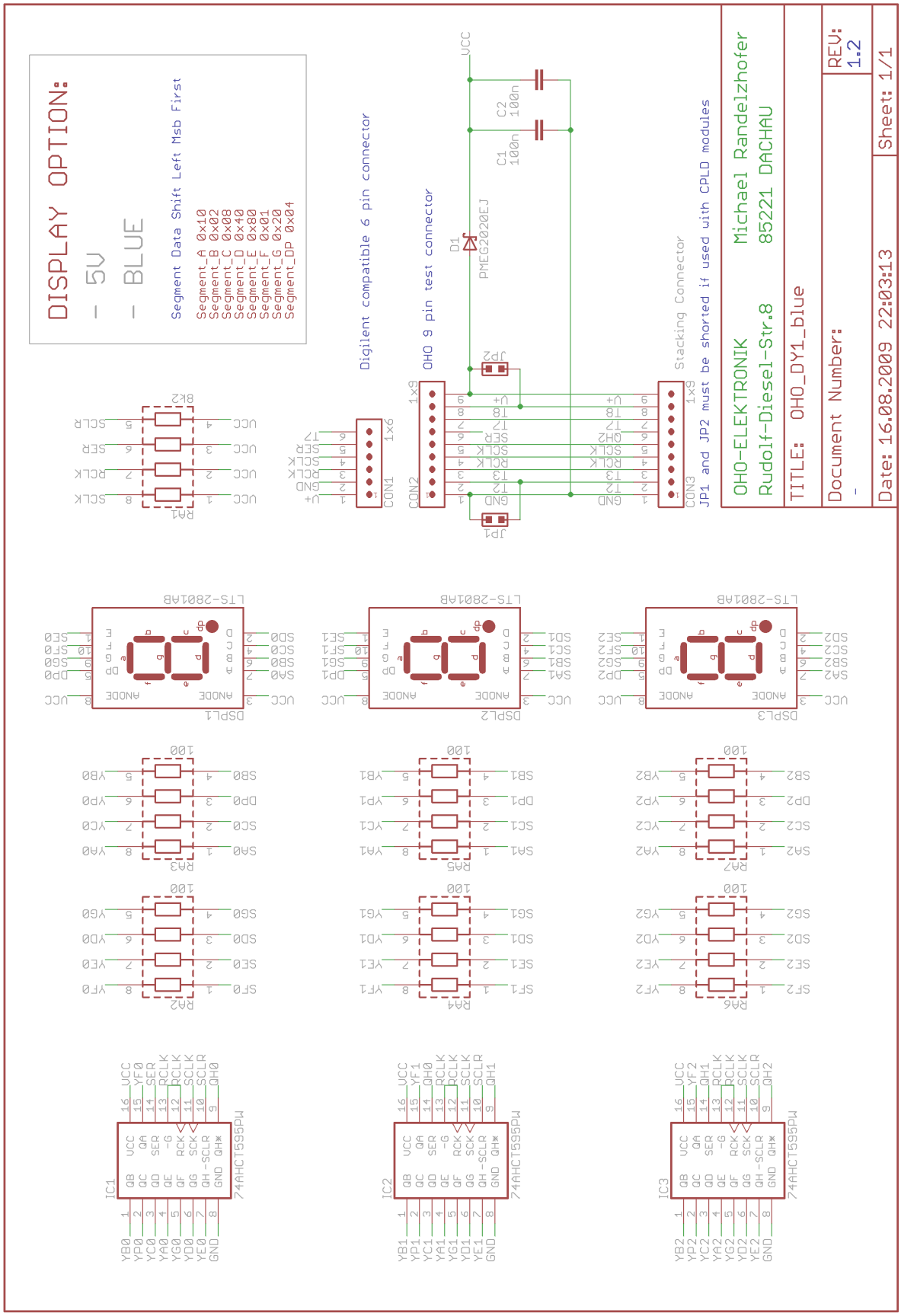
6. Schematics 3,3V Version



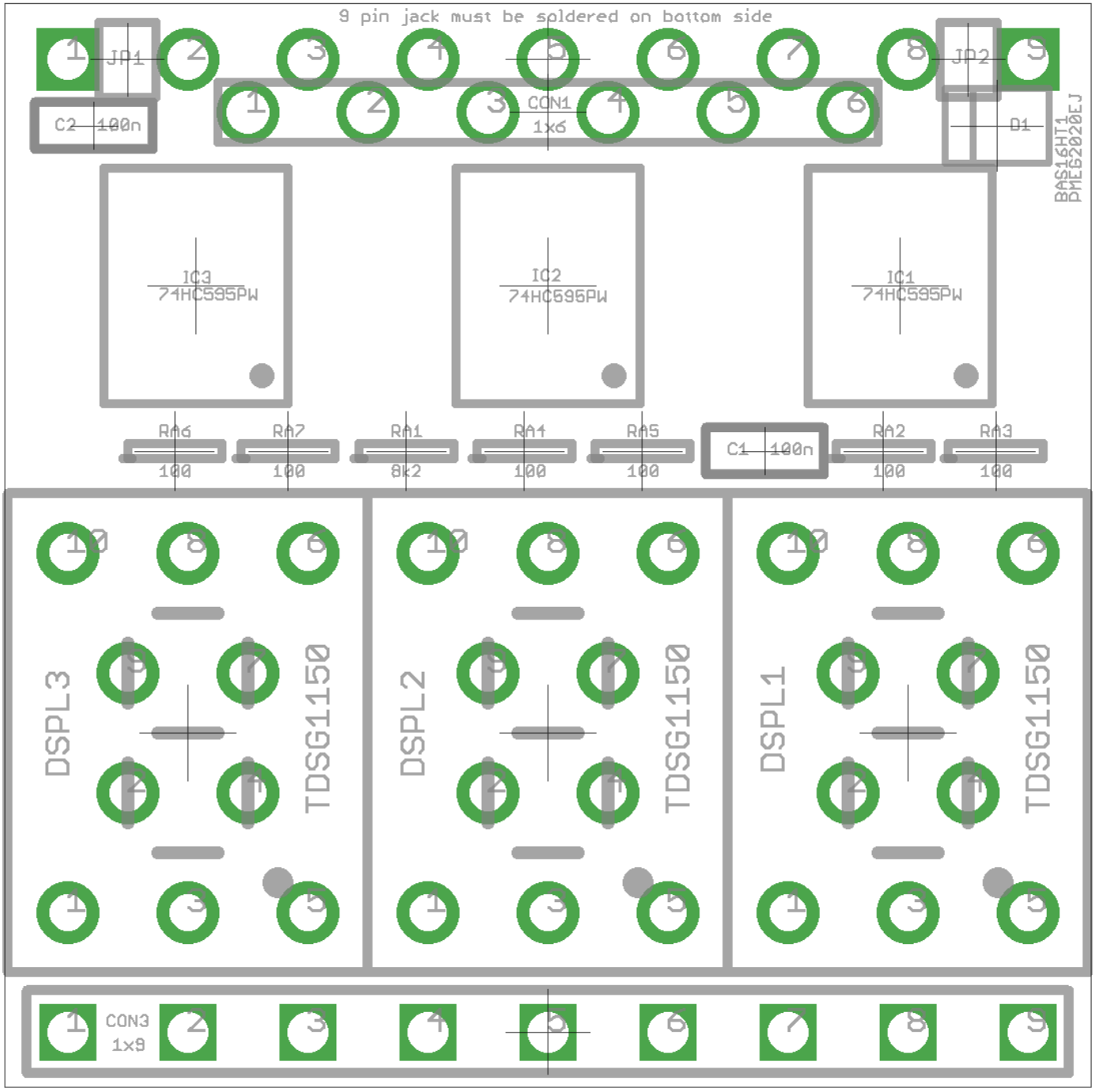
7. Schematics 5V non blue Version



8. Schematics 5V blue Version

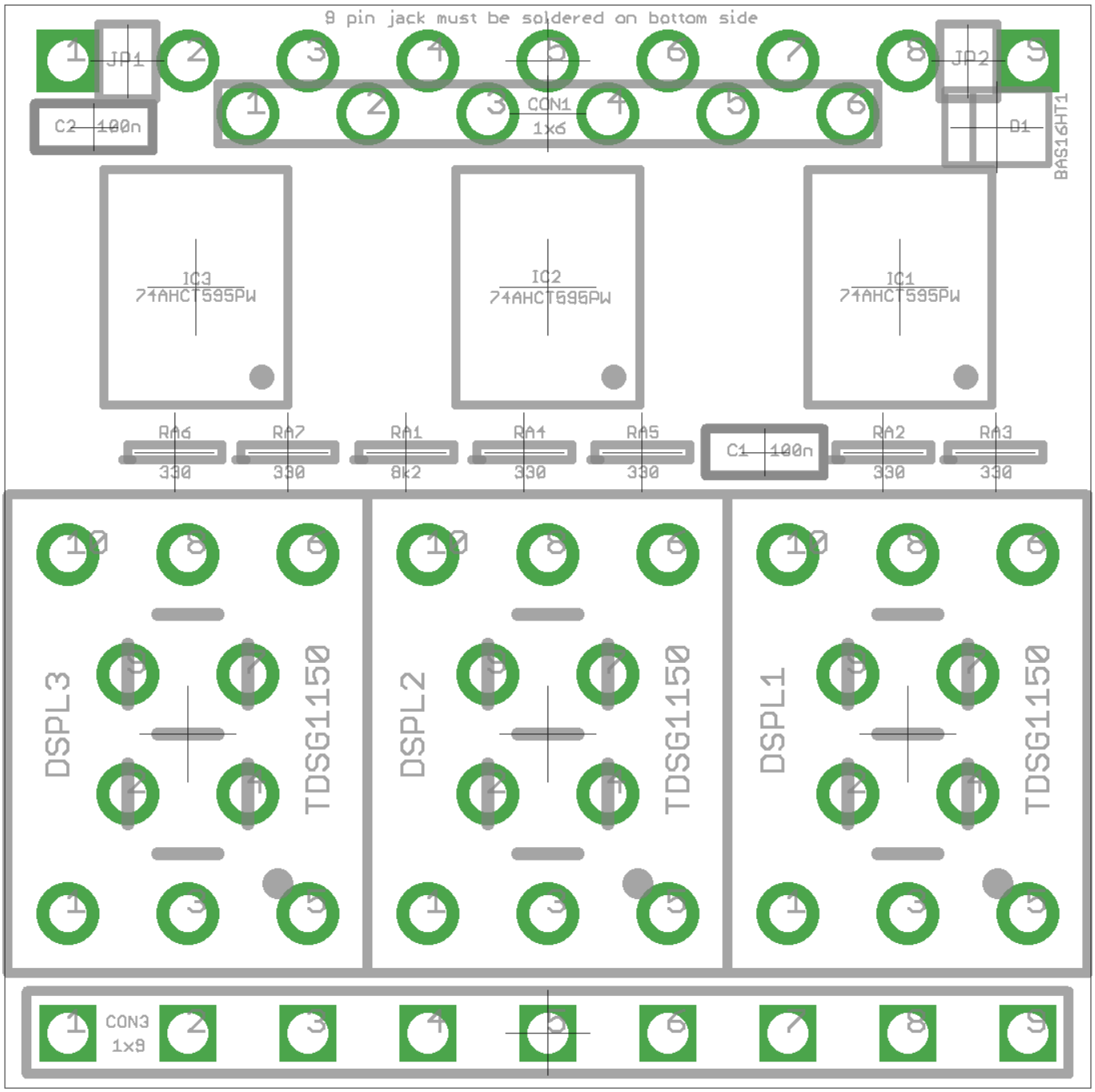


9. Module Layout 3,3V Version



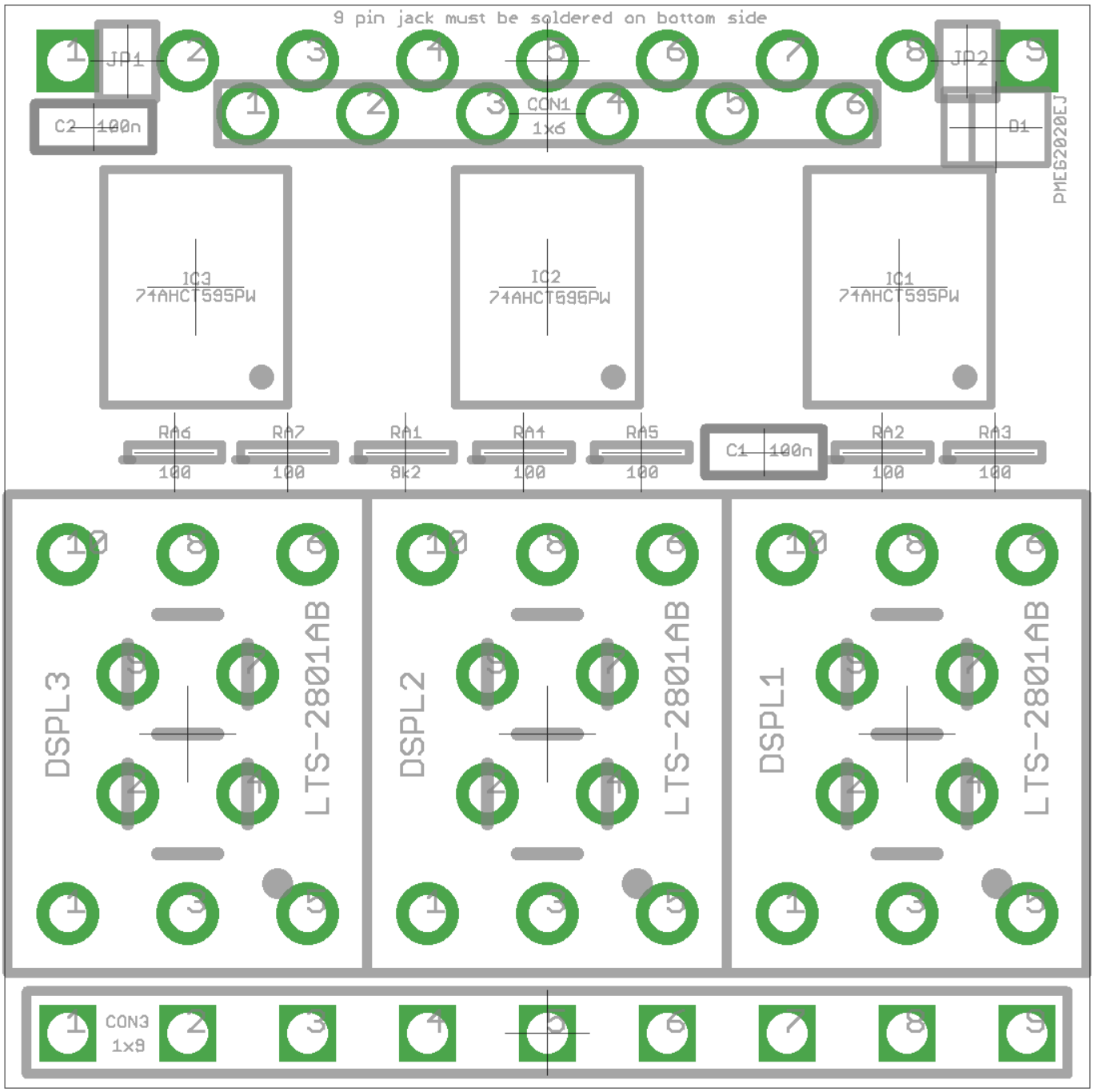
Top view

10. Module Layout 5V non blue Version



Top view

11. Module Layout 5V blue Version



Top view

12. USER'S MANUAL Revisions

Version	Date (d/m/y)	Comments
V1.0	20/07/2009	First Release
V1.1	21/07/2009	Small corrections
V1.2	16/08/2009	Small corrections, new module variants