APDCAM

Digital Avalanche Photodiode camera

User's Guide

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1. Introduction

APDCAM is a 4x8 pixel Avalanche Photodiode Detector camera containing all detector infrastructure and data acquisition in one compact package connecting to a computer via 1 Gbit Ethernet connecction. This type of detector is designed for special applications where low light level has to be measured with extreme high speed (up to several MHz). The detector pixels have large area (1.6x1.6 mm) compared to CCD sensors therefore they are easier to match to low f-number optics used in low light applications. All pixels of the detector are read out simultaneously; therefore the throughput is not limited by readout time. The intrinsic gain of the detector allows measurement under conditions where photodiodes would not be applicable. Stable gain is provided by the temperature stabilised detector and the calibration process is made easy by the built-in shutter and calibration light source.

The digital part of the camera contains individual Analog to Digital Converters for all 32 channels. These ADCs continuously digitize data with 14 bit resolution and 10-50 MHz frequency. The resulting data stream can be digitally filtered and downsampled in the camera to provide an output data flux matching the capacity of the Gbit data connecti-ton. The resampled data stream is transferred to a computer via standard 1 Gbit Ethernet communication, either over UTP or fibre cable. The same connection is used for camera control.

Various triggering and sampling schemes are available for the data acquisition, including external, internal, post-trigger, external sample control. Technical specifications of the system are shown in *Table 1.* and *Table 2*. *Figure 1.* shows photos of APDCAM where the location of its elements are indicated.

1.1. Using this document

Section 0 briefly describes the information needed for setting up and operating the camera. Section 2 contains a detailed reference documentation intended for software developers and for advanced users. Technical data are contained in Section 0 while various order options are listed in Section 0.

Detector	
Detector type	Avalanche Photodiode array Hamamatsu S8550 (micro-lens array optional)
Array size	4 x 8
Pixel size	1.6 x 1.6mm
Pixel pitch	2.3 mm (2.6 mm between the two 2x8 sub-arrays)
Spectral response range	300 to 1000 nm
Peak quantum efficiency	85% typical at 650 nm
Detector Gain	Typical 50, max 100
Temperature control range[1]	Typical 10...30 ºC
Temperature control type	Peltier, cooling/heating
Optical interface	
Lens mount	Nikon F mount (custom design options available)
Window material	BK7 with antireflection coating (other window types available)
Shutter	
Type	Electromagnetically operated mechanical
Control	Software or external input
Calibration light	
Type	Red LED with fibre coupling
Control	DC set from software
Sensitivity and noise	
Sensitivity @ Gain=100, 14 bit mode[2]	2.4 10^6 photon/s/digit
Noise equivalent photon flux @ no light[2]	Typical 5 10^7 photon/s
Analog bandwidth[2]	1 MHz
Digitizer	
Internal sampling rate / bits	10-50 MHz / 14 bits
Digital filter	5-point FIR + 1stage recursive
Output bits	14/12/8 (MSB from internal 14 bits)
Ring buffer	0...1024 samples/channel
Trigger	Internal level/External TTL/software
Trigger delay	1µs....1000s
Resampling control	Internal fixed divider or external TTL input
Clock base	Internal 20 MHz or external

Table 1. Technical specifications of APDCAM, part 1.

[1] Temperature range depends on ambient temperature.
[2] Standard setting. Sensitivity and bandwidth can be specified at order time. Selection affects noise level.

Data transmission	
Data and control interface	Gigabit Ethernet over UTP and Fibre
Communication format	UDP, both directions
Fibre interface	Multimode, Duplex SC
Max. data rate @ 32 channels[3]	2 MHz/14bit
Power input	
Power input	12 V DC, max. 6A
Power connector on power supply	Lemo FFA.0S.302.CLAK68
Mechanical	
Size (L,W,H)	36*16*19 cm
Weight without power supply	6.7 kg

Table 2. Technical specifications of APDCAM, part 2.

[3] For typical PCIe computer card. For certain interface cards and computer configurations data rate might be significantly lower.

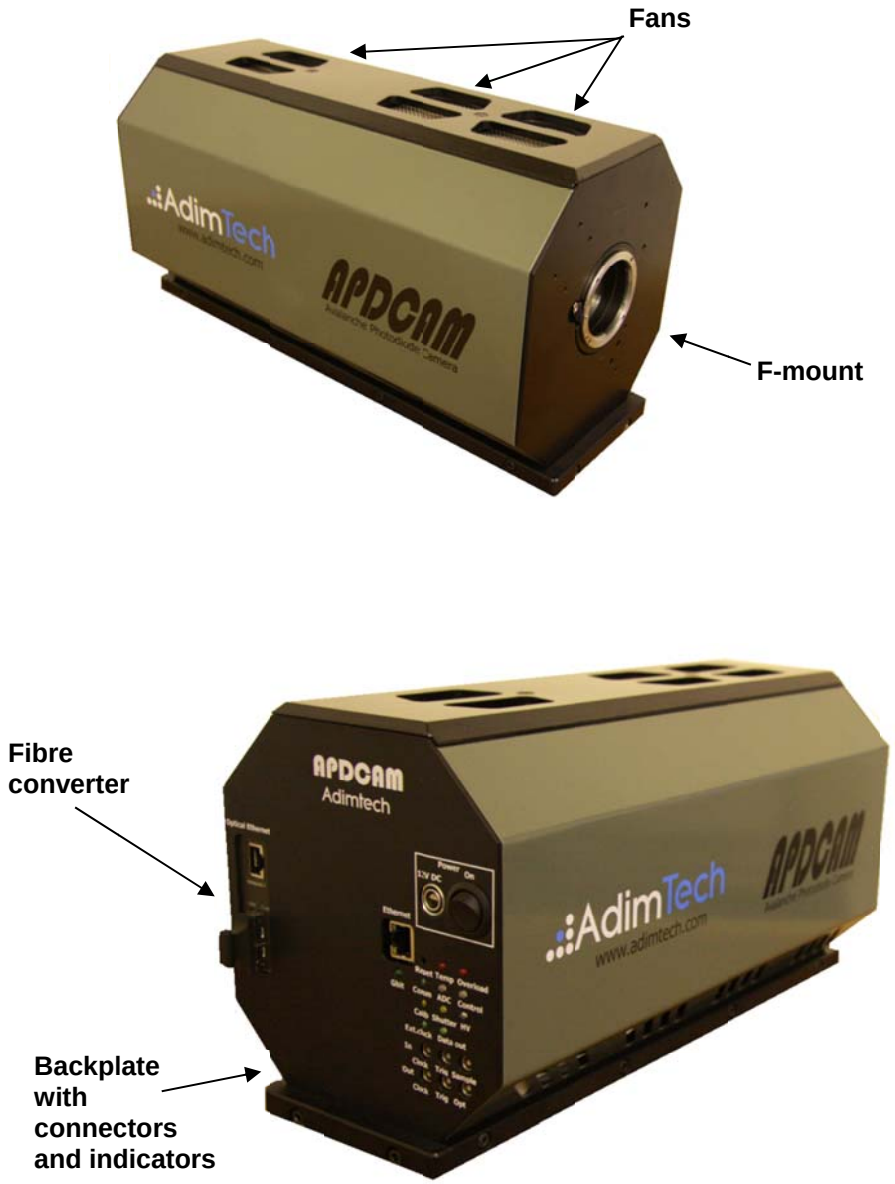


Figure 1. View of APDCAM.

Using APDCAM

1.2. Power connection

APDCAM is delivered with an external 12 V DC power adaptor. This unit has a replaceable power chord, please use one which matches your local mains outlet. The camera needs a single 12 V DC input, maximum current is 6A. The power adaptor is usable from 100 to 230 V mains voltage.

1.3. Operating environment

Some effort might be needed in the setup to minimise noise pick up by the camera. Although APDCAM is housed in a grounded Aluminium enclosure and the detector and analog amplifiers are housed in an additional Faraday shield strong environmental electrical noise sources might cause disturbances in the signals. To avoid such conditions separate the camera ground from noisy electronic equipment. The camera housing is connected to electrical ground on the power supply mains connector.

1.4. Camera cooling

APDCAM has three independent fans on the top of the device which circulate air from the openings on the lower part of the camera out through the fans. The openings should be free to provide the necessary air flow. In the default setup the speed of the three fans is set to maximum. If lower speed is desired due to e.g. vibration or noise considerations the camera can be configured in the factory for software adjustable fan speed. In this case the user is responsible for setting a minimum fan speed for sufficient cooling.

1.5. Configuration

The operating parameters of APDCAM are set up in two internal register tables, one for the data acquisition and one for the camera control. Status of the camera can also be read from these registers. Settings are stored in non-volatile memory, therefore after switching off and on the camera the setup will remain the same. There are a few exceptions from this rule:

- Detector bias voltage is always off and disabled after switching on the camera.
- The desired number of samples in the measurement are set to 0 on power-on.

The camera also contains configuration information which can only be read by the user. An example is the maximum allowed detector bias voltage. These register values can be changed by the manufacturer only.

1.6. PC communication

APDCAM can be connected to a PC either via UTP cable or fibre optics communications. In both cases Gigabit Ethernet is used with 100/10 Mbit as fallback. For using the maximum data acquisition bandwidth it is essential to use a Gigabit interface card on the PC side which connects to the internal bus via a PCI Express interface. A card connected to the PCI bus will not deliver the maximum performance although camera operation at lower acquisition speeds will not be affected.

If UTP (electrical) connection is intended simply connect a Gbit compatible UTP cable between the APDCAM UTP port and the PC interface card.

In case of optical communication a media converter is needed on the PC side. Adimtech recommends D-Link DMC-700SC media converters, which were extensively tested with APDCAM. Prior to use the D-Link interface internal switches have to be set the following way:

SW1: on (forced)

SW2: off

On the camera side the media converter is included in the camera. Connect a short UTP cable between the camera UTP port and the camera Fibre module's UTP port. Connect the optical cable to the camera fibre converter optical connector. On the PC side similarly connect the media converter between the PC Gigabit interface and the optical cable.

To communicate with APDCAM the PC Ethernet interface IP address should be set up to the same subnet as the camera. The default IP address of the camera is 10.123.13.101, therefore the PC can be set up e.g. to 10.123.13.202. The netmask should be 255.255.255.0. The camera Gigabit interface can be set up for a different IP address using a software command over the internet connection; therefore it can also be connected to a local network shared by other devices. However, in applications needing high data acquisition performance this is not recommended as high network traffic can result in loss of data.

If the camera network address was set up in a wrong way or the address is not noted it can happen that the PC cannot find the camera on the network. In such cases the reset procedure in Section should be followed in

1.7. Software interface

A user program can control APDCAM by sending UDP datagrams to the Gbit communications module (Gigabit Ethernet Controller, ByteStudio, www.bytestudio.hu). The control datagrams fall into two basic categories: control for the Gbit interface and register read/write in one of the two internal modules of APDCAM: the data acquisition module and the control module. The camera may answer to these UDP datagrams by sending one ore more responding UDP datagrams.

For a standard setup the Gigabit interface parameters need not be modified. For special settings please consult the separate Gigabit interface documentation.

Additionally to register read/write operations data form the camera are also sent to the PC in UDP datagrams. This form of communication is optimal for sending large amounts of data but it has no feedback to the sending device. This means that if a data packet is lost the camera will not resend it. UDP packets are counted sequentially, therefore the receiving program can detect when data loss occurred. The camera may send large amounts of data through the Ethernet interface, therefore a direct connection between the PC and the camera is recommended in all cases.

On the computer side data during measurement is stored into memory, therefore large physical memory and fast CPU is recommended. Either Windows (XP, 7) or Linux operating systems may be used but for high throughput some settings need to be optimized. Windows Home edition is not suitable as it cannot be set up properly.

For program development a C language Application Programming Interface (API) is available for Windows and Linux operating systems. For standard tasks a scriptable program (APDTest) is available. The use of the API and APDTest is presented in a separate document. A graphical user inteface is currently under development.

1.7.1. System setup under Windows

The data transfer rate to disks is lower than the data transfer rate from APDCAM to the PC, therefore data is stored in physical memory during measurement. For this the operating system must ensure that allocated memory is locked in memory and not replaced by virtual memory. This can be done by opening "Local Security Policy" in „Administrative Tools" under Windows 7. In the "Local Policies-> User Rights Assignments" panel click "Lock pages in memory" with the right mouse button and select "Properties" from the menu. Add the user to the list who is going to run the data acquisition program and reboot the computer. Some recent security updates in windows enable the use of this feature only for programs run by Administrator, therefore run the APCAM related programs as administrator.

1.7.2. System setup under Linux

To optimize network throughput for APDCAM the network buffer sizes have to be set larger than default. This is done (as root) by adding two lines to /etc/rc.d/rc.local:

```
echo 1000000 > /proc/sys/net/core/rmem_default
echo 1000000 > /proc/sys/net/core/rmem_max
```

The above commands set this buffer to 1 Mbyte. This takes effect on next reboot. If the following two commands are run the buffer sizes are changed immediately:

```
sysctl -w net.core.rmem_max=1000000
sysctl -w net.core.rmem_default=1000000
```

The APDCAM related programs need to lock large amount of memory in physical space. This is normally not allowed. To allow it two lines should be added to file `/etc/security/limits.conf`:

```
apd hard memlock 2000000000
apd soft memlock 2000000000
```

Here "apd" is the name of the user under which runs the APDCAM measurement program. 2000000000 indicates that 2 Gbyte is the maximum lockable memory. This setting takes effect when the user logs in.

The next setting to be done is to allow receiving UDP packets from unknown sources. Firewalls in many case block incoming UDP packets from machines which did not receive packets from the same port. APDTest uses 4 UDP ports for data receiving: 57000 through 57003. These should be opened or in some way receive enabled.

1.8. Optical input interface

APDCAM has a standard Nikon F-mount as optical input interface. A BK7 glass window is located in the F-mount therefore dust will not enter the detector housing. A shutter is mounted between the window and the detector. The shutter can be opened either with a software command or via an external TTL signal. A calibration light source is coupled to the detector surface which can be set up via software to emit various levels of constant light on the detector, thus allowing calibration. The light level is not strictly proportional to the setting and the illumination of the detector is not uniform, therefore the calibration light cannot be used for calibrating the relative sensitivity of the pixels.

The calibration light is also useful for setting up the optical system. As APDCAM has low spatial resolution viewing its image does not help in adjusting the lens focus. Instead

it can be done by illuminating the detector with the calibration light and observing its image on a screen at the object.

1.9. The detector and its operation

The detector has 32 identical Avalanche Photodiode elements (pixels) biased from a single voltage. The bias voltage determines the internal gain of the detector. The detector bias voltage should be set between 200-400V using the appropriate control register. Although the detector and electronics are protected from overload, damage cannot be excluded if e.g. only a single pixel is illuminated over an extensive period of time. To protect accidental switch-on of the bias voltage a voltage enable register is provided where an appropriate code should be entered. Voltage can be switched on only after this.

An additional protection against overload is provided by the digital electronics. If enabled it can switch off the detector bias voltage when the signal level is above a certain limit over a predefined time.

In order to stabilise the gain the detector temperature should be kept constant. This is accomplished by a temperature control circuit. The standard detector temperature is 18 C which under normal room temperature does not require too much cooling and prevents condensation of humidity. If the environmental temperature is much lower or higher 20-25 Celsius the detector reference temperature can be set to a different value.

1.10. Data acquisition

The logical scheme of the data acquisition is shown in *Figure 2.* This scheme is operating for all 32 channels independently; all channels can be enabled/disabled. The Analog to Digital Converter (ADC) continuously samples the amplified detector signal to 14 bits

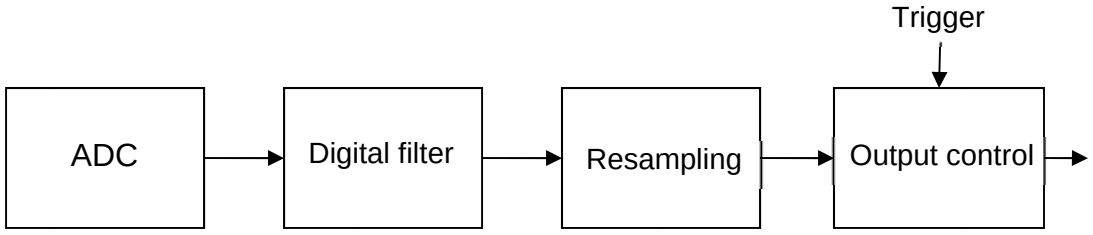


Figure 2. Logical scheme of the basic data acquistion sytem.

at a frequency between 10-50 MHz. A configurable digital filter provides high frequency cutoff. The filtered signal is resampled at a lower frequency or using an external clock to reduce data load to the computer. The data output can be controlled from external or internal trigger or software command. A ring buffer is also available which can store the last maximum 1023 resampled data. When the trigger arrives data output starts with the contents of the buffer, this post-trigger operation is possible. This is very useful in combination with the internal trigger mode, as APDCAM can trigger itself on the incoming light signal. The camera can also produce an output trigger when the output is started.

In the standard setup the data acquisition system timing is based on in internal quartz oscillator. However, if needed this can be replaced by an external clock signal to provide strictly synchronous operation between several cameras or other devices.

1.11. Controls and indicators

APDCAM has several indicator LEDs and input-output connectors mounted on its back-plate. Their function is described in *Table 3.* The photo of the backplate where these units are mounted is shown in *Figure 3.*

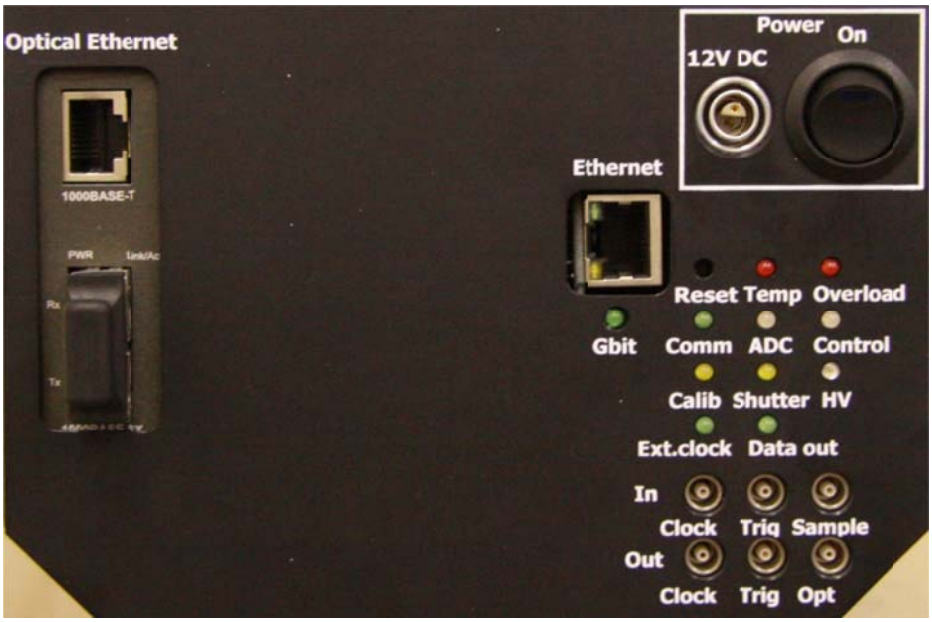


Figure 3. Photo of the backplate of APDCAM with the controls, connectors and indicators.

Controls	
Power switch	Switches the input power.
Reset button	This depressed button can be operated with a pen or other pointed device. Pressing it causes both the control unit and the data acquisition unit to return to factory default settings.
Connectors	
Power connector	Receives input 12 V DC power.
Clock in	Reference TTL clock input. Synchronises clock base of APDCAM to external source. (Signal standard 3.3 V CMOS)
Clock out	Reference clock output. Can be used to synchronize clock base of external device. (Signal standard 3.3 V CMOS)
Trigger in	Data acquisition start trigger signal input. (Signal standard 3.3 V CMOS)
Trigger out	Outputs High level while data transmission is active. (Signal standard 3.3 V CMOS)
Sample in	Input resample clock. (Signal standard 3.3 V CMOS)
Opt	Optional input-output. Can be selected among various internal signals in the factory.
Ethernet	UTP connection to PC.
Optical Ethernet UTP	UTP cable connection from Ethernet connector of APDCAM if fibre communication is desired.
Optical Ethernet fibre	Fibre data connection to PC
LEDs	
Temp.	Red light means temperature alarm. Some element of the camera is overheated.
Overload	Red light means overload condition occurred, detector bias voltage is switched off.
Comm.	Green light flashes when control communication occurs between PC and camera
ADC	Data acquisition module state: Green indicates normal state, red means error condition.
Control	Control module state: Green indicates normal state, red means error condition.
Calib.	Yellow light means calibration light is on.
Shutter	Yellow light means shutter is open
HV	Blue light means detector bias voltage is on.
Ext. Clock	Green light means external reference clock signal is accepted.
Data out	Green light indicates data output to PC.
Gbit	Ethernet interface is operating at Gigabit speed.

Table 3. List of controls, connectors and LED indicators of APDCAM.

2. APDCAM Reference Manual

In this section a detailed description is given of the APDCAM system.

2.1. System Overview

The block scheme of APDCAM is shown in *Figure 4*. The APD array detector is mounted on a copper tab which can be cooled/heated by a Peltier element. This way the temperature of the detector is stabilised at a reference value which can be somewhat (max ~15 C) below or above the ambient temperature. Cooling the detector does not offer advantages in terms of noise, therefore the temperature control is provided only to stabilise the gain. A shutter is mounted in front of the detector so that it can be coupled off from the input light and can be calibrated using the calibration light. The DC current of the calibration LED is set digitally while the light is coupled to the detector via four optical fibres which illuminate the detector from 4 directions. The detector bias voltage is also controlled digitally thus having the possibility of adjusting the detector gain to the requirements.

The photocurrent from each of the 32 detector pixels is amplified by a sensitive low noise amplifier. To compensate for the offset drift the output offset level of the amplifiers can be controlled digitally through 32 Digital to Analog Converters (DAC). The final analog output signal is digitized at 10-50 MHz/14 bit. The data stream can be digitally filtered and finally it is resampled to produce the output data stream which is packed into UDP packets and transmitted through the Ethernet connection to the PC. Communication with the PC can be done via the UTP connection. If needed fibre optics communication is also possible through the built-in media converter.

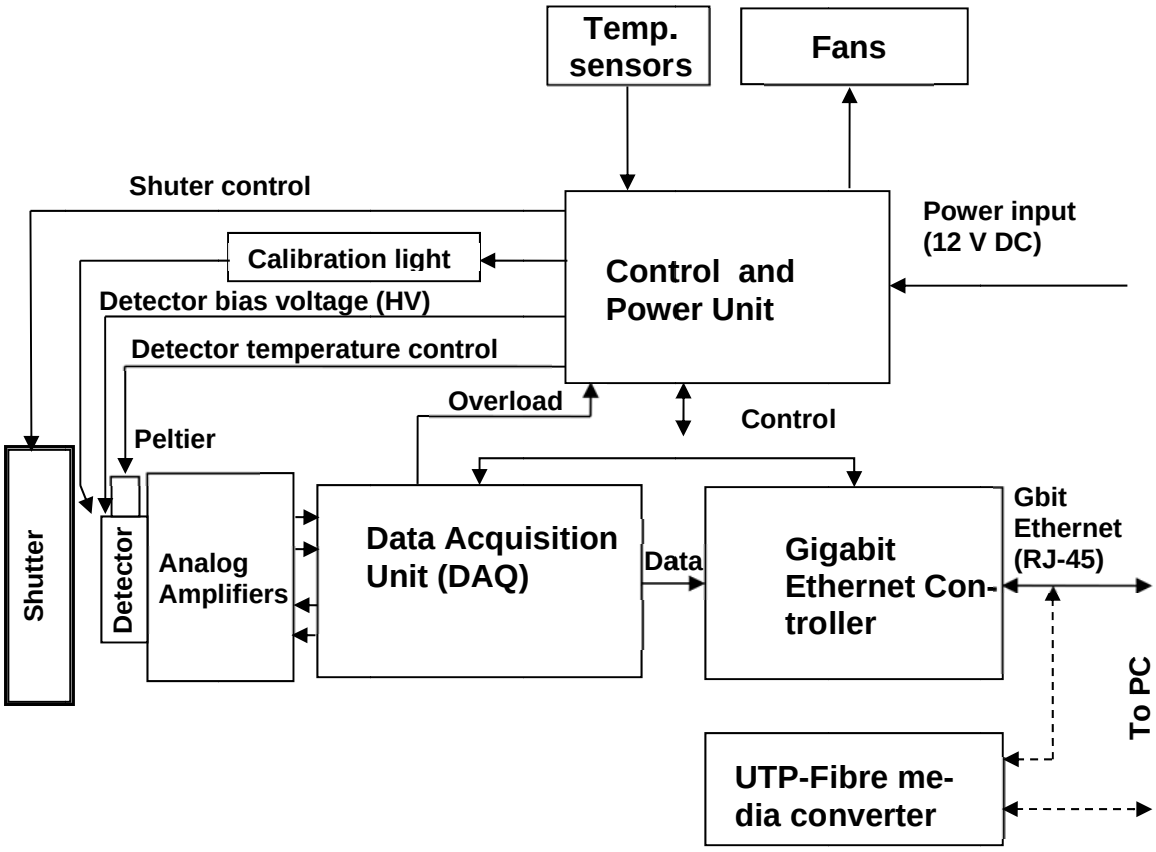


Figure 4. Block scheme of APDCAM.

The ADC works all the time, therefore it is possible to perform some triggering operations inside the camera. One possibility is internal triggering, where the data acquisition starts when the signal reaches a certain level. The trigger level can be set individually for all 32 channels. Another possibility is detector protection from extended periods of overload. If the signals are above a certain level over a specified time the bias voltage of the detector is switched off. Details of the data acquisition operation are given in Section 2.2.

The Control and Power Unit provides power for all the other units and controls the detector infrastructure: detector bias voltage, temperature, calibration light, shutter, fans. The detector bias voltage can be set by the user up to a factory set limit in the range of 400-500 V. The exact limit is dependent on the individual detector. There is also a minimum recommended detector bias voltage of 200 V, below that the crosstalk through the pixels causes excessive noise. The control card also controls the detector temperature by cooling or heating it via a Peltier element. No computer intervention is needed for the control, only parameters can be set from the PC.

Operation parameters of the camera are set by setting registers in the ADC or the control unit. For a description of the register tables see Sections 2.2 and 2.4.

The communication between APDCAM and the host PC is performed by a general purpose Gigabit communication card. It communicates with the two internal units via an internal bus. The register tables of the camera can be written or read by sending UDP datagrams to the Gigabit card. Acquired data is also sent via this card.

2.2. Detector and analog electronics

The detector has 32 identical Avalanche Photodiode elements (pixels) connected to a common positive bias voltage. The arrangement and dimensions of pixels is shown in *Figure 5*. The mapping to/from detector pixels to data acquisition is shown in *Table 4*.

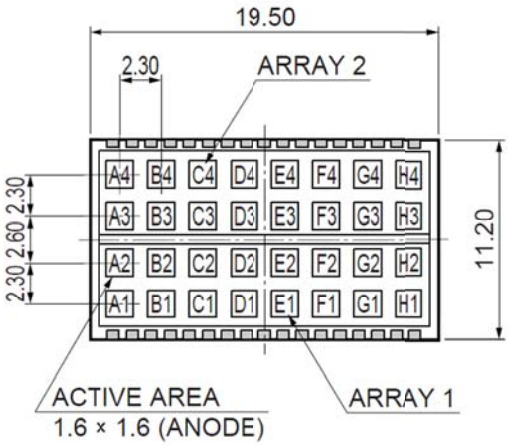


Figure 5. Detector dimensions and arrangement of pixels viewing the detector from the front of the camera. All dimensions are in mm.

APD#	Channel	APD#	Channel	APD#	Channel	APD#	Channel
A1	18	A2	19	A3	15	A4	14
B1	20	B2	17	B3	13	B4	12
C1	21	C2	22	C3	16	C4	11
D1	23	D2	24	D3	10	D4	9
E1	25	E2	26	E3	8	E4	7
F1	27	F2	32	F3	6	F4	5
G1	28	G2	29	G3	1	G4	4
H1	30	H2	31	H3	3	H4	2
Channel	APD#	Channel	APD#	Channel	APD#	Channel	APD#
1	G3	9	D4	17	B2	25	E1
2	H4	10	D3	18	A1	26	E2
3	H3	11	C4	19	A2	27	F1
4	G4	12	B4	20	B1	28	G1
5	F4	13	B3	21	C1	29	G2
6	F3	14	A4	22	C2	30	H1
7	E4	15	A3	23	D1	31	H2
8	E3	16	C3	24	D2	32	F2

Table 4. Allocation of data acquisition channels for the detector pixels.

The detector bias voltage determines the internal gain of the pixels. The gain as a function of the applied voltage is shown together with the Quantum efficiency (QE) in *Figure 6*. Besides the gain the bias voltage also changes the detector capacitance, it decreases with increasing voltage. As all pixels are operated from a common bias voltage at low voltage setting the crosstalk increases between channels which results in an increase of the noise and its coherency between channels. Below about 150 V the 32 channel amplifier system oscillates between minimum and maximum output, therefore no measure-

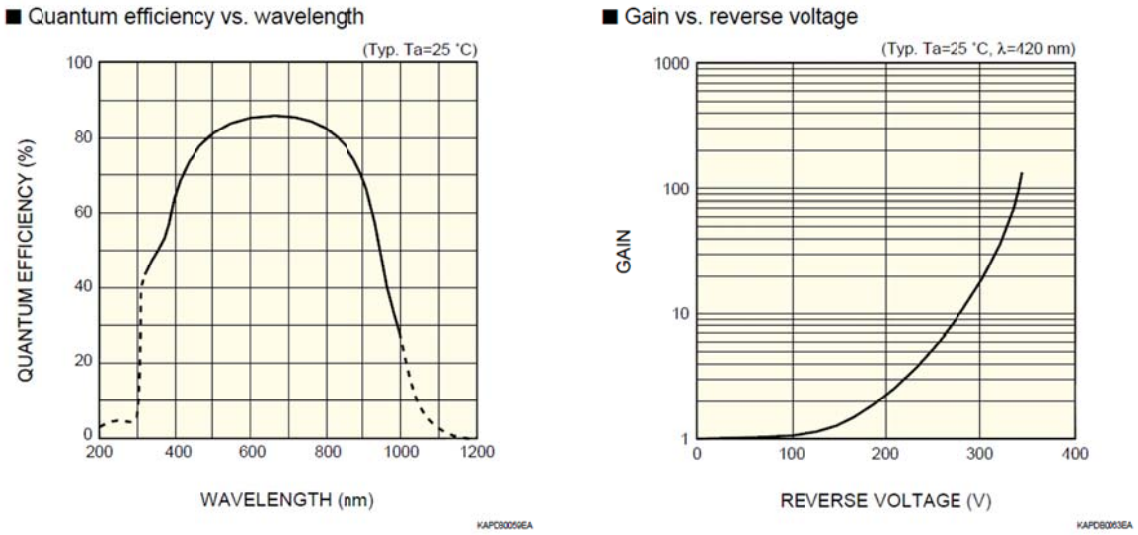


Figure 6. Detector typical Quantum Efficiency (QE) and Gain.
(Source: Hamamatsu S8550 datasheet.)

ment can be done. The exact limit and the noise as a function of bias voltage depends on the amplifier bandwidth but above 200 V bias voltage the detector is stable. The noise level decreases slightly until about 300 V.

The detector can be overloaded if high input light level is applied while the bias voltage is on. Although the detector and electronics is protected against overload under the most unfavourable conditions about 0.4W heat can be generated in the detector which might result in damage if present for an extensive time. To prevent damage the camera electronics contains an overload protection function which switches off the detector bias voltage if the output signal is above a limit for an adjustable time.

An additional measure to prevent overload is the two-step bias voltage switch-on procedure. When APDCAM is switched on the bias voltage is off. First a bias voltage enable code should be written into the bias enable register and the voltage can be switched on only after that. This procedure prevents accidental biasing die to any accidental software error.

The detector is mounted on a temperature controlled tab. The reference temperature is set in a register of the control module. This temperature can be either below or above the environmental temperature. (The environmental temperature is measured on the base of the camera and can be read from the register table.) Cooling the camera does not provide specific advantage, but temperature changes affect the detector, therefore the aim of temperature control is to provide a stable gain. 18 C is recommended for detector temperature as it is slightly below usual room temperature but it does not cause condensation of air humidity on the detector. Please note that the temperature of the detector has an effect on the gain as well. Applying the same bias voltage at lower temperature causes higher gain. Please consult the Hamamatsu S8550 datasheet for details.

The analog electronics utilize two amplifier stages for each channel, their bandwidth is from DC to a maximum frequency. Parameters of the first stage (feedback resistor and capacitance) determine the bandwidth and also the noise level. For setting an optimal Signal to Noise ratio some information on the expected light level is required. As default the amplifier is set up for about 10^{10} photons/s light level and 1 MHz bandwidth. For considerable different conditions the amplifier should be mounted with different components, therefore a rough estimation of the light level and required bandwidth is necessary at manufacturing time.

The high sensitivity amplifiers and the detector bias current can cause some drift in the signal DC level. In order to compensate for this the analog electronics is equipped with a DC offset input which can be set for each channel individually in the data acquisition unit. The analog signals are negative in response to the input light, therefore the DC offset should be set to a high positive value to fit the signal into the 0-2V range of the digitizer.

The detector is mounted directly on to the analog amplifier circuit board and cooled by a cooling tab. The whole unit is mounted inside an Aluminium housing. The temperature of the detector, the analog electronics and the housing are measured.

2.3. Data Acquisition Unit

The block scheme of the data acquisition unit (DAQ) is shown in *Figure 7*, while the register map is in *Table 5. and Table 6.* After power-on different registers are set from various sources as indicated in the table. Most of the registers recover their last data from an on-board EEPROM memory, therefore they preserve their settings. Several of the registers will show the factory default value. This factory default can be regenerated for all registers by writing a code into the FACTORY_RESET register. This is identical to pressing the reset button at the camera back.

Parameter	*R/W*	*Offset (byte)*	*Size (byte)*	*Value after start*	*Description*
BOARD_VERSION	R	0	1	factory	Board version code. Bits 0...4: board version Bits 5...7: 1
MC_VERSION	R	1	2	factory	Microcontroller program version code.
SERIAL	R	3	2	factory	Board unique serial No.
FPGA_VERSION	R	5	2	factory	FPGA program version code.
STATUS1	R	8	1	N/A	Status flags, group 1 Bit 0: ADC PLL locked Bit 1: Stream PLL locked Bit 2-7: Reserved
STATUS2	R	9	1	N/A	Bit 0: Reserved Bit 1: Overload Bit 2: External clock PLL locked Bit 3: Reserved Bit 4-7: ADC 1-4 sample enable
CONTROL	R/W	11	1	EEPROM	Various control bits: Bit 0: External clock select Bit 1: Clock out enable Bit 2: External sample select Bit 3: Sample out enable Bit 4: Digital filter enable Bit 5: Reserved Bit 6: Reverse bit order in stream (1: LSB first) Bit 7: Preamble enable
ADC_PLL_MULT	R/W	12	1	EEPROM	PLL multiplier for ADC clock generation. Valid: 20...50
ADC_PLL_DIV	R/W	13	1	EEPROM	PLL divider for ADC clock generation. Valid: 8...100
STREAM_PLL_MULT	R/W	14	1	EEPROM	PLL multiplier for ADC clock generation. Valid: 20...50
STREAM_PLL_DIV	R/W	15	1	EEPROM	PLL divider for ADC clock generation. Valid: 8...100
STREAM_CTRL	R/W	16	1	0	The four lower bits enable the data output to the four streams.
SAMPLE_NUMBER	R/W	17	4	0	Requested number of samples. 0 for infinite.
CH_ENABLE	R/W	21	4	EEPROM	Enable bits for the 32 channels.
RINGBUFSIZE	R/W	25	2	EEPROM	Size of the ring buffer in samples per channel. (Valid: 0...1023)
RESOLUTION	R/W	27	1	EEPROM	Output resolution. 0: 14 bit, 1: 12 bit, 2: 8 bit.
SAMPLEDIV_X_7	R/W	28	2	EEPROM	Divider for generation of the sample clock from 7xADC_CLOCK. E.g. to take every second sample write 14.
TRIGGER	R/W	30	1	EEPROM	Trigger enable bits. Bit 0: Enable external trigger rising edge. Bit 1: Enable external trigger falling edge. Bit 2: Enable internal trigger. (For polarity see INT_TRIG_LEVEL

Table 5. Register table of the DAQ unit, part one.

Parameter	*R/W*	*Offset (byte)*	*Size (byte)*	*Value after start*	*Description*
ADC_TEST_MODE	R/W	32	4	EEPROM	Each byte controls the mode of one ADC, first is ADC 1. The codes in the lower 3 bits are: 0: Normal measurement 1: 10 0000 0000 0000 2: 11 1111 1111 1111 3: 00 0000 0000 0000 4: 10 1010 1010 1010, 01 0101 0101 0101 5: Long pseudorandom (See Sect. 5.6 of ITU-T 0.150 (05/96) standard) 6: Short pseudorandom (See Sect. 5.1 of ITU-T 0.150 (05/96) standard) 7: 11 1111 1111 1111, 00 0000 0000 0000
FACTORY_RESET	W	37	1	N/A	Writing hex CD into this register causes all settings to return to factory reset.
BYTE_PER_SAMPLE	R	40	4	N/A	The ADC indicates here the number of bytes per sample sent in one stream. The four bytes correspond to the four streams, (See section 1.7)
CLOCK_PLL_MULT	R/W	46	1	EEPROM	External clock PLL multiplier. Valid: 2..33
CLOCK_PLL_DIV	R/W	47	1	EEPROM	External clock PLL divider. Valid: 1..32
OFFSET	R/W	48	64	EEPROM	These are the 32x2byte offset settings for the 32 analog channels. Standard values are 500..1000.
INT_TRIG_LEVEL	R/W	112	64	EEPROM	32x2 bytes internal trigger setting for each channel: Bits 0...13: trigger level Bit 14: 0: positive trigger (level) 1: negative trigger (level) Bit 15: Enable trigger from this channel
ACT_SAMPLE	R	176	16	0	4x4 byte indicating the number of acquired samples per stream. As the sample timing is identical for all channels these values are normally identical.
OVERLOAD_LEVEL	R/W	192	2	EEPROM	Overload condition setting for all channels: Bits 0...13: level Bit 14: 0: overload above level 1: overload below level Bit 15: Overload enable.
OVERLD_STATUS	R/W	194	1	0	Bit 0: overload status Writing this register clears overload.
OVERLD_TIME	R/W	195	2	EEPROM	Overload time in 10 µs units.
TRIGGER_DELAY	R/W	197	4	EEPROM	Delay of data transmission start after any trigger condition in units of the base clock period time.
FILTER_COEFF	R/W	208	16	EEPROM	Signed 16 bit integer coefficients for digital filter. These should be written sequentially, they are loaded into the FPGA when the last byte is written. Order of 2-byte coefficients: COEFF_01...COEFF_05: FIR coefficients COEFF_06: Recursive filter coefficient. COEFF_07: Reserved Coeff_08: Filter divide factor: 0...11.

Table 6. Register table of theDAQ unit, part two.

At the beginning of the register map some registers describe the program and hardware versions and the unique serial number of the ADC board.

After power-up the red-green bicolor ADC LED is lit green on the camera backplate. If the ADC unit encounters a fatal problem this LED is red.

The DAQ unit is attached to the analog output signals at the backside of the detector housing. The 32 input channels have an analog bandwidth of about 3 MHz, the input voltage range is 0-2V. The input channels are grouped into 8-channel blocks, each block is served by an 8-channel pipeline ADC chip. Data from one block is sent to one data stream on the Gigabit communication card. The four streams are sent in separate UDP datagrams on a single Gigabit connection to separate software ports in the PC.

2.3.1. ADC Timing

The timing is identical for all 32 channels and it is based on a single clock. This can be either an internal 20 MHz oscillator or an external clock (clock in). Selection is done with bit 0 in the CONTROL register. The external clock frequency is multiplied/divided by a PLL (see CLOCK_PLL_MULT, CLOCK_PLL_DIV), therefore different input clock frequencies can be accommodated in the 1...40 MHz range. The base clock generated from the external clock should be between 19 and 40 MHz.

The ADC clock is generated from the selected base clock with a PLL (see ADC_PLL_MULT, ADC_PLL_DIV), the resulting ADC clock must be between 10 and 50 MHz. An additional limitation is that the base clock multiplied by ADC_PLL_MULT should be between 400 and 1000 MHz.

The status of the PLL units can be read from the STATUS1 and STATUS2 registers. This is important especially if external clock is used. The external clock PLL status is also shown on the camera backplate by the green Ext. Clock LED.

The 8-channel ADC blocks have a built-in test pattern generator which can be activated individually for all 4 blocks using the ADC_TEST_MODE register. This forces all 8 channels in one block to send the same test pattern.

2.3.2. Filtering, resampling and channel selection

The ADCs generate a data stream with 32x14 bits. A digital filter can be enabled in the CONTROL register which filters all 32 channel data with identical settings. The layout of one filter is shown in *Figure 8*. The 14 bit data is fed in from the left side. A 5-stage FIR filter allows steep cut of the frequency band somewhat below the sampling frequency of the ADC. An additional recursive filter is implemented after the FIR filter to allow for lower frequency cut-off, albeit with less steep characteristic. The recursive filter implementation with integer arithmetic deserves some attention as long integration times can cause overflow in the data. To handle this situation some flexibility is provided at the end of the filter where the output 8, 12 or 14 bit data is cut out: the location of the output bits can be selected.

The following procedure is proposed for calculation of the filter coefficients. The desired cutoff frequency of the recursive filter (f_{rec}) should be selected. From this the `COEFF_06` is

$$\texttt{COEFF\_06} = 8192 \times e^{-2\pi f_{rec}/f_{ADC}} .$$

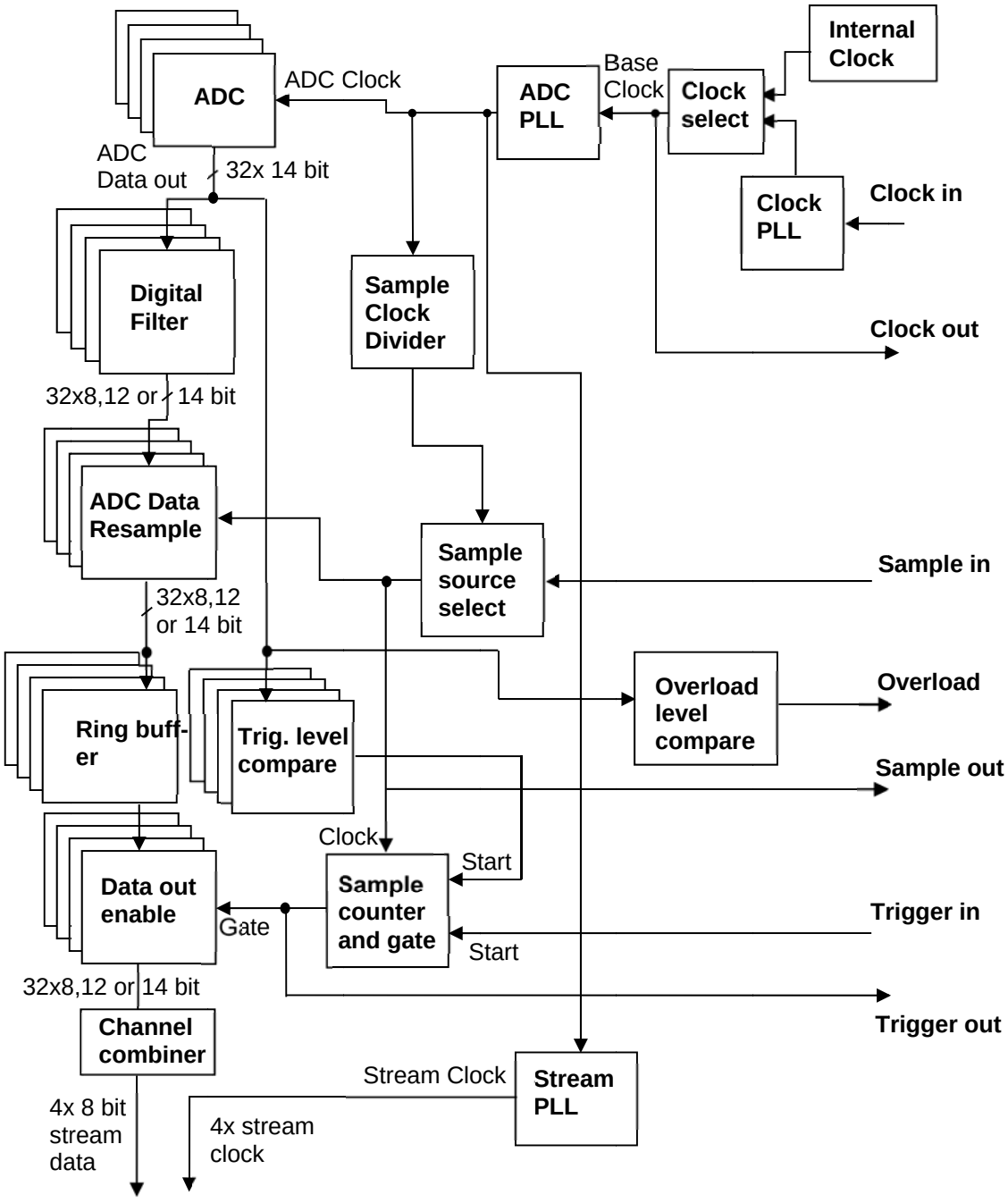


Figure 1. Block scheme of the data acquisition unit.

If the recursive filter is not to be used, `COEFF_06`=0. The impulse transfer function h_i of the FIR filter should be calculated at 5 points using $1/f_{ADC}$ as the time resolution of the function. This can be done with some filter design toolbox. If the FIR filter is not to be used h_1 is 1, all the others are 0. These h_i coefficients should be normalised by their sums and multiplied by (4096-c)/8 to yield the coefficients of the FIR filter:

$$\texttt{COEFF\_0}i = \frac{h_i}{\sum_{i=1}^{5} h_i} \ (4096\text{-}\texttt{COEFF\_06})/8, \qquad i=1...5.$$

The two last coefficients should always have the same value:

$$\texttt{COEFF\_07} = 0, \qquad \texttt{COEFF\_08}=9.$$

The filter coefficients are listed for selected cases in *Table 7*. Here the ADC frequency is assumed to be 10 MHz. If a different ADC frequency is used all frequencies should be scaled proportionally.

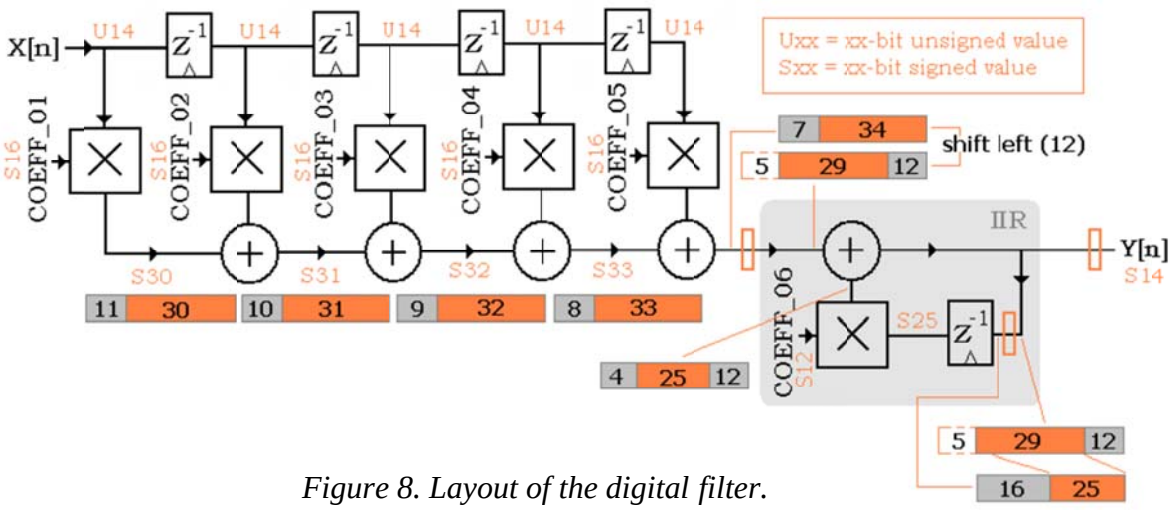


Figure 8. Layout of the digital filter.

		Filter Coefficients `COEFF_01...COEFF_08`							
f_{REC} [MHz]	f_{FIR} [MHz]	01	02	03	04	05	06	07	08
50.0	5.0	2048	0	0	0	0	0	0	11
50.0	2.0	1160	00808	00192	-80	-40	0	0	11
50.0	1.0	760	656	408	168	32	0	0	11
0.5	5.0	552	0	0	0	0	5982	0	11
0.5	2.0	312	216	48	-16	-8	5982	0	11
0.5	1.0	200	176	104	40	8	5982	0	11
0.1	5.0	120	0	0	0	0	7692	0	11
0.1	2.0	64	48	8	0	0	7692	0	11
0.1	1.0	40	40	24	8	0	7692	0	11

Table 7. Filter coefficients for some selected cases for f_{ADC}=10MHz.

Figure 9. shows the simulated frequency transfer functions of the same cases. From these it is clear that the FIR filter is effective down to about 1/10-th of the ADC frequency. For lower frequency cutoffs it can be used in combination with the recursive filter. The recursive filter works at least down to 100 kHz, but at these low frequency cuts the FIR filter has no effect.

After the filter the desired number of output bit resolution (8,12 or 14 bits, see RESOLUTION register) is selected by keeping the most significant bits.

The resulting amount of data could not be transferred through the Ethernet connection when all the channels are operating, therefore some data reduction is needed. This can be done either by reducing the number of active channels or by resampling the data (decimation) to lower frequency.

Channels can be enabled individually, see CH_ENABLE register.

Resampling can be done for all active channels in the same way. The resampling clock can be either a divided version of the ADC clock (see register SAMPLEDIV_X_7) or it can be an external input clock. In this latter case it has to be noted, that the data acquisition unit will not sample exactly at the time of the input clock pulse, but will take the latest sample when the sample clock arrives. Depending on ADC clock This can result in 20...100 ns jitter.

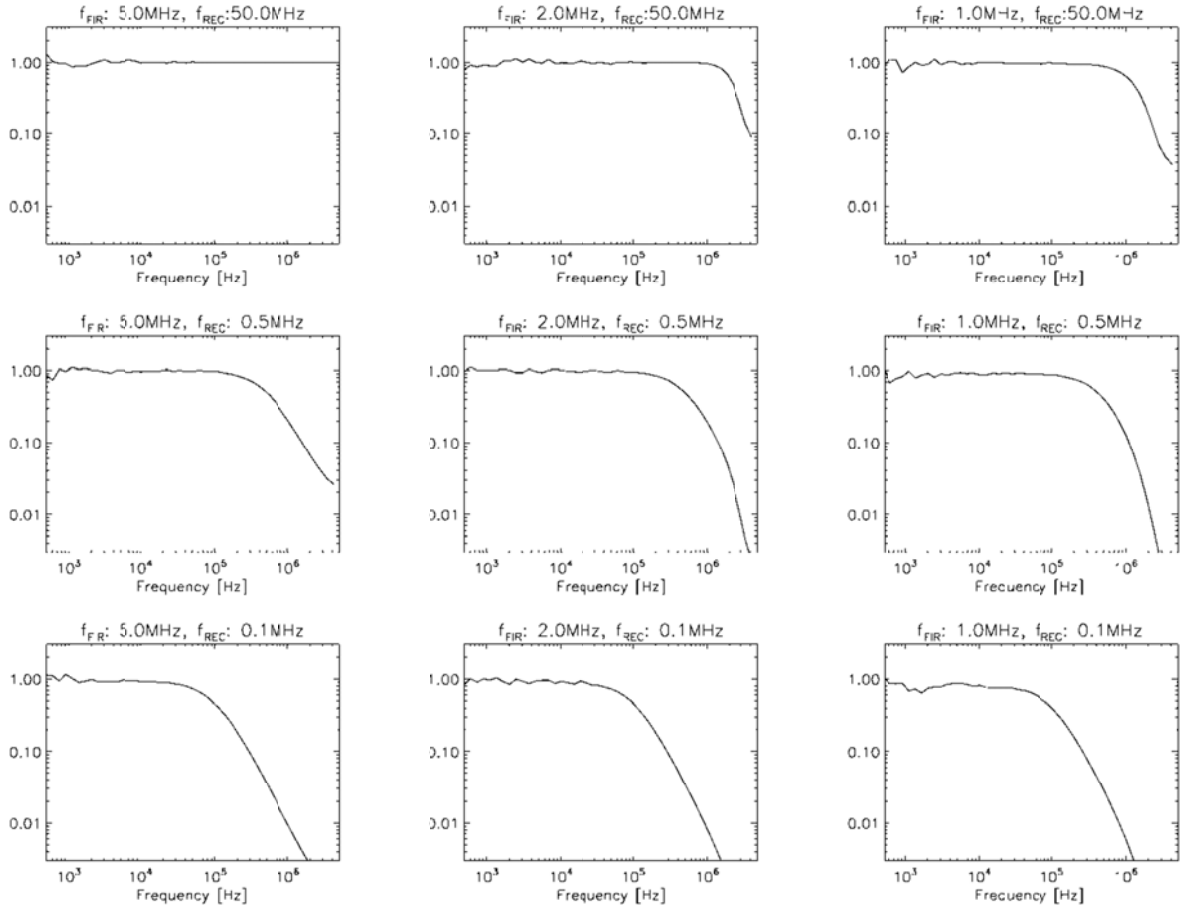


Figure 9. Simulated frequency transfer functions of the filter cases listed inTable 7. Filter coefficients for some selected cases.Table 7 .

By balancing the bit resolution, the channel number and the resampling rate the bandwidth of the data transmission can be used optimally. E.g. 10 MHz/12bit measurement is possible if one channel is selected in each block or 2 MHz/12bit if all 32 channels are working.

2.3.3. Triggering, overload protection

The ADC measurement, digital filtering and resampling works continuously in APDCAM. but data output to the host is enabled only when data is needed. The first requirement for data transmission is that the STREAM_CTRL bits should be set to enable data output from the four 8-channel blocks of the DAQ unit to the Gigabit card. If no triggering scheme is enabled data transmission starts immediately.

When the data transfer is started a certain number of samples per channel (SAMPLE_NUMBER register) are transmitted to the host and after that the data transmission is stopped. The exception is when SAMPLE_NUMBER=0 for which the transmission runs for an unlimited time. The actual number of transmitted samples are shown in 4 32 bit long ACT_SAMPLE registers.

Triggering of data transmission can be achieved using several schemes:

- **External trigger.** Bit 0 or 1 of the TRIGGER register should be set and the TTL trigger signal connected to the Trigger In connector. Depending on the bit set the trigger event happens on rising or falling edge.
- **Internal trigger.** This enables starting the data acquisition when the signal level in the detector channels is above or below some level. This is not an edge trigger mode, which means that if the stream inputs are enabled when the level fulfils the condition the measurement starts immediately. Internal trigger is globally enabled by bit 2 of the TRIGGER register while the 32 INT_TRIG_LEVEL registers set the internal trigger parameters for all channels independently. Bit 15 enables, while bit 14 sets the polarity for the corresponding channel. the trigger level is set by the 14 least significant bits. The trigger event happens when any of the 32 channels fulfils the trigger condition. It has to be emphasized that light input to the detector causes negative signal, therefore for triggering on rising light negative trigger should be set.

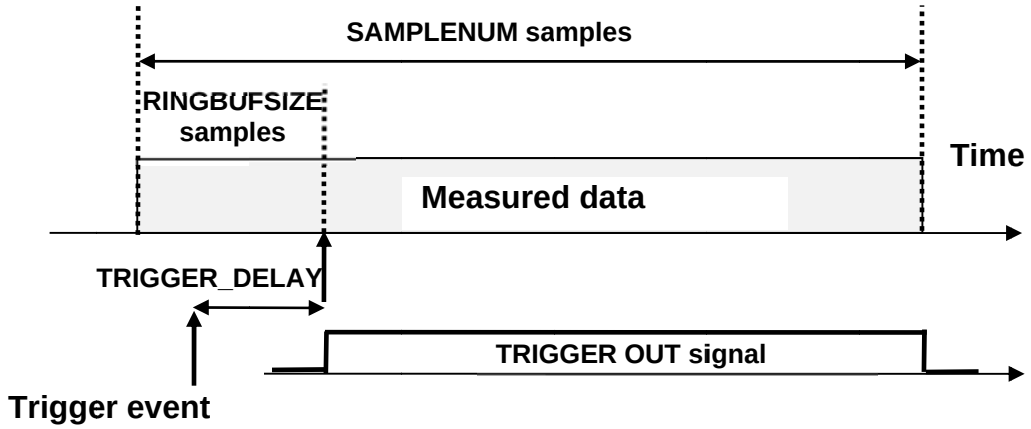


Figure 10. Triggered start of measurement.

After the trigger event the data transmission can be delayed by setting the TRIGGER_ DELAY register which allows several ten second delay. After the TRIGGER_DELAY time data transmission starts and the Trigger Out signal goes to H on the backplate. At the same time the Data LED shows the active data transmission.

Data from the measurement are continuously filling a ring buffer which size can be set in register RINGBUFSIZE. This enables a post-trigger capability that is, samples acquired before the trigger event can be transmitted. This is extremely useful when APDCAM is measuring a fast transient event as the staring phase can be measured without any external trigger.

The timing scheme of a triggered measurement *is shown in Figure 10.*

A separate scheme, similar to the internal trigger, is used for overload protection of the detector. Although it is protected from excess light imput under very unfavourable conditions a long-term overload might cause considerable power dissipation in the detector which might in turn result in damage. To avoid this an overload protection scheme can be switched on in the OVERLOAD register. Bits 14 and 15 should be set to 1 to enable the overload feature and the desired overload level should be entered in bits 0...13. A typical level would be close to 0 as the detector delivers negative signal. An overload event is generated when any of the signals fulfills the overload condition for more than OVERLD_TIME. The overload event switches off the detector bias voltage and lits the red Overload LED on the backplate. The status of the overload can be read from OVERLD_STATUS and writing any value into this register clears the overload. The bias voltage should be switched back in the Control unit. This overload protection works without the measurement enabled.

2.3.4. Data output format

After a trigger event or stream enable first a preamble block is sent to the output data stream. This identities the start of the data and contains the stream ID. After that data is sent in identical sample blocks each containing data from the same sampletime of all the enabled channels of the given 8-channel ADC block. The data bits are packed bit-continuously into the sample block and padded to the next full byte. Details are described in section **Hiba! A hivatkozási forrás nem található.**.

2.3.5. Offset control

The sensitive analog amplifiers or the detector leakage current can cause a drift in the detector offset voltage. To compensate for this the DAQ unit contains 32 12bit Digital to Analog Converters (DACs) which can be used to shift the analog input signal to the ADC. The corresponding values can be entered in the OFFSET register. These values are 12bit unsigned numbers, increasing values shift the in put signal to higher values. As the analog amplifiers deliver negative signal the offset should be set close to the upper limit of the ADCs. Typical needed values are in the 700-900 range.

2.4. Control unit

The Control unit fulfils the following tasks:

- Detector bias voltage setting
- Detector temperature control,
- Shutter open/close,
- Calibration light setting,
- Temperature measurements,
- Fan control for regulating the camera internal temperature.

The operating parameters of the Control unit can be found in its register table listed in *Table 8 and Table 9*. The unit stores its actual settings in an EEPROM non volatile memory. After power on the registers marked with EEPROM reload their data from this storage. These way settings need not be always re-entered from scratch. There is one important exception from this rule, the BIAS_ON and BIAS_ENABLE registers are set to 0 on power on. This causes the detector voltage to be switched off but the set value preserved in BIAS_SET.

The factory default values can be recovered by writing a code into the FACTORY_RESET register.

The electronics version code and the microcontroller program version code can be read from the BOARD_VERSION and MC_VERSION registers, respectively. The unique serial number of the board is stored in BOARD_SERIAL.

After power-up the red-green bicolor Control LED is lit green on the camera backplate. If the Control unit encounters a fatal problem this LED is red.

2.4.1. Detector bias voltage setting

In order to prevent accidental setting by e.g. software error the detector bias voltage is set in several steps. First the required value is entered in the BIAS_SET register. Please note the conversion factor. The Control unit limits bias voltage to a maximum value (BIAS_MAX) set during factory calibration. This aims at setting a detector-specific maximum. If the user tries to set a bias voltage higher than this maximum only the maximum will be set and an error code is written into ERROR_CODE.

After setting the voltage the output should be enabled by writing code hex $AB to BIAS_ENABLE. As a final step the voltage can be switched on by setting bit 0 in BIAS_ON. The actual bias voltage can be read in BIAS_MONITOR. After the switch-on procedure the set value can be changed if a different voltage is intended to be set.

When the bias voltage is enabled and switched on the blue HV LED is lit on the camera backplate.

2.4.2. Temperature control

The detector can be cooled/heated by a Peltier element. Depending on its current direction this pumps heat in either directions between the detector and a heatsink. The detector temperature is measured and available in TEMP_DETECTOR. This value is compared by the control unit against a set value (DET_TEMP_SET) and the Peltier current is driven through a PID controlled. The weight factors of this can be set in the PID_P, PID_I, PID_D registers. For strongly different temperature settings these might need to

be modified from the factory default. The actual Peltier current can be read in PELTIER_OUT. The operation of the temperature control can be suspended if all three PID_x registers are filled with 0. This means no current will be driven through the Peltier element.

The camera internal temperature is controlled by three variable-speed fans located on the top of the housing. They are controlled by the Control unit using measured temperatures in the camera (TEMP_xxx registers). From the detector side the first fan cools the detector housing and the DAQ card. The second moves air through the heatsink of the Peltier element. It will switch on gradually when the heatsink is either cooler or warmer than 25 degrees. The third fan cools the Control unit, power supplies and communication cards. The actual fan speeds can be read from registers FAN_xxx.

The temperature control scheme of APDCAM is highly reconfigurable by special configuration programs from the PC. If the camera is intended to be operated in an environment where the temperature is significantly different from room temperature or when the fans need to be controlled manually please consult the manufacturer.

2.4.3. Shutter and calibration light

The shutter is mounted in front of the detector but behind the camera window. It is operated with and electromagnet controlled from the Control unit. In its basic setup (SHUTTER_MODE=0) the SHUTTER_STATE register opens and closes the shutter. The drive electronics is not designed to open/close the shutter at high frequency, but it is intended for single open/close cycles every few seconds as the shortest period time. The shutter can be kept open or closed for any time. When the shutter is open the yellow Shutter LED is lit on the camera backplate.

In SHUTTER_MODE=1 the shutter can be controlled externally by an electrical signal. For this the shutter signal should be routed to the Optional signal connector in the backplate using an internal jumper. The shutter state signal can also be output on the same connector. Please consult the manufacturer if such operation is needed.

The aim of the calibration light is to enable verification of the detector operation, measurement of SNR levels and noise spectra with variable light input. It is intended neither for absolute calibration of the sensitivity nor for relative calibration of the pixels.

The light source is an ultra bright red LED. To avoid any electrical interference the LED is mounted in the Control unit and the light is coupled into the detector housing using four 1 mm diameter optical fibres. These illuminate the detector from four directions providing more-or less uniform illumination. The current of the LED is provided by a current generator which can be controlled digitally through the CALIB_LIGHT register. At 0 settings there is no light emission. At about 100-200 the light saturates the detector amplifier with ~350 V detector voltage. As the detector gain is typically around 30-50 at this bias voltage the maximum light emission at 4095 approximately saturates the detector with low gain around 200 V. (Below 150 V bias voltage the amplifiers show excessive noise.)

When the calibration light is on at any level the yellow Calibration LED is lit on the camera backplate.

Parameter	*R/W*	*Offset (byte)*	*Size (byte)*	*Value after start*	*Description*
BOARD_VERSION	R	0	1	factory	Board version code. Bits 0...4: Version Bits 5...7: 2
MC_VERSION	R	2	2	factory	Microcontroller program version code.
BIAS_MONITOR	R	4	2	actual	The measured detector bias voltage. The conversion factor is 0.12V/digit.
TEMP_ADC	R	12	8	actual	The temperature of the 4 ADC blocks. (2 bytes each in 0.1 ºC units.)
TEMP_DETECTOR	R	20	2	actual	The temperature of the detector in 0.1 ºC units.
TEMP_ANALOG	R	22	2	actual	The temperature of the analog amplifier in 0.1 ºC units.
TEMP_DETHOUSE	R	24	2	actual	The temperature of the detector housing in 0.1 ºC units.
TEMP_PELTIER	R	26	2	actual	The temperature of the Peltier cooler/heater heatsink in 0.1 ºC units.
TEMP_CONTROL	R	28	2	actual	The temperature of the Control unit heatsink in 0.1 ºC units.
TEMP_BASE	R	30	2	actual	The temperature of APDCAM baseplate in 0.1 ºC units.
TEMP_DAQ	R	40	2	actual	The temperature of the DAQ unit FPGA in 0.1 ºC units.
PELTIER_OUT	R	44	2	actual	Signed 2-s complement 16 bit value representing the status of the Peltier cooler/heater. Negative values mean cooling, positive heating. The maximum is about 4000.
PID_P	R/W	80	2	EEPROM	Weights of the P, I and D components of the detector temperature controller.
PID_I	R/W	82	2	EEPROM	
PID_D	R/W	82	2	EEPROM	
BIAS_SET	R/W	86	2	EEPROM	The set value of the detector bias voltage. The conversion factor is 0.12V/digit.
BIAS_ON	R/W	94	1	0	Bit 0 switches on the detector bias voltage. The bias voltage should be enabled first in BIAS_ENABLE.
BIAS_ENABLE	W	96	1	0	A hex $AB (decimal 171) should be written into this register to enable detector bias voltage.
DET_TEMP_SET	R/W	106	2	EEPROM	The detector temperature set value. This is the reference for the Peltier PID controller. (0.1 ºC units.)
FAN_PELTIER	R	108	1	actual	The actual speed of the fan cooling the Peltier heatsink (range 0...255).
FAN_ELECTRONICS	R	110	1	actual	The speed of the fan cooling the electronics (except DAQ) (range 0...255).
FAN_DAQ_DET	R	112	1	actual	The speed of the fan cooling the DAQ and the detector shielding (range 0...255).
CALIB_LIGHT	R/W	122	2	EEPROM	The current of the calibration LED. (valid: 0...4095). 0 means no light.

Table 8. Register map of the Control unit, part one.

Parameter	*R/W*	*Offset (byte)*	*Size (byte)*	*Value after start*	*Description*
SHUTTER_MODE	R/W	128	1	EEPROM	Bit 0 controls shutter mode. 0: Shutter controlled by SHUTTER_STATE 1: Shutter controlled from Opt. connector if set up in factory.
SHUTTER_STATE	R/W	130	1	EEPROM	Bit 0 controls shutter state in manual mode. 0: closed, 1: open.
FACTORY_RESET	W	132	1	0	Writing hex $CD (decimal 205) into this register causes all settings to return to factory default.
ERROR_CODE	R	134	1	0	Error code. (Write 0 to erase.) 0: No error 0x41: BIAS_SET set higher than BIAS_MAX. 0x50: Write attempt to read only register. 0x7C: Peltier controller has no valid weight values or temp sensor error.
BOARD_SERIAL	R	256	2	factory	Board unique serial No.
BIAS_MAX	R	258	2	factory	Maximum allowed value for detector bias.

Table 9. Register map of the Control unit, part two.

2.5. Ethernet Communication

Communication over the Ethernet connection is performed using a Gigabit Ethernet Controller (GEC) by ByteStudio Ltd. This device receives data in four 8-bit streams, packs it into UDP datagrams and sends them to a destination address. Additionally to the data transmission to the PC the card can also communicate with the APDCAM DAQ and Control units on an internal bus and arrange register read-write operations between the PC and APDCAM. Communication on this internal bus is shown by blinking of the green Communication LED on the camera backplate. Details of the GEC card are described in its own documentation.

The GEC has a standard electrical Gigabit connector. Below it the green Gbit LED indicates when Gigabit communication is set up with the host. If this is not possible GEC falls back to 100 Mbit or 10 Mbit speed.

To allow long-range fibre optic communication with APDCAM a D-Link DMC-700SC UTP-fibre media converter has been integrated into APDCAM. To use fibre communication a short UTP cable can be connected between the GEC UTP port and the fibre media converter. The fibre cable should be connected to the media convert's fibre port. The connector type is duplex SC, the fibre cable is multimode. The fibre communication signal should be converted back to UTP on the camera side. For the camera side conversion the same unit (D-Link DMC-700SC) is recommended. There are two jumpers on this card, they should be set as follows:

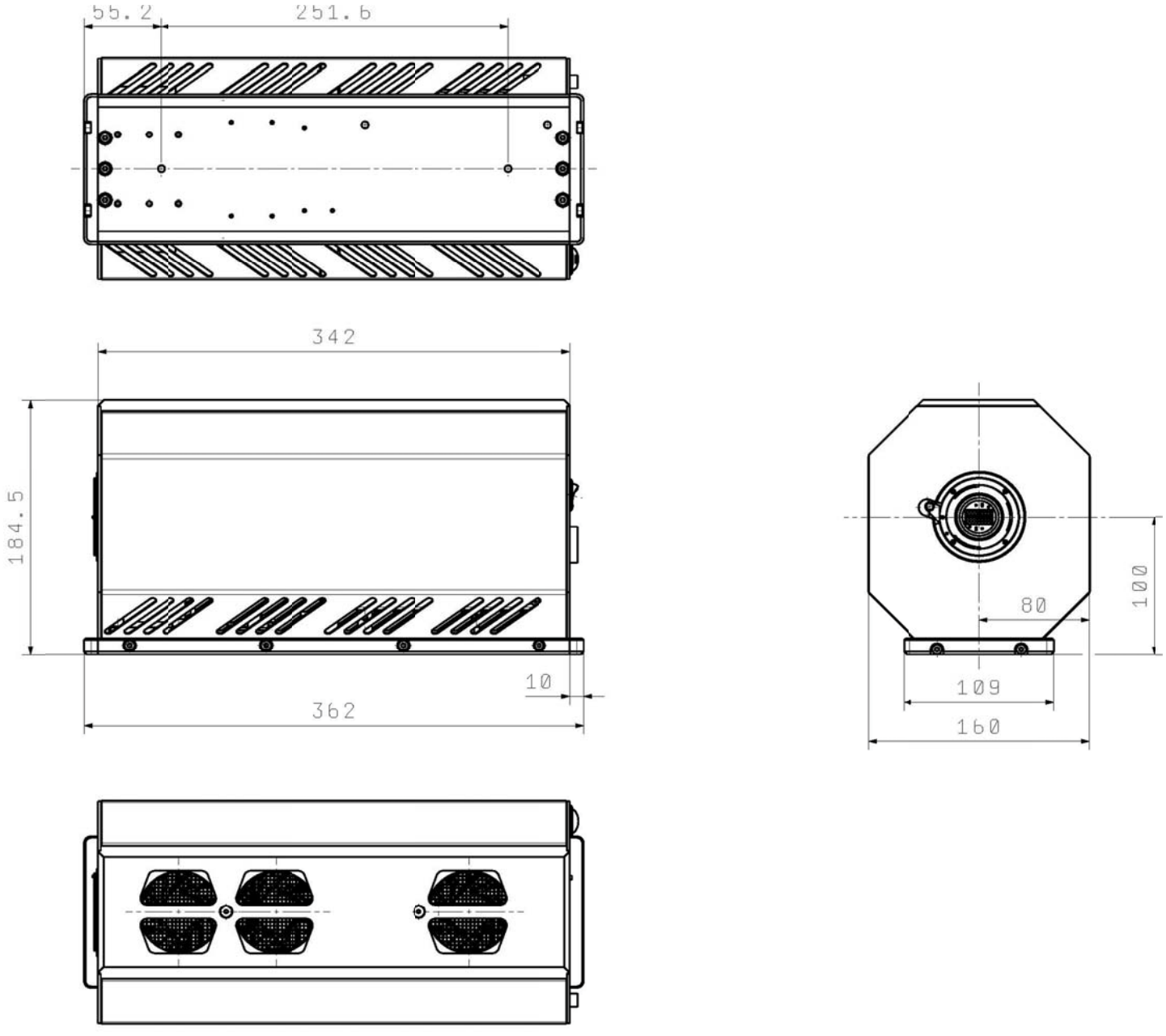
SW1: on (forced)
Sw2: off

2.6. Software interface

Control of APDCAM is performed using an Application Programming Interface and the APDTest scriptable program. Both are documented in the API description.

Appendix A: Mechanical dimensions

The figures below show the main dimensions of APDCAM. For more information please consult the manufacturer.



Appendix B: Troubleshooting

This section helps to solve some common problems which might occur during the use of APDCAM.

Signals are oscillating or clamped at min/max of measurement range

If the detector bias voltages are not on the amplifiers oscillate or clamp. Set a minimum of 200 V detector bias voltage.

Setting factory defaults

If the camera configuration becomes corrupted or the IP address is changed and lost it might be necessary to reset the camera to the factory default configuration. This can be done in two ways:

- Pressing the Reset buttton on the backplate resets all components
- Setting the appropriate code in the factory reset register of the individual ADC and control units.

Please note that reset might change some factory adjusted parameters in the camera. If problems found after reset please consult the manufacturer. Factory setting can be set back by a special setup program sent by the manufacturer on request.

Some pixels stop working when the detector is strongly cooled.

If the detector is operated considerably below room temperature and/or the ambient humidity is high moisture might condense on the detector and cause failure of operation in some pixels. If such a problem is suspected the detector temperature has to be set to above room temperature (e.g. 40C) for several hours. If the pixels shoe normal offset and noise no additional action is required.

Some data are lost during measurement, APDTest program indicates "Continuity error".

This problem occurs if the computer cannot receive or process the received data fast enough. There might be various reasons behind:

- The camera is not connected to a dedicated Gbit interface and traffic on the Ethernet line reduces the data bandwidth. Always use a dedicated Ethernet line for the camera.
- The Ethernet line quality is low, not suitable for Gbit communication. For longer distances use CAT5 or better cable or use optical communication.
- The computer (especially laptops) might be configured not to use maximum CPU or PCI bus speed. Laptops are often configured in a way that when running on battery performance is reduced. Set CPU and PCI bus speed to maximum.
- The computer might not be fast enough or some programs limit performance. In some cases it was found that E.g. skype and certain virus protection programs or firewalls, dropbox can deteriorate the network performance.

- Under Linux set up network buffers and other parameters as described in Section 1.7.2

Program crashes when trying to allocate memory under Windows.
Under Windows operating systems it has to be enabled that the program fixes allocated memory in physical address space. The procedure is described in Section 1.7.1.

Appendix C: Order options

APDCAM devices are all manufactured individually taking into account the needs of the customer. The following table lists the standard options which can be specified at order time. More customized versions are also possible, please ask.

APDCAM 1G specification sheet		
Option	Value	Comment
Magnetic field hardening	Yes/No	Yes: Camera can operate in magnetic fields up to 100 mT
Optical interface	F-mount/None/Special	Standard is F-mount None: rectangular socket with 4 screwholes Special: special insert in rectangular socket (additional price)
Optical window	BK7 with broadband coating/None/Special	Standard is BK7 with broadband coating
Micro-lens array	Yes/No	additional price
Fan speed	Fixed/Software	
Analog sensitivity and bandwidth		0: 1 MHz, low standard sensitivity 1: 250 kHz, high sensitivity 2: 100 kHz, high sensitivity 3: 70 kHz, high sensitivity
Amplifier gain		Standard is 50
Optional connector signal	Shutter control (input) Shutter state (output) HV state (output) HV trip (input) Spare out (output)	