

# Low Power RF Designs Layout Review Techniques

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# Abstract

- The presentation provides guidelines and a checklist to copy TI reference designs for optimum performance. It explains basic concepts for a RF PCB design. It also provides various commonly-made RF PCB design mistakes. Following the suggested recommendations will allow the designers to have designs with optimum performance on their first board fabrications reducing design time and the costs involved.

# Outline

1. Basics of RF PCB Design
2. Copying TI Reference Designs
3. Commonly Made Mistakes
4. Debug Socket on the Design
5. Questions

# Basics of RF PCB Design

# What does an RF PCB look like?

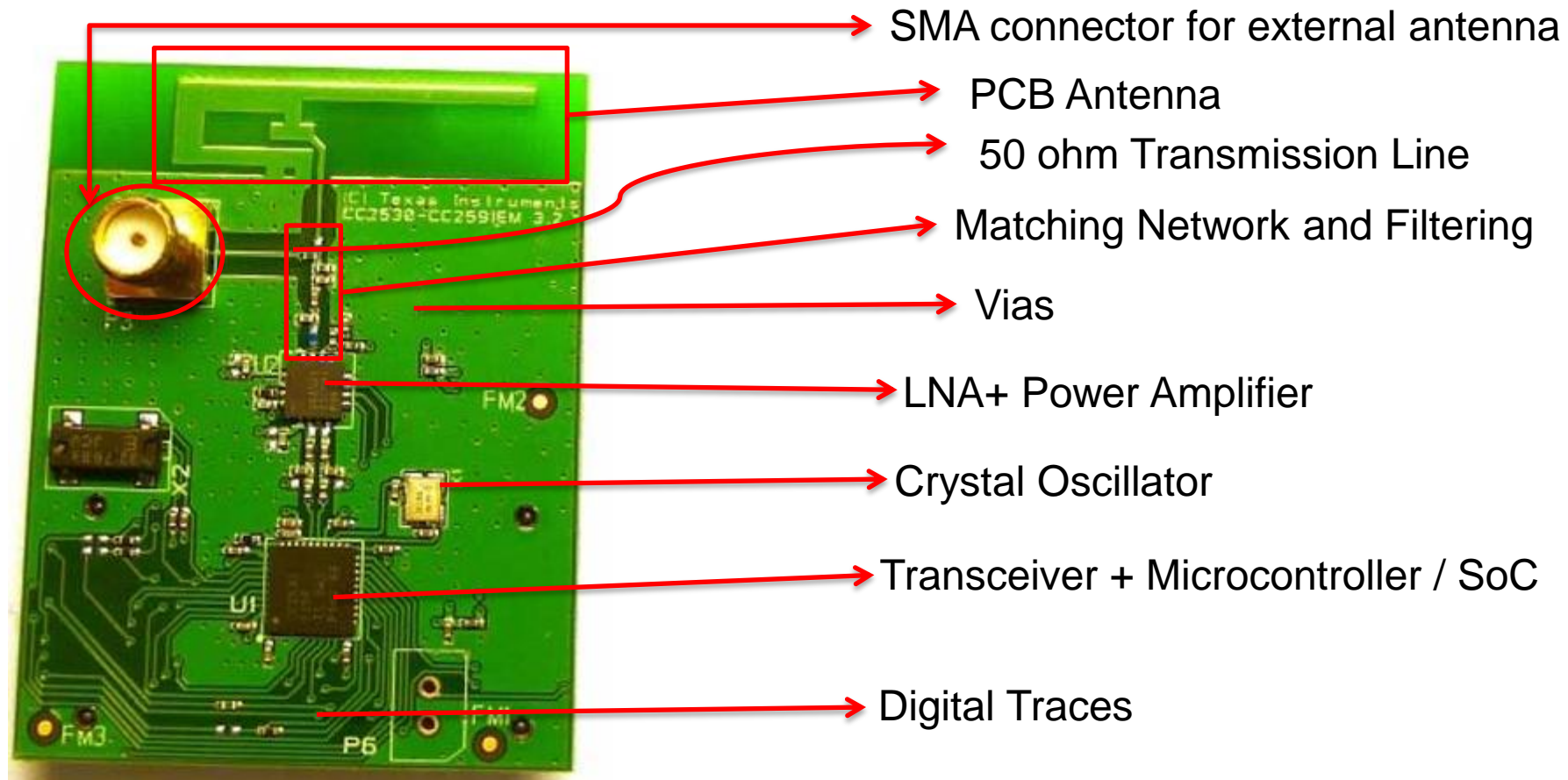


Fig: CC2530 – CC2591 Evaluation Module

# RF Transmission Lines

- PCB traces at radio frequencies have to be designed carefully to account for their distributed character due to their small size as compared to the wavelength.
- Impedance of a single micro-strip trace over a ground plane depends primarily upon
  - Width of the trace
  - Height above the ground plane
  - Dielectric constant of the PCB's dielectric
  - Loss Tangent of the PCB's Dielectric
  - Distance to nearby trace or the ground pour on same plane
- A simplified formula for calculating the impedance is [1]

$$Z_0 = \frac{60}{\sqrt{\epsilon_{eff}}} \cdot \ln \left( \frac{8h}{w} + \frac{w}{4h} \right) \quad \text{where} \quad \epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[ \frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.04 \left( 1 - \frac{w}{h} \right)^2 \right]$$

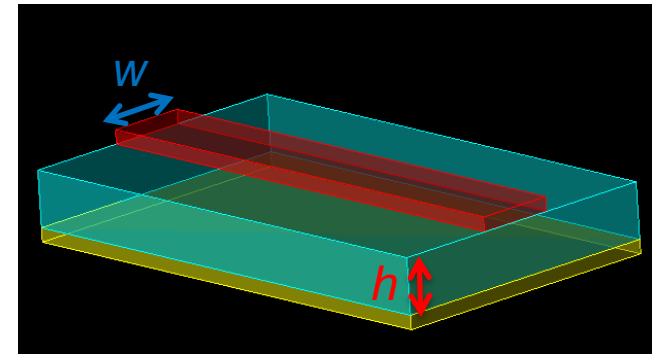


Fig: Micro-strip line

- Rule of thumb for FR-4 with  $\epsilon_r = \sim 4.5$ , for  $50\Omega \rightarrow w/h \sim 1.8$
- Various line impedance calculators are available for impedance calculations

[1]. David M. Pozar "Microwave Engineering – Third Edition", John Wiley 2005

# Ground Plane

- Return Current follows the path of least impedance
- If the ground plane/return path is divided, under the RF section
  - Return current paths may become longer → Higher spurious emission.
  - Add undesired inductance → Undesired performance.

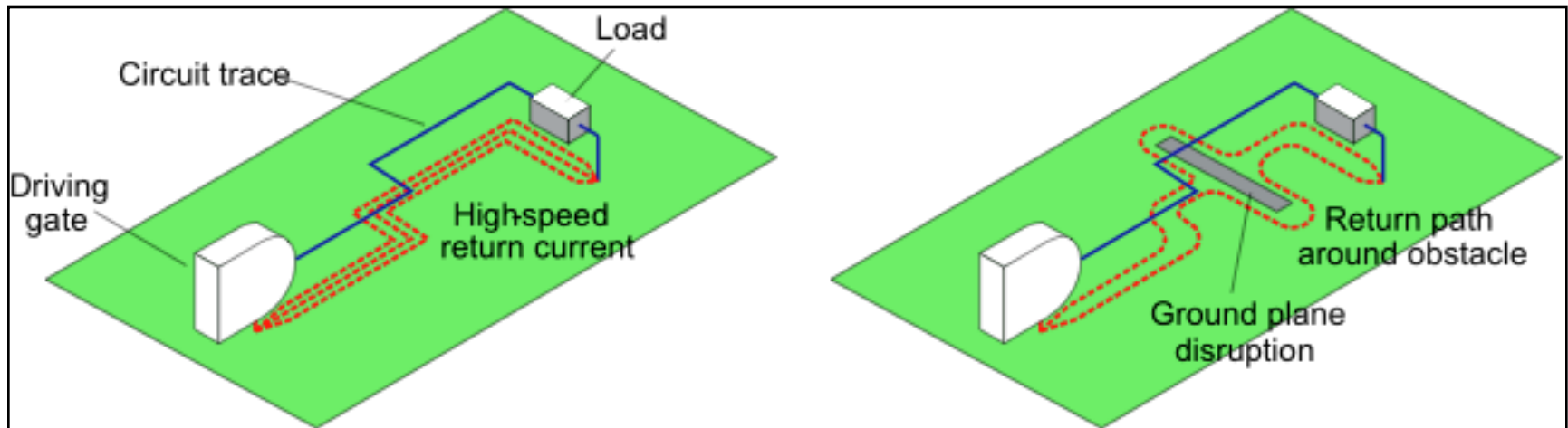


Fig: Showing the effect of slotted ground plane on return current path

# Ground Plane

- A continuous ground also provides for easy connection to the ground by allowing one to drop vias from the pads to be grounded.
  - No additional trace to connect to ground -> eliminates unwanted inductance.

## Reduce board radiations and coupling

- Fill the unused area on top plane with ground plane and then connect this top fill with the ground plane below with several vias spaced about  $1/10^{\text{th}}$  of the wavelength apart.
- Via Fencing : Having a grounded via shield around the RF section to protect the RF section from coupling to other sections on a larger board or from nearby interfering sources.
- Via Fencing also helps to reduce unwanted board edge radiations.

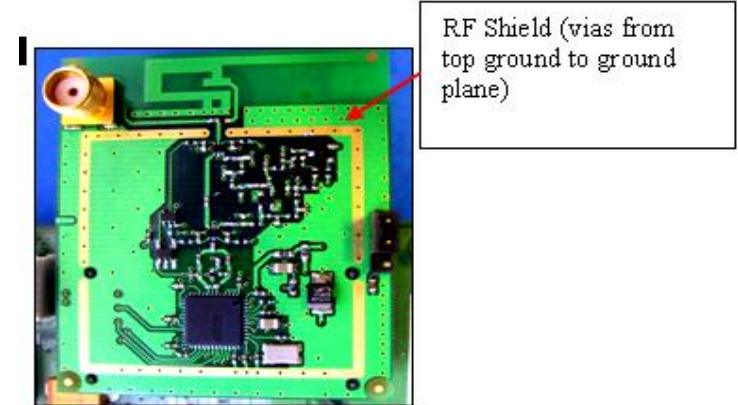


Figure: Showing RF design with Grounded Via Shield



# Power Supply Routing and Decoupling

Sources of high frequency noise on the power supply lines may be –

- Transient demand of current by active device
  - Generates high frequency harmonics.
  - The generated noise can travel to the power supply pins of the devices, producing undesired performance.
  - Solution - Power supply pins of the devices are bypassed to the ground plane using a capacitor which provides low impedance path for the high frequency noise.
- Crystal Oscillator/Digital section of the design switches rail to rail rapidly
  - Generates high frequency harmonics.
  - Can couple on the power supply lines
  - Solution - Power supply is routed and decoupled properly.
- Undesired coupling between the power supply lines.
  - Solution – Proper decoupling

# Power Supply Routing and Decoupling

- Bypass/decoupling capacitor must be carefully selected taking into consideration the self resonance frequency (SRF) of the capacitor.
- Above the SRF the capacitor behaves as an inductor.

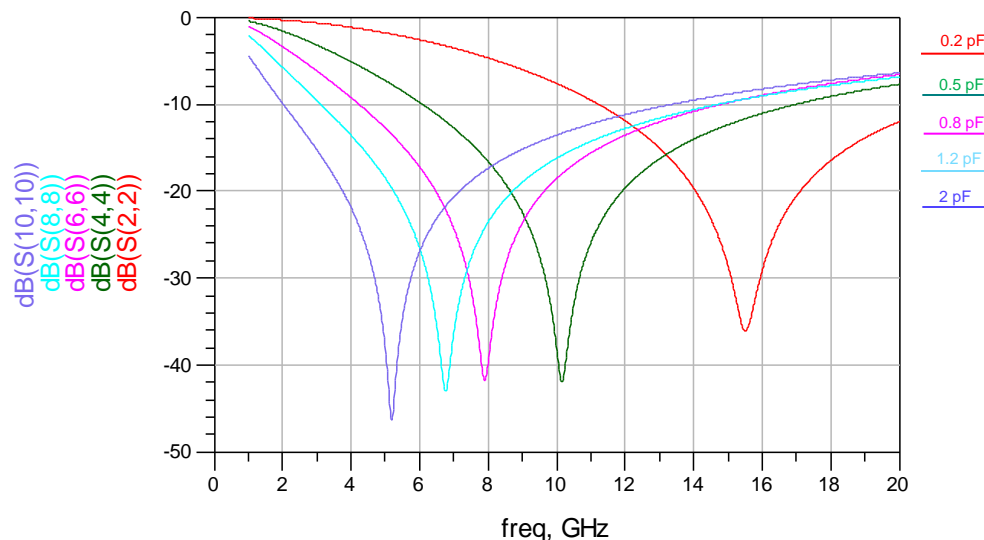


Figure: SRF vs. Capacitor Value (This is a general representation of SRF variation with capacitor values but capacitor of different types and from different vendors will have different SRF)

- Recommendation - Follow the TI reference designs

# Component Orientation

- Inductors and capacitors on the PCB have associated with them a electromagnetic fields that can couple with other components and can affect the design performance in undesired manner,
  - Do not place parallel inductors/capacitors close to each other unless it is required to utilize the field coupling.
  - If required, place components perpendicular to each other to minimize coupling.
- TI reference designs are designed carefully considering such coupling effects, and thus it is recommended to follow the component placement and orientation on TI reference designs.

# Board Stack-up

- RF PCB designs are usually designed on 2- or 4-layer boards
- 2-layer PCB board design
  - Provides cost savings compared to a four layer PCB design
  - Can provide comparable performance to a four layer design, but requires careful signal routing and component placement.
- 4-layer PCB design
  - Provides easy routing for ground and power planes and relaxes routing considerations compared to a 2-layer PCB.
  - Provides easy decoupling of the power plane placed between the ground plane and bottom layer, which is predominantly ground.
  - In a 4-layer board it is recommended to have the layer structure as defined below.
    - 1<sup>st</sup> Layer: Component and Signal
    - 2<sup>nd</sup> Layer: Ground Plane (*Always below the component layer*)
    - 3<sup>rd</sup> Layer: Power Plane
    - 4<sup>th</sup> Layer: Ground Plane and Signal Routing

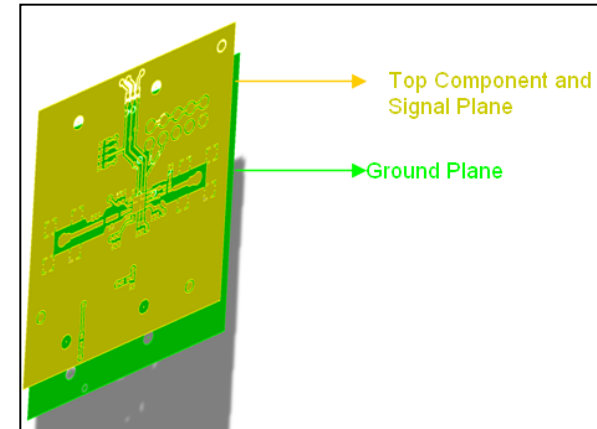


Figure: A general two layer RF PCB

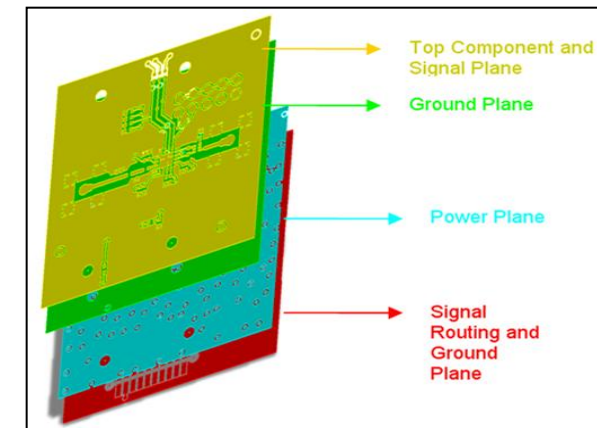


Figure: A general two layer RF PCB

# Copying TI Reference Designs

# Copying TI Reference Designs

- Step 1: Understand the PCB board properties
  - PCB stack-up
  - PCB board dielectric properties (dielectric constant and loss tangent).
  - TI reference designs include a document describing above properties
- If recommended specifications cannot be used in cases such as
  - Including design on existing boards.
  - Require translating a two-layer TI reference design to a four-layer PCB

Refer to the application note AN068 on how to adapt the reference designs for the board stack-up changes.
- TI reference designs includes a white box silkscreen that shows the extent of the RF layout.
  - Everything inside the box should be copied exactly for optimum performance.
  - Anything outside the box can be changed freely.
- Copy the design closely and follow the checklist

# Copying TI Reference Designs - Checklist

The checklist below provides important RF PCB design considerations to be followed

1. Verify the stack-up matches the reference design. If the design is a 4-layer PCB; verify that ground plane is layer two right below top/component side.
2. Changing the layer spacing/stack-up will affect the matching in the RF signal path and should be carefully accounted for as explained in AN068
3. Ensure that you follow the datasheet layout recommendation unique to the part (CCXXXX).
4. 0603 (mils) discrete parts are not recommended because of size and parasitic values.
5. Verify that bypassing/decoupling capacitors are as close as possible to the power supply pins that they are meant to bypass/decouple.
6. Ensure each decoupling capacitor only decouples the specific pins recommended on the reference design and that the capacitor is correct value and type.
7. Ensure that decoupling is done pin<>capacitor<>via to power.
8. Each capacitor shall have a separate via to ground

# Copying TI Reference Designs - Checklist

9. Verify that the ground plane matches the reference design. There should be a solid ground plane below the device and the RF path.
10. Verify that RF signal path matches the reference design as closely as possible. Components should be arranged in a very similar way and oriented the same as the reference design.
11. The crystal oscillator should be as close as possible to the oscillator pins of the part. Long lines to the oscillator should be avoided if possible.
12. Verify that the top ground pours are stitched to the ground plane layer and bottom layer with many vias around the RF signal path. Compare to the reference design. Vias on the rest of the board should be no more than  $\lambda/10$  apart.
13. If the part has differential output, ensure that the traces in the differential section are symmetrical as in the reference design.
14. If the reference design specifies using T-Lines (Transmission Lines), it is very critical to ensure that the T-Lines match the reference design exactly.
15. The board should specify impedance controlled traces. That is, the layer spacing and FR4 permittivity should be controlled and known.



# Copying TI Reference Designs - Checklist

16. Verify that the under-the-device power pad layout is correct. The solder pads and mask should match and the opening size should ensure correct amount of paste. Vias should be the correct number and masked/tented to ensure that they don't suck up all the solder, leaving none to solder the chip to pad. (Refer to the datasheet for the recommended layout for the corresponding part)

## Important considerations for Antennas:

18. If the design uses a battery (such as a coin cell), the battery will act as a ground plane and should therefore not be placed under the antenna.
19. If using an antenna from a TI reference design, be sure to copy the design exactly and check if the stack-up in the reference design matches your stack-up.
20. Changes to feed line length of antenna will change input impedance match.
21. PCB and chip antennas should not have any ground plane under them.
22. Any metal in close proximity, plastic enclosure, and human body will change the antennas input impedance and resonance frequency, which must be considered in the design.
23. For multiple antenna on same board, use antenna polarization and directivity to isolate.
24. For chip antennas verify that the spacing from and orientation with respect to the ground plane is correct as specified in their datasheet.

# Commonly Made Mistakes

# Long RF Trace Lengths and Mismatched Traces in Differential RF Sections

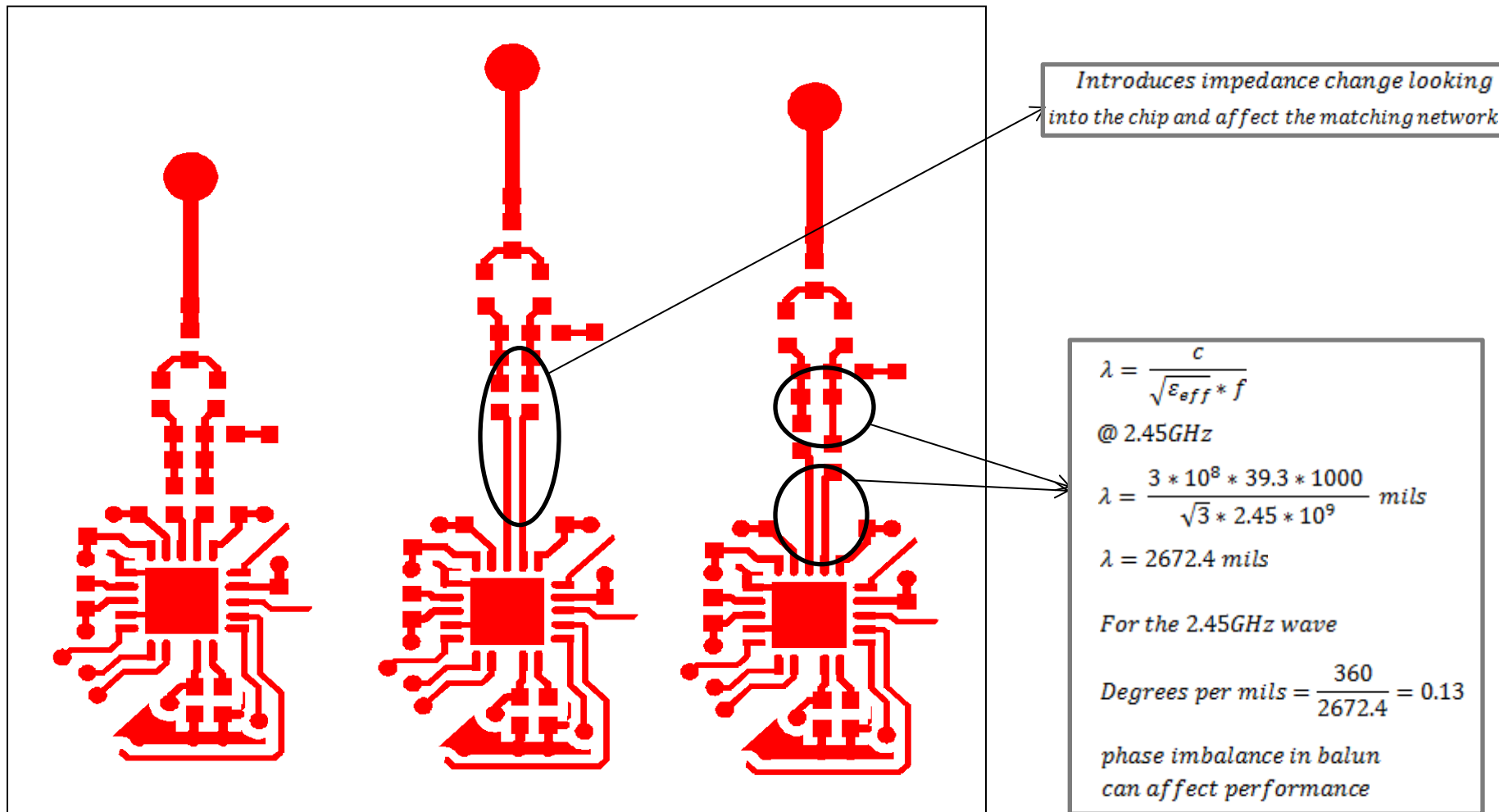


Figure: (a) Ideal Case (b) Extended RF Transmission Lines (c) Mismatched RF Lines

# Digital Lines Near/Below the RF Path

- Layout with digital traces near/below the RF path.
  - The transition on digital lines are rail to rail -> High Frequency Harmonics
  - Coupling with RF lines where the signal amplitude can be very small gives undesired operation.

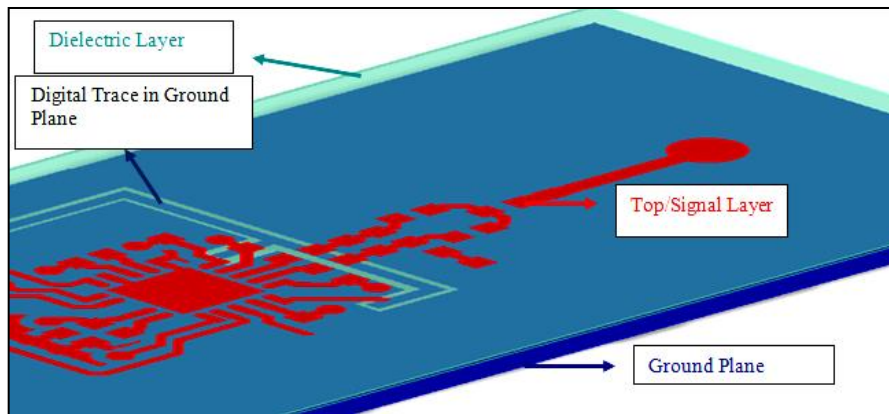


Fig: Example layout with digital trace below the RF path

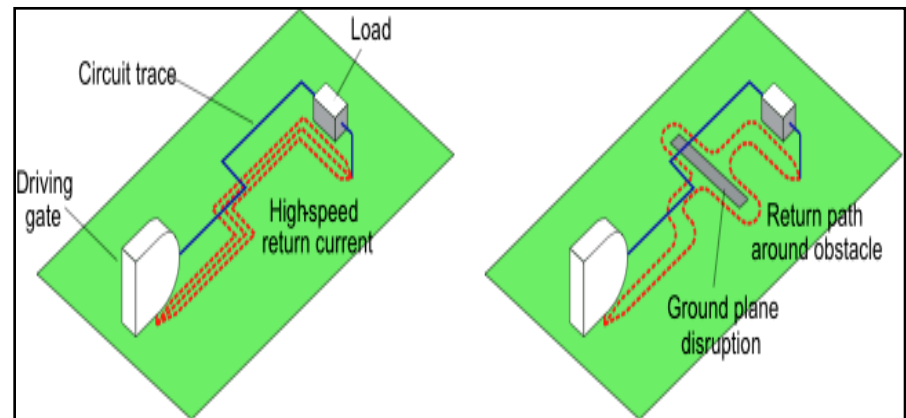


Fig: Showing the effect of slotted ground plane on return current path

- If digital trace is drawn on the ground plane under the RF section it introduces longer return paths for RF current, may cause undesired performance.
- Recommendation - Have a solid ground plane especially under the RF section.

# RF Trace near Crystal Oscillator Trace

- Crystal Oscillator switches rail to rail rapidly and generates high frequency noise.
- If placed near to RF traces coupling can result in un-desired performance

# Decoupling Capacitor Placement

- The layout should be via followed by capacitor connected close to the pin i.e. route the vias into the decoupling caps and then into the active component.
- The more vias the better to reduce inductance.
- The wider the power line traces the better .
- The closer the bypass cap to the pins on the active device the better

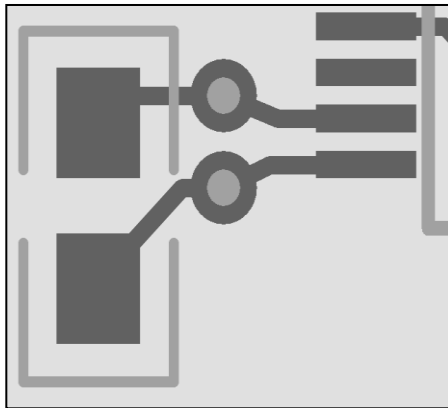
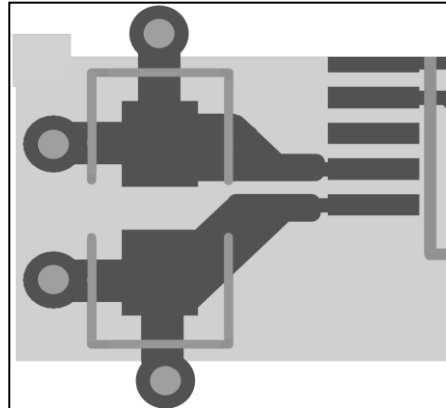


Figure: (a) Poor Bypassing Layout



(b) Good Bypassing Layout

# PCB Layers Swapped while Manufacturing

- One common mistake may occur when giving the final PCB design to the board manufacturing house by not defining the layer mapping
- This can cause significant effect on the performance of the design.  
Reason - change in the trace impedance caused by the increased distance between the top signal plane and the ground plane.

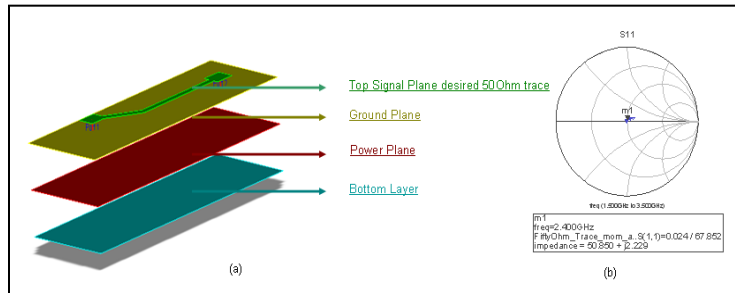


Figure: Showing desired board stack up. Top plane with desired 50ohm trace followed by ground, power and then bottom layer. The simulated impedance of the trace is shown in (b) to be  $50.85 + j*2.229$  at 2.4GHz

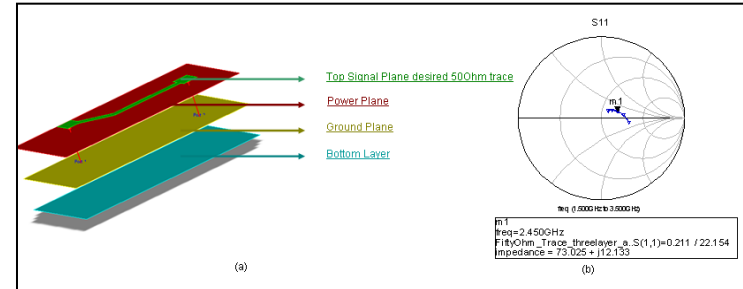


Figure: Showing board stack up with ground and power planes swapped. Top plane with desired 50ohm trace followed by ground, power and then the bottom layer. The simulated impedance of the trace is shown in (b) to be  $73.025 + j*12.133$  at 2.4GHz

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- Recommendation: Send a readme file (e.g., as included with the TI reference designs) or fabrication notes to the manufacturer or fill-out the online forms carefully.

# Silk Screen Below the Chip

- Silkscreen markings below the area where the chip is to be placed provides obstructions for the chip to be soldered properly to the PCB pads, leading to undesired performance

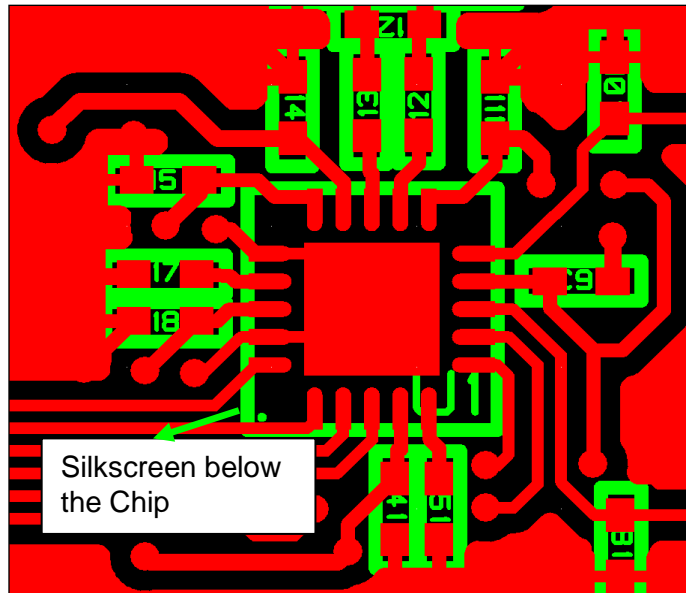


Figure: Showing Silkscreen markings in the area under the chip



# Power Pad Layout

- Power pad layout is critical for successful operation of a RF design using CCXXXX devices
- Used for ground connection and shall be connected to the ground plane with several vias for good thermal performance and sufficiently low inductance to ground.
- The datasheet (e.g., Figure) and the reference designs specify the layout for this section
- Important - Have the vias “tented” (covered with solder mask) on the component side/bottom side of the PCB to avoid migration of solder through the vias during the solder reflow process.

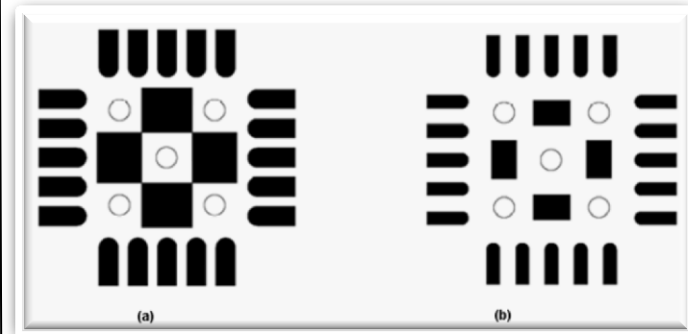


Figure: Showing an example of power pad layout given in the CC1101 datasheet. (a) Top Solder Resist Mask (Negative), (b) Top Paste Mask. Circles are Vias

# Trace Corners

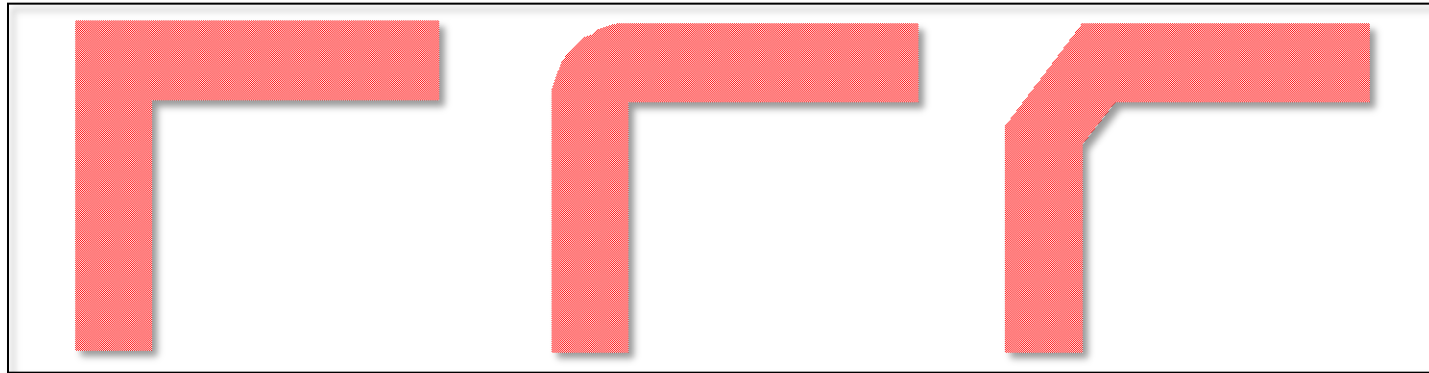


Figure (a) Bad

(b) Fair

(c) Good

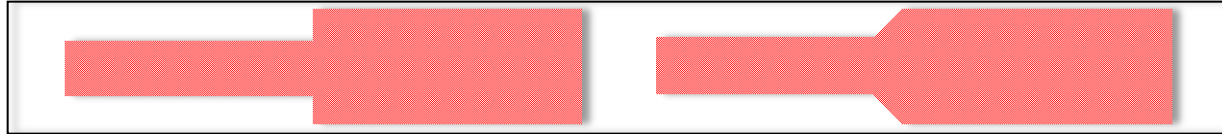


Figure (a) Bad

(b) Good

- Avoid sharp edges on the RF path to reduce the field radiations.

# T-Lines on CC2590/1 Designs

- T-Lines specified on pin 1,10 and 13 on CC2590/91 designs are critical for the design.
- Important to follow the length and width and “stack-up” for the T-lines

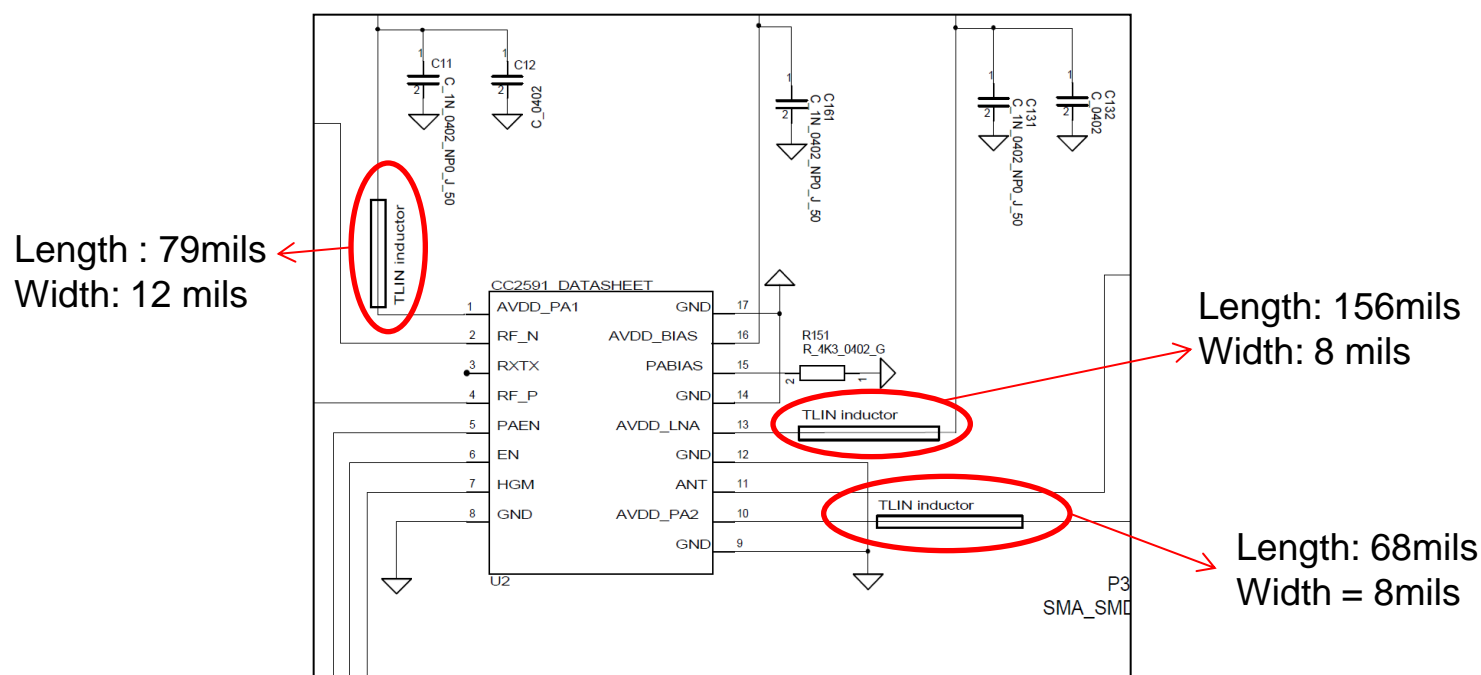


Figure: Snapshot from CC2520-CC2591 Reference design showing critical T-lines on CC2591

**Thank you for your attention.**

**Questions/Comments?**

# Debug Socket on the Design

# Debug Socket On Design

- A good method to perform quick RF performance checks of a design, such as PER, range, etc.
- SmartRF04EB, SmartRF05EB, CC-Debugger boards provide debug connector to interface custom designs to SmartRF™ Studio.
- The pin out of this 10-pin connector is given in table.
- Usually the prototype boards lack space for a 10-pin connector:
  - Required pins to interface a LPW transceiver are
    - CSn, SCLK, SI, SO, VCC and GND,
  - Required pins to interface LPW SoC devices are
    - DD, DC, Reset\_N, VCC and GND.

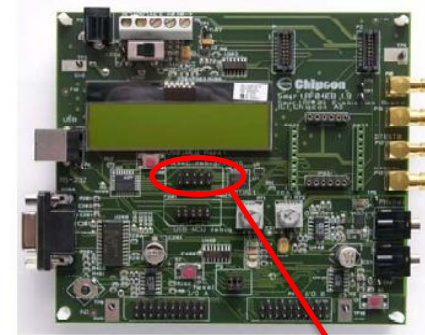


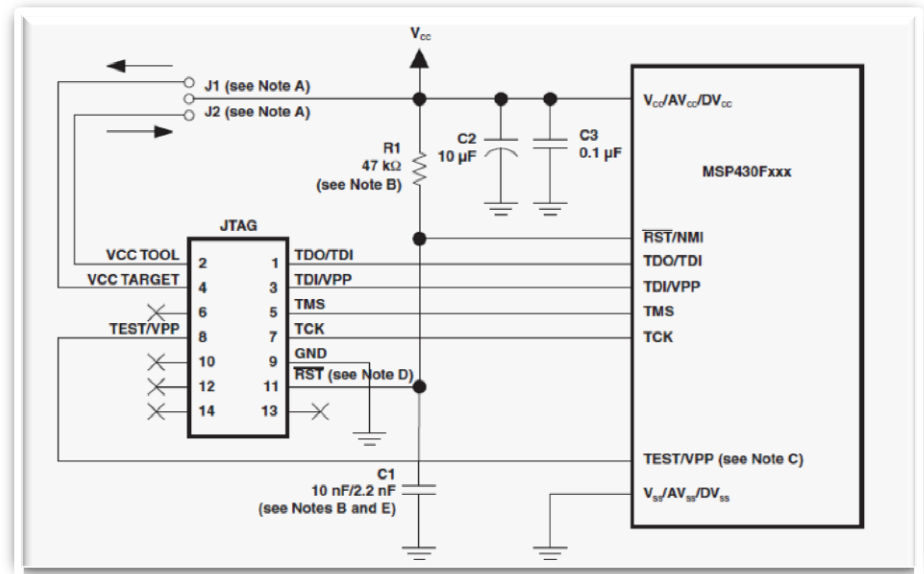
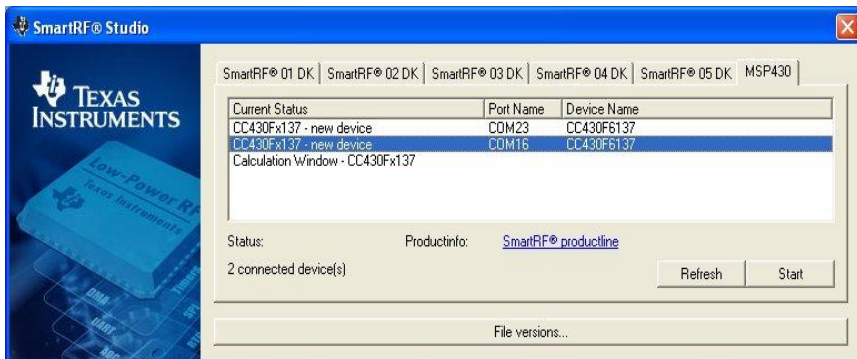
Figure: (a) SmartRF04EB (b) Zoomed view of SoC Debug Connector

Pin	Function	Note
1	GND	
2	VDD	Used to set correct voltage for voltage level converter
3	Debug Clock (DC)	
4	Debug Data (DD)	
5	CSn	
6	SCLK	
7	Reset_N	
8	MOSI	
9	3.3V VDD, alt NC	Delivers VDD from SmartRF04EB
10	MISO	

Table: 10-Pin connector description

# Debug Socket On Design – CC430 Devices

- CC430 can be interfaced to the PC for evaluation with SmartRF Studio using 14 pin FET connector
- Refer to the [CC430 Wireless Development Tools](#)



## Signal Connections for 4-Wire JTAG Communication

- A Make either connection J1 in case a local target power supply is used or connection J2 to power target from the debug/programming adapter.
- B The RST/NMI pin R1/C1 configuration is device family dependent. See the respective MSP430 family user's guide for the recommended configuration.
- C The TEST pin is available only on MSP430 family members with multiplexed JTAG pins. See the device-specific data sheet to determine if this pin is available.
- D The connection to the JTAG connector RST pin is optional when using 4-wire JTAG communication mode capable-only devices and not required for device programming or debugging. However, this connection is required when using 2-wire JTAG communication mode capable devices in 4-wire JTAG mode.
- E When using 2-wire JTAG communication capable devices in 4-wire JTAG mode, the upper limit for C1 should not exceed 2.2 nF. This applies to both TI FET interface modules (LPT/USB FET).

# Combo Designs CCXXXX with CC2590/1

- Section between the chips must be copied exactly i.e. trace width, trace lengths and component values.
- Reason - The inductance values are fine-tuned using specified lengths and widths of traces for optimum performance and it is recommended to copy them exactly.



Fig: CC2530 – CC2591 Evaluation Module