Lecture – 7

Shift Registers

Lesson Outcomes

After completing this lecture, students will be able to

- *Identify the basic forms of data movement in shift registers*
- *Explain how serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift registers operate*
- *Describe how a bidirectional shift register*
- *Use a shift register as a counter*
- *Use a shift register as a time-delay device*

Key Terms

BIDIRECTIONAL Having two directions. In a bidirectional shift register, the stored data can be shifted right or left.

LOAD To enter data into a shift register.

REGISTER One or more flip-flops used to store and shift data.

STAGE One storage element in a register.

Register

- A *register* is a digital circuit with two basic functions: *data storage* and *data movement*. The storage capability of a register makes it an important type of *memory device*.
- The *storage capacity* of a register is the total number of bits (1s and 0s) of digital data it can retain. Each stage (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity.
- The *shift capability* of a register permits the movement of data from stage to stage within the register or into or out of the register upon application of clock pulses.
- There are four types of shift registers based on data input and output (inputs/outputs): serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out.

Shift Register Operation

- When 1 is applied to the data input as shown, and a clock pulse is applied that stores the 1 by setting the flip-flop. When the 1 on the input is removed, the flip-flop remains in the SET state, thereby storing the 1. A similar procedure applies to the storage of a 0 by resetting the flip-flop.

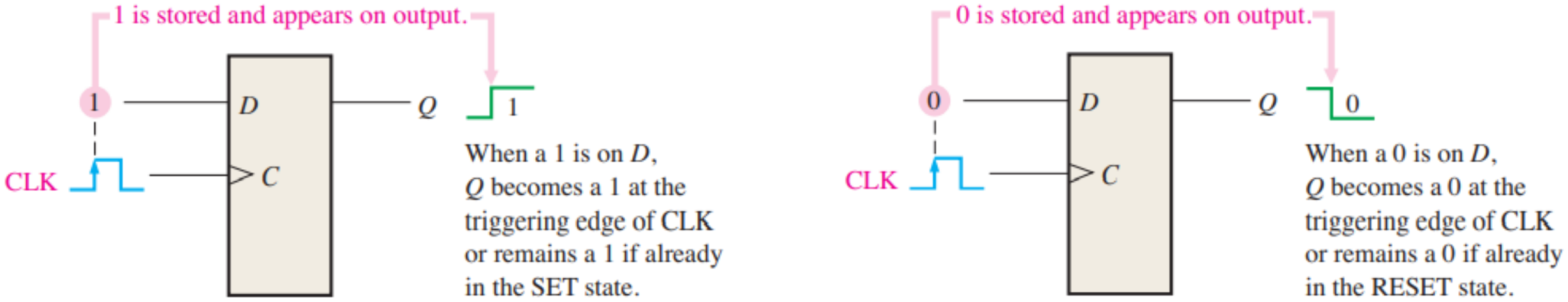


FIGURE 8–1 The flip-flop as a storage element.

Data movement in shift register

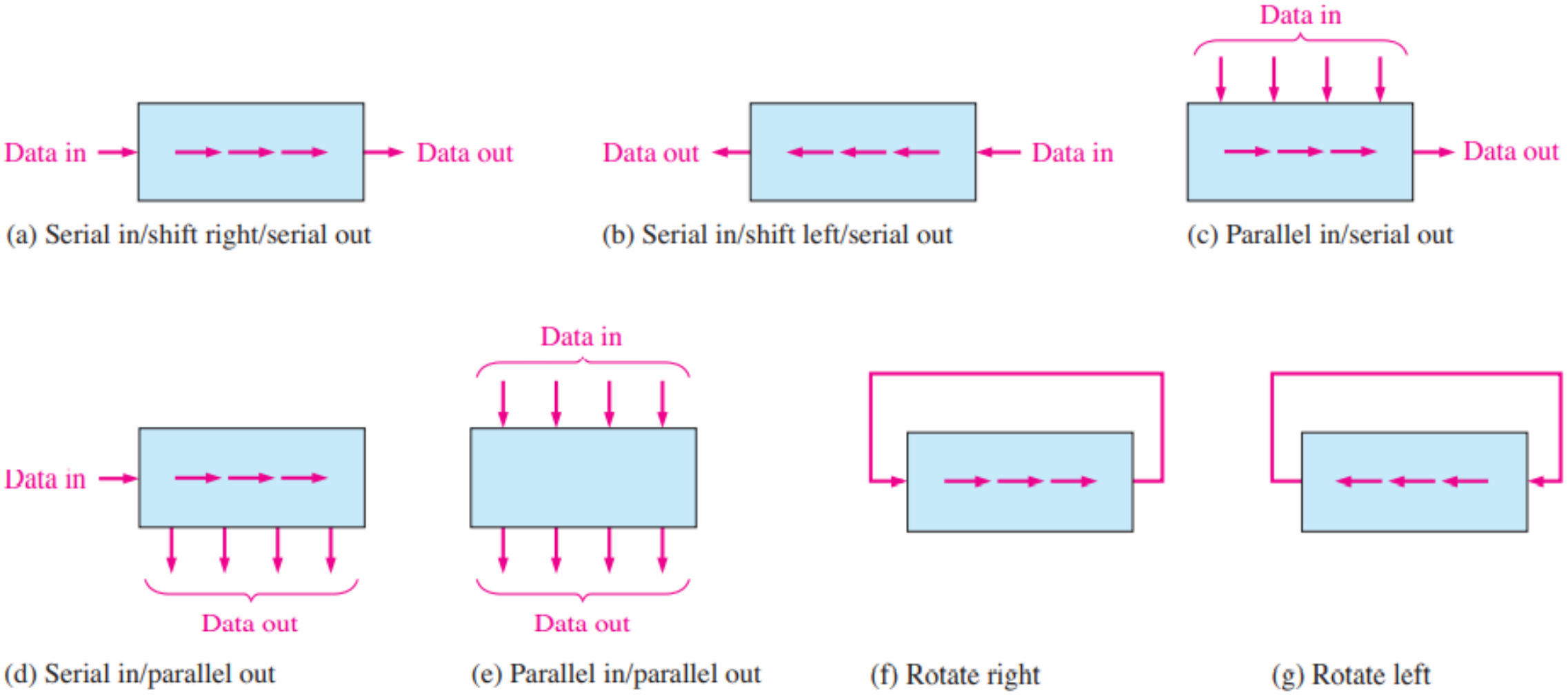


FIGURE 8–2 Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)

Serial in / Serial out shift register

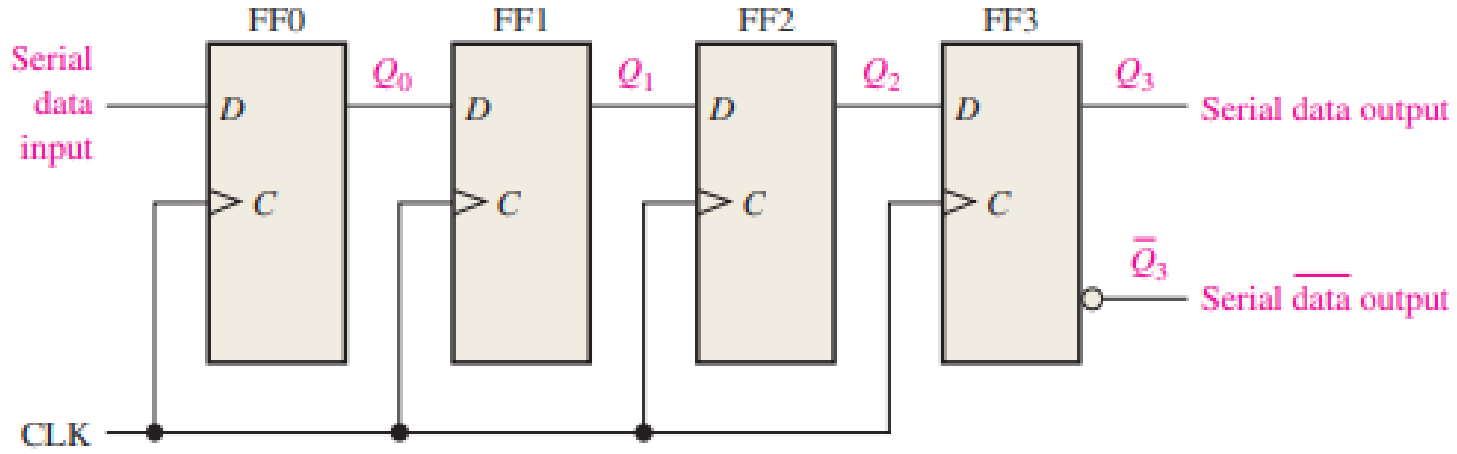


FIGURE 8–3 Serial in/serial out shift register.

TABLE 8–1

Shifting a 4-bit code into the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

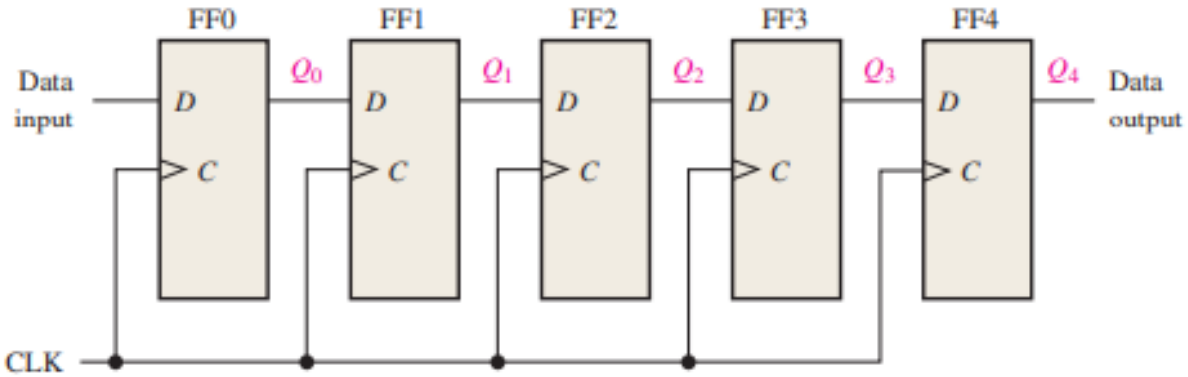
TABLE 8–2

Shifting a 4-bit code out of the shift register in Figure 8–3. Data bits are indicated by a beige screen.

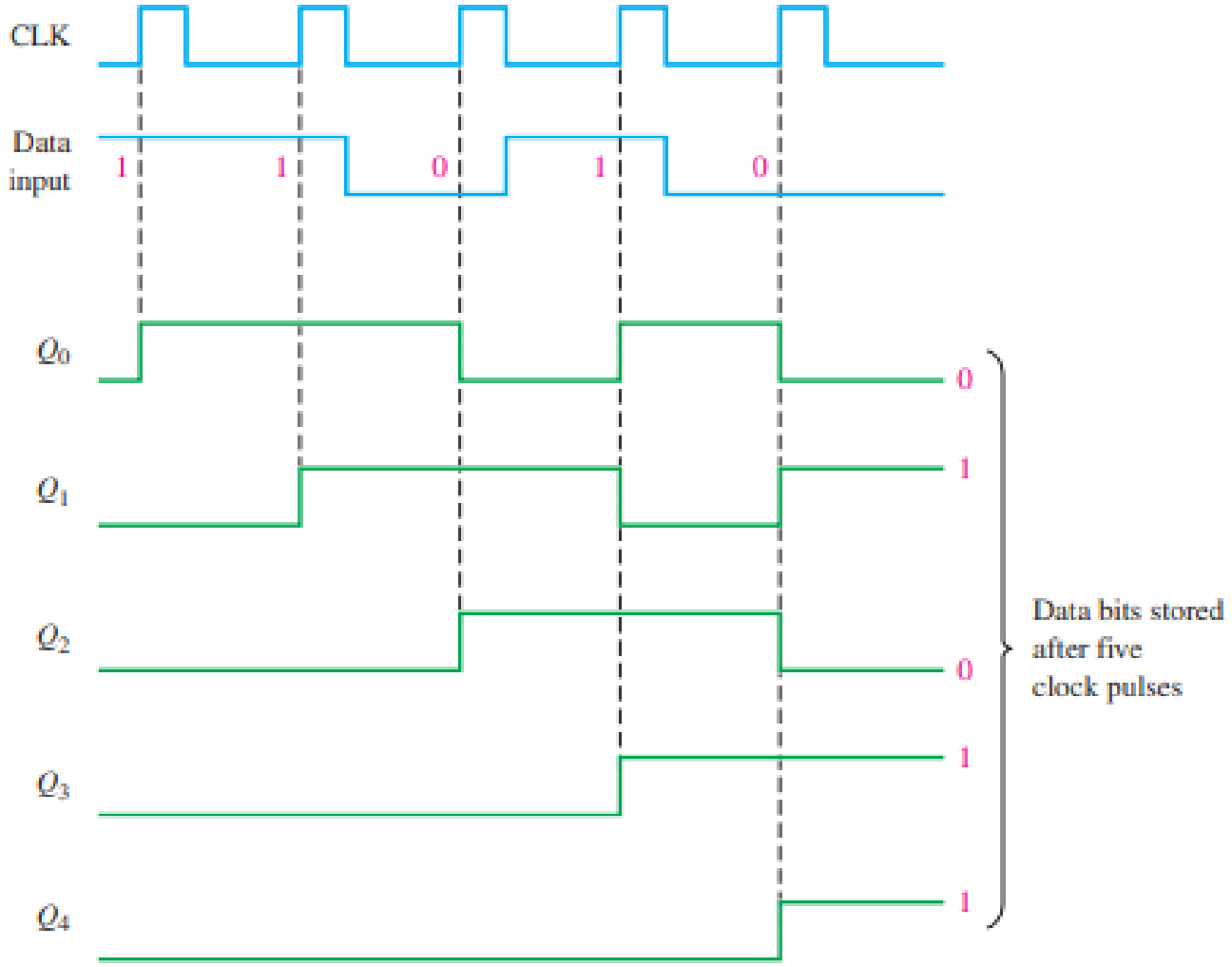
CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

Example

PROBLEM. Show the states of the 5-bit register in Figure (a) for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s).

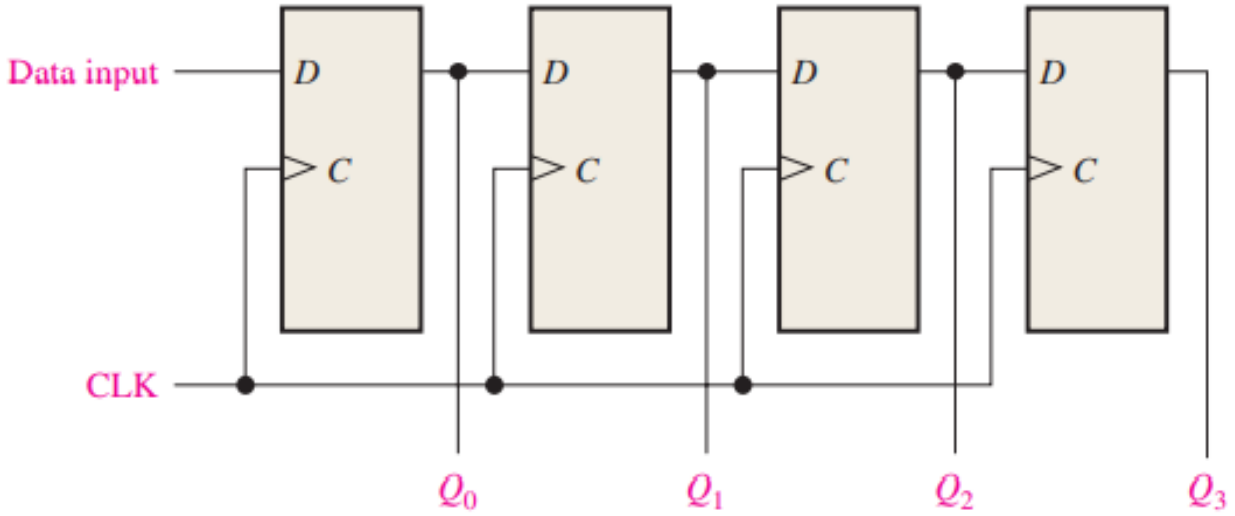


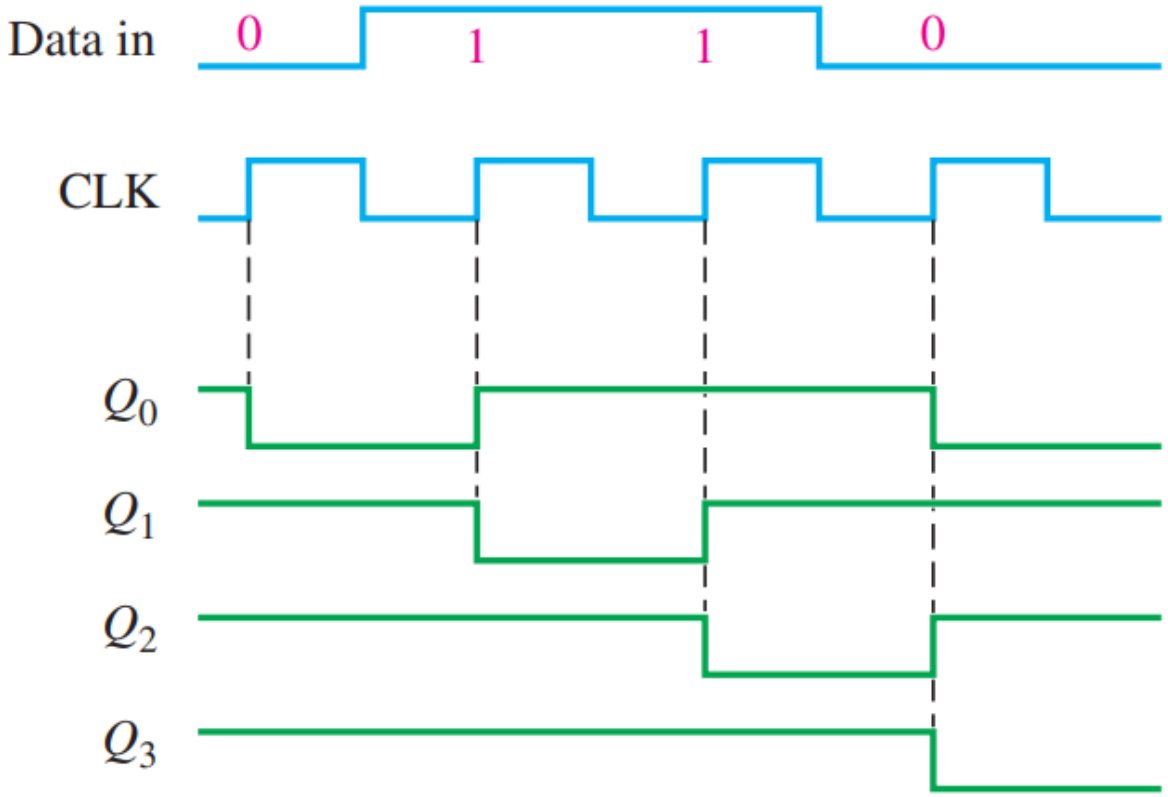
(a)



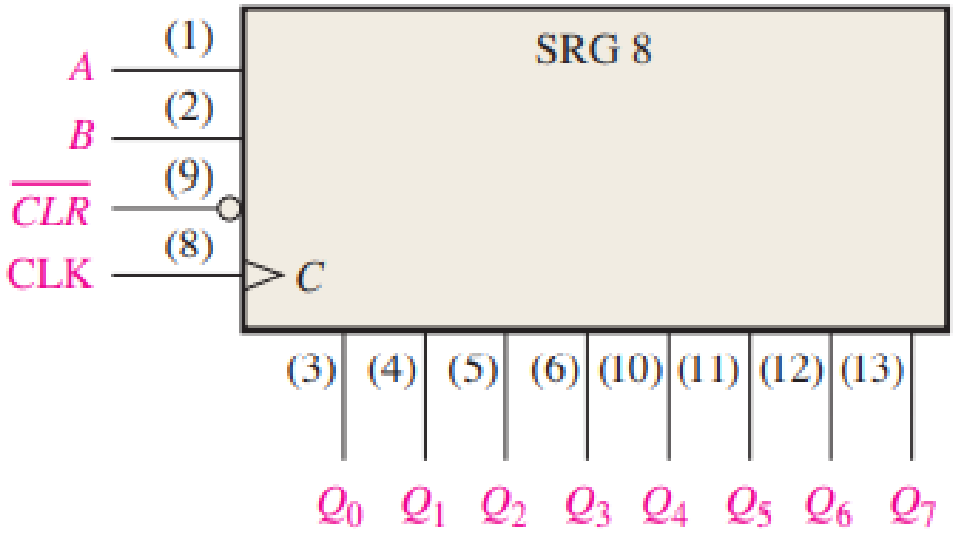
(b)

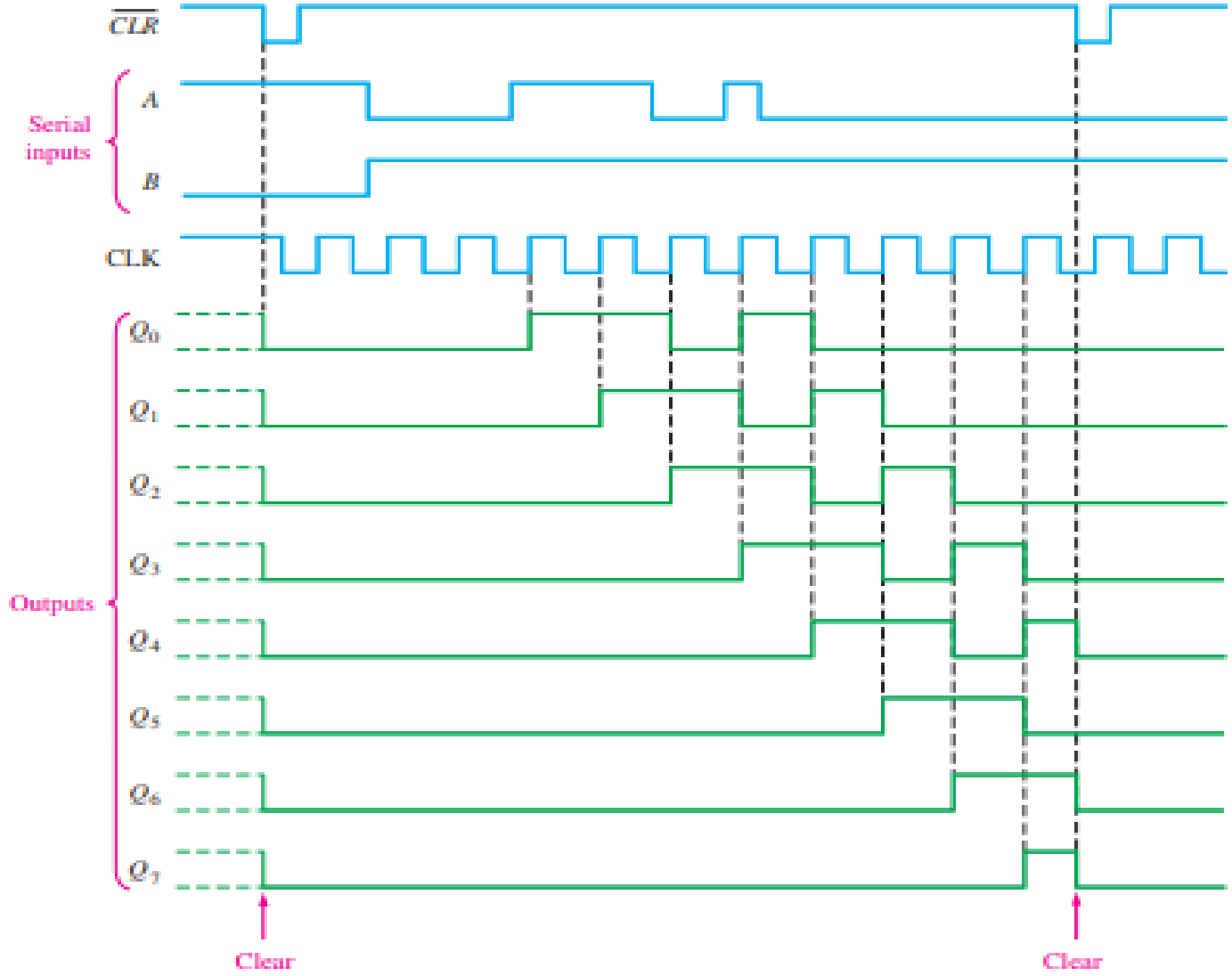
Serial in parallel out register



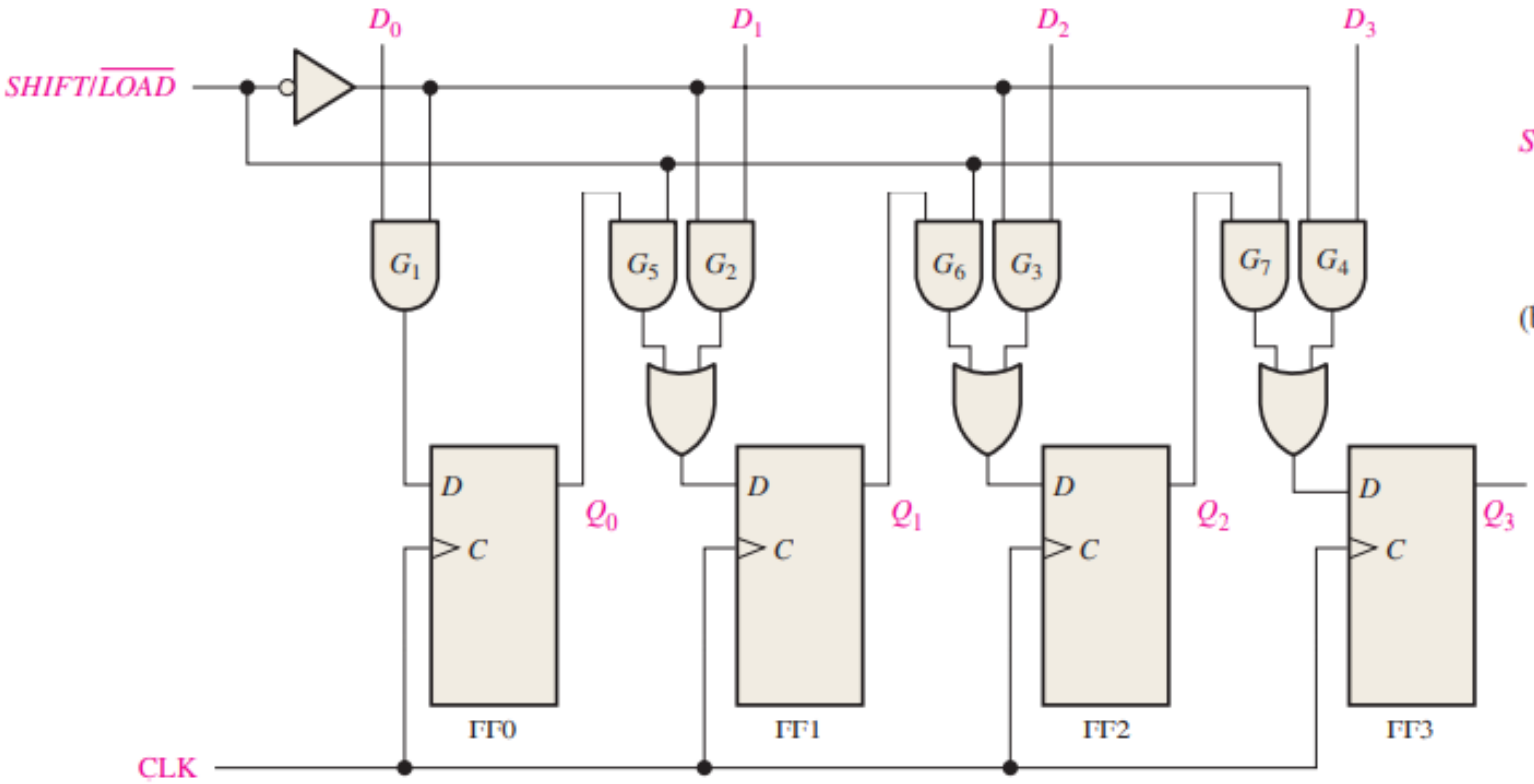


74HC164 8-bit serial in/parallel out shift register

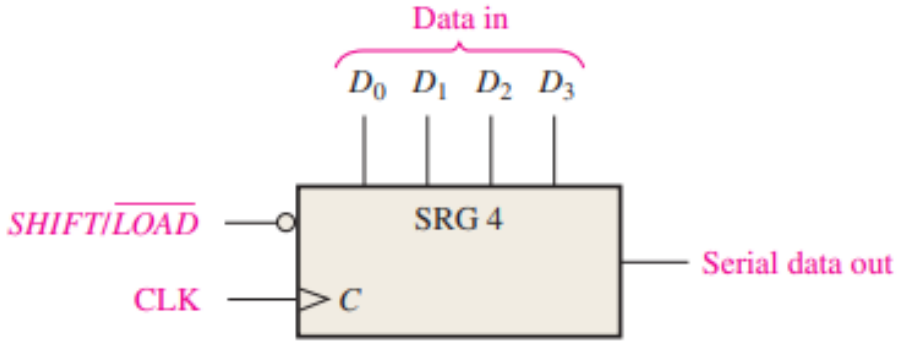




Parallel in serial out register



(a) Logic diagram

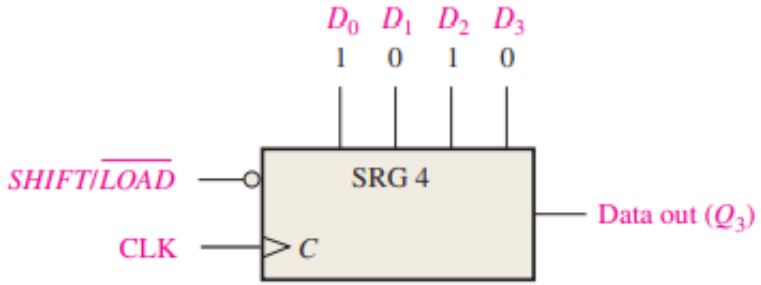


(b) Logic symbol

Example

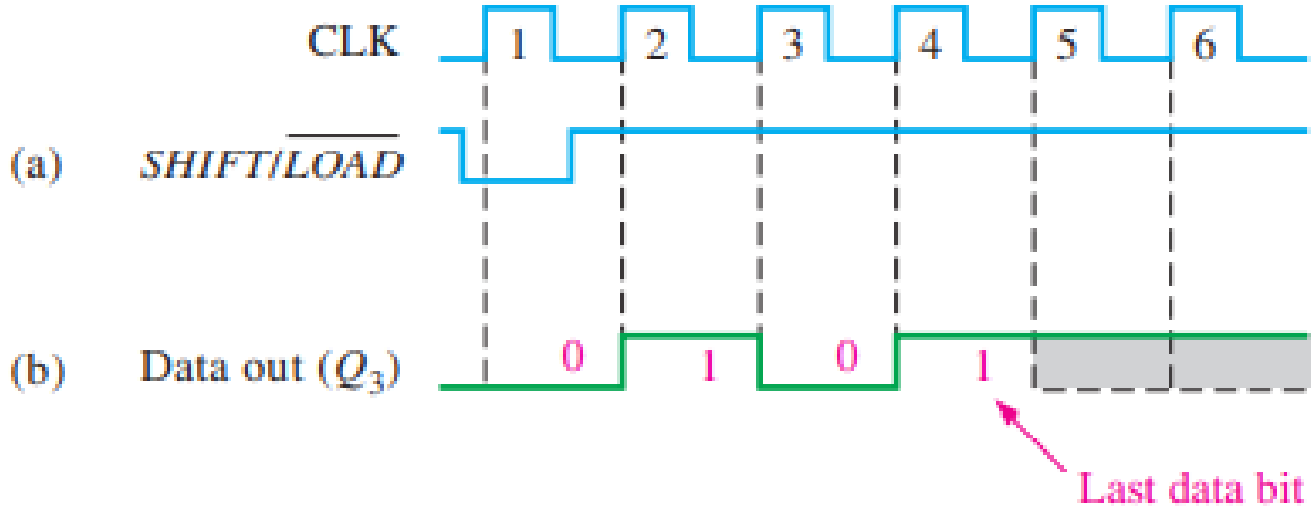
EXAMPLE 8–3

Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT*/$\overline{LOAD}$ waveforms given in Figure 8–11(a). Refer to Figure 8–10(a) for the logic diagram.

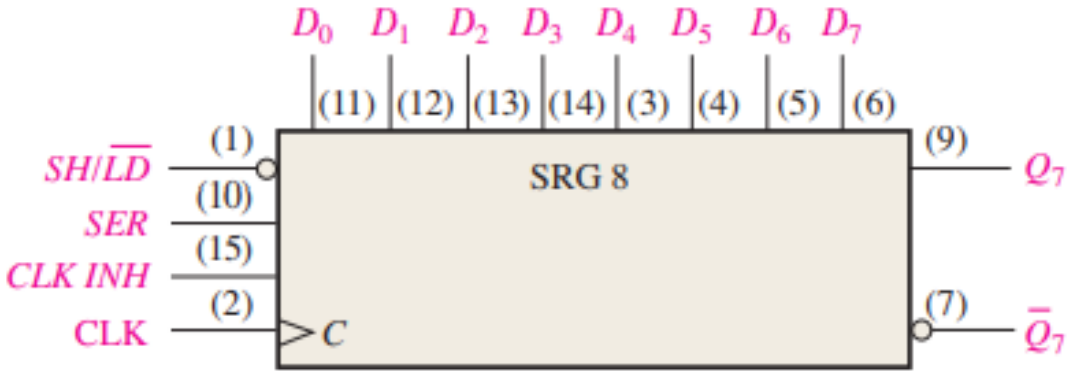


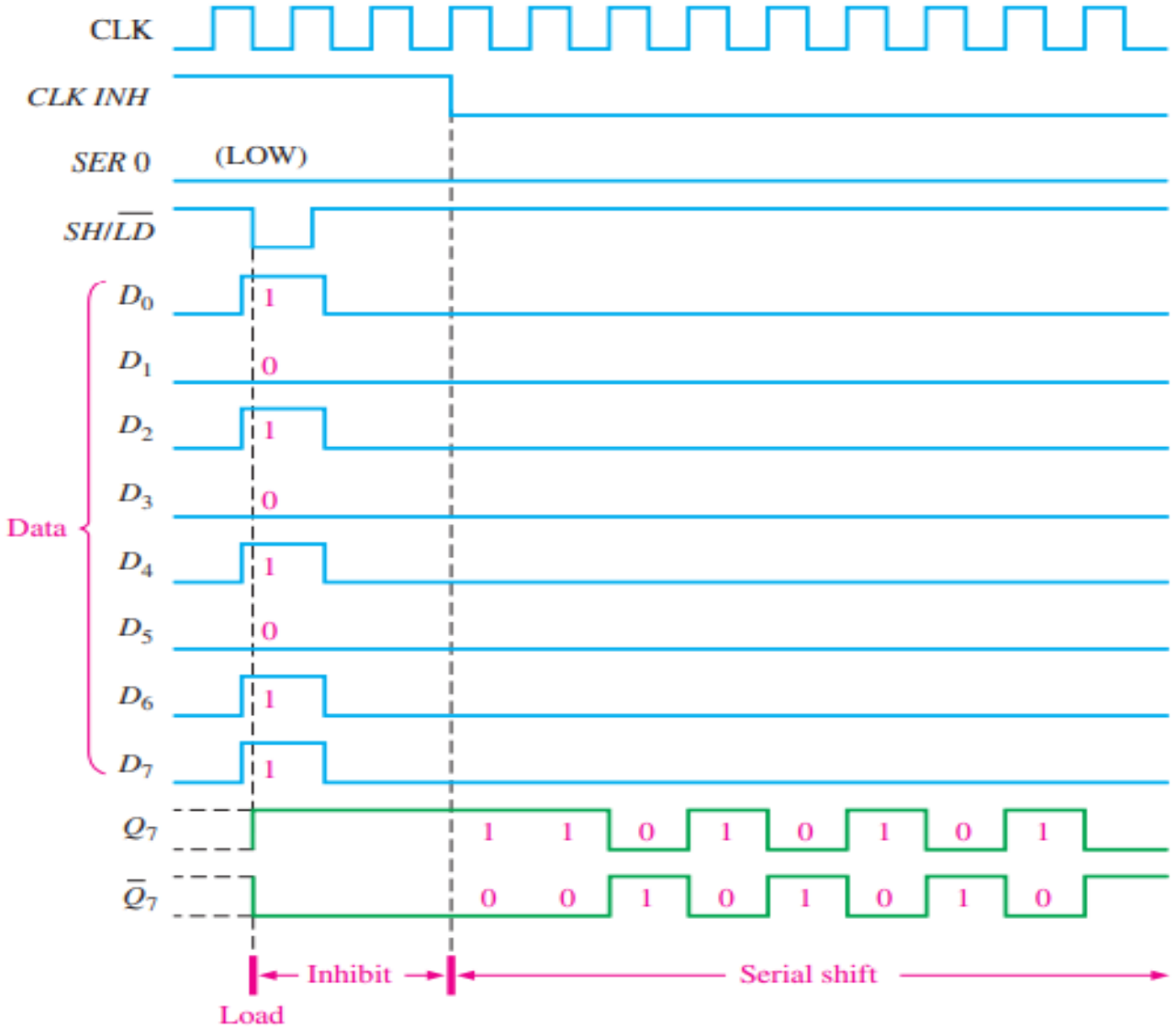
Solution

On clock pulse 1, the parallel data ($D_0D_1D_2D_3 = 1010$) are loaded into the register, making Q_3 a 0. On clock pulse 2 the 1 from Q_2 is shifted onto Q_3; on clock pulse 3 the 0 is shifted onto Q_3; on clock pulse 4 the last data bit (1) is shifted onto Q_3; and on clock pulse 5, all data bits have been shifted out, and only 1s remain in the register (assuming the D_0 input remains a 1). See Figure 8–11(b).

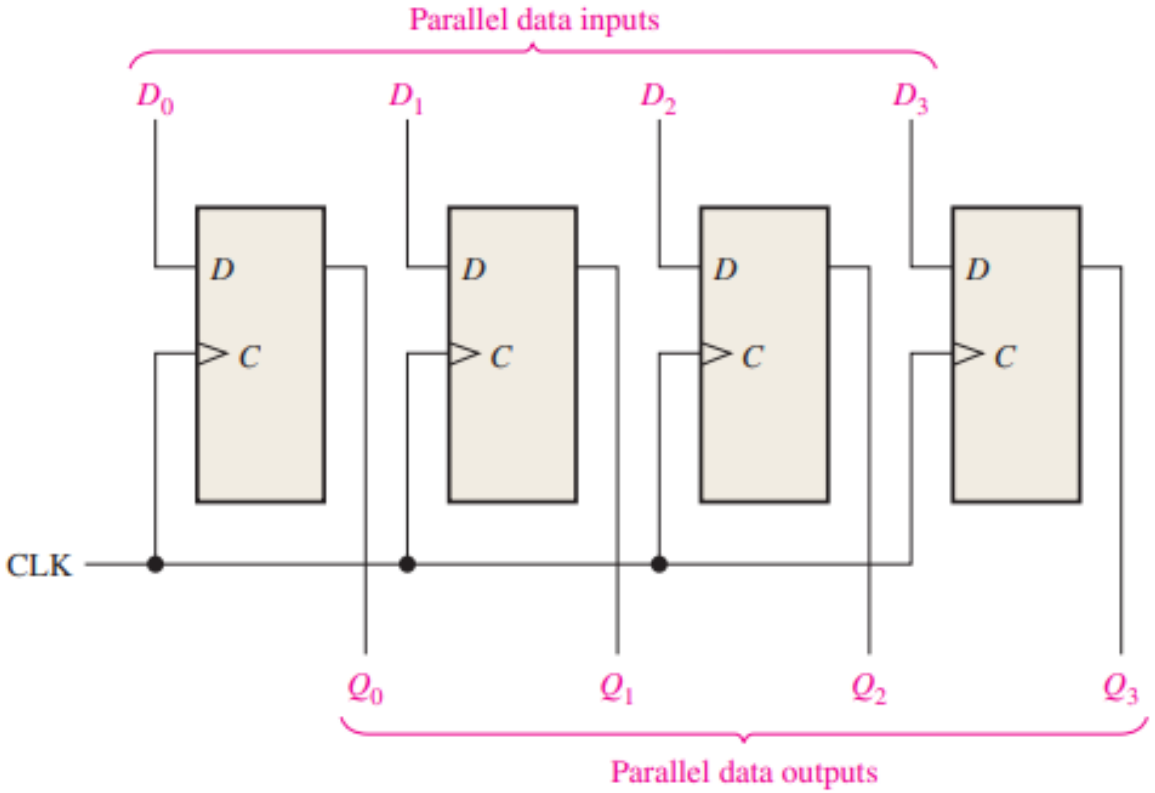


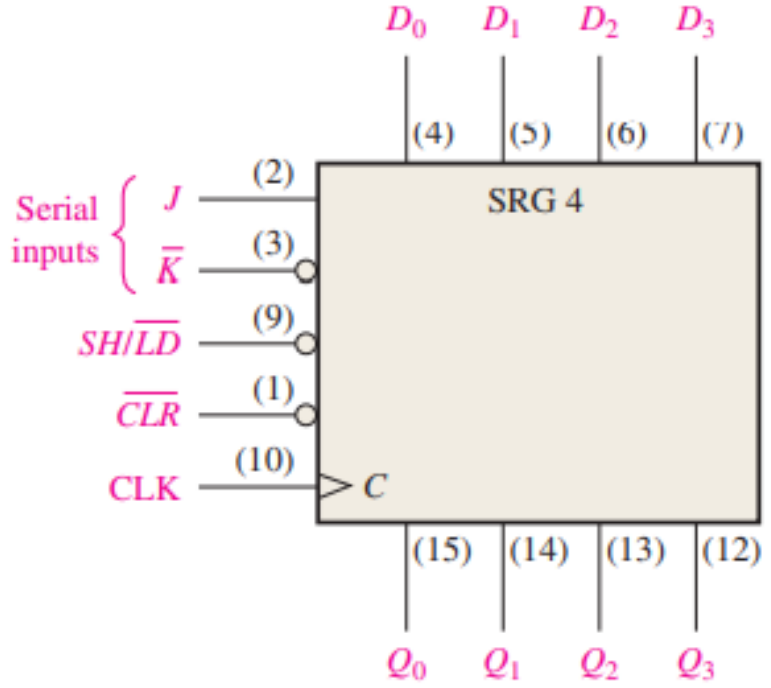
74HC165 8-bit parallel load shift register





Parallel in parallel out register

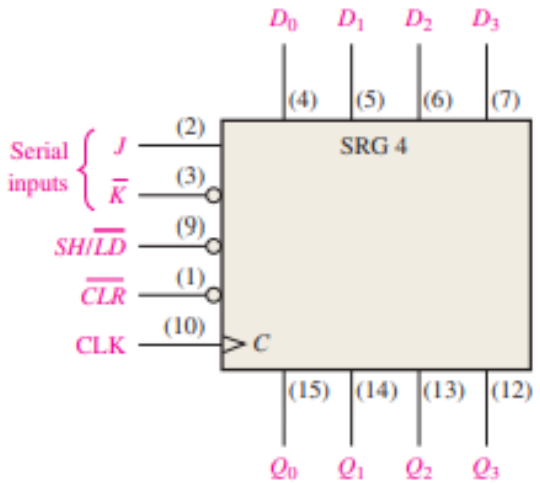


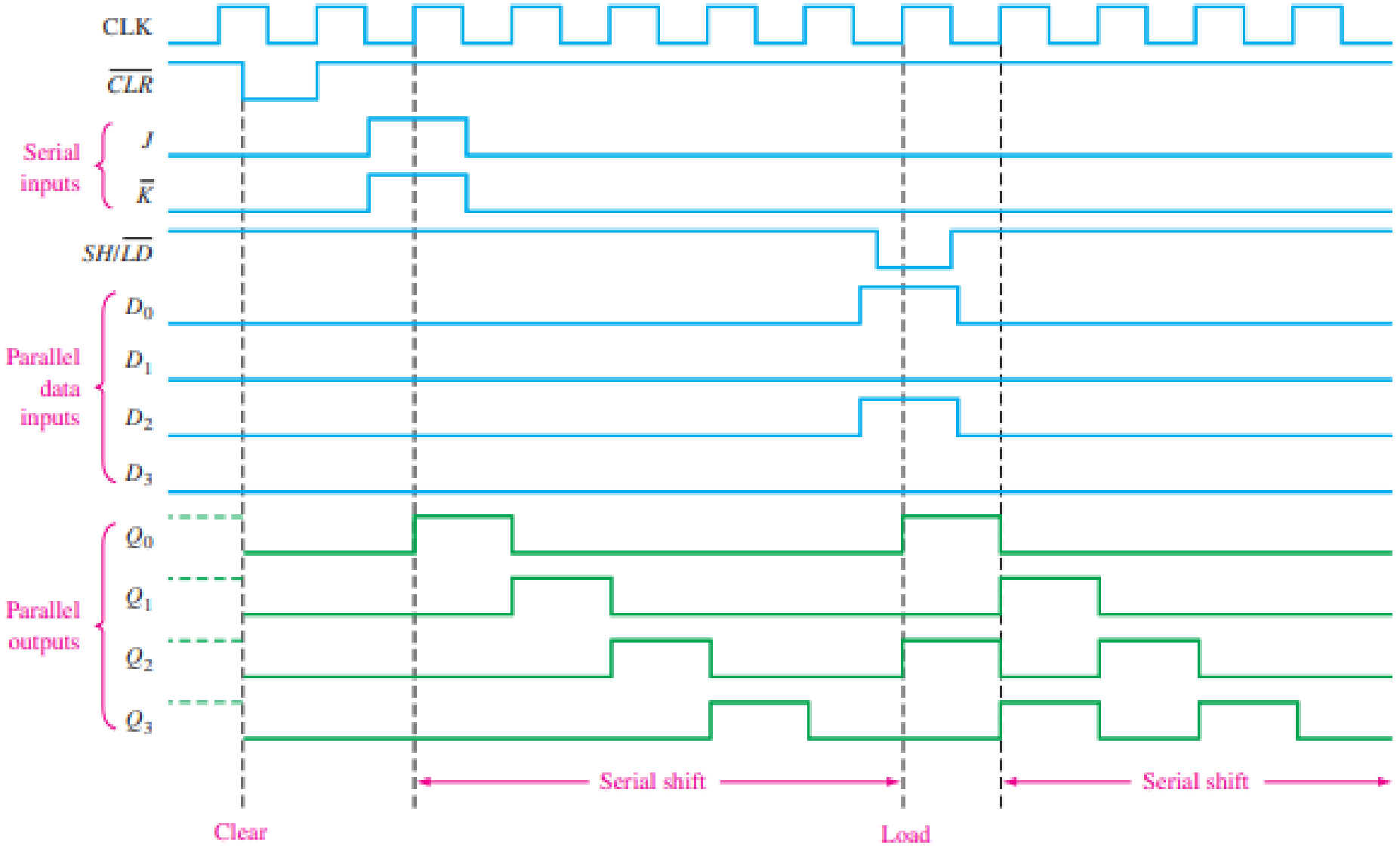


The 74HC195 4-bit parallel access shift register.

When the $SHIFT/\overline{LOAD}$ input ($SH/\overline{LD}$) is LOW, the data on the parallel inputs are entered synchronously on the positive transition of the clock. When ($SH/\overline{LD}$) is HIGH, stored data will shift right (Q_0 to Q_3) synchronously with the clock. Inputs J and $\overline{K}$ are the serial data inputs to the first stage of the register (Q_0); Q_3 can be used for serial output data. The active-LOW clear input is asynchronous.

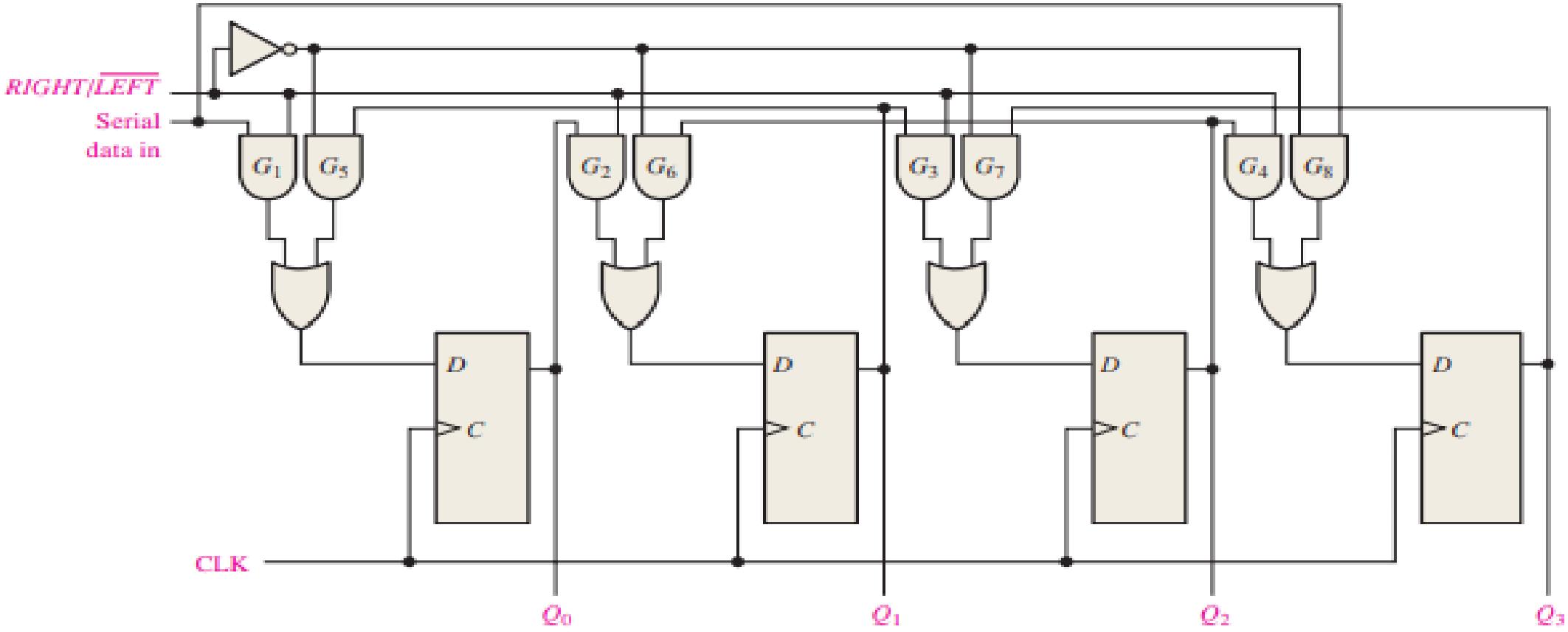
Timing diagram for a 74HC195 shift register





Bidirectional shift register

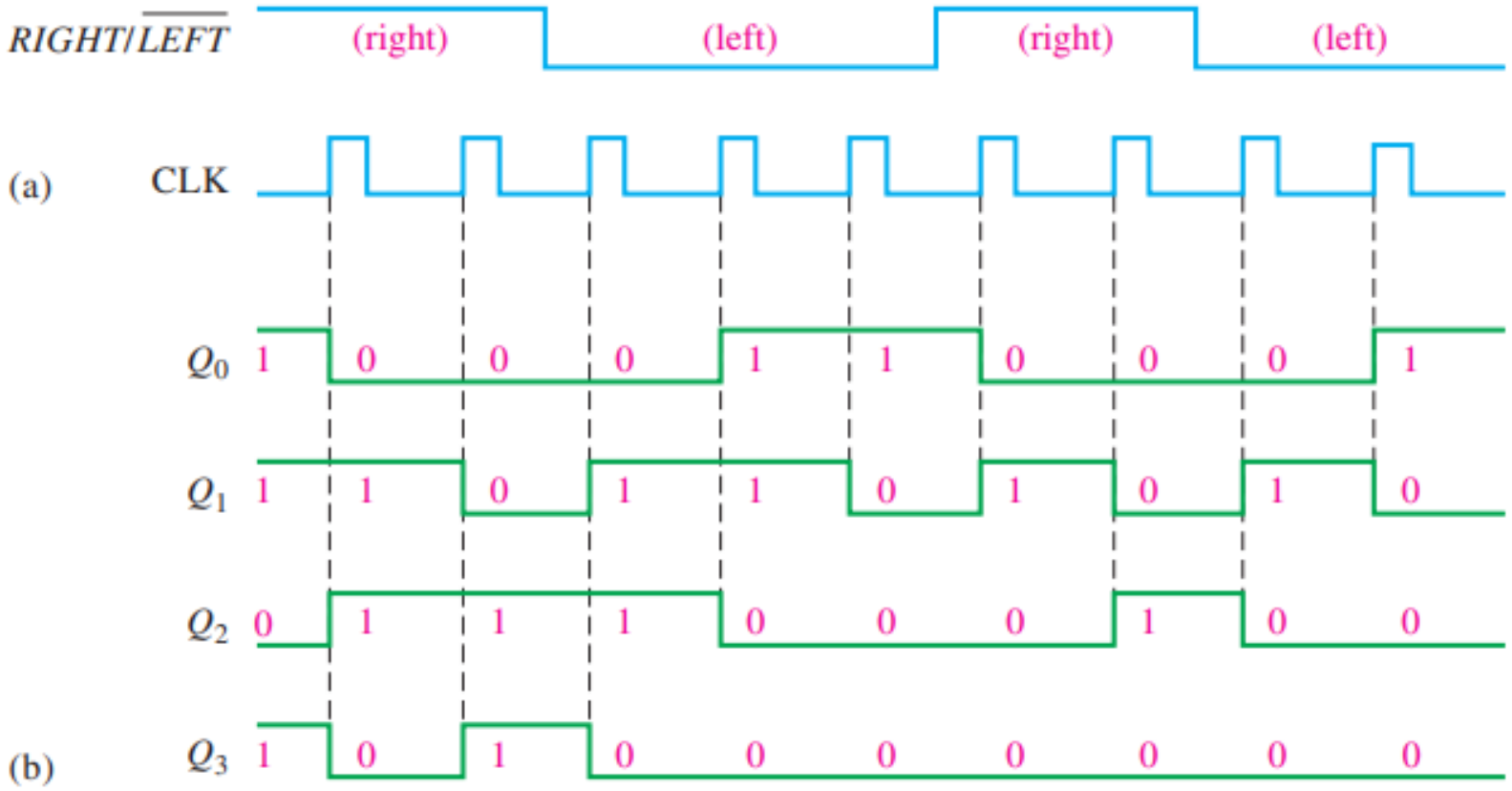
- A bidirectional shift register is one in which the data can be shifted either left or right. It can be implemented by using gating logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left, depending on the level of a control line.



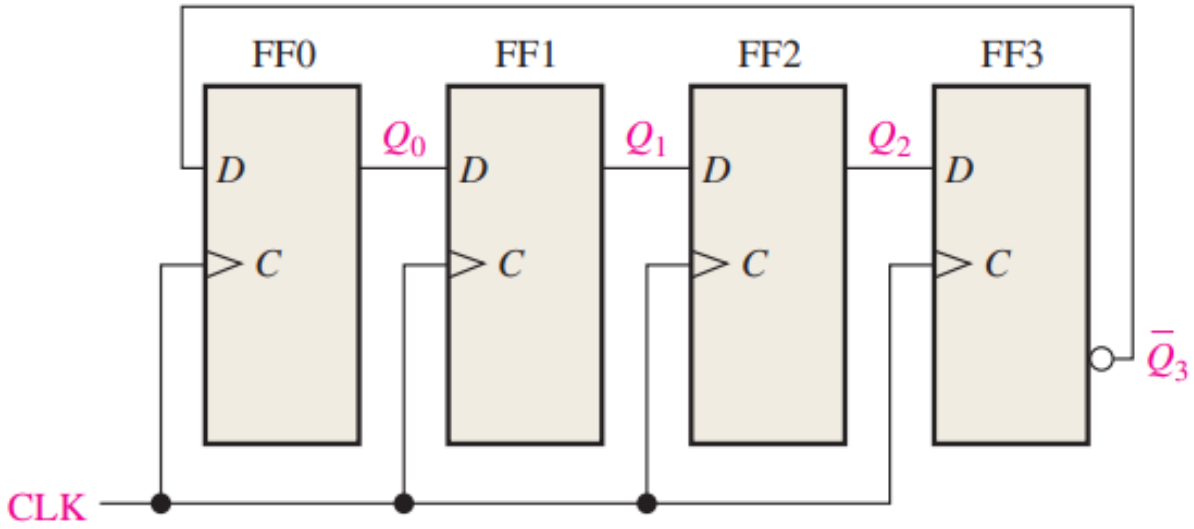
Example

EXAMPLE 8–4

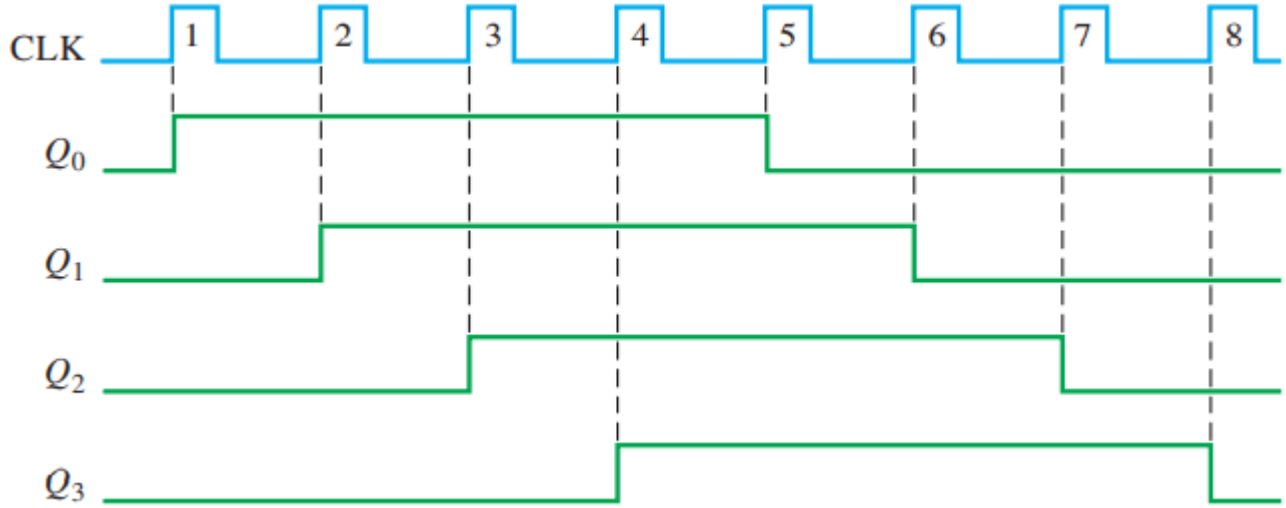
Determine the state of the shift register of Figure 8–17 after each clock pulse for the given *RIGHT*/$\overline{LEFT}$ control input waveform in Figure 8–18(a). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.



Shift register application – Johnson counter



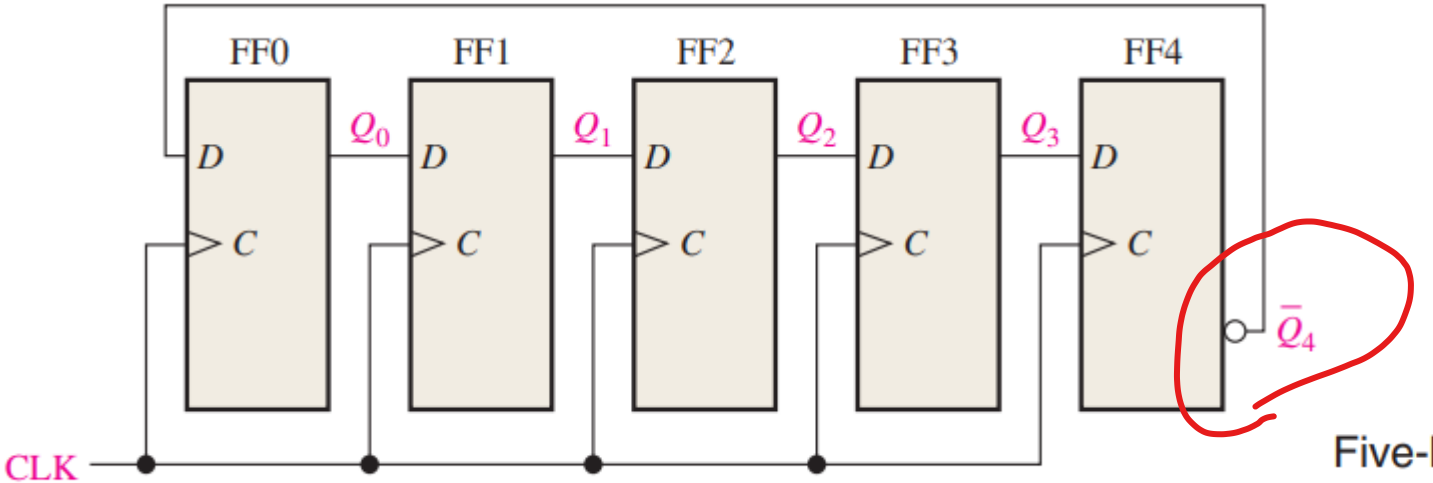
(a) Four-bit Johnson counter



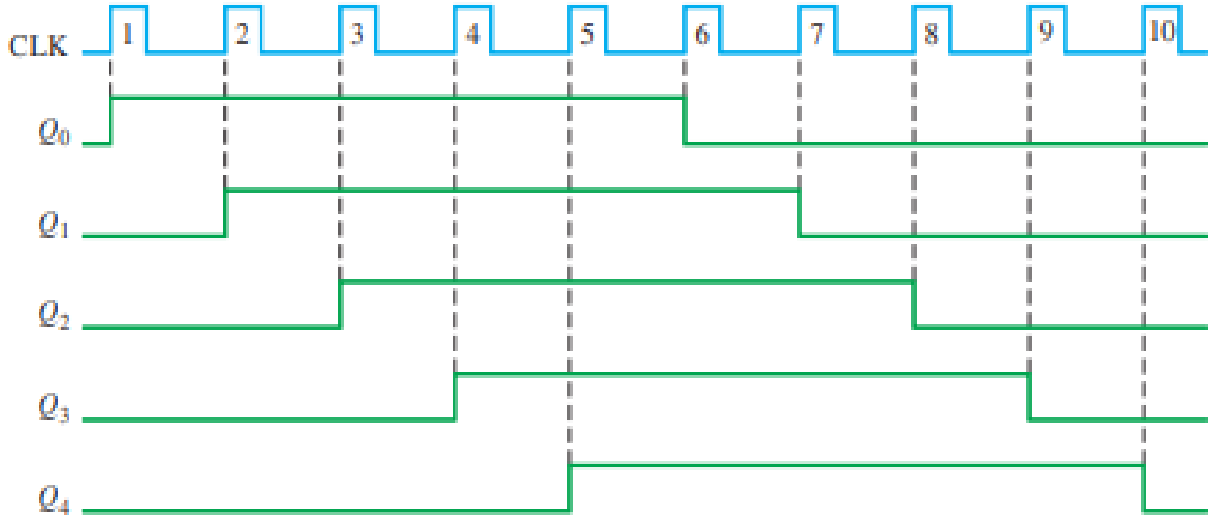
Four-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Shift register application – Johnson counter



(b) Five-bit Johnson counter

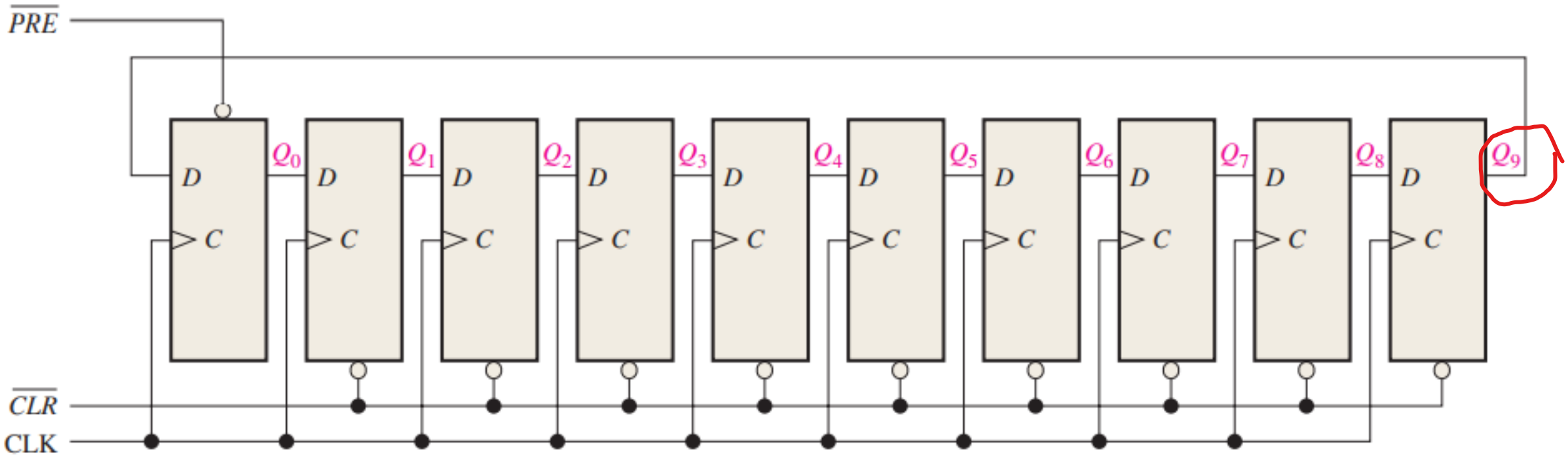


Five-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Shift register application – ring counter

- Initially, a 1 is preset into the first flip-flop, and the rest of the flip-flops are cleared.
- The ten outputs of the counter indicate directly the decimal count of the clock pulse. For instance, a 1 on Q0 represents a zero, a 1 on Q1 represents a one, a 1 on Q2 represents a two, a 1 on Q3 represents a three, and so on. You should verify for yourself that the 1 is always retained in the counter and simply shifted "around the ring," advancing one stage for each clock pulse.



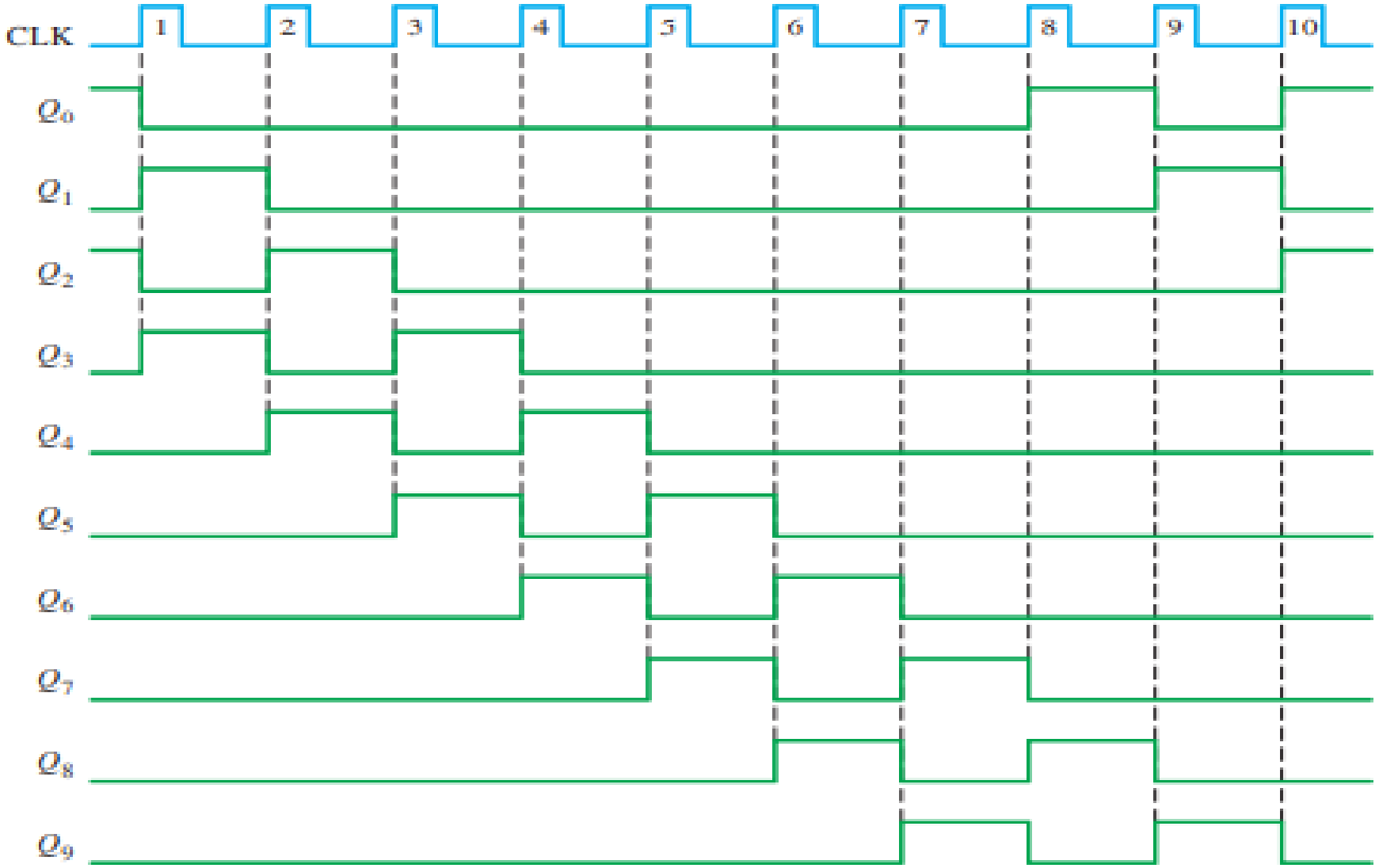
Shift register application – ring counter

Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

Shift register application – Johnson counter

PROB. If a 10-bit ring counter has the initial state 1010000000, determine the waveform for each of the Q outputs.



Shift register application – time delay

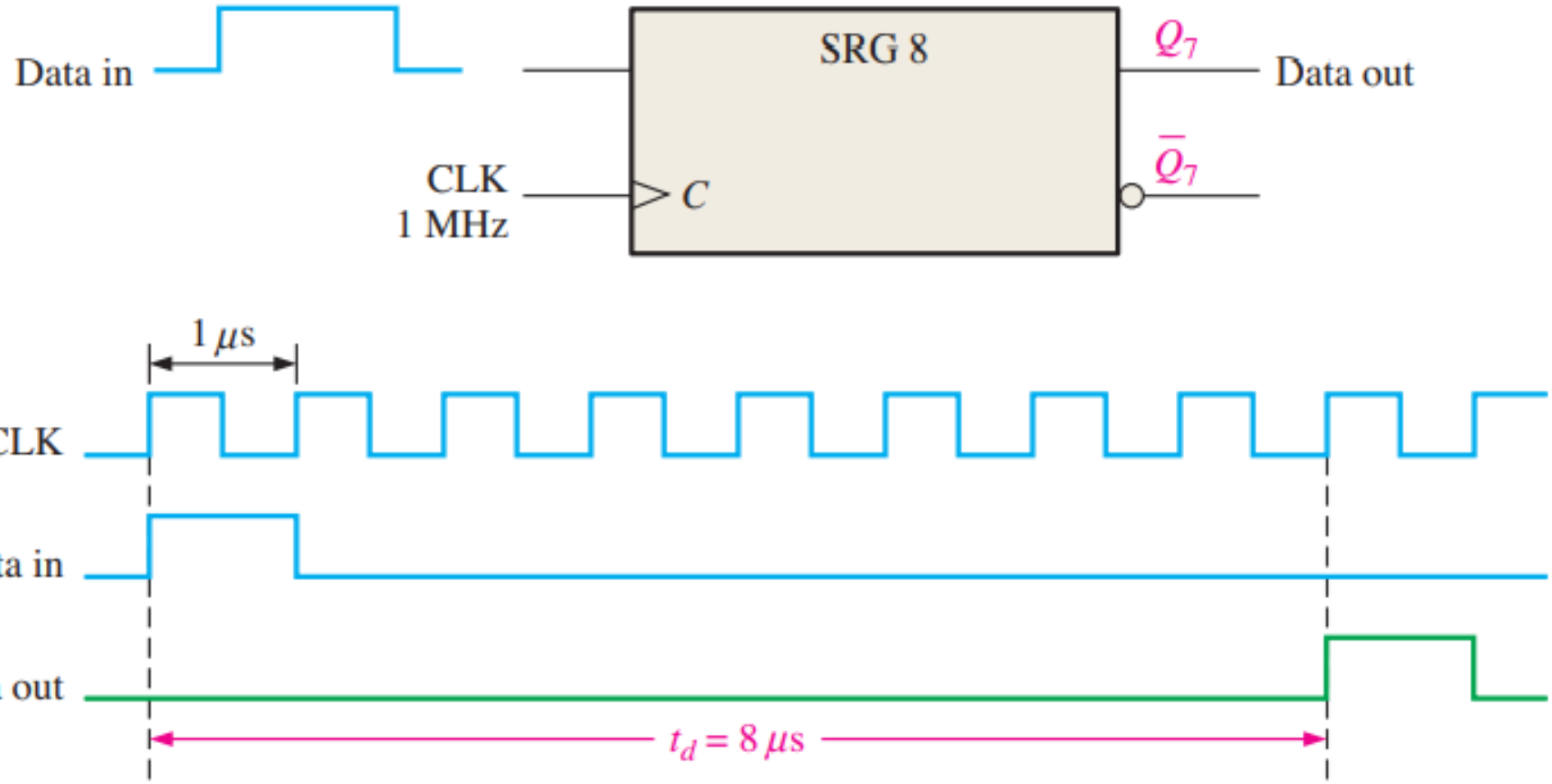
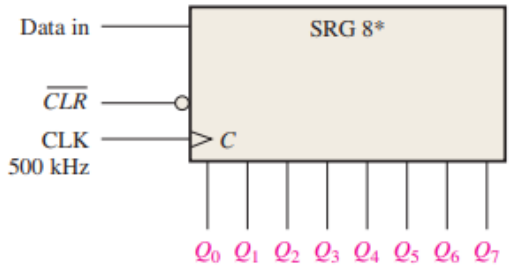


FIGURE 8–26 The shift register as a time-delay device.

Shift register application – time delay

EXAMPLE 8–6

Determine the amount of time delay between the serial input and each output in Figure 8–27. Show a timing diagram to illustrate.

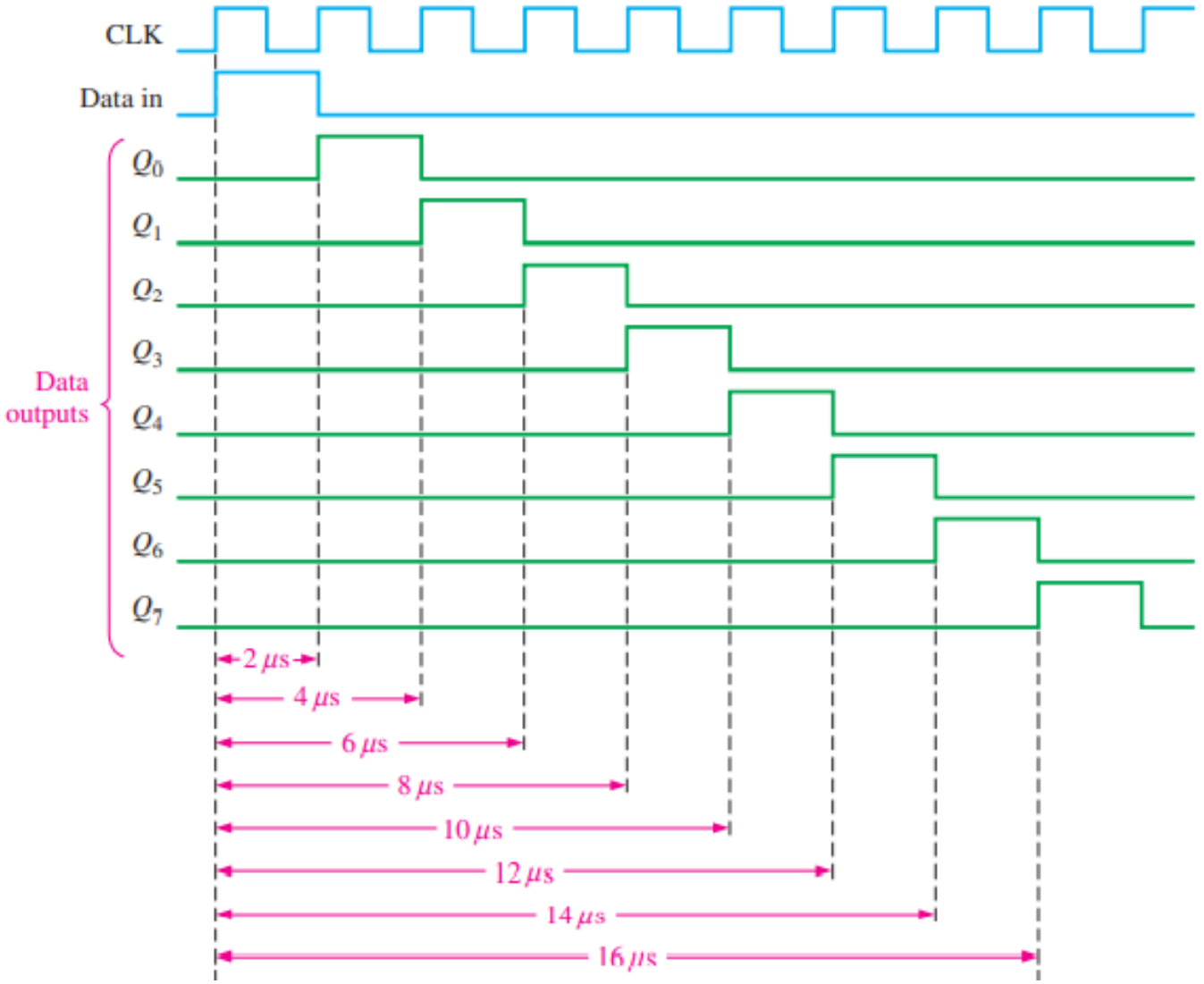


* Data shifts from Q_0 toward Q_7.

FIGURE 8–27

Solution

The clock period is 2 μs. Thus, the time delay can be increased or decreased in 2 μs increments from a minimum of 2 μs to a maximum of 16 μs, as illustrated in Figure 8–28.



References

1. ***Digital Fundamentals*** by Thomas Floyd, Pearson International Edition, 11th Edition, Chapter 8, Page 449-495.

Next class

Counters