Lecture – 6

Latches, Flip-Flops and Their Applications

Lesson Outcomes

After completing this lecture, students will be able to

- *Use logic gates to construct basic latches*
- *Recognize the difference between a latch and a flip-flop*
- *Understand the significance of propagation delays, set-up time, hold time, maximum operating frequency, minimum clock pulse widths, and power dissipation in the application of flip-flops*
- *Apply flip-flops in basic applications*

Key Terms

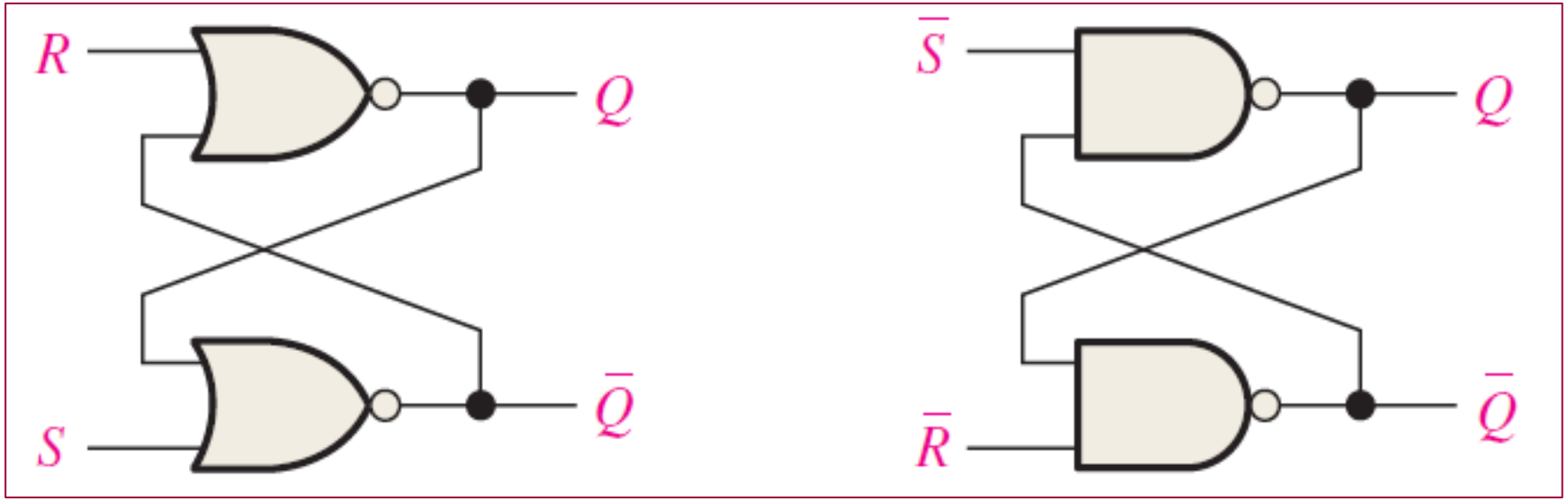
- **Astable** Having no stable state. An astable multivibrator oscillates between two quasi-stable states.
- **Bistable** Having two stable states. Flip-flops and latches are bistable multivibrators.
- **Clock** The triggering input of a flip-flop.
- **D flip-flop** A type of bistable multivibrator in which the output assumes the state of the *D* input on the triggering edge of a clock pulse.
- **Edge-triggered flip-flop** A type of flip-flop in which the data are entered and appear on the output on the same clock edge.
- **Hold time** The time interval required for the control levels to remain on the inputs to a flip-flop after the triggering edge of the clock in order to reliably activate the device.
- **J-K flip-flop** A type of flip-flop that can operate in the SET, RESET, no-change, and toggle modes.
- **Latch** A bistable digital circuit used for storing a bit.

Key Terms

- **Monostable** Having only one stable state. A monostable multivibrator, commonly called a *oneshot,* produces a single pulse in response to a triggering input.
- **One-shot** A monostable multivibrator.
- **Preset** An asynchronous input used to set a flip-flop (make the *Q* output 1).
- **Propagation delay time** The interval of time required after an input signal has been applied for the resulting output change to occur.
- **RESET** The state of a flip-flop or latch when the output is 0; the action of producing a RESET state.
- **SET** The state of a flip-flop or latch when the output is 1; the action of producing a SET state.
- **Set-up time** The time interval required for the control levels to be on the inputs to a digital circuit, such as a flip-flop, prior to the triggering edge of a clock pulse.
- **Synchronous** Having a fixed time relationship.
- **Timer** A circuit that can be used as a one-shot or as an oscillator.
- **Toggle** The action of a flip-flop when it changes state on each clock pulse.

Latch (NAND latch, NOR latch)

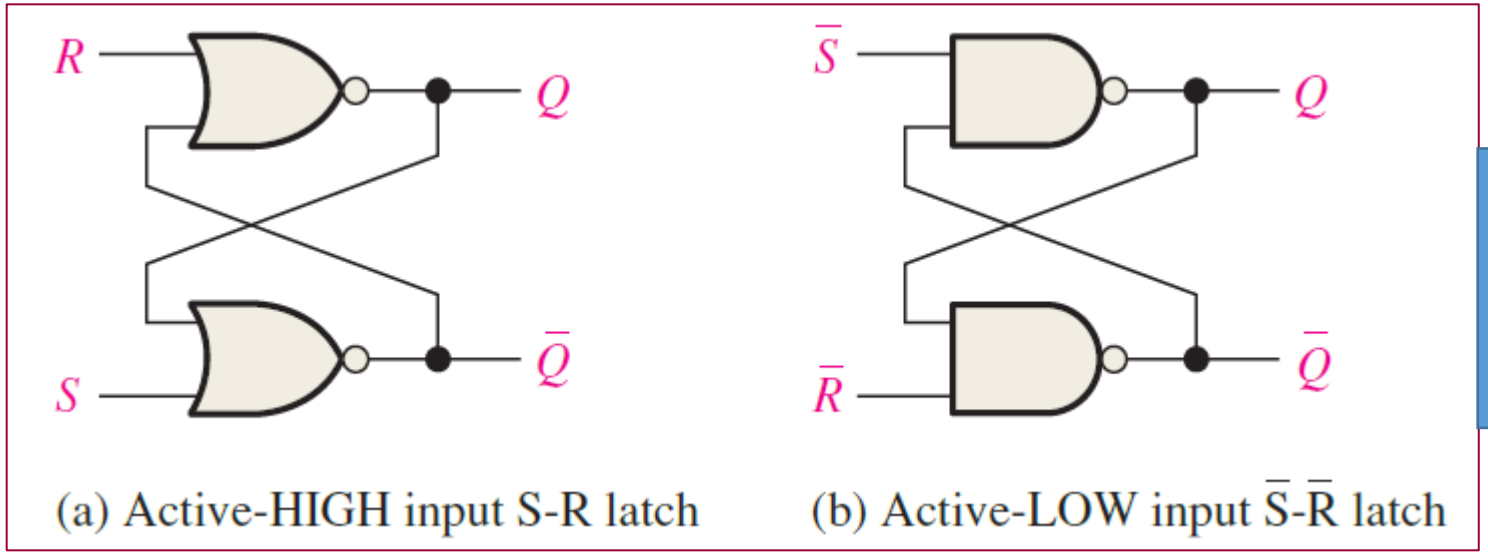
- The **latch** is a type of temporary storage device that has two stable states (bistable) and is normally placed in a category separate from that of flip-flops.
- Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs.
- The main difference between latches and flip-flops is in the method used for changing their state.



S-R Latch

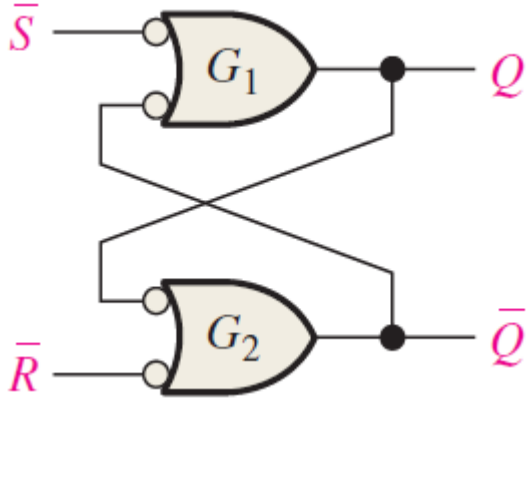
- A **latch** is a type of bistable logic device or multivibrator.
- An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates, as shown in Figure (a); an active-LOW input $\underline{S}$ $\underline{R}$ latch is formed with two cross-coupled NAND gates, as shown in Figure (b).
- The outputs of a latch are always complements of each other.

When Q is HIGH, $\overline{Q}$ is LOW, and when Q is LOW, $\overline{Q}$ is HIGH.

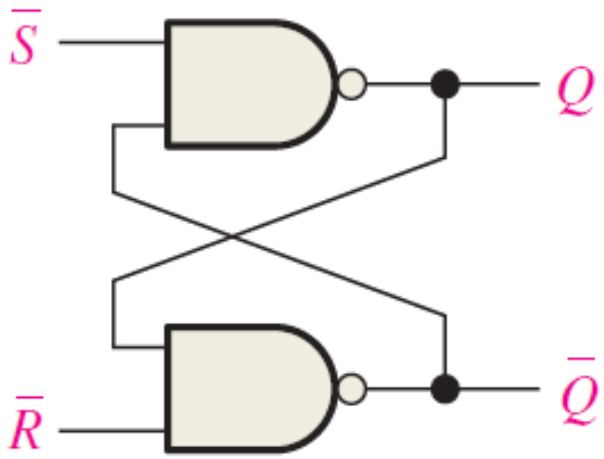


(a) Active-HIGH input S-R latch (b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

Negative-OR equivalent of $\underline{S}$ $\underline{R}$ latch



S-R latch



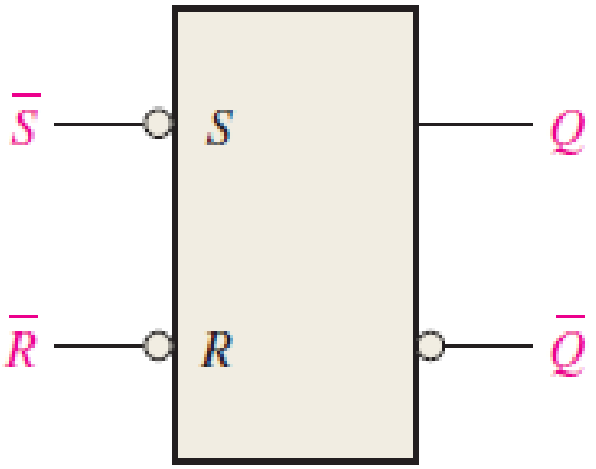
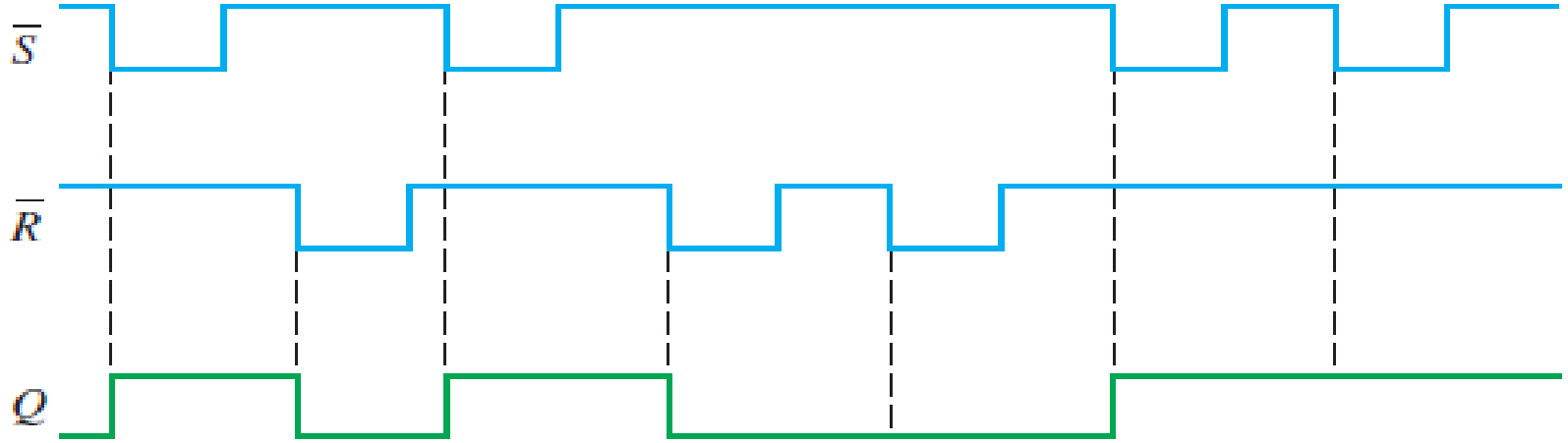


TABLE 7–1

Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

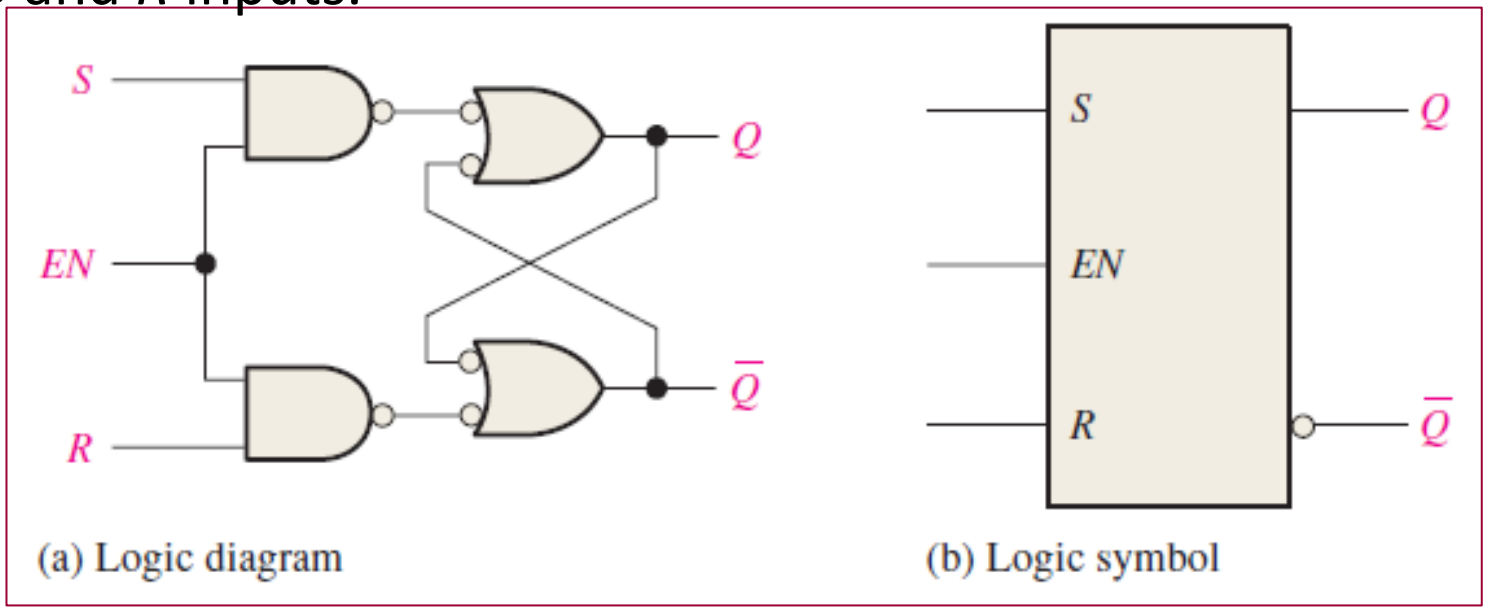


Gated S-R Latch

- A gated latch requires an enable input, *EN* (*G* is also used to designate an enable input). The logic diagram and logic symbol for a gated S-R latch are shown in Figure. The *S* and *R* inputs control the state to which the latch will go when a HIGH level is applied to the *EN* input.

- The latch will not change until *EN* is HIGH; but as long as it remains HIGH, the output is controlled by the state of the *S* and *R* inputs.

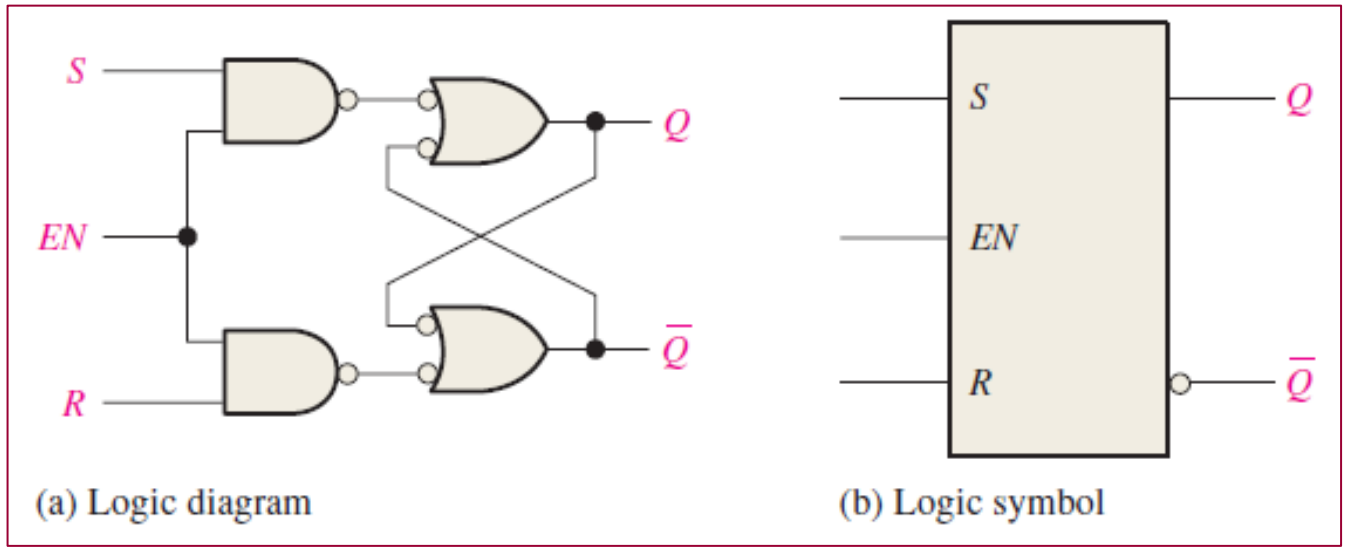
- The gated latch is a *level-sensitive* device. In this circuit, the invalid state occurs when both *S* and *R* are simultaneously HIGH and *EN* is also HIGH.



(a) Logic diagram (b) Logic symbol

Gated S-R Latch

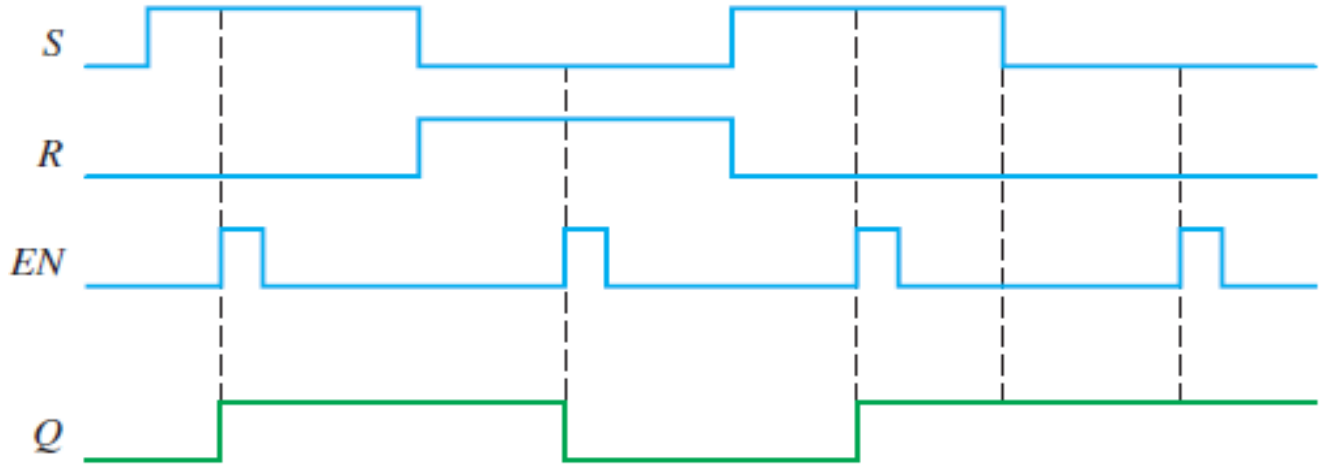
- **PROBLEM.** Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.



(a) Logic diagram (b) Logic symbol

SOLUTION:

- When S is HIGH and R is LOW, a HIGH on the EN input sets the latch. When S is LOW and R is HIGH, a HIGH on the EN input resets the latch.
- When both S and R are LOW, the Q output does not change from its present state.



Flip-Flops

- **Flip-flops** are *synchronous bistable devices*, also known as *bistable multivibrators.*
- In this case, the term *synchronous* means that the output changes state only at a specified point (leading or trailing edge) on the *triggering input called the* ***clock*** (CLK), which is designated as a control input, *C*; that is, changes in the output occur in synchronization with the clock.
- Flip-flops are edge-triggered or edge-sensitive whereas *gated latches are level-sensitive*.

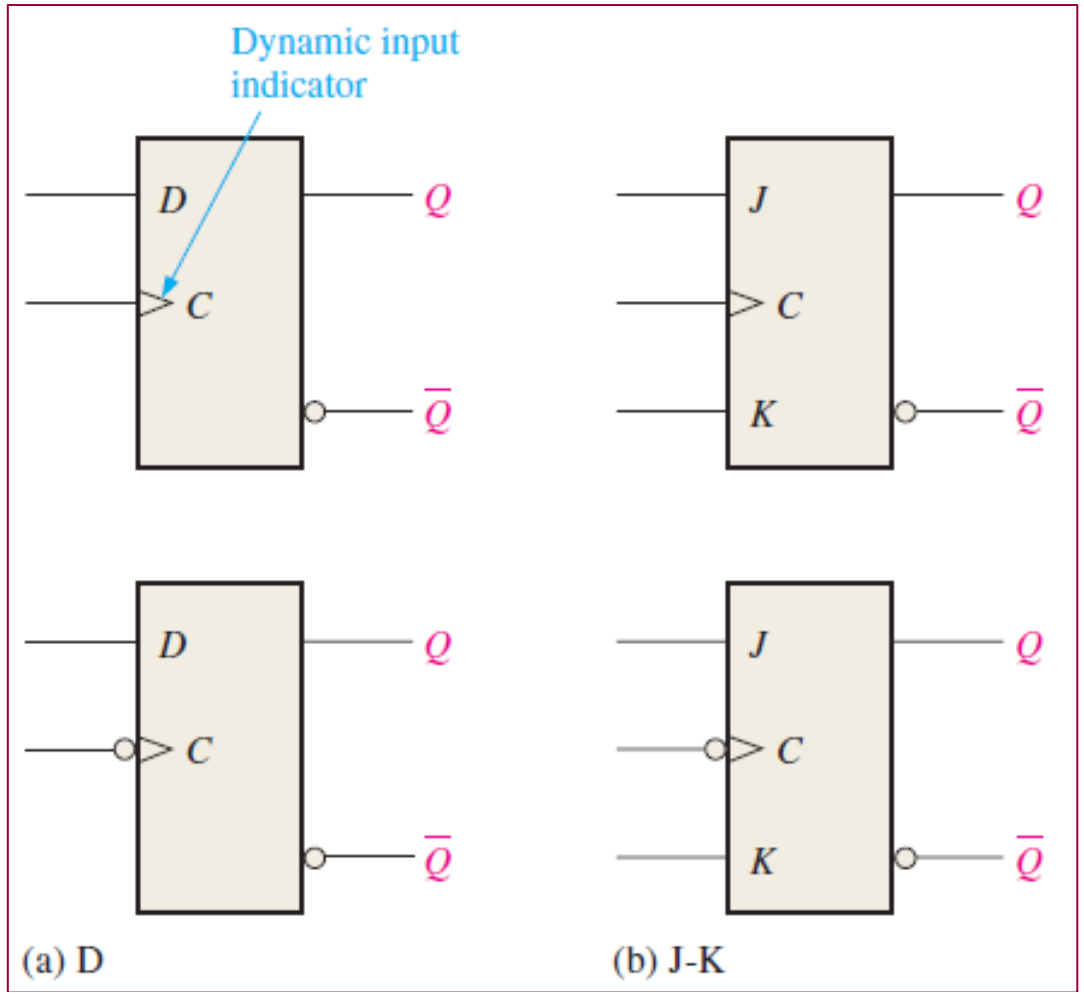
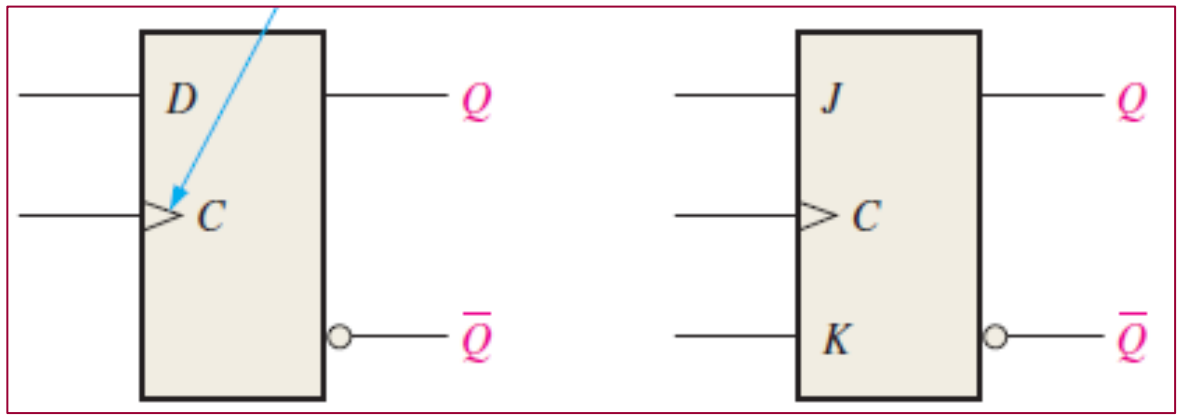


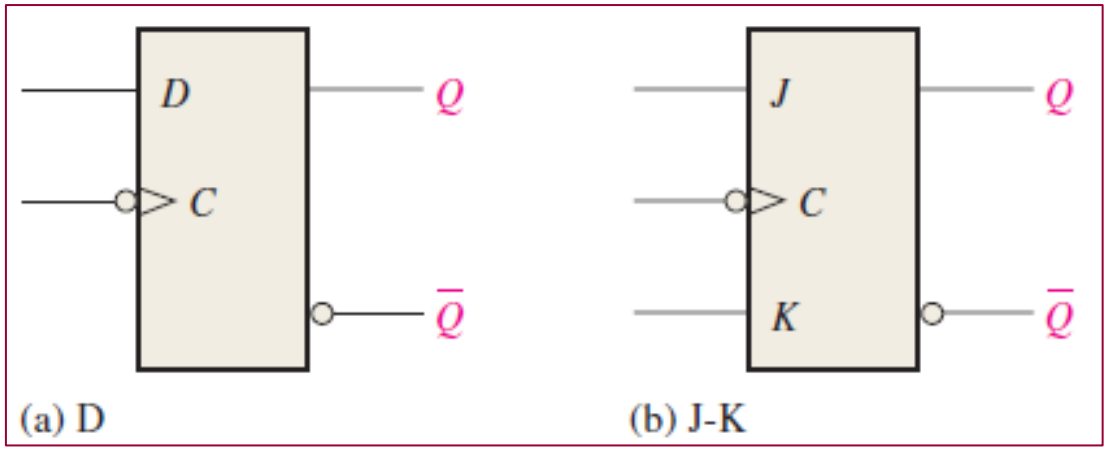
FIGURE 7–13 Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

Edge-triggered Flip-Flops

- An edge-triggered flip-flop changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.
- Two types of edge-triggered flip-flops are: D and J-K.
- The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (*C*) input. This triangle is called the *dynamic input indicator.*



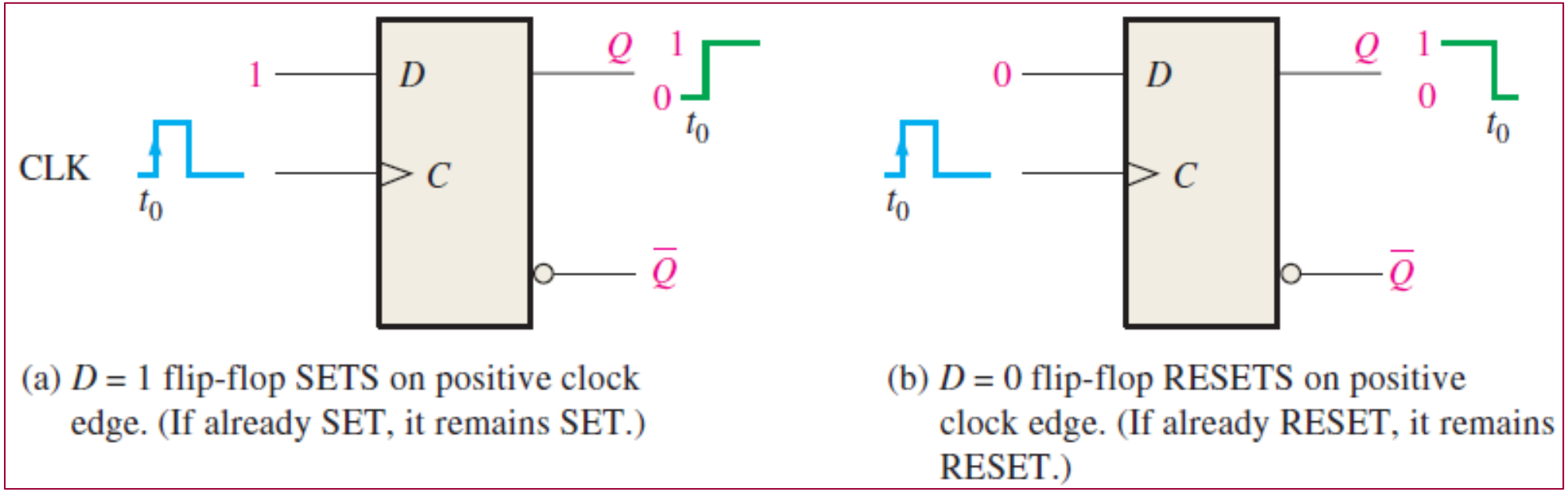
Positive edge-triggered flip-flops



Negative edge-triggered flip-flops

D Flip-Flops

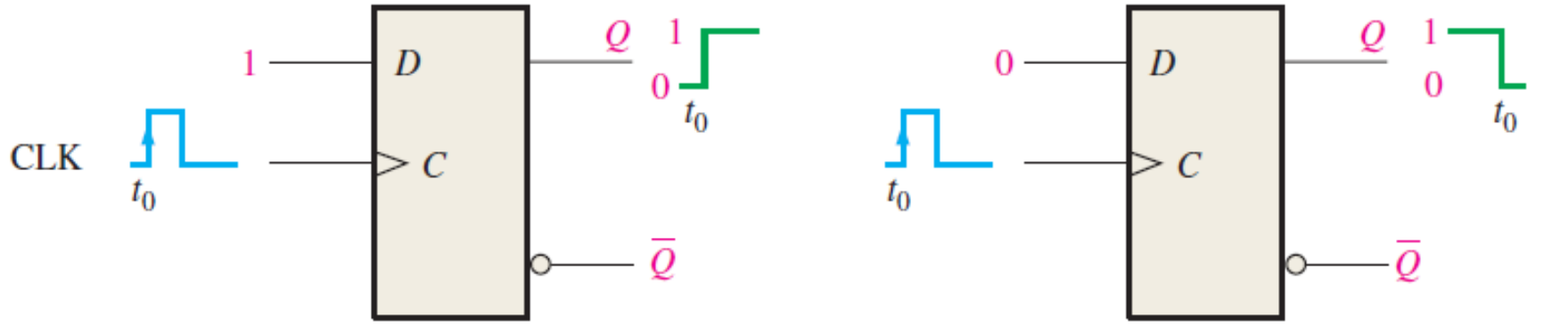
- The D input of the D flip-flop is a synchronous input because data on the input are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- When D is HIGH, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
- When D is LOW, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

D Flip-Flops



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

FIGURE 7–14 Operation of a positive edge-triggered D flip-flop.

- This basic operation of a positive edge-triggered D flip-flop is illustrated in Figure 7–14, and Table 7–2 is the truth table for this type of flip-flop.

TABLE 7–2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

D Flip-Flops

EXAMPLE 7–4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

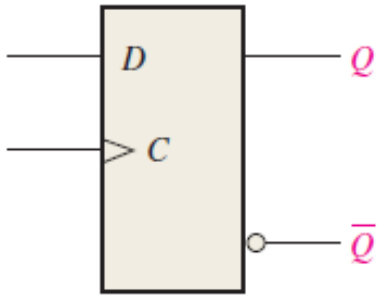


FIGURE 7–15

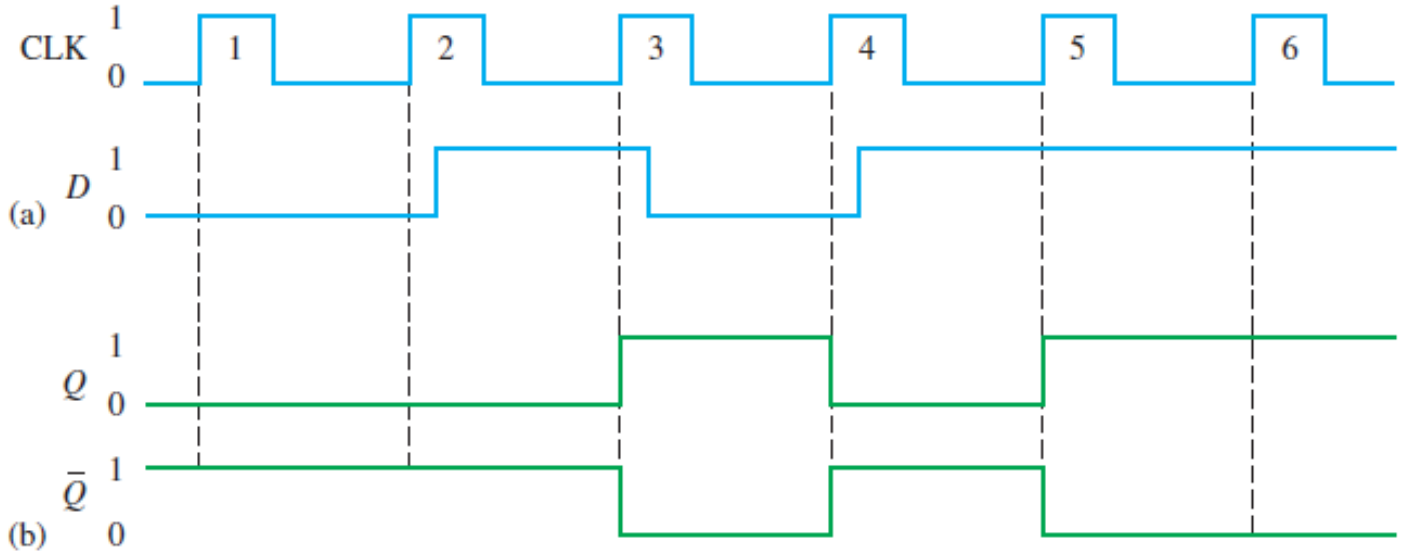


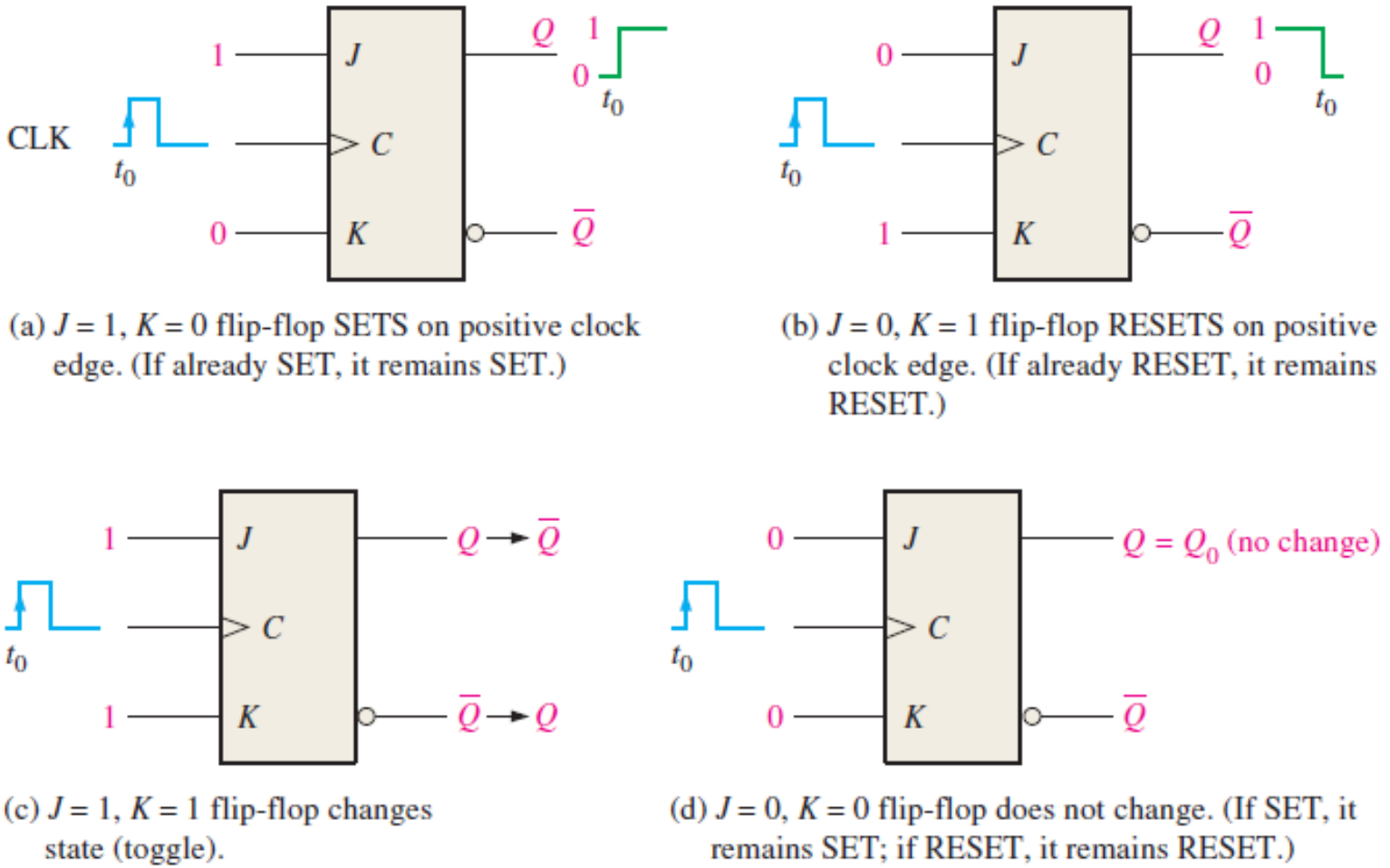
FIGURE 7–16

Solution

1. At clock pulse 1, D is LOW, so Q remains LOW (RESET).
2. At clock pulse 2, D is LOW, so Q remains LOW (RESET).
3. At clock pulse 3, D is HIGH, so Q goes HIGH (SET).
4. At clock pulse 4, D is LOW, so Q goes LOW (RESET).
5. At clock pulse 5, D is HIGH, so Q goes HIGH (SET).
6. At clock pulse 6, D is HIGH, so Q remains HIGH (SET).

J-K Flip-Flops

- The J and K inputs of the **J-K flip-flop** are synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- When J is HIGH and K is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
- When J is LOW and K is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.
- When both J and K are LOW, the output does not change from its prior state. When J and K are both HIGH, the flip-flop changes state. This called the **toggle** mode.



(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

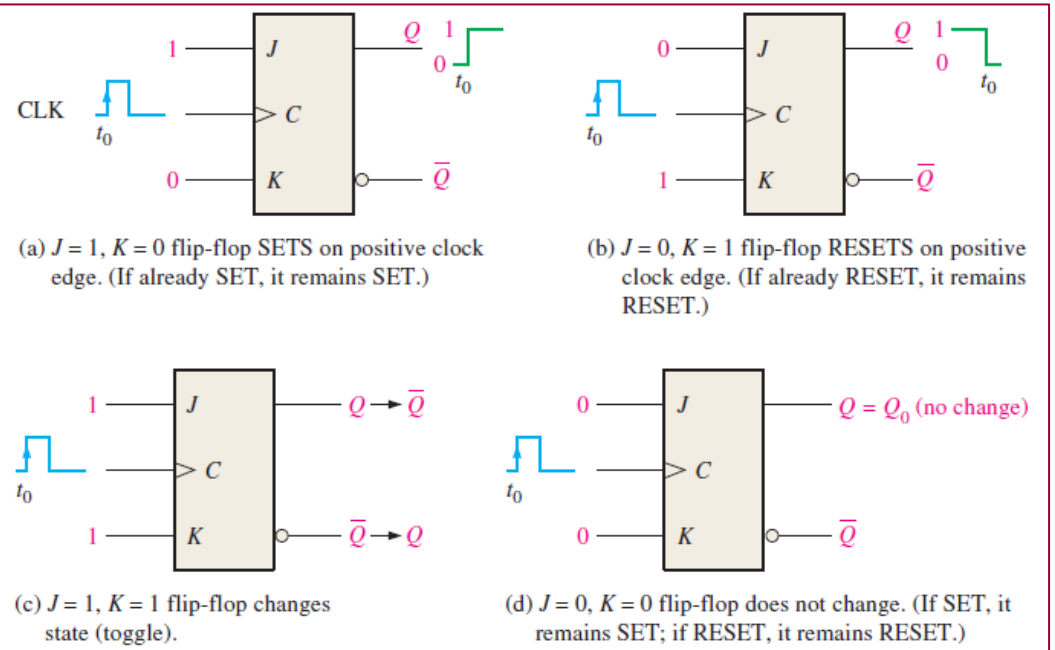
(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).

(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

FIGURE 7–17 Operation of a positive edge-triggered J-K flip-flop.

J-K Flip-Flops

- This basic operation of a positive edge-triggered flip-flop is illustrated in Figure 7–17, and Table 7–3 is the truth table for this type of flip-flop.
- *The flip-flop cannot change state except on the triggering edge of a clock pulse.*
- The *J* and *K* inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output.



(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).

(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

FIGURE 7–17 Operation of a positive edge-triggered J-K flip-flop.

TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	*K*	CLK	*Q*	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

J-K Flip-Flops

EXAMPLE 7–5

The waveforms in Figure 7–18(a) are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

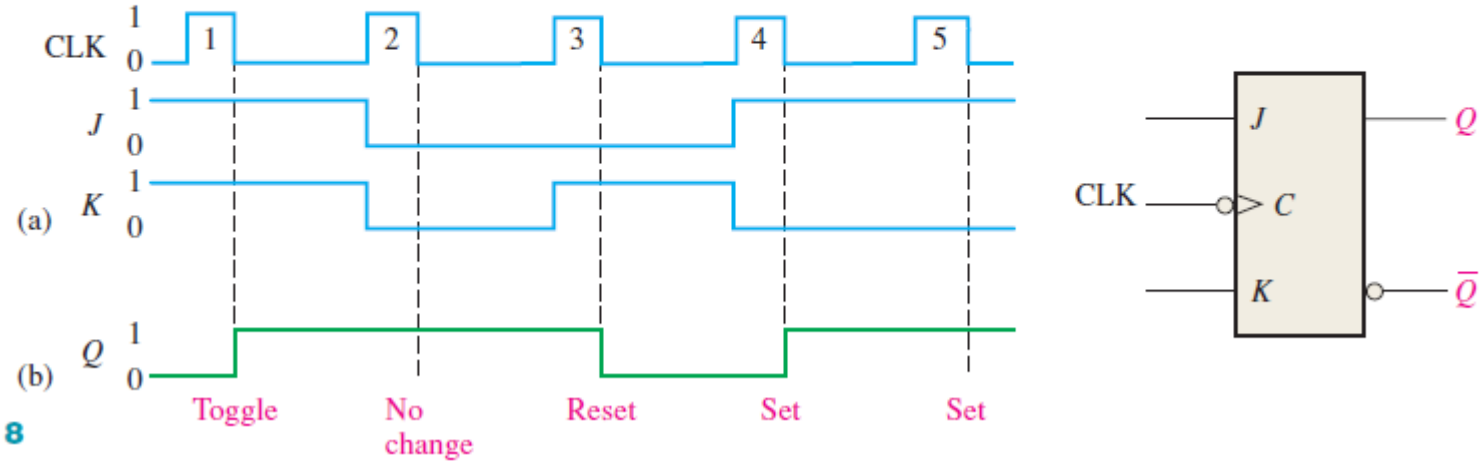


FIGURE 7–18

Solution

Since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the *Q* output will change only on the negative-going edge of the clock pulse.

1. At the first clock pulse, both *J* and *K* are HIGH; and because this is a toggle condition, *Q* goes HIGH.
2. At clock pulse 2, a no-change condition exists on the inputs, keeping *Q* at a HIGH level.
3. When clock pulse 3 occurs, *J* is LOW and *K* is HIGH, resulting in a RESET condition; *Q* goes LOW.
4. At clock pulse 4, *J* is HIGH and *K* is LOW, resulting in a SET condition; *Q* goes HIGH.
5. A SET condition still exists on *J* and *K* when clock pulse 5 occurs, so *Q* will remain HIGH.

Edge triggering

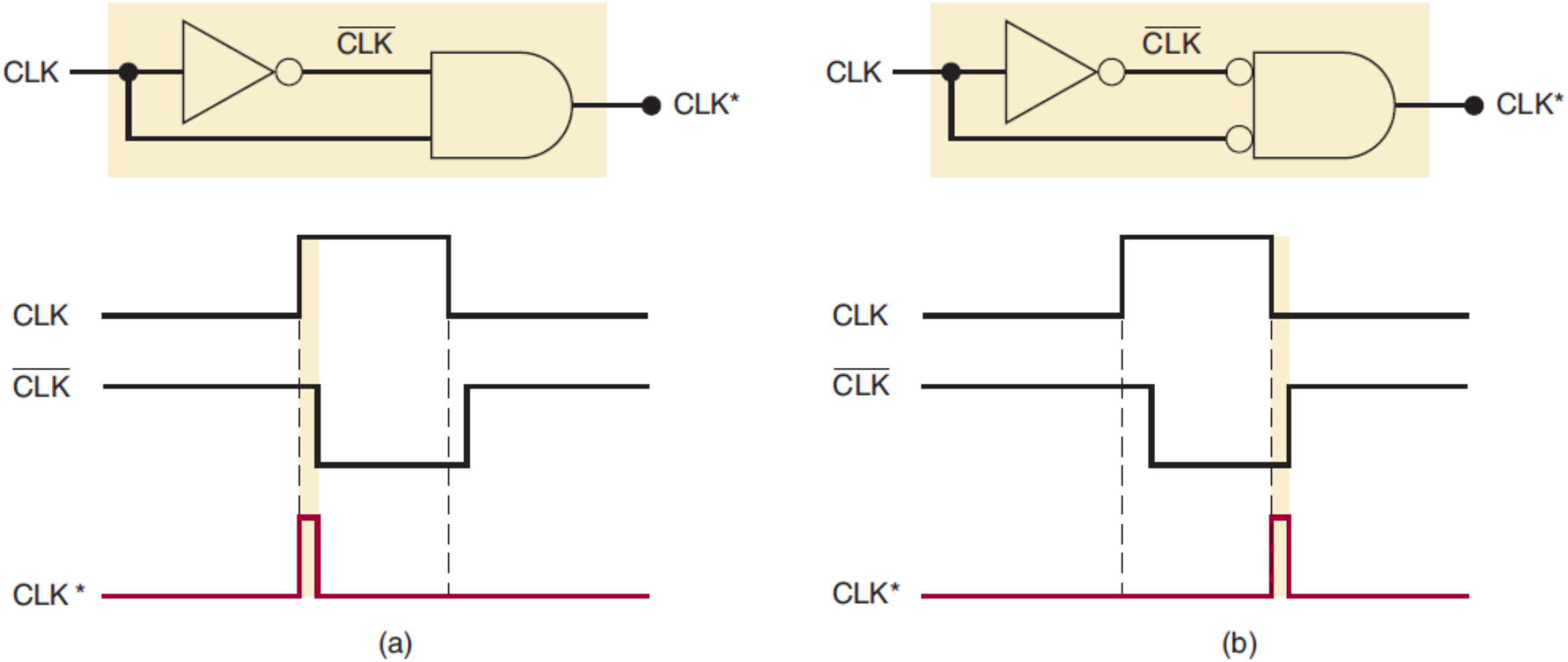


FIGURE 5-23 Implementation of edge-detector circuits used in edge-triggered flip-flops: (a) PGT; (b) NGT. The duration of the *CLK** pulses is typically 2–5 ns.

Edge-triggered D flip-flops (RESET to SET)

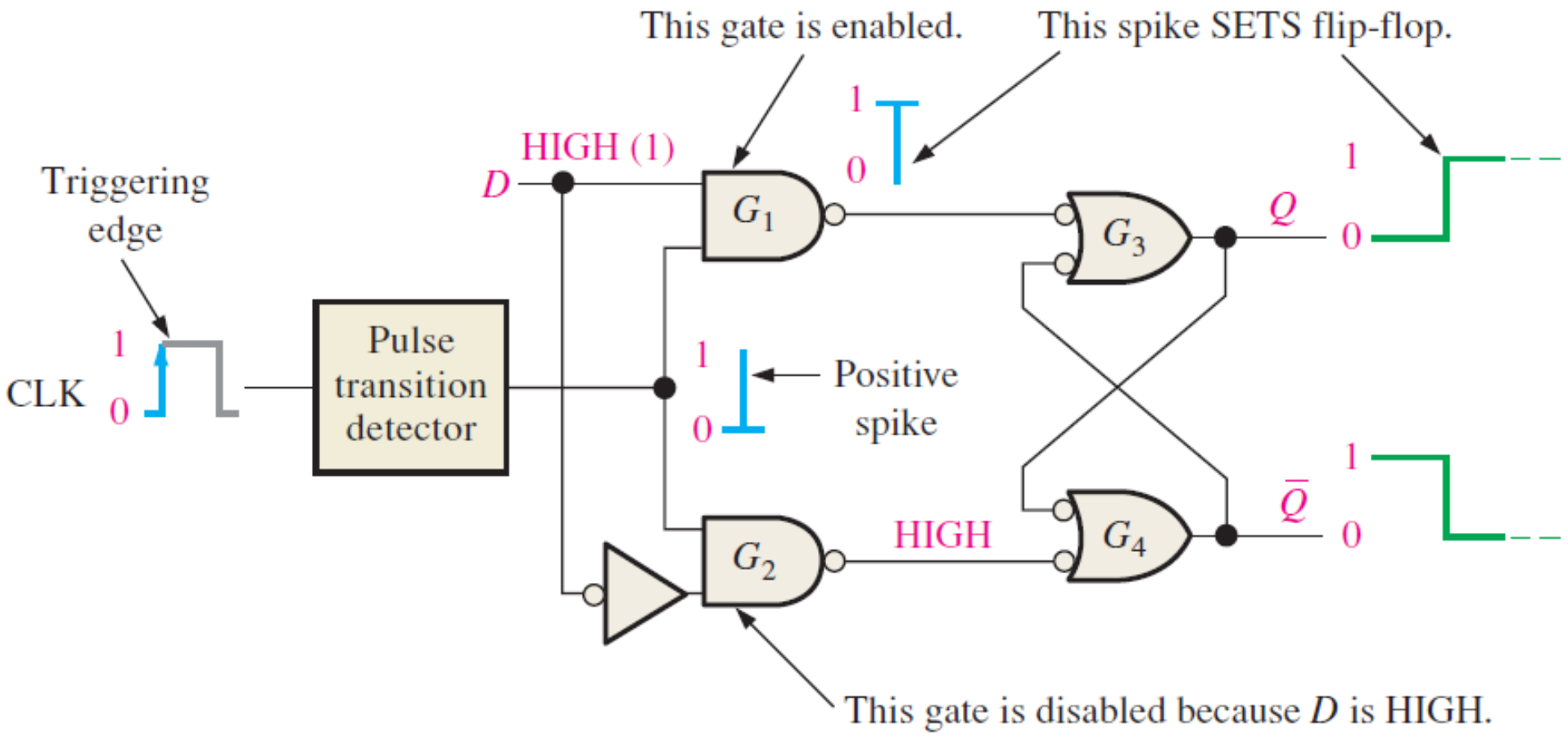


FIGURE 7–20 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

Edge-triggered D flip-flops (SET to RESET)

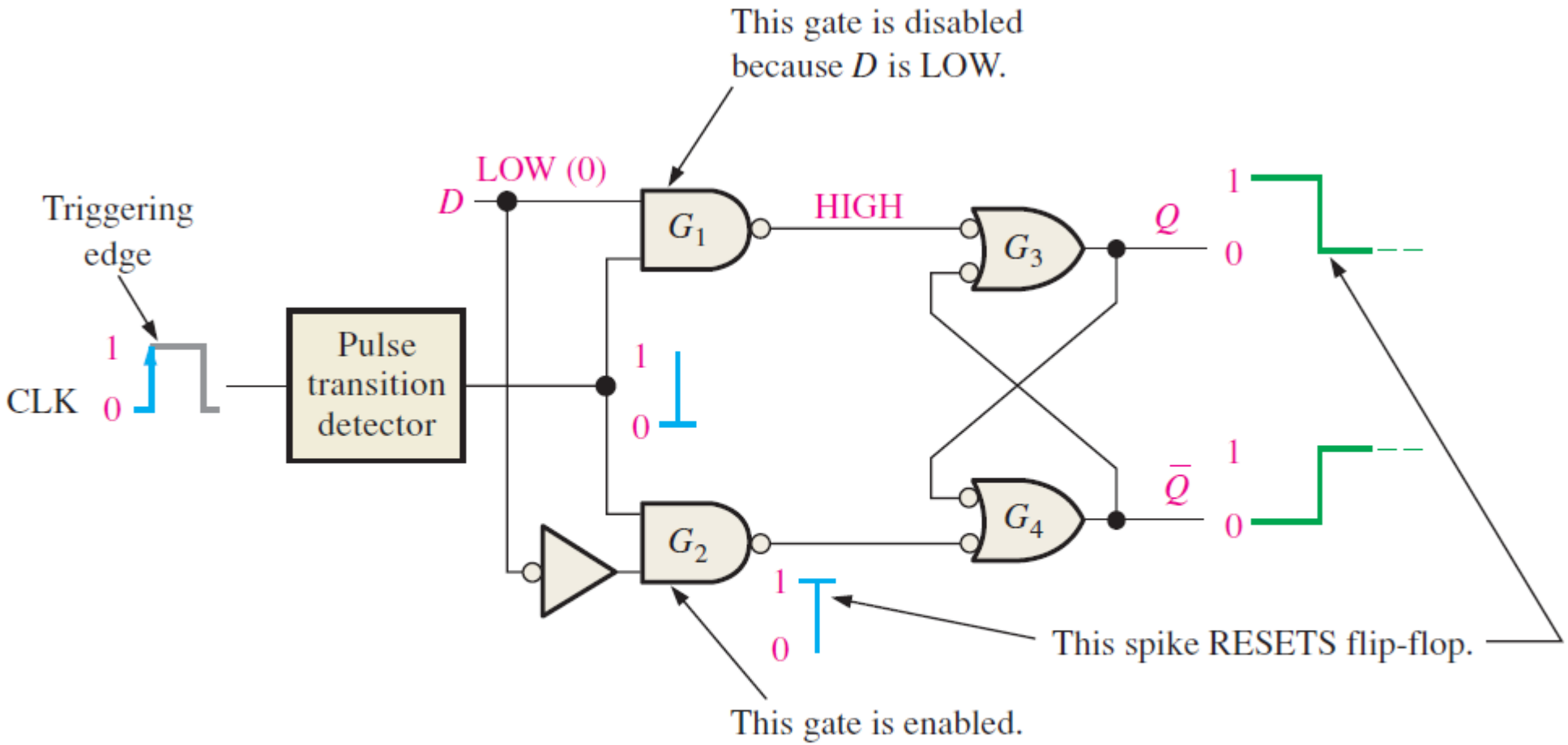


FIGURE 7–21 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

Propagation delays, set-up time, hold-time

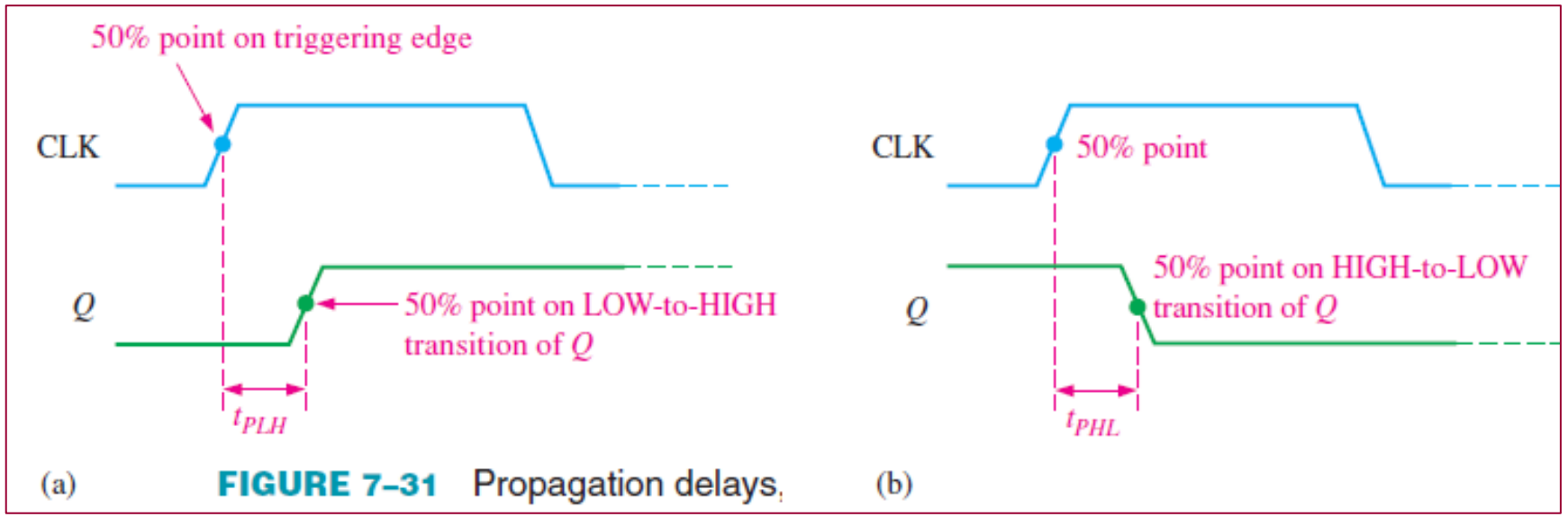


FIGURE 7–31 Propagation delays.

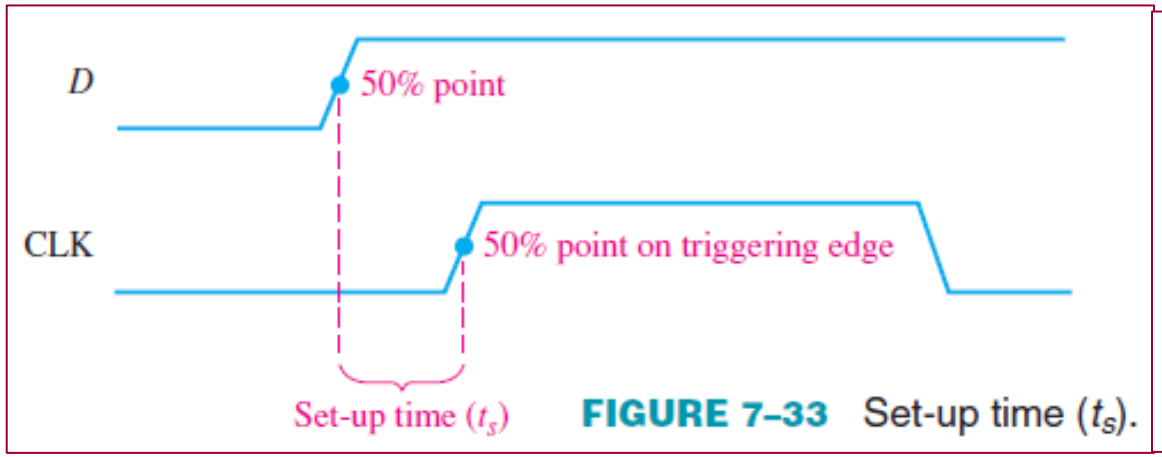


FIGURE 7–33 Set-up time (t_s).

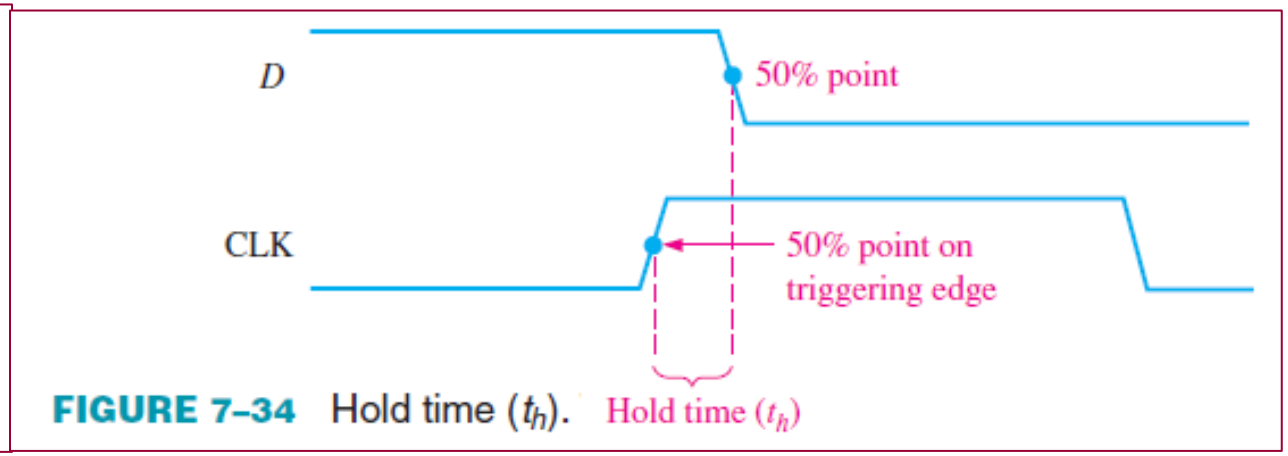


FIGURE 7–34 Hold time (t_h).

Maximum clock frequency, pulse width and power dissipation

- The **maximum clock frequency** (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

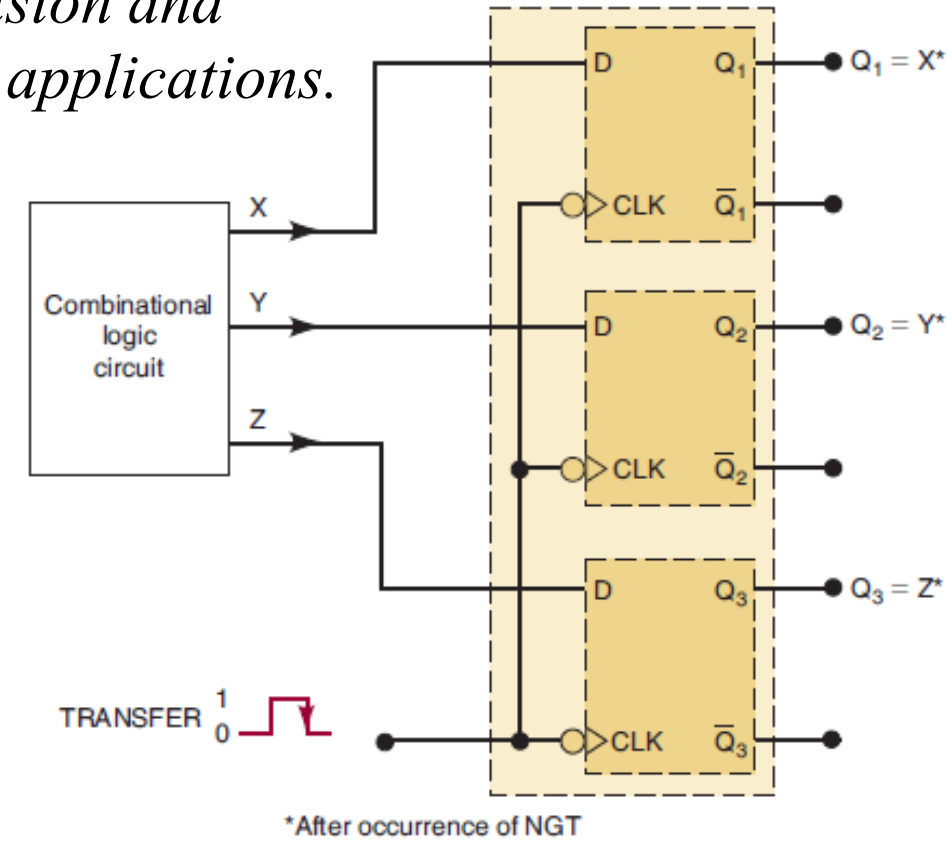
- Minimum **pulse widths** (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

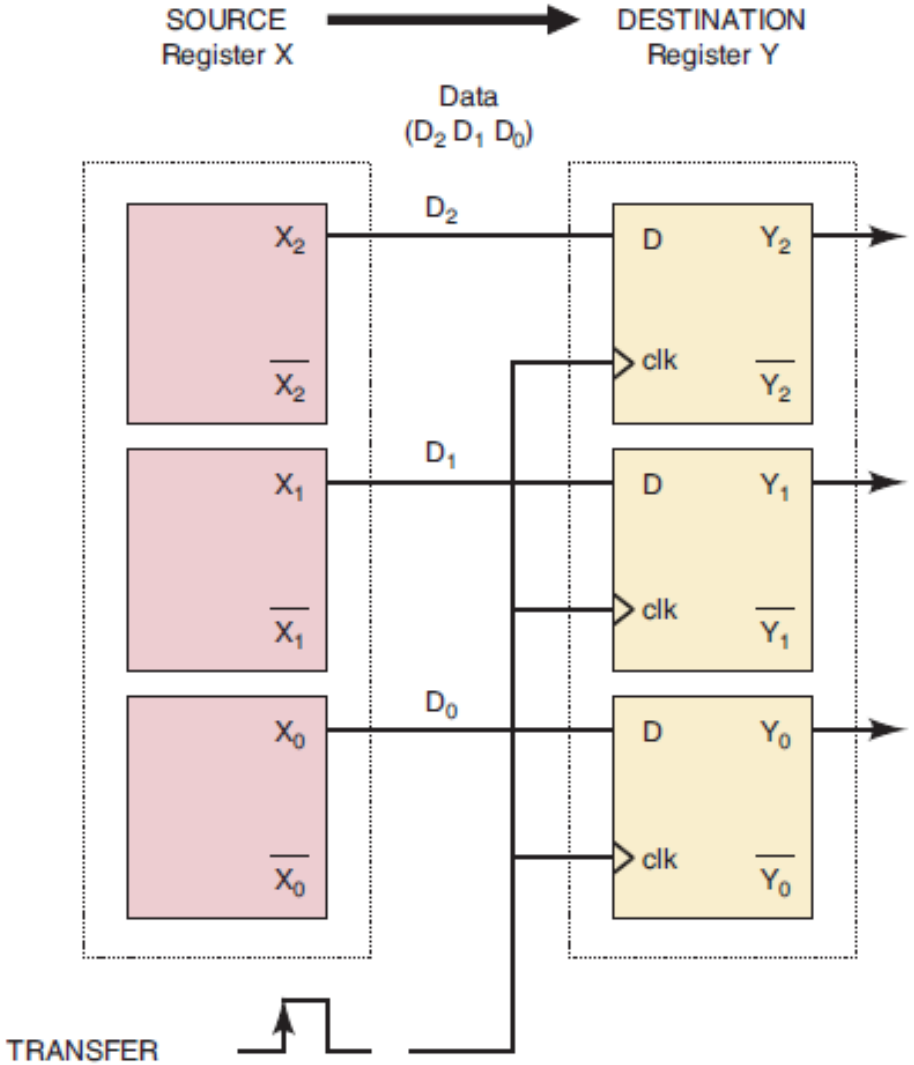
- The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5\ \text{V} \times 5\ \text{mA} = 25\ \text{mW}$$

Flip-Flops applications – *parallel data transfer*

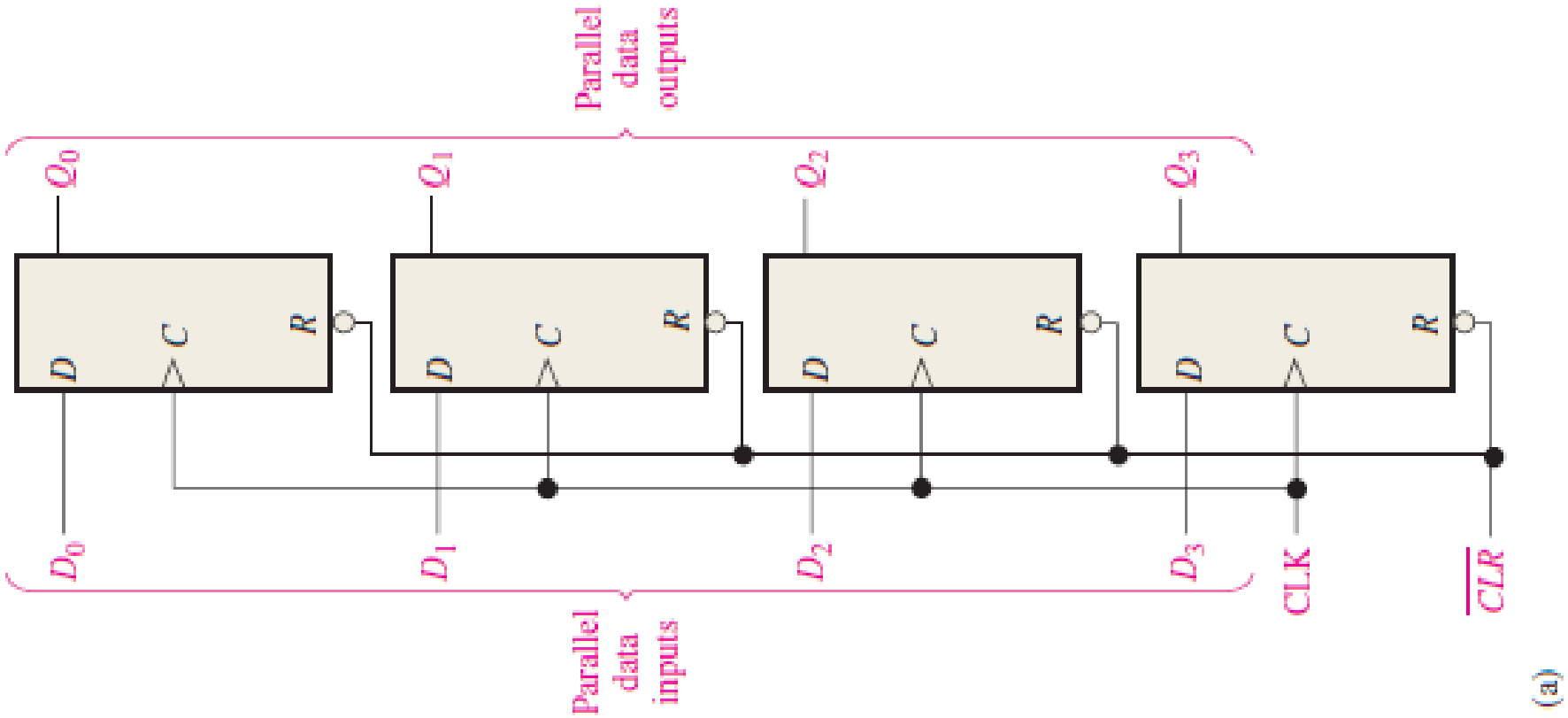
- Flip-flops are used in
  - ✓ *parallel data transfer / storage,*
  - ✓ *frequency division and*
  - ✓ *basic counter applications.*





Flip-Flops applications – *data storage*

- Flip-flops are used in *data storage*, *frequency division* and *basic counter* applications.



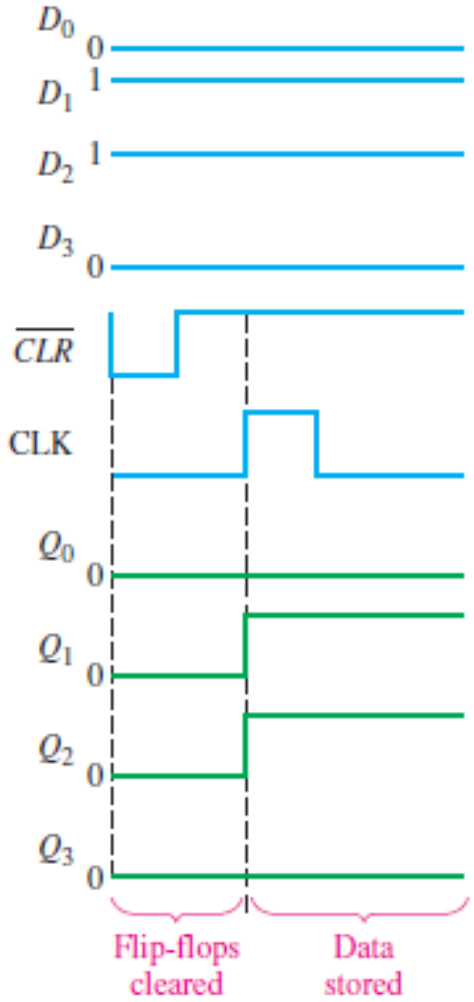
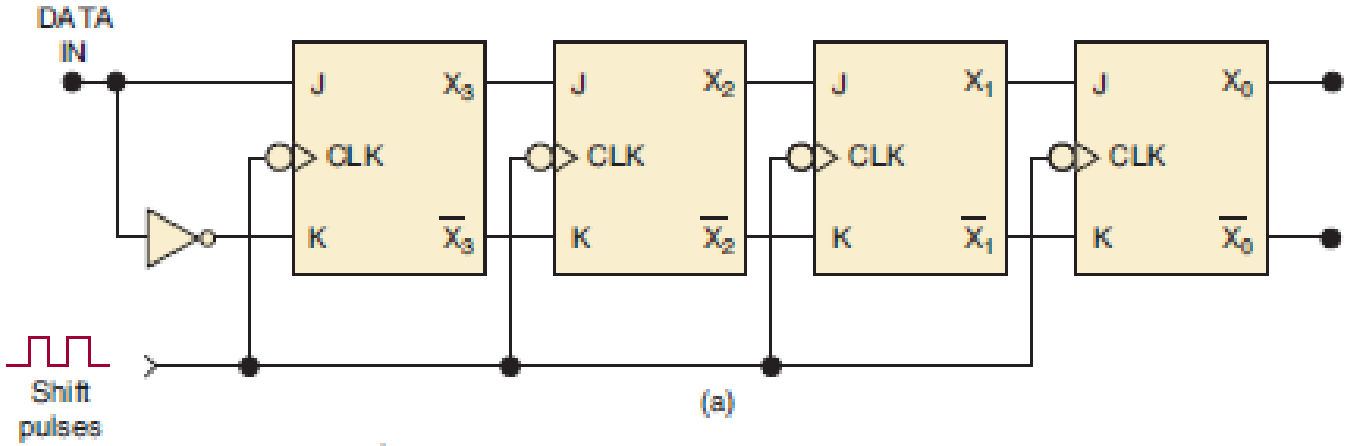


FIGURE 7–35 Example of flip-flops used in a basic register for parallel data storage.

Flip-Flops applications – *serial data transfer*



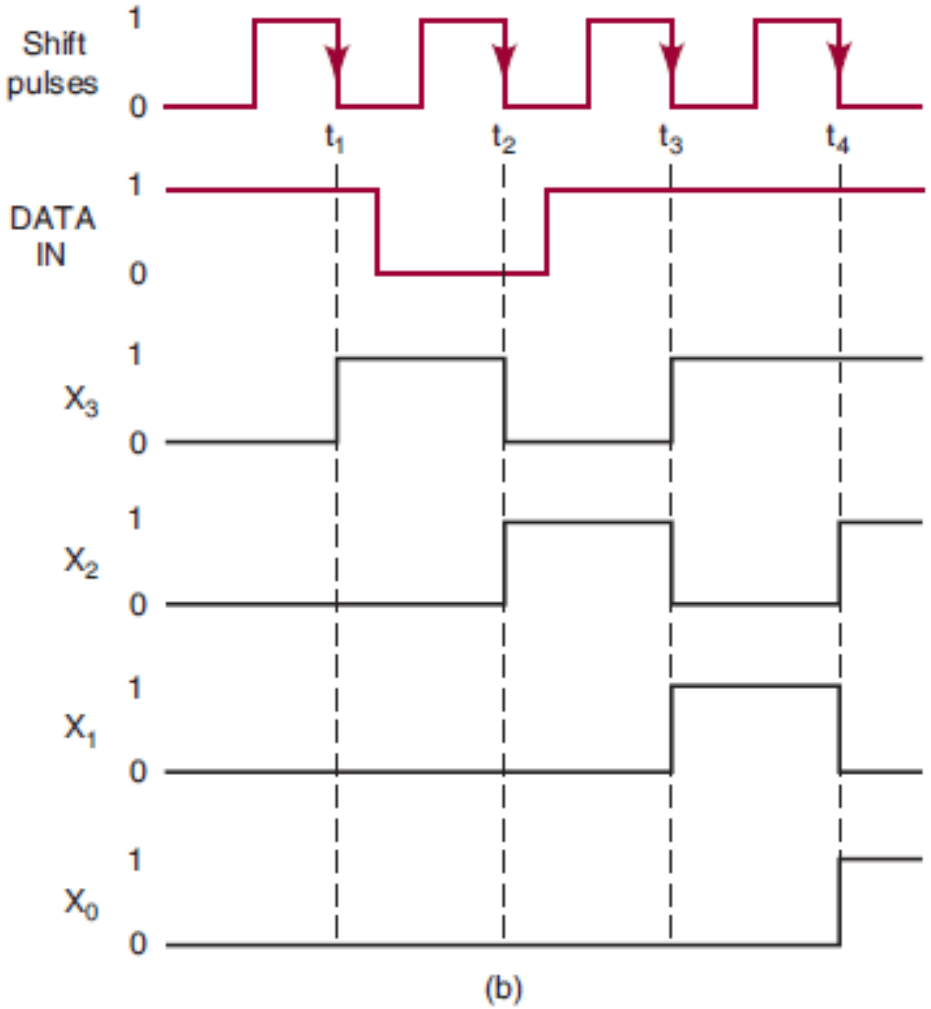
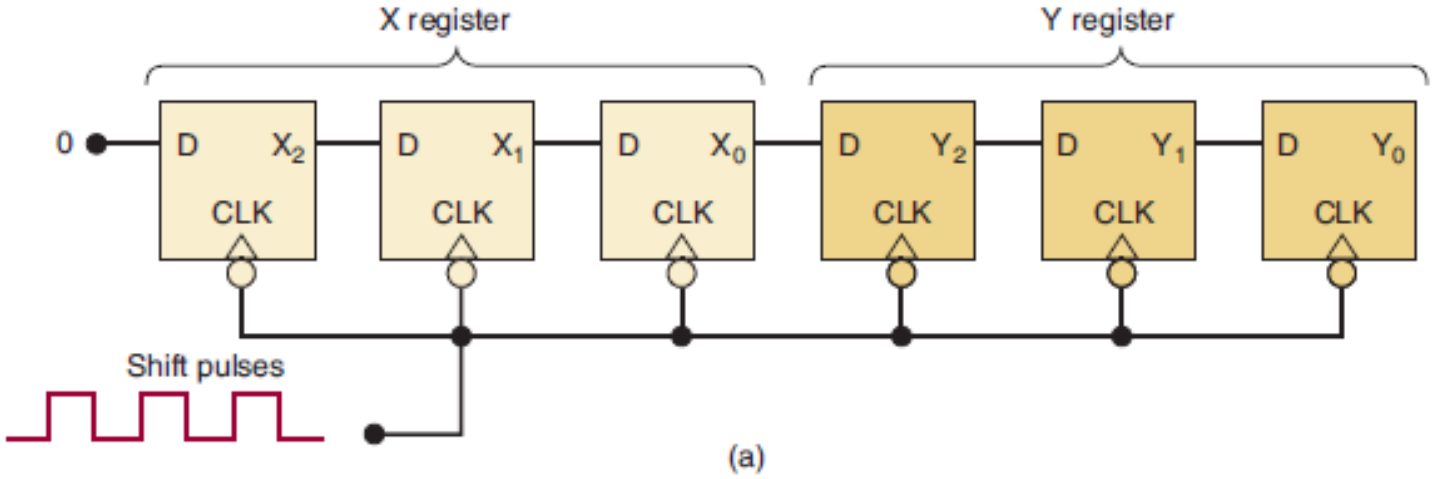


FIGURE 5-46 Four-bit shift register.

Serial data transfer between registers

- Figure shows two three-bit shift registers using D flip-flops. Contents of the *X* register will be serially transferred (shifted) into register *Y.*
- Notice how *X*0, the last FF of register *X*, is connected to the *D* input of *Y*2, the first FF of register *Y.*
- The shift pulses are applied, the information transfer takes place as follows: *X*2→*X*1→*X*0→*Y*2→*Y*1→*Y*0.
- Flip-flop *X*2 will go to a state determined by its *D* input. For now, *D* will be held LOW, so that *X*2 will go LOW on the first pulse and will remain there.



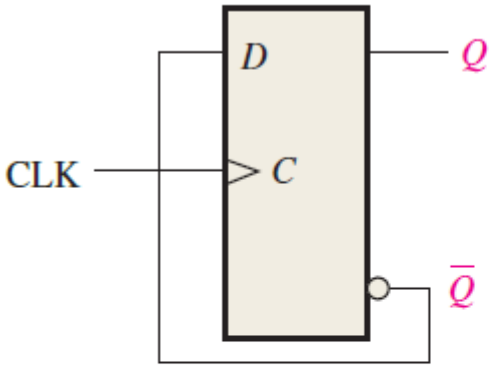
X_2	X_1	X_0	Y_2	Y_1	Y_0	
1	0	1	0	0	0	Before pulses applied
0	1	0	1	0	0	After first pulse
0	0	1	0	1	0	After second pulse
0	0	0	1	0	1	After third pulse

(b)

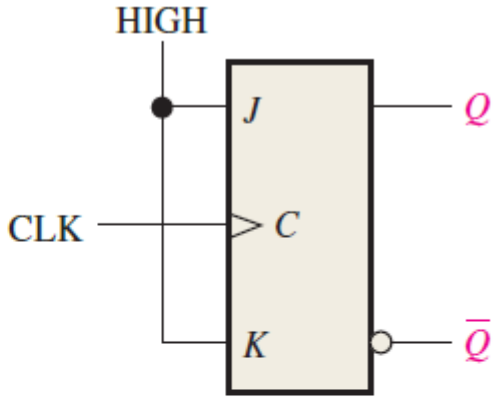
FIGURE 5-47 Serial transfer of information from X register into Y register.

Flip-Flops applications – *frequency division*

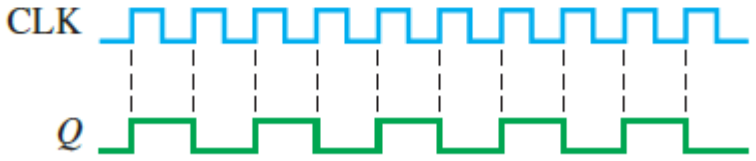
- When a pulse waveform is applied to the clock input of a D or J-K flip-flop that is connected to toggle ($D = Q$ or $J = K = 1$), the Q output is a square wave with one-half the frequency of the clock input.
- Thus, a single flip-flop can be applied as a divide-by-2 device.



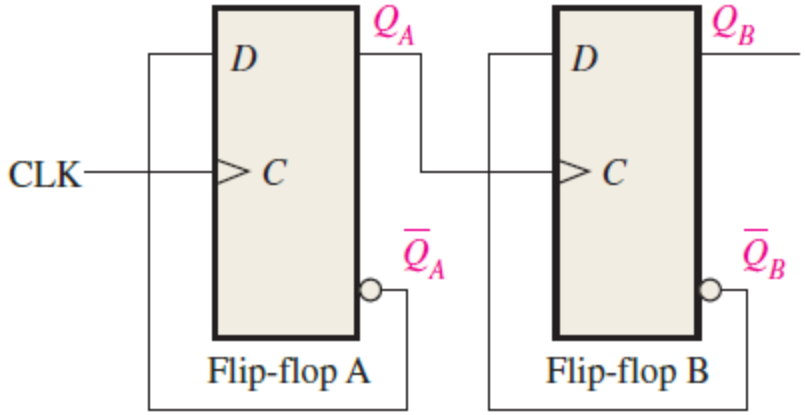
(a)

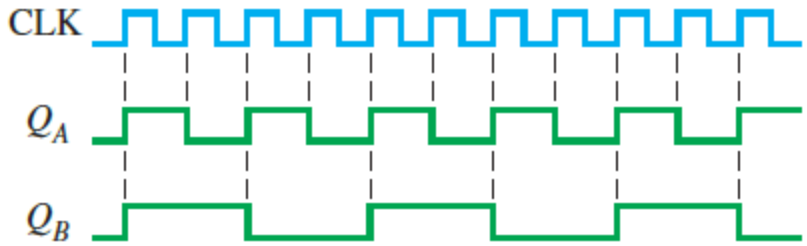


(b)



(c)

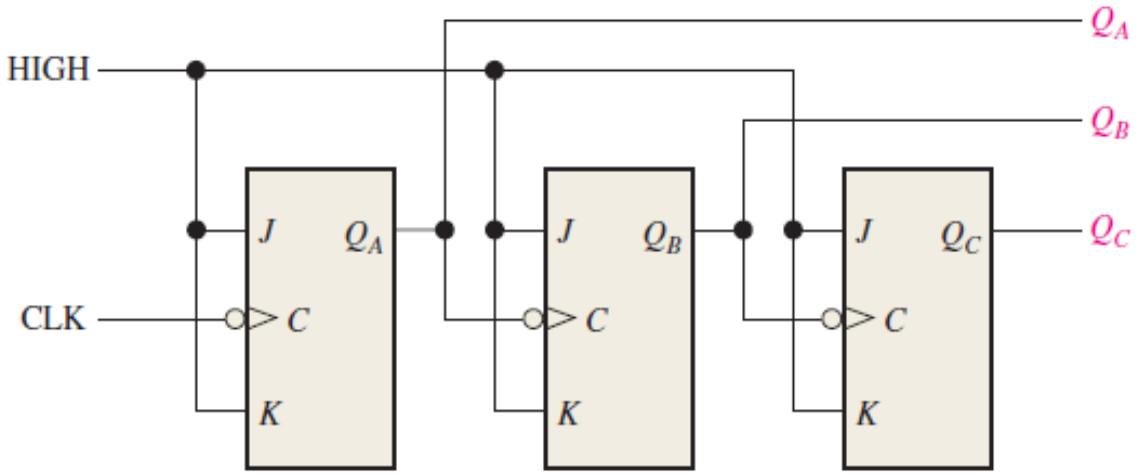


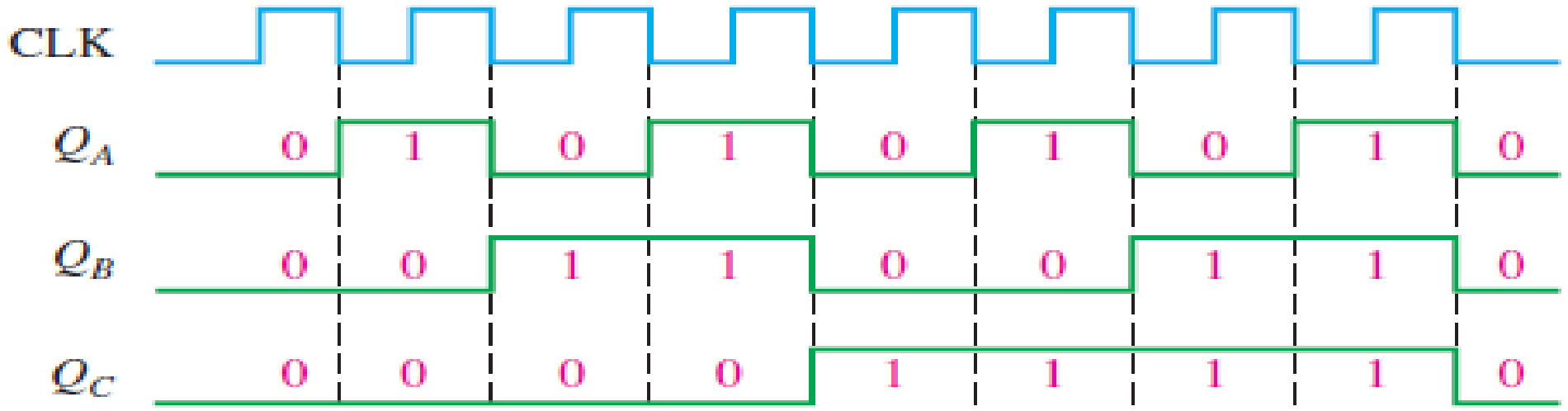


Flip-flop application – *frequency division*

PROBLEM. Determine the output waveforms in relation to the clock for Q_A, Q_B, and Q_C in the circuit of Fig. and show the binary sequence represented by these waveforms.

SOLUTION:





Flip-flops applications – *counting (2-bit)*

- Another important application of flip-flops is in digital counters.
- Negative edge trigger is considered. Both flip-flops are initially RESET.
- Flip-flop A toggle on the negative-going transition of each clock pulse.

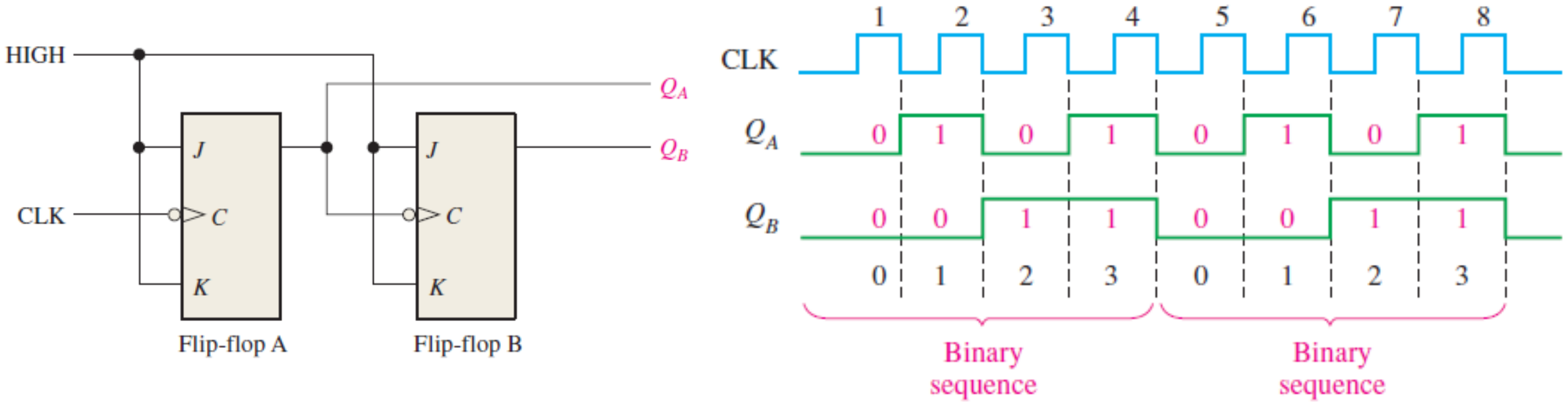


FIGURE 7–40 J-K flip-flops used to generate a binary count sequence (00, 01, 10, 11). Two repetitions are shown.

Flip-flops applications – *counting (3-bit)*

EXAMPLE 7–10

Determine the output waveforms in relation to the clock for Q_A, Q_B, and Q_C in the circuit of Figure 7–41 and show the binary sequence represented by these waveforms.

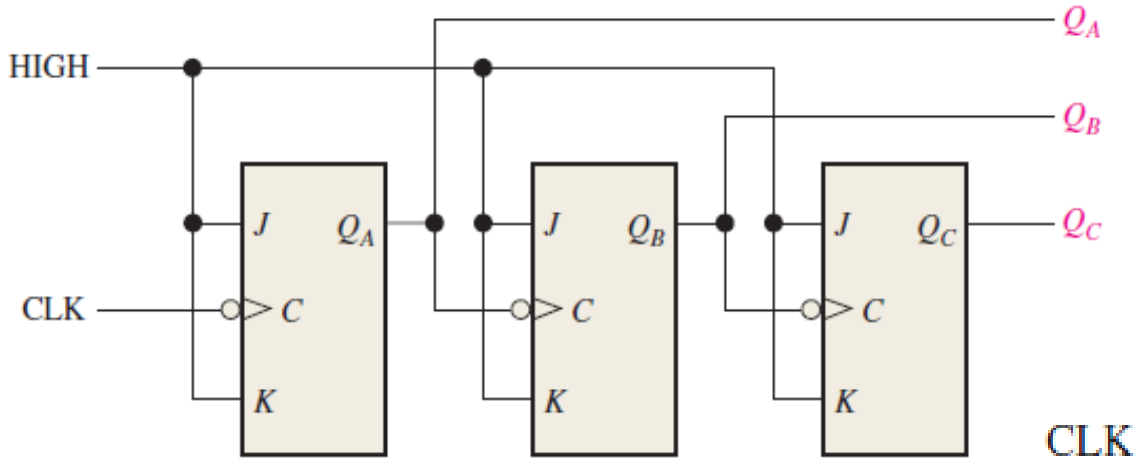
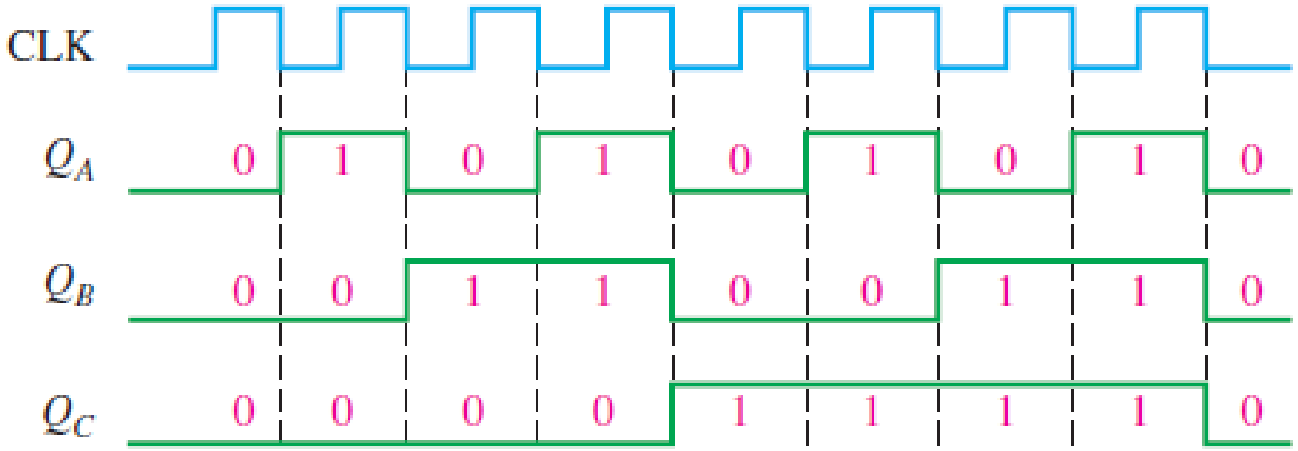


FIGURE 7–41



References

1. ***Digital Fundamentals*** by Thomas Floyd, Pearson International Edition, 11th Edition, Chapter 7, Page 387-448.

2. ***Digital Systems: Principles and Applications*** by Ronald Tocci, Neal Widmer and Greg Moss, Pearson International Edition, 12th Edition, Chapter 5, Page 236-339.

Next class

Register