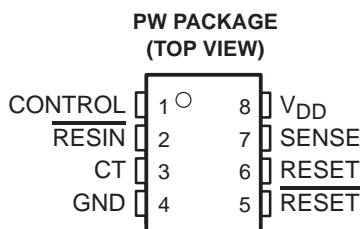


TLC7701-EP, TLC7705-EP, TLC7733-EP MICROPOWER SUPPLY VOLTAGE SUPERVISORS

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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1 \text{ V}$**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 μA**
- **Power Saving Totem-Pole Outputs**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} ($\geq 2 \text{ V}$) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(\text{SENSE})}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d , is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T$$

Where

C_T is in farads

t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d , has expired.

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{\text{CS}}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{\text{CSH1}}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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ORDERING INFORMATION†

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Tape and reel	TLC7701QPWREP	7701QE
	TSSOP – PW	Tape and reel	TLC7705QPWREP	7705QE
	TSSOP – PW	Tape and reel	TLC7733QPWREP	7733QE

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

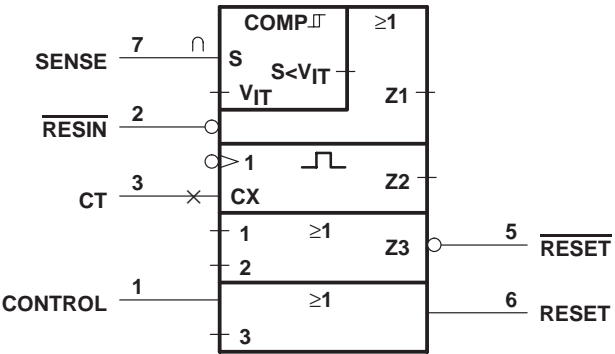
‡ The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7701QPWREP).

FUNCTION TABLE

CONTROL	RESIN	V _I (SENSE)>V _{IT} +	RESET	RESET
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L§	H§
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H§

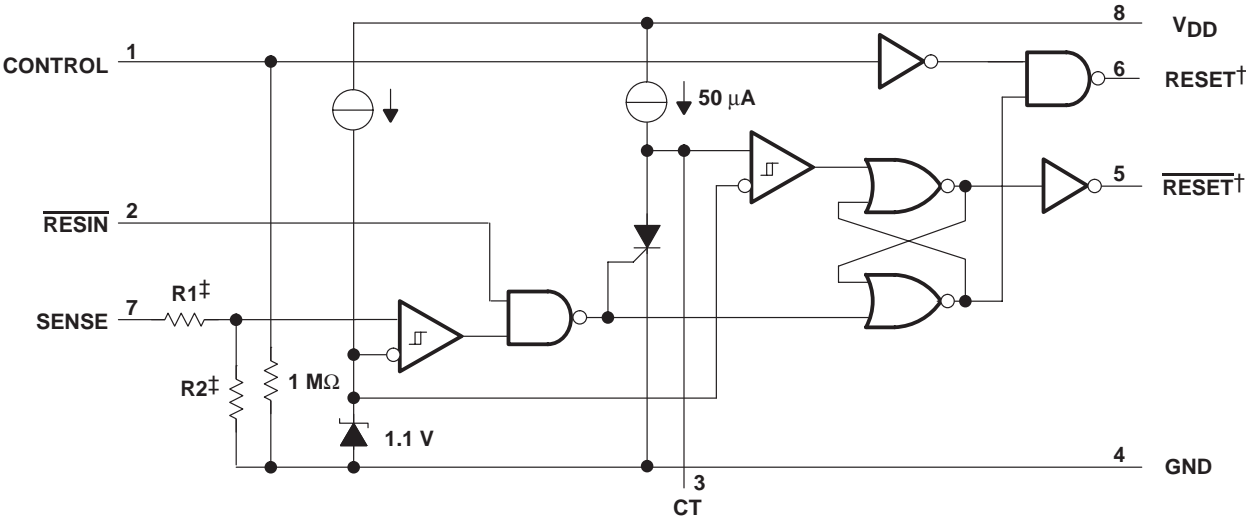
§ RESET and RESET states shown are valid for t > t_d.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617-12.

functional block diagram

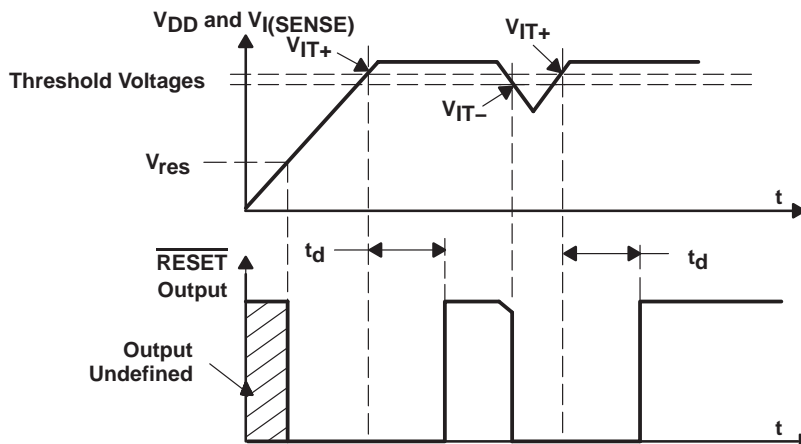


† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.

‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7705	910 kΩ	290 kΩ
TLC7733	750 kΩ	450 kΩ

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	7 V
Input voltage range, CONTROL, $\overline{\text{RESIN}}$, SENSE (see Note 1)	–0.3 V to 7 V
Maximum low output current, I_{OL}	10 mA
Maximum high output current, I_{OH}	–10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TL77xxQ	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
PW	525 mW	4.2 mW/°C	273 mW	105 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage, V_I	0	V_{DD}	V
High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL [‡] , V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL [‡] , V_{IL}		$0.2 \times V_{DD}$	V
High-level output current, I_{OH}		–2	mA
Low-level output current, I_{OL}		2	mA
$V_{DD} \geq 2.7$ V			
Input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	125	°C

[‡] To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

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MICROPOWER SUPPLY VOLTAGE SUPERVISORS

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electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TLC77xx			UNIT
				MIN	TYP†	MAX	
V _{OH} High-level output voltage	I _{OH} = −20 μA		V _{DD} = 2 V	1.8		V	
			V _{DD} = 2.7 V	2.5			
			V _{DD} = 4.5 V	4.3			
	I _{OH} = −2 mA	V _{DD} = 4.5 V	3.7				
V _{OL} Low-level output voltage	I _{OL} = 20 μA		V _{DD} = 2 V		0.2	V	
			V _{DD} = 2.7 V		0.2		
			V _{DD} = 4.5 V		0.2		
	I _{OL} = 2 mA	V _{DD} = 4.5 V		0.5			
V _{IT−} Negative-going input threshold voltage, SENSE (see Note 3)	TLC7701	V _{DD} = 2 V to 6 V		1.04	1.1	1.16	V
	TLC7705			4.43	4.5	4.63	
	TLC7733			2.855	2.93	3.03	
V _{hys} Hysteresis voltage, SENSE	TLC7701	V _{DD} = 2 V to 6 V		30		mV	
	TLC7705			70			
	TLC7733						
V _{res} Power-up reset voltage‡			I _{OL} = 20 μA			1	V
I _I Input current	RESIN		V _I = 0 V to V _{DD}			2	μA
	CONTROL		V _I = V _{DD}		7	15	
	SENSE		V _I = 5 V		5	10	
	SENSE, TLC7701 only		V _I = 5 V			2	
I _{DD} Supply current			RESIN = V _{DD} , SENSE = V _{DD} ≥ V _{ITmax} + 0.2 V CONTROL = 0 V, Outputs open		9	16	μA
I _{DD(d)} Supply current during t _d			V _{DD} = 5 V, V _{CT} = 0 , RESIN = V _{DD} , SENSE = V _{DD} , CONTROL = 0 V, Outputs open		120	150	μA
C _I Input capacitance, SENSE			V _I = 0 V to V _{DD}		50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which RESET becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 µs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 µF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be connected near the supply terminals.

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switching characteristics at $V_{DD} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$, $T_A = \text{Full Range}$ (unless otherwise noted)

PARAMETER	MEASURED		TEST CONDITIONS	TLC77xx			UNIT
	FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d Delay time	$V_{I(\text{SENSE})} \geq V_{IT+}$	RESET and RESET	$\overline{\text{RESIN}} = 0.7 \times V_{DD}$, $\text{CONTROL} = 0.2 \times V_{DD}$, $C_T = 100\text{ nF}$, $T_A = \text{Full range}$, See timing diagram	1.1	2.1	4.2	ms
t_{PLH} Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, $\text{CONTROL} = 0.2 \times V_{DD}$, $C_T = \text{NC}^\dagger$			20	μs
t_{PHL} Propagation delay time, high-to-low-level output		$\overline{\text{RESET}}$				5	
t_{PLH} Propagation delay time, low-to-high-level output		RESET				5	
t_{PHL} Propagation delay time, high-to-low-level output		RESET				20	
t_{PLH} Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, $\text{SENSE} = V_{IT+max} + 0.2\text{ V}$, $\text{CONTROL} = 0.2 \times V_{DD}$, $C_T = \text{NC}^\dagger$			20	μs
t_{PHL} Propagation delay time, high-to-low-level output		$\overline{\text{RESET}}$				60	ns
t_{PLH} Propagation delay time, low-to-high-level output		RESET				65	
t_{PHL} Propagation delay time, high-to-low-level output		RESET				20	μs
t_{PLH} Propagation delay time, low-to-high-level output	CONTROL	RESET	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$, $\text{SENSE} = V_{IT+max} + 0.2\text{ V}$, $\overline{\text{RESIN}} = 0.7 \times V_{DD}$, $C_T = \text{NC}^\dagger$			58	ns
t_{PHL} Propagation delay time, high-to-low-level output						58	ns
Low-level minimum pulse duration to switch RESET and RESET	SENSE		$V_{IH} = V_{IT+max} + 0.2\text{ V}$, $V_{IL} = V_{IT-min} - 0.2\text{ V}$,	3			μs
	$\overline{\text{RESIN}}$		$V_{IL} = 0.2 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1			
t_r Rise time		RESET and RESET	10% to 90%		8		ns/V
t_f Fall time		RESET and RESET	90% to 10%		4		

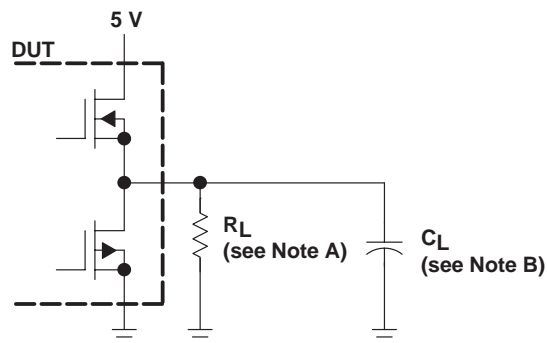
† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. For switching characteristics, $R_L = 2\text{ k}\Omega$.
B. $C_L = 50\text{ pF}$ includes jig and probe capacitance.

Figure 1. RESET AND $\overline{\text{RESET}}$ Output Configurations

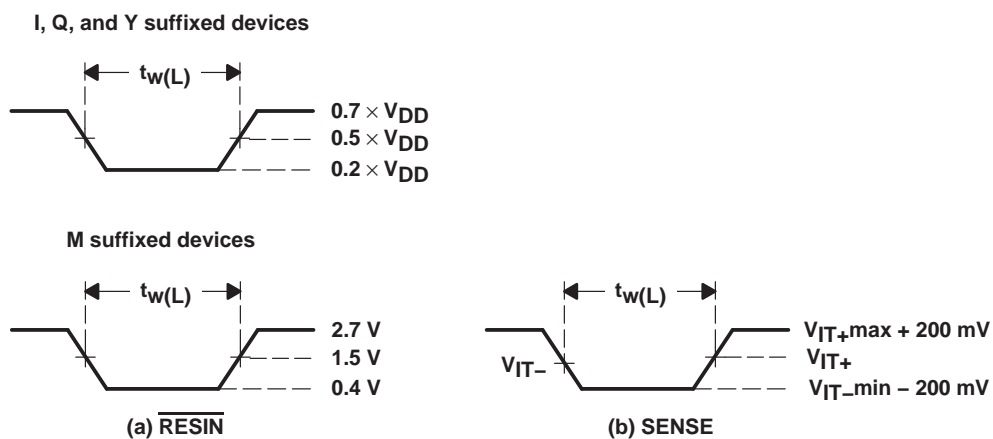


Figure 2. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

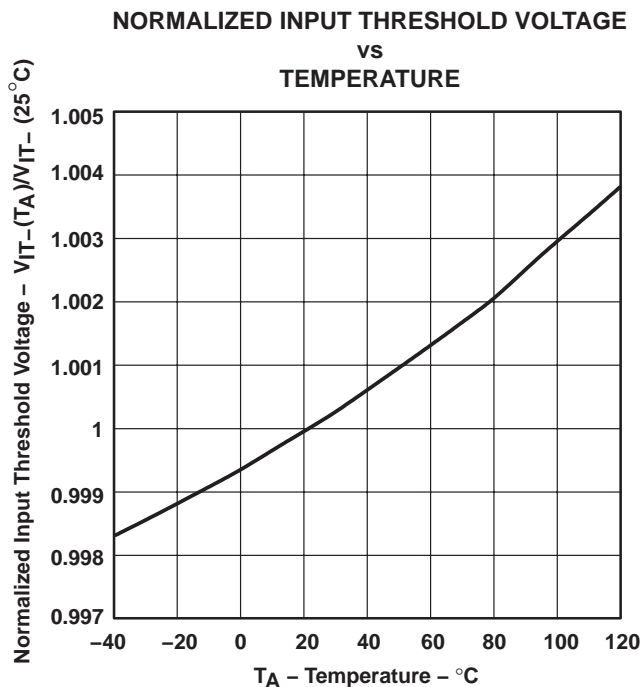


Figure 3

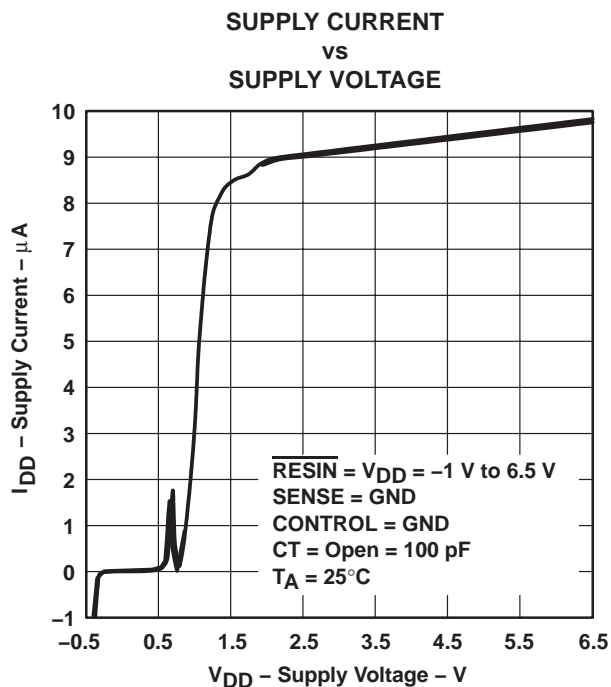


Figure 4

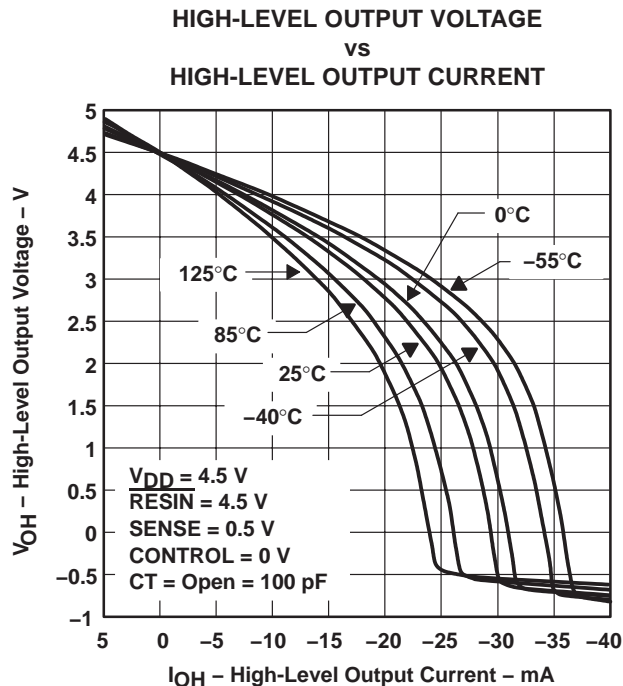


Figure 5

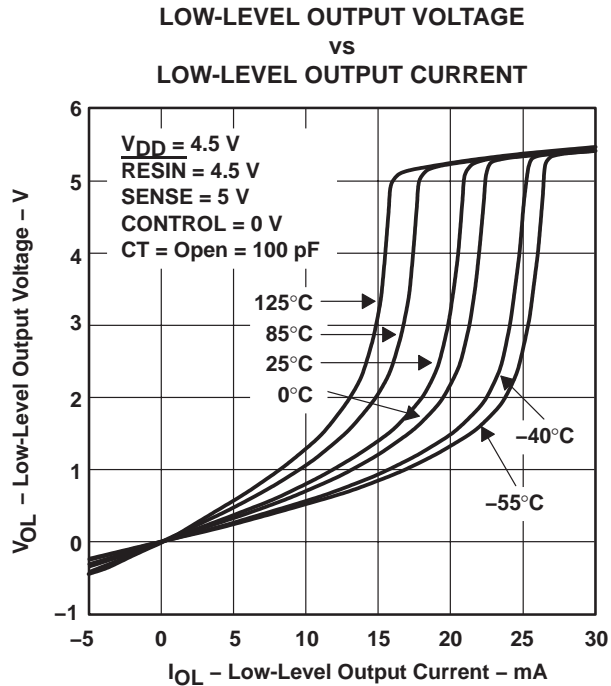


Figure 6

TYPICAL CHARACTERISTICS

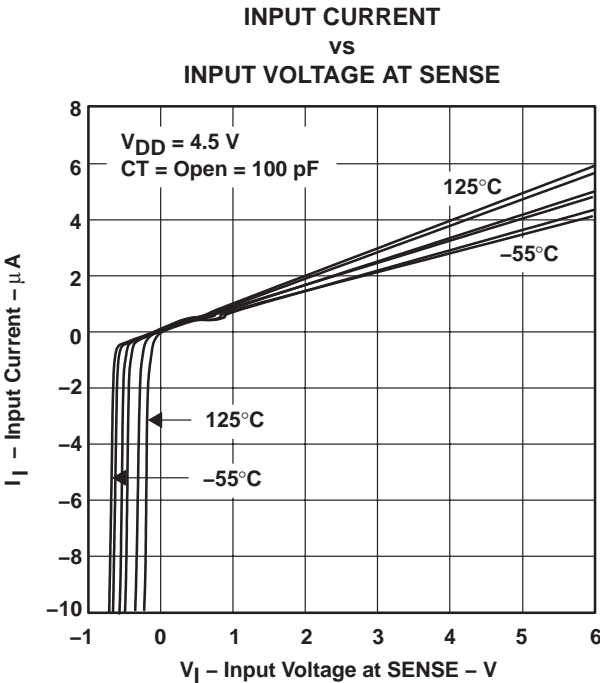


Figure 7

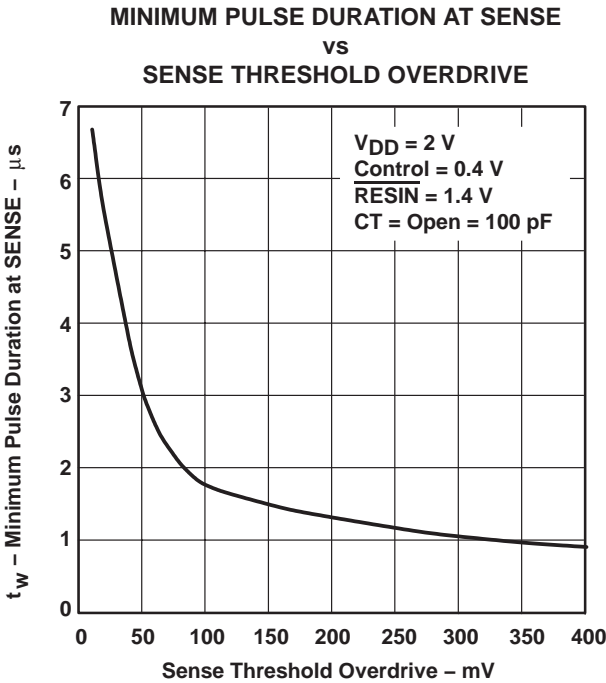


Figure 8

APPLICATION INFORMATION

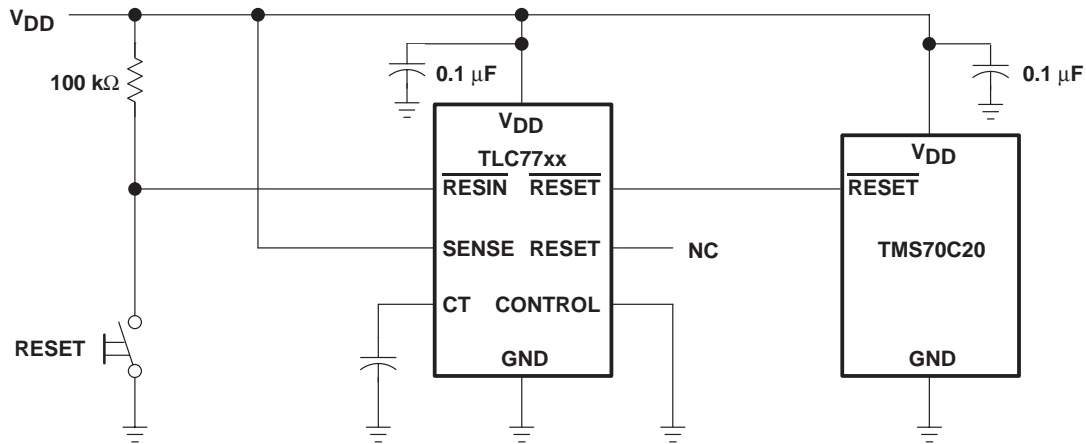


Figure 9. Reset Controller in a Microcomputer System

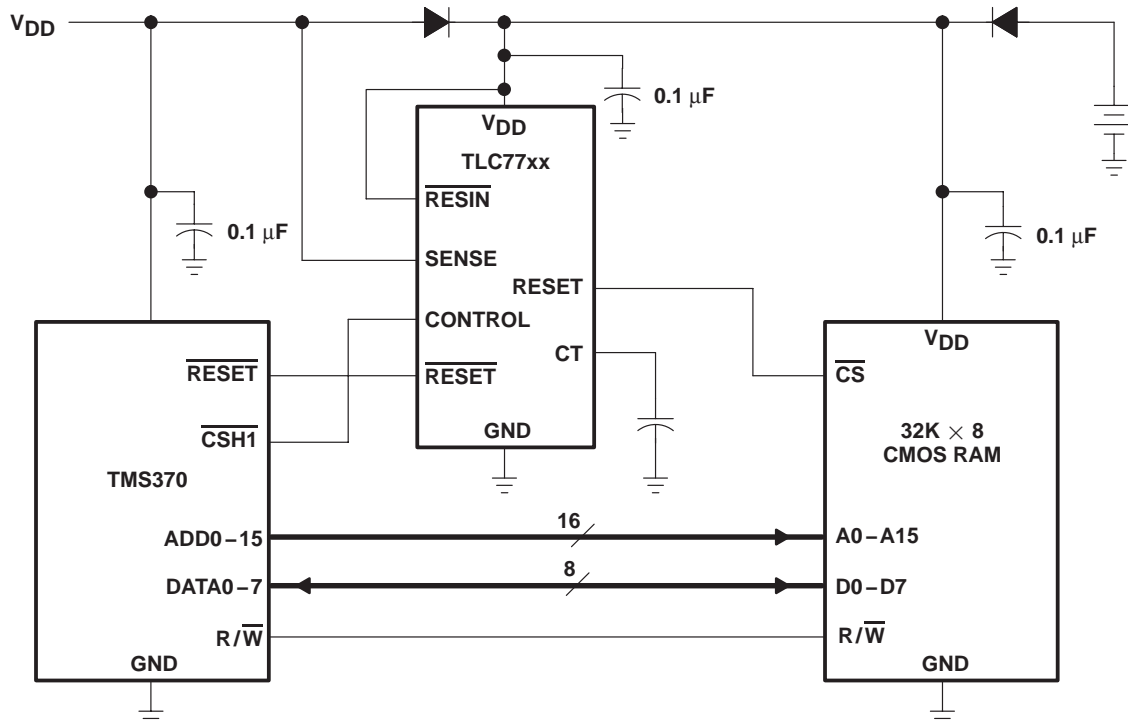


Figure 10. Data Retention During Power Down Using Static CMOS RAMs

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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