FAIRCHILD SEMICONDUCTOR®

April 2000
Revised February 2005

NC7SZ57 • NC7SZ58
TinyLogic® UHS Universal Configurable 2-Input Logic Gates

General Description

The NC7SZ57 and the NC7SZ58 are Universal Configurable 2-Input Logic Gates. Each device is capable of being configured for 1 of 5 unique 2-input logic functions. Any possible 2-input combinatorial logic function can be implemented as shown in the Function Selection Table. Device functionality is selected by how the device is wired at the board level. Figure 1 through Figure 10 illustrate how to connect the NC7SZ57 and NC7SZ58 respectively for the desired logic function. All inputs have been implemented with hysteresis.

The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The input and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 5.5V independent of V_{CC} operating range.

Features

- Space saving SC70-6 lead surface mount package
- Ultra small MicroPak™ Pb-Free leadless package
- Ultra High Speed
- Capable of implementing any 2-input logic function
- Typical usage replaces 2 TinyLogic® gate devices
- Reduces part counts in inventory
- Broad V_{CC} operating range: 1.65V to 5.5V
- Power down high impedance input/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ57P6X	MAA06A	Z57	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ57P6X_NL (Note 1)	MAA06A	Z57	Pb-Free 6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ57L6X	MAC06A	KK	Pb-Free 6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel
NC7SZ58P6X	MAA06A	Z58	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ58P6X_NL (Note 1)	MAA06A	Z58	Pb-Free 6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ58L6X	MAC06A	LL	Pb-Free 6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

Pin Descriptions

Pin Name	Description
I_0, I_1, I_2	Data Inputs
Y	Output

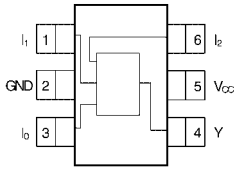
Function Table

Inputs			NC7SZ57	NC7SZ58
I_2	I_1	I_0	$Y = (\bar{I}_0)\bullet(\bar{I}_2)+(I_1)\bullet(I_2)$	$Y = (I_0)\bullet(\bar{I}_2)+(\bar{I}_1)\bullet(I_2)$
L	L	L	H	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	H
H	L	H	L	H
H	H	L	H	L
H	H	H	H	L

H = HIGH Logic Level L = LOW Logic Level

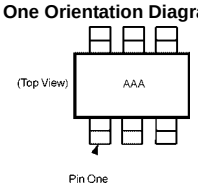
Connection Diagrams

Pin Assignments for SC70



(Top View)
NC7SZ57 and NC7SZ58

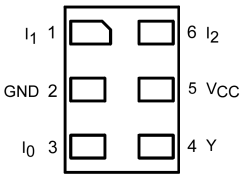
Pin One Orientation Diagram



AAA = Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignment for MicroPak



(Top Thru View)

Function Selection Table

2-Input Logic Function	Device Selection	Connection Configuration
2-Input AND	NC7SZ57	Figure 1
2-Input AND with inverted input	NC7SZ58	Figures 7, 8
2-Input AND with both inputs inverted	NC7SZ57	Figure 4
2-Input NAND	NC7SZ58	Figure 6
2-Input NAND with inverted input	NC7SZ57	Figures 2, 3
2-Input NAND with both inputs inverted	NC7SZ58	Figure 9
2-Input OR	NC7SZ58	Figure 9
2-Input OR with inverted input	NC7SZ57	Figures 2, 3
2-Input OR with both inputs inverted	NC7SZ58	Figure 6
2-Input NOR	NC7SZ57	Figure 4
2-Input NOR with inverted input	NC7SZ58	Figures 7, 8
2-Input NOR with both inputs inverted	NC7SZ57	Figure 1
2-Input XOR	NC7SZ58	Figure 10
2-Input XNOR	NC7SZ57	Figure 5

Logic Configurations NC7SZ57

Figure 1 through Figure 5 show the logical functions that can be implemented using the NC7SZ57. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

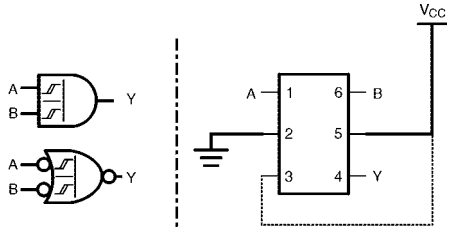


FIGURE 1. 2-Input AND Gate

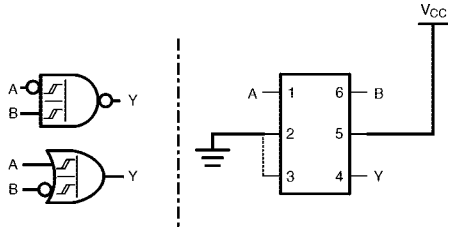


FIGURE 2. 2-Input NAND with Inverted A Input

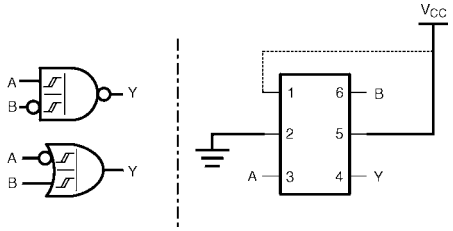


FIGURE 3. 2-Input NAND with Inverted B Input

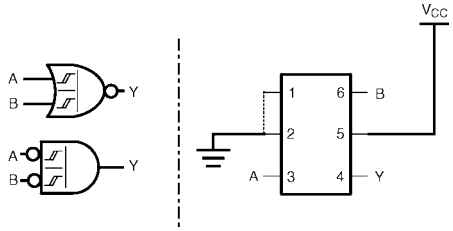


FIGURE 4. 2-Input NOR Gate

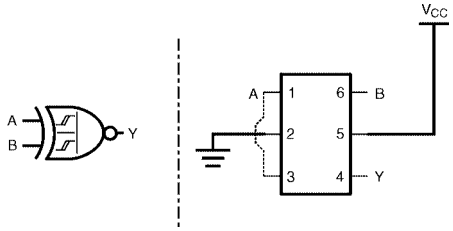


FIGURE 5. 2-Input XNOR Gate

Logic Configurations NC7SZ58

Figure 6 through Figure 10 show the logical functions that can be implemented using the NC7SZ58. The diagrams show the DeMorgan's equivalent logic duals for a given 2-input function. Next to the logical implementation is the board level physical implementation of how the pins of the function should be connected.

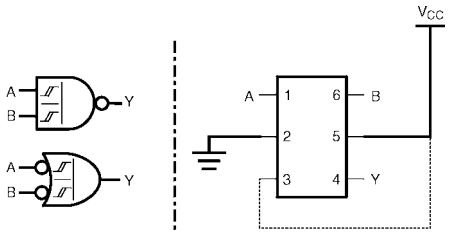


FIGURE 6. 2-Input NAND Gate

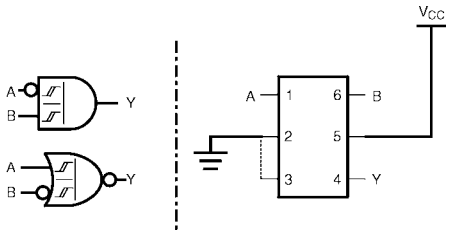


FIGURE 7. 2-Input AND with Inverted A Input

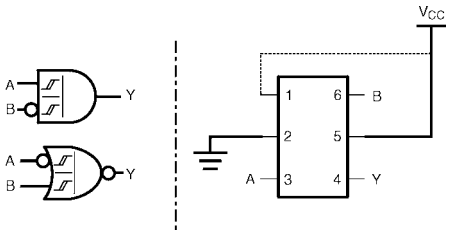


FIGURE 8. 2-Input AND with Inverted B Input

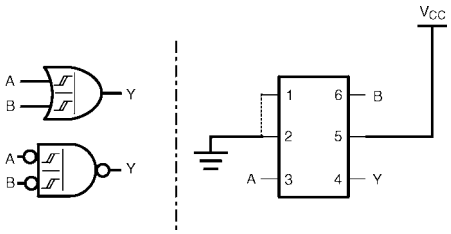


FIGURE 9. 2-Input OR Gate

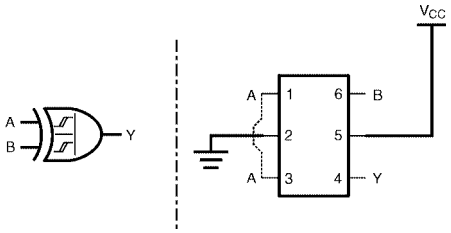


FIGURE 10. 2-Input XOR Gate

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@ $V_{IN} \le 0.5V$	−50 mA
DC Output Diode Current (I_{OK})	
@ $V_{IN} \le -0.5V$	−50 mA
DC Output Source/Sink Current (I_{OUT})	±50 mA
DC V_{CC} or Ground Current (I_{CC} / I_{GND})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature under Bias (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @+85°C	
SC70-6	180 mW

Recommended Operating Conditions

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Thermal Resistance (θ_{JA})	
SC70-6	350°C/W

Note 2: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
		(V)	Min	Typ	Max	Min	Max			
V_P	Positive Threshold Voltage	1.65	0.6	0.99	1.4	0.6	1.4			
		2.3	1.0	1.39	1.8	1.0	1.8			
		3.0	1.3	1.77	2.2	1.3	2.2	V		
		4.5	1.9	2.49	3.1	1.9	3.1			
		5.5	2.2	2.95	3.6	2.2	3.6			
V_N	Negative Threshold Voltage	1.65	0.2	0.50	0.9	0.2	0.9			
		2.3	0.4	0.75	1.15	0.4	1.15			
		3.0	0.6	0.99	1.5	0.6	1.5	V		
		4.5	1.0	1.43	2.0	1.0	2.0			
		5.5	1.2	1.70	2.3	1.2	2.3			
V_H	Hysteresis Voltage	1.65	0.15	0.48	0.9	0.15	0.9			
		2.3	0.25	0.64	1.1	0.25	1.1			
		3.0	0.4	0.78	1.2	0.4	1.2	V		
		4.5	0.6	1.06	1.5	0.6	1.5			
		5.5	0.7	1.25	1.7	0.7	1.7			
V_{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55				
		2.3	2.2	2.3		2.2		V	V_{IN} = V_{IH}	I_{OH} = −100 μA
		3.0	2.9	3.0		2.9			or V_{IL}	
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29				I_{OH} = −4 mA
		2.3	1.9	2.15		1.9			V_{IN} = V_{IH}	I_{OH} = −8 mA
		3.0	2.4	2.80		2.4		V	or V_{IL}	I_{OH} = −16 mA
		3.0	2.3	3.68		2.3				I_{OH} = −24 mA
		4.5	3.8	4.20		3.8				I_{OH} = −32 mA
V_{OL}	LOW Level Output Voltage	1.65		0.0	0.10		0.10			
		2.3		0.0	0.10		0.10		V_{IN} = V_{IH}	I_{OL} = 100 μA
		3.0		0.0	0.10		0.10	V	or V_{IL}	
		4.5		0.0	0.10		0.10			
		1.65		0.08	0.24		0.24			I_{OL} = 4 mA
		2.3		0.10	0.3		0.3		V_{IN} = V_{IH}	I_{OL} = 8 mA
		3.0		0.15	0.4		0.4	V	or V_{IL}	I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1	μA	V_{IN} = 5.5V, GND	

DC Electrical Characteristics (Continued)

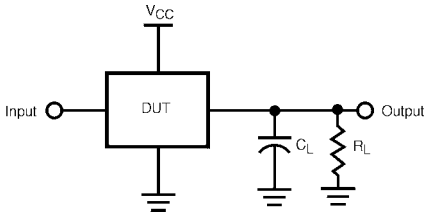
Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
I_{OFF}	Power Off Leakage Current	0.0			1		10	μA	V_{IN} or V_{OUT} = 5.5V
I_{CC}	Quiescent Supply Current	1.65–5.5			1		10	μA	V_{IN} = 5.5V, GND

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay I_n to Y	1.8 ± 0.15	3.0	8	14.0	3.0	14.5	ns	C_L = 15 pF R_L = 1 MΩ	Figures 11, 13
		2.5 ± 0.2	1.5	4.9	8.0	1.5	8.5			
		3.3 ± 0.3	1.2	3.7	5.3	1.2	5.7			
		5.0 ± 0.5	0.8	2.8	4.3	0.8	4.6			
t_{PLH} t_{PHL}	Propagation Delay I_n to Y	3.3 ± 0.3	1.5	4.2	6.0	1.5	6.5	ns	C_L = 50pF R_L = 500Ω	Figures 11, 13
		5.0 ± 0.5	1.0	3.4	4.9	1.0	5.3			
C_{IN}	Input Capacitance	0		2				pF		
C_{PD}	Power Dissipation Capacitance	3.3		14				pF	(Note 3)	Figure 12
		5.0		17						

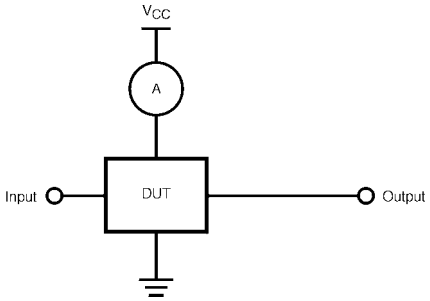
Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 12) C_{PD} is related to I_{CCD} dynamic operatic current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{in}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray Capacitance
Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 11. AC Test Circuit



Input = AC Waveforms
PRR = Variable; Duty Cycle = 50%

FIGURE 12. I_{CCD} Test Circuit

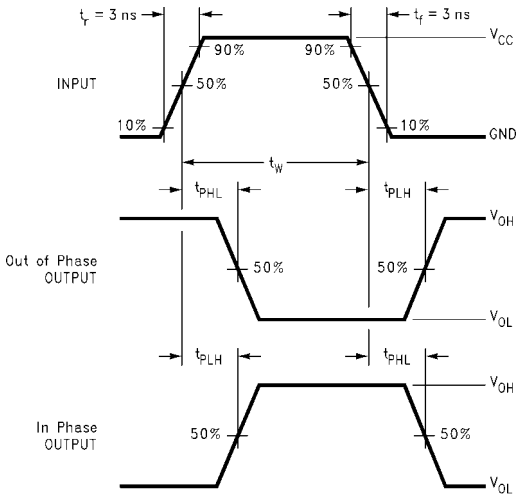


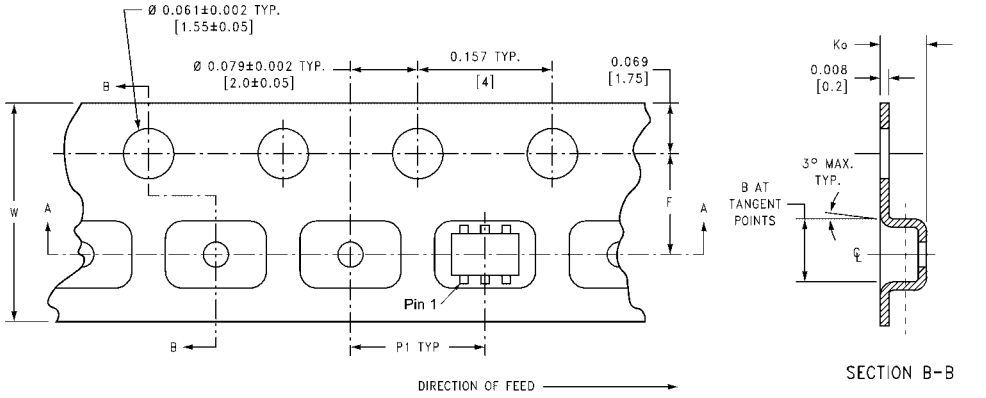
FIGURE 13. AC Waveforms

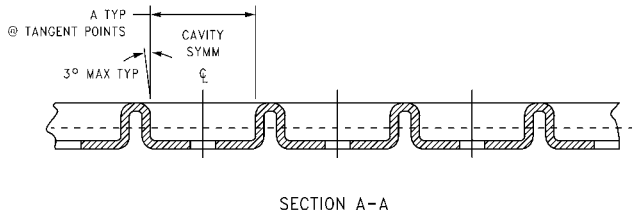
Tape and Reel Specification

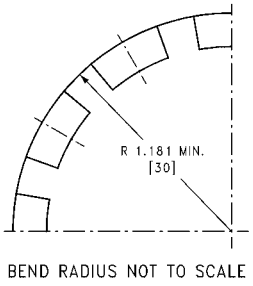
TAPE FORMAT for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)





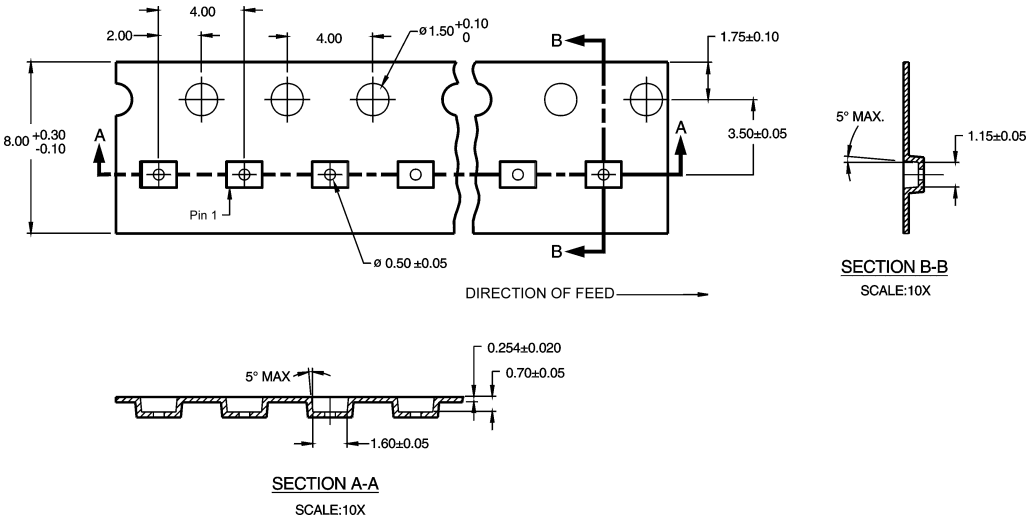


Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

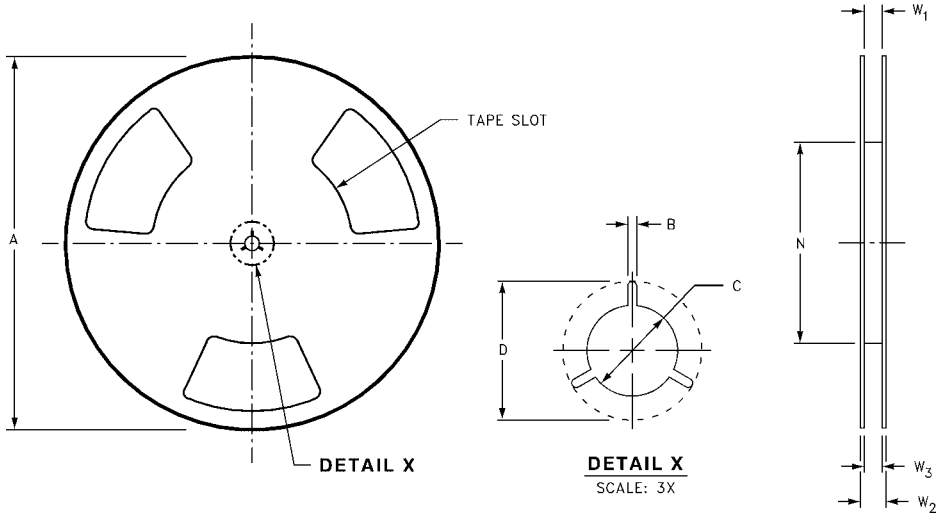
Tape and Reel Specification (Continued)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

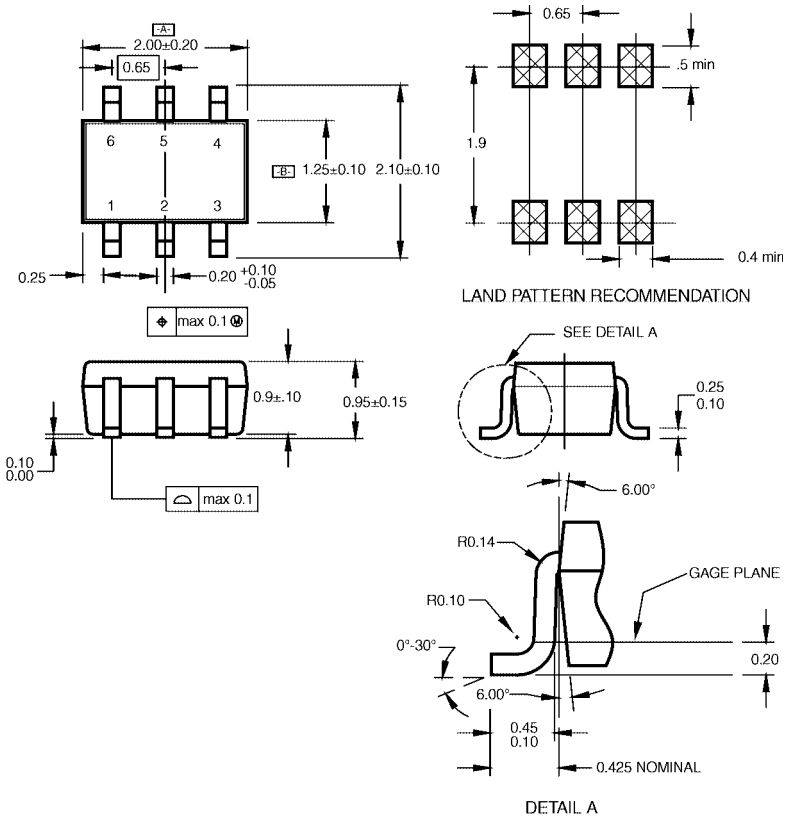


REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



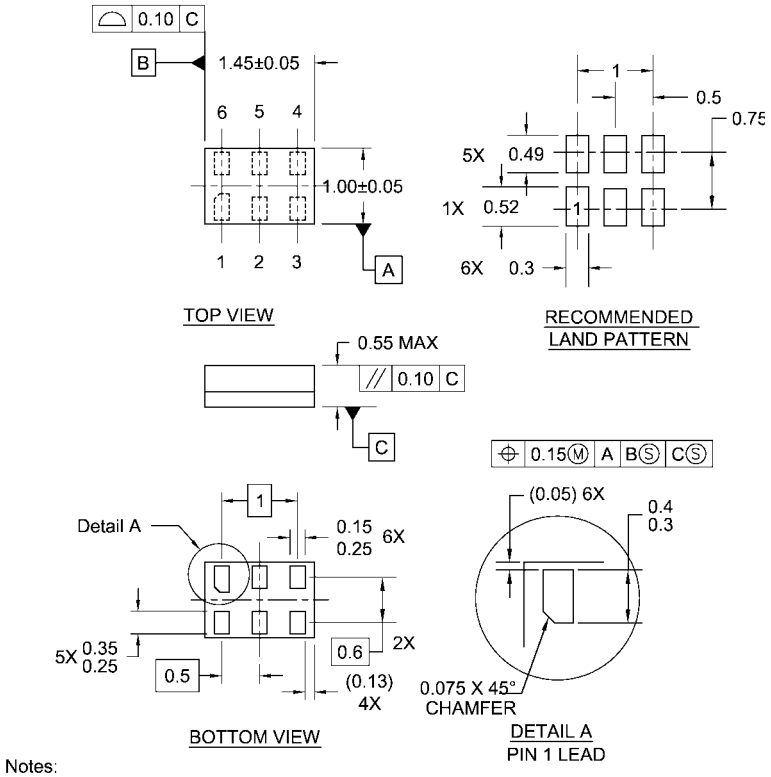
NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

Pb-Free 6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A