**Birzeit University**

**ENCS, Computer Systems Engineering department**

**ENCS3330, DIGITAL INTEGRATED CIRCUITS**

**H.W 3**

**Prepared by:**

**Jubran Khoury - 1201264**

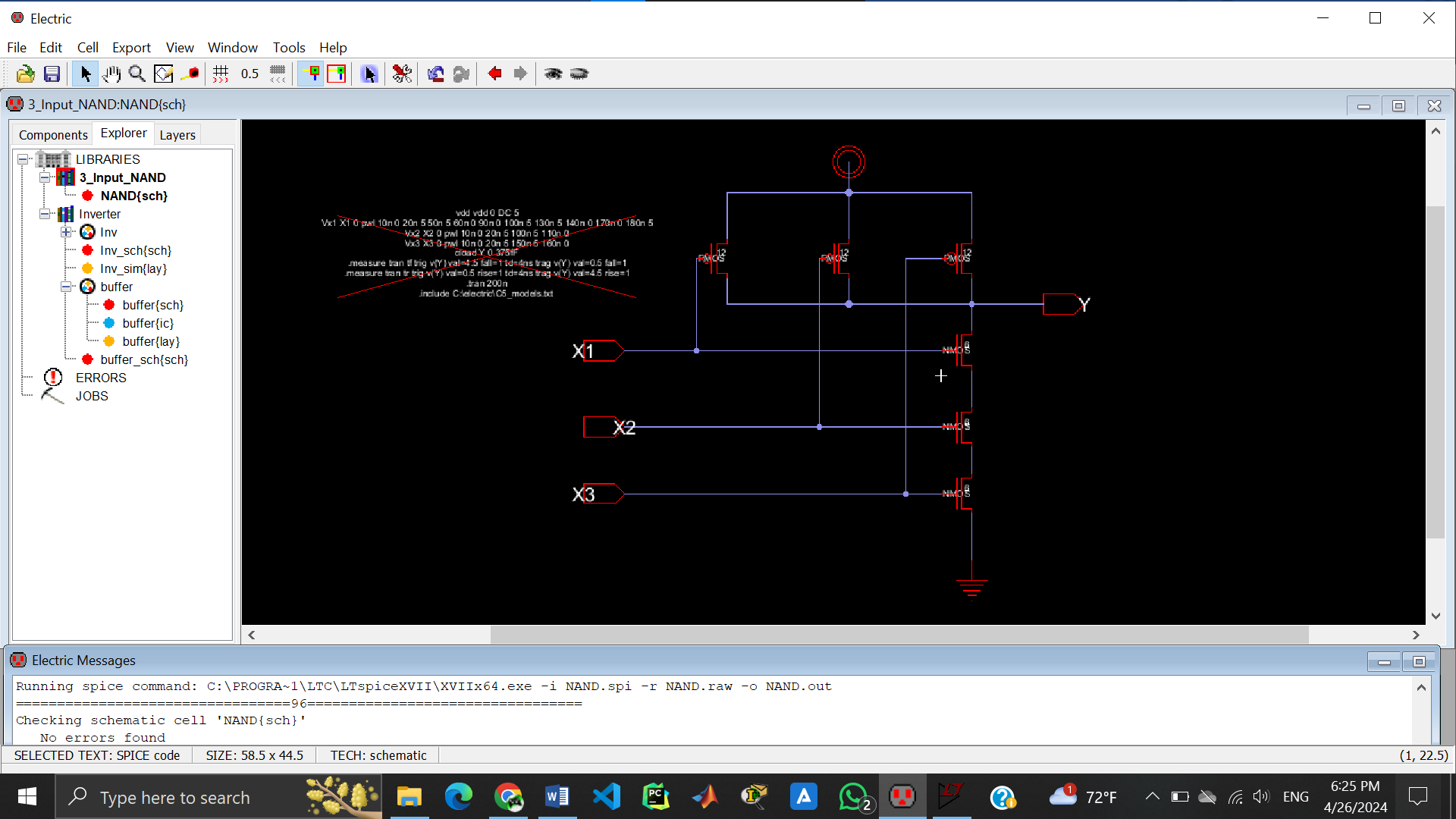
**Instructor: Dr.** **Khader Mohammad**

**Section: 2**

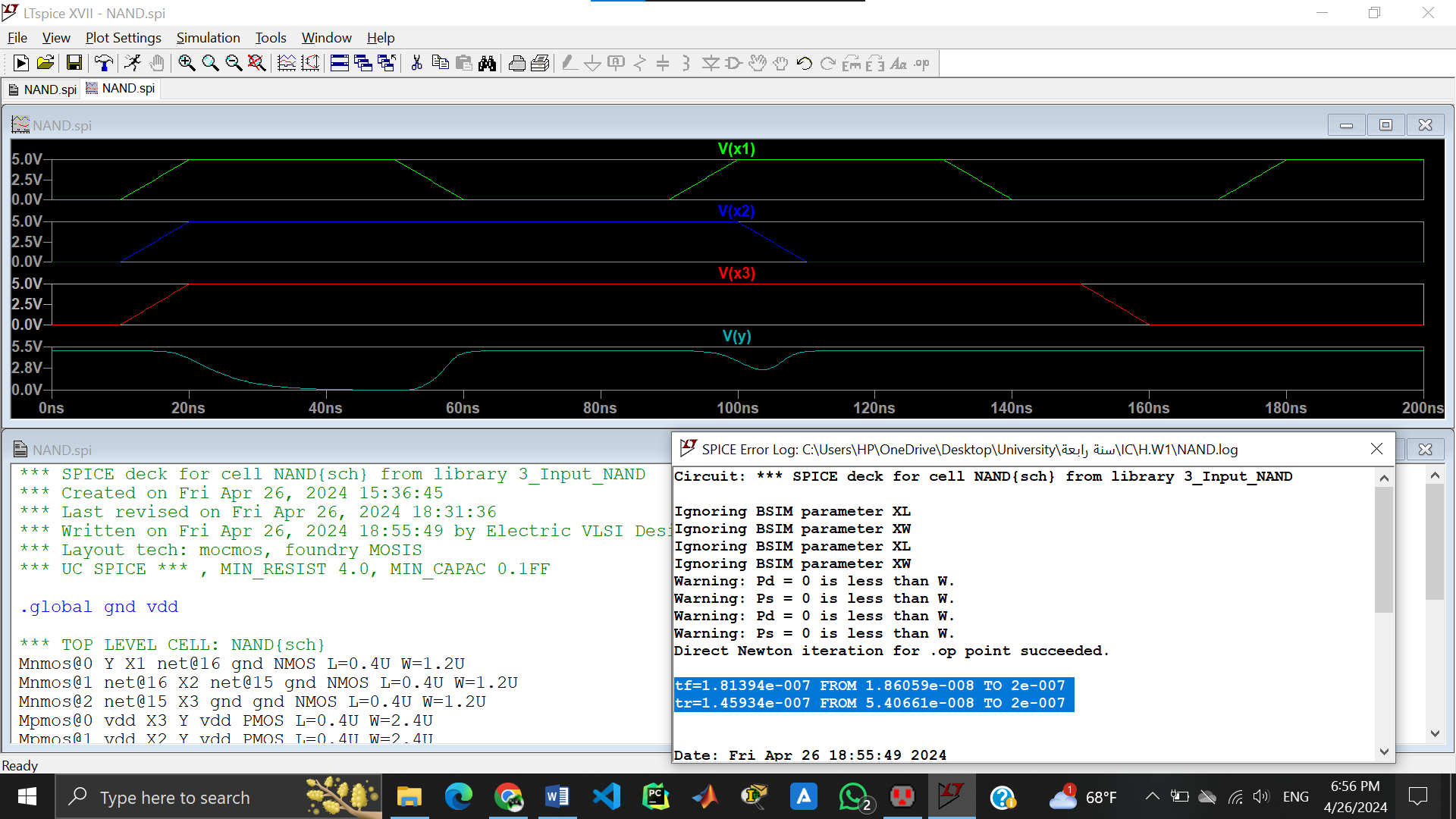
**Date of submission: 26 April 2024**

**1) 3-Input NAND gate**

**Schematic**

****

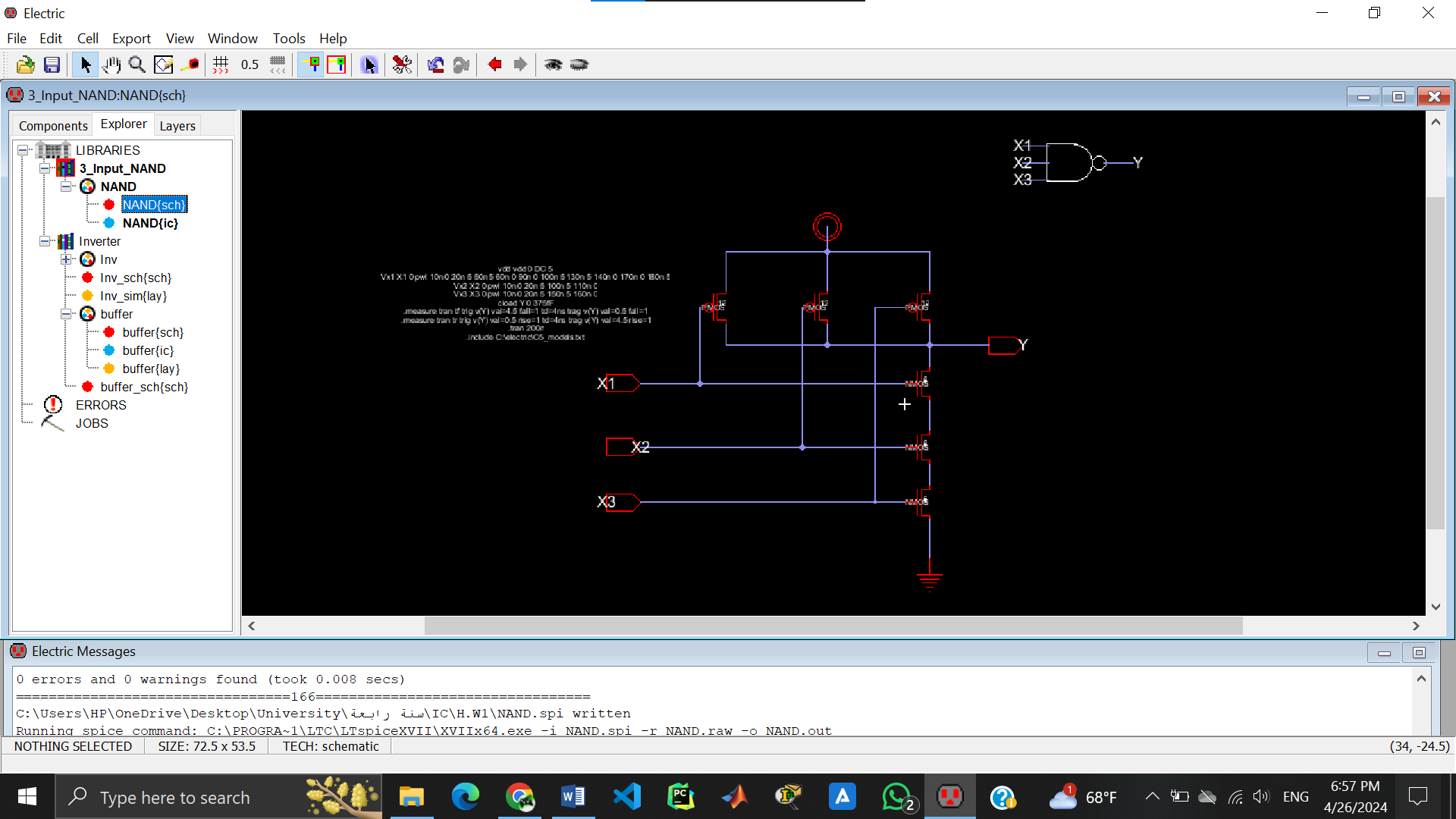
**Simulation**

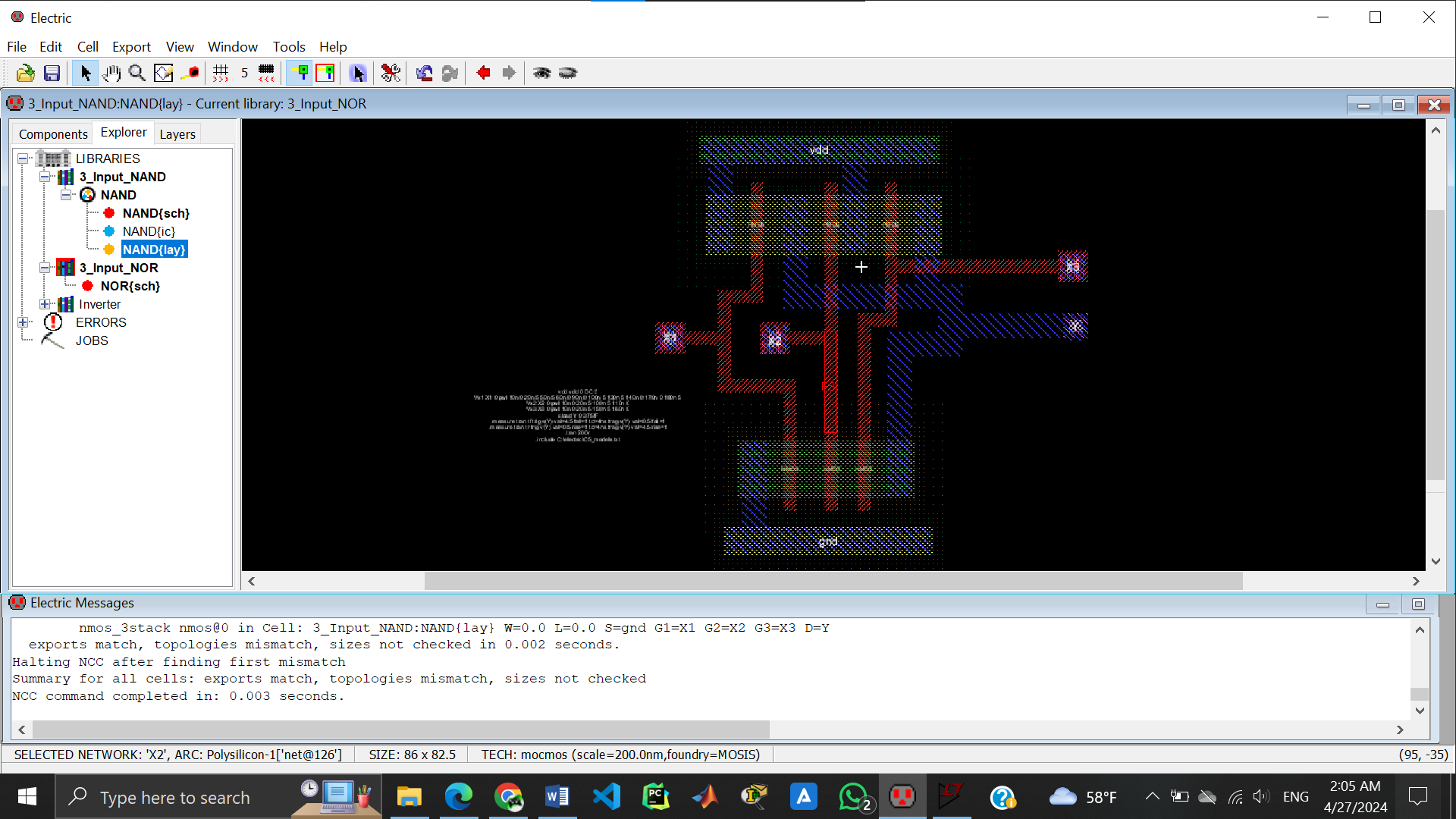
****

As shown above, the 3-input NAND gate works correctly.

Also, tf & tr is shown above.

**Symbol view**

****

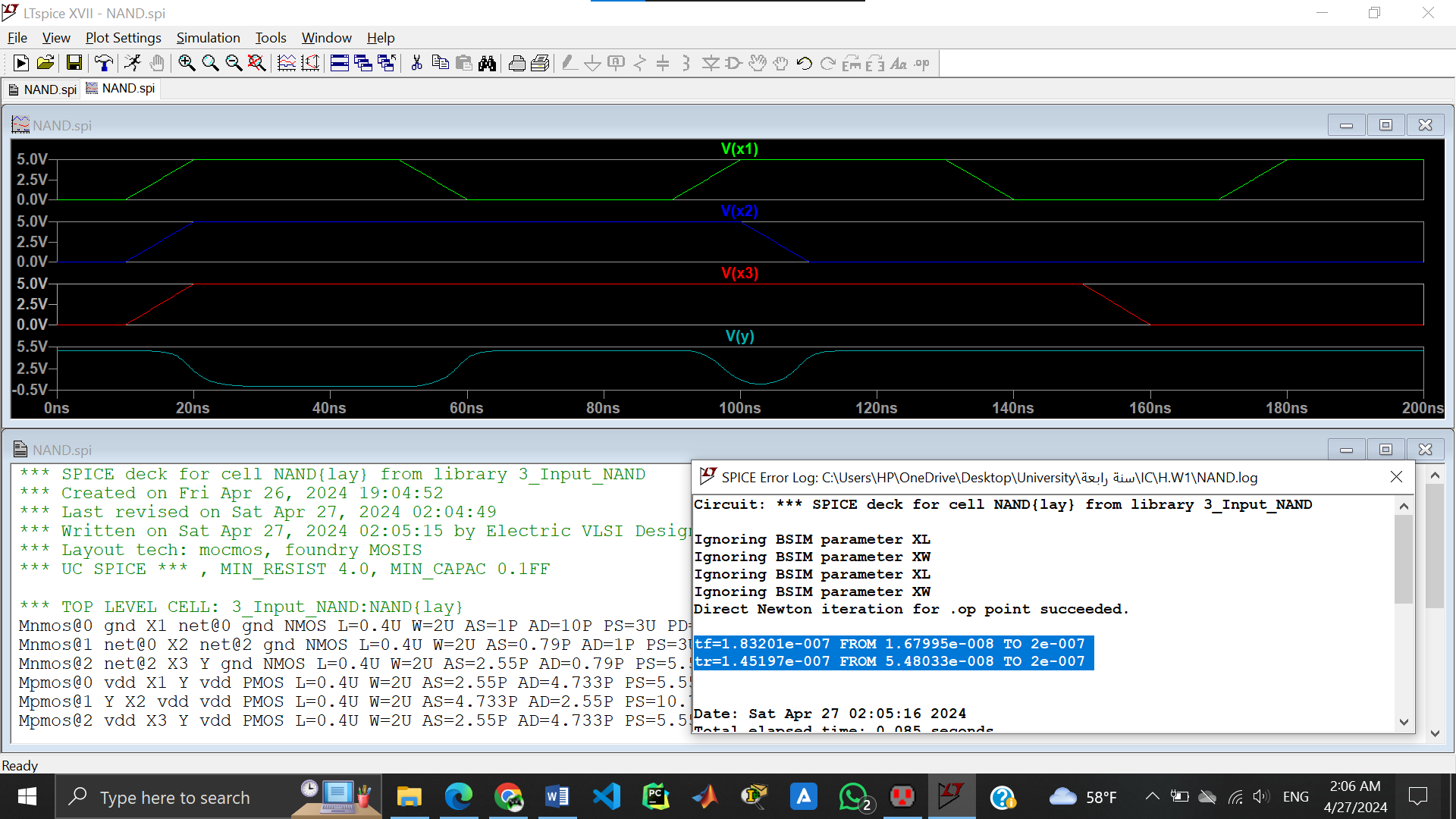
**Layout   
  
**

DRC (successfully completed, no errors).

NCC command completed (as shown above).

No Well errors found.

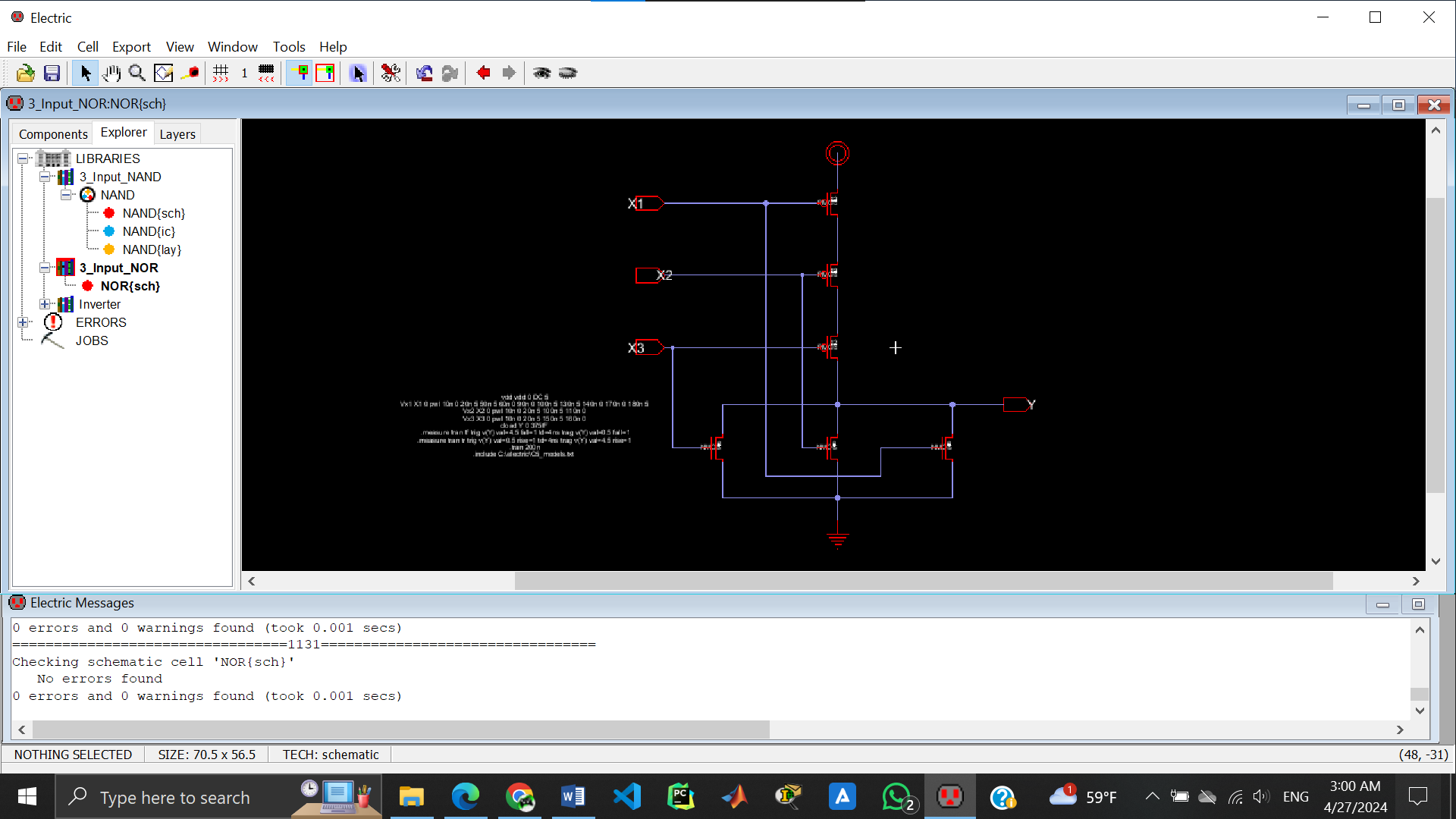
**Simulation**



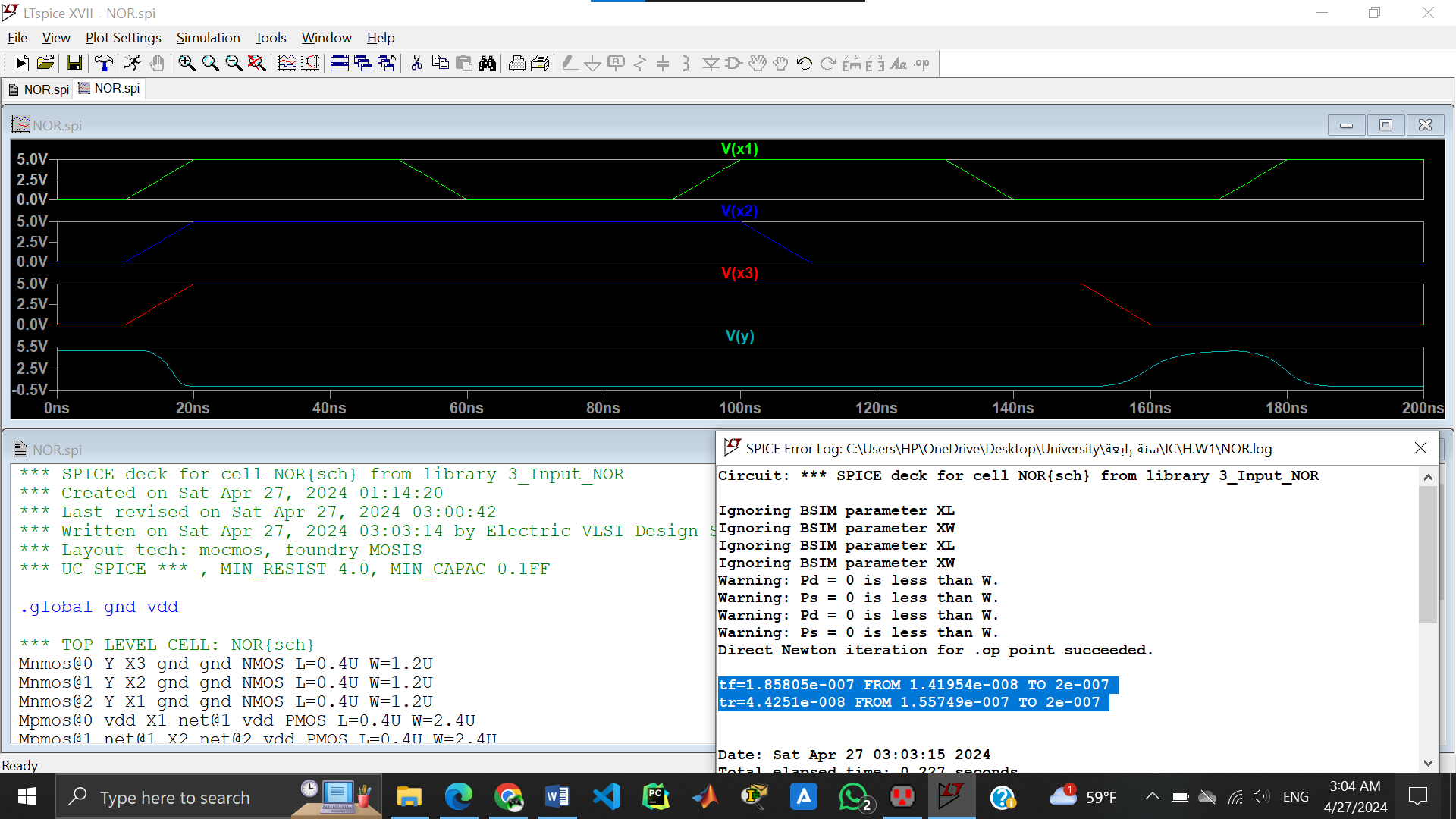
As shown above the simulation is correct and identical to schematic simulation.

**2) 3-Input NOR gate**

**Schematic**



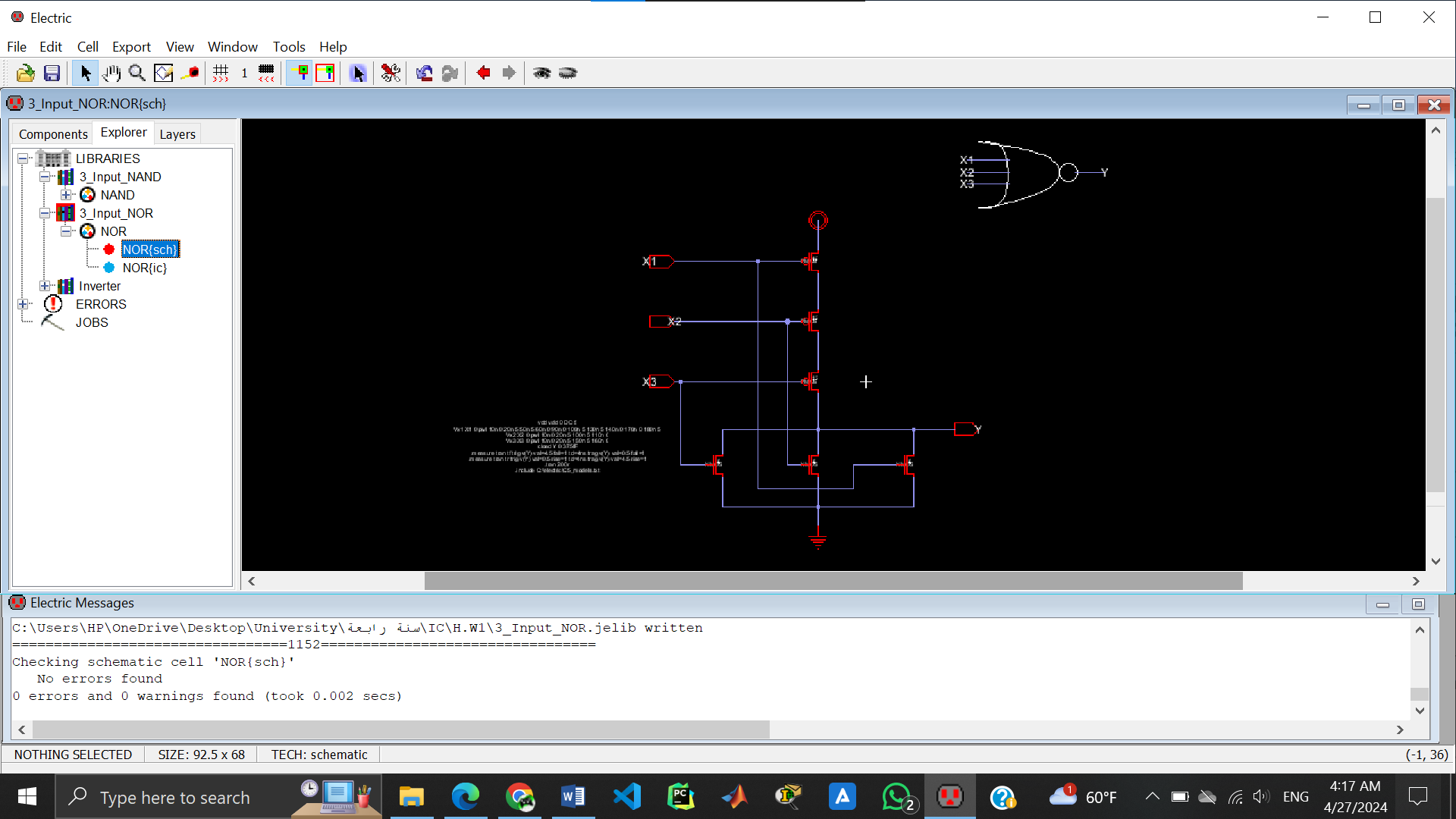
**Simulation**

****

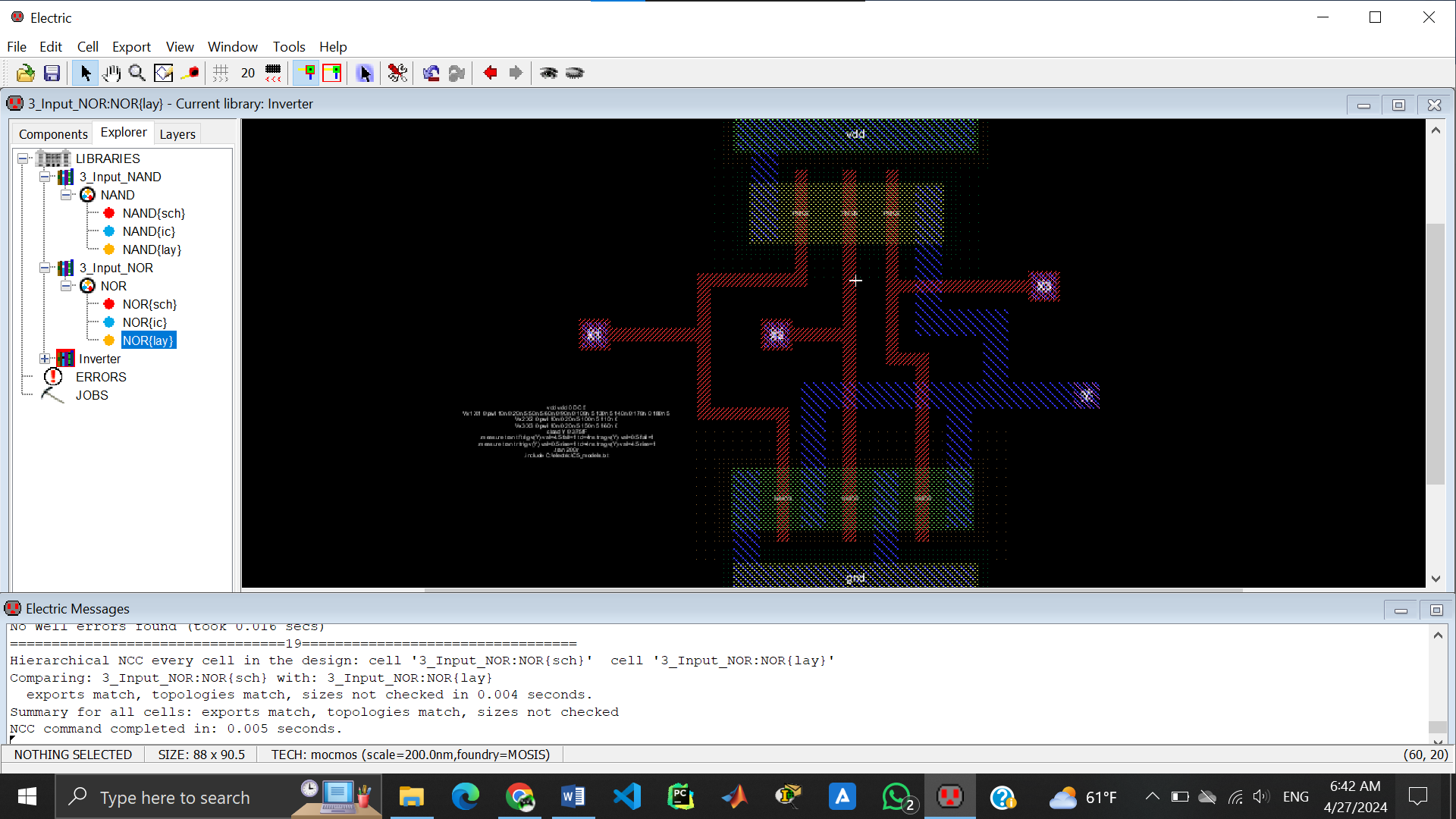
As shown above, the 3-input NOR gate works correctly.

Also, tf & tr is shown above.

**Symbol view**



**Layout**

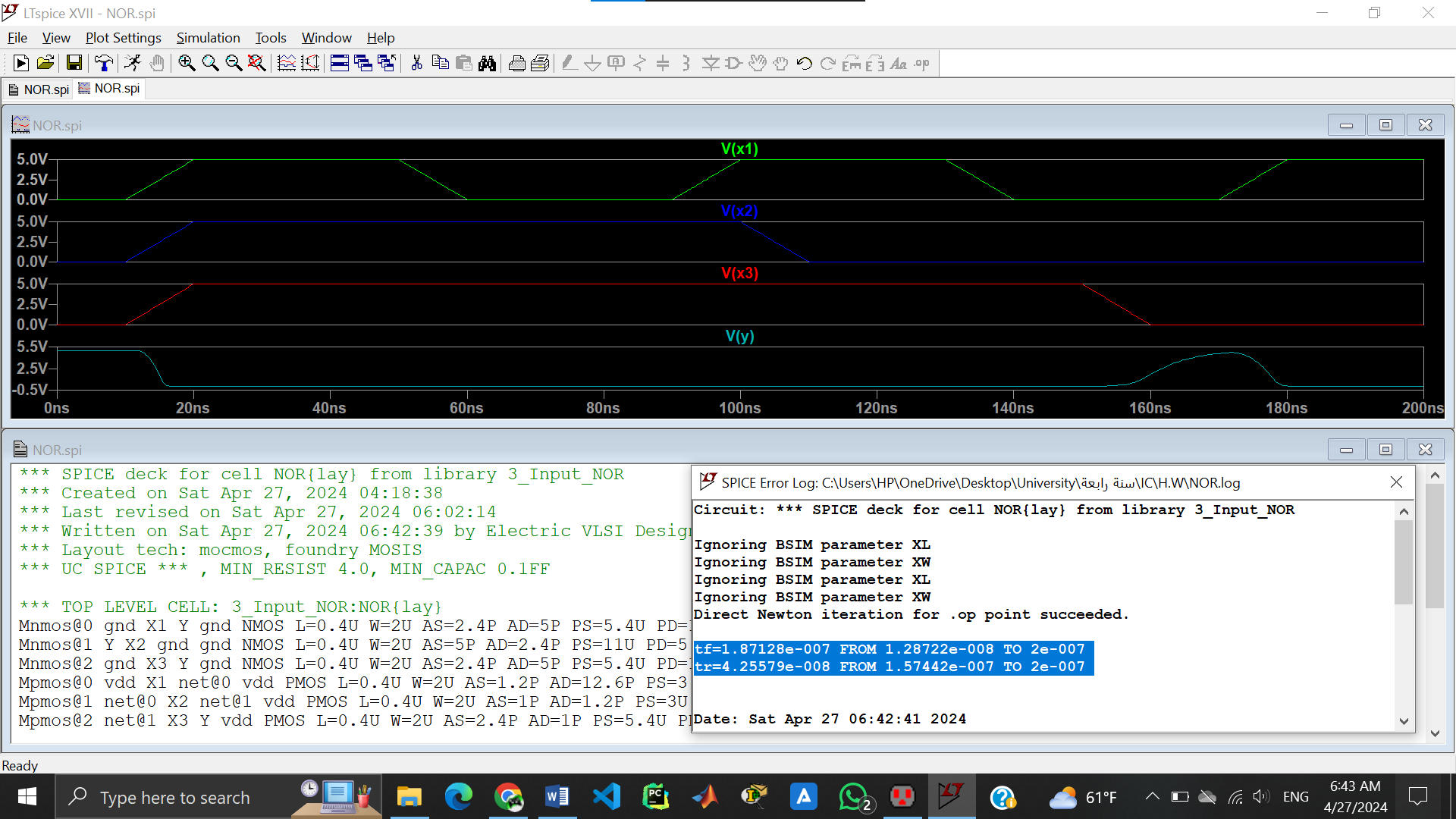


DRC (successfully completed, no errors).

NCC command completed (as shown above).

No Well errors found.

**Simulation**

****

As shown above the simulation is correct and identical to schematic simulation.