



FUNDAÇÃO EDSON QUEIROZ
UNIVERSIDADE DE FORTALEZA
ENSINANDO E APRENDENDO

T566 –SISTEMAS DIGITAIS AVANÇADOS

Aula 12- Ferramentas EDA/ Quartus II

Prof. Danilo Reis



Principais fabricantes (FPGA)

SRAM-based FPGAs

Xilinx Inc. – www.xilinx.com

Altera Corp. – www.altera.com

Atmel Corp. – www.atmel.com

Lattice Semiconductor Corp.

– www.latticesemi.com

Antifuse and flash-based FPGAs

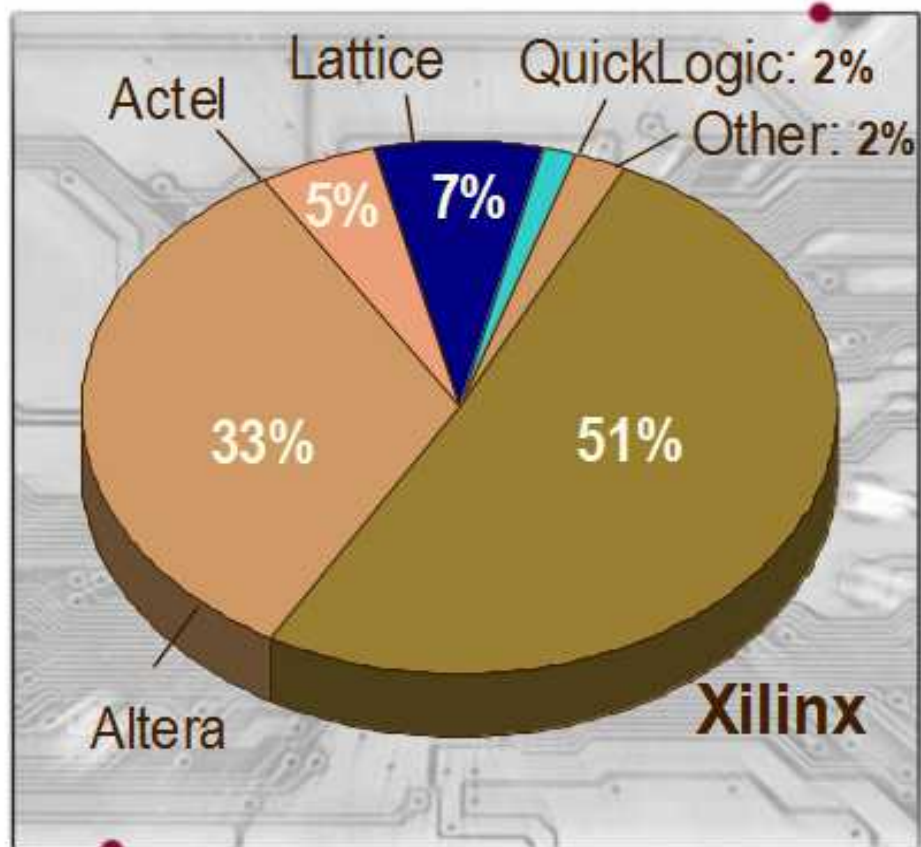
Actel Corp. – www.actel.com

QuickLogic Corp. – www.quicklogic.com

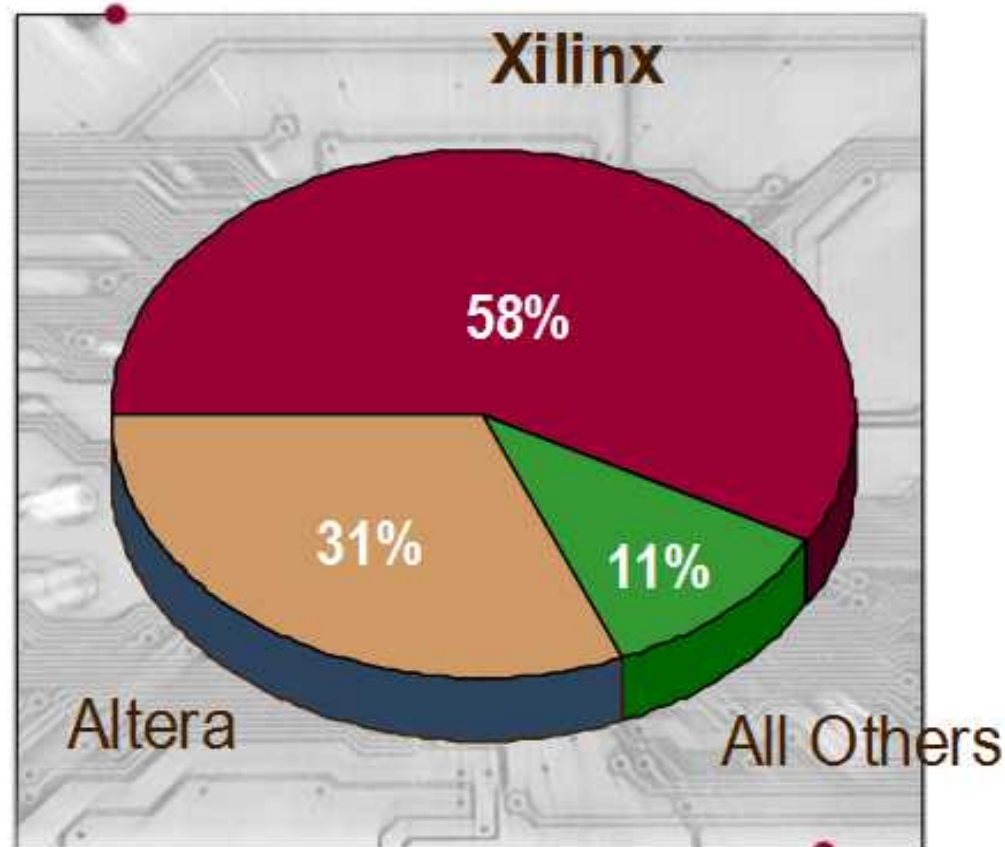


Calendar Year 2005

PLD Segment



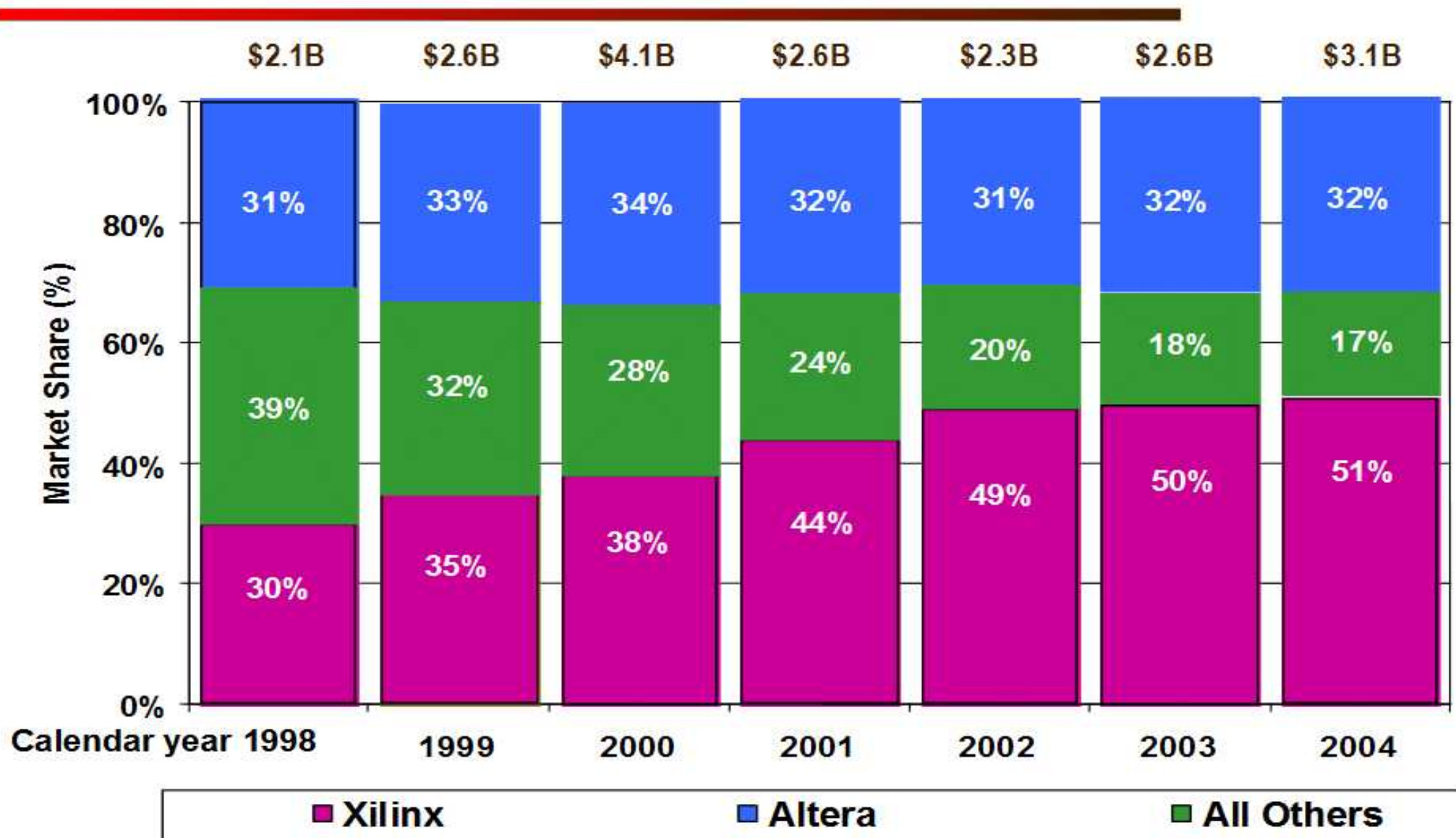
FPGA Sub-Segment



Two dominant suppliers, indicating a maturing market



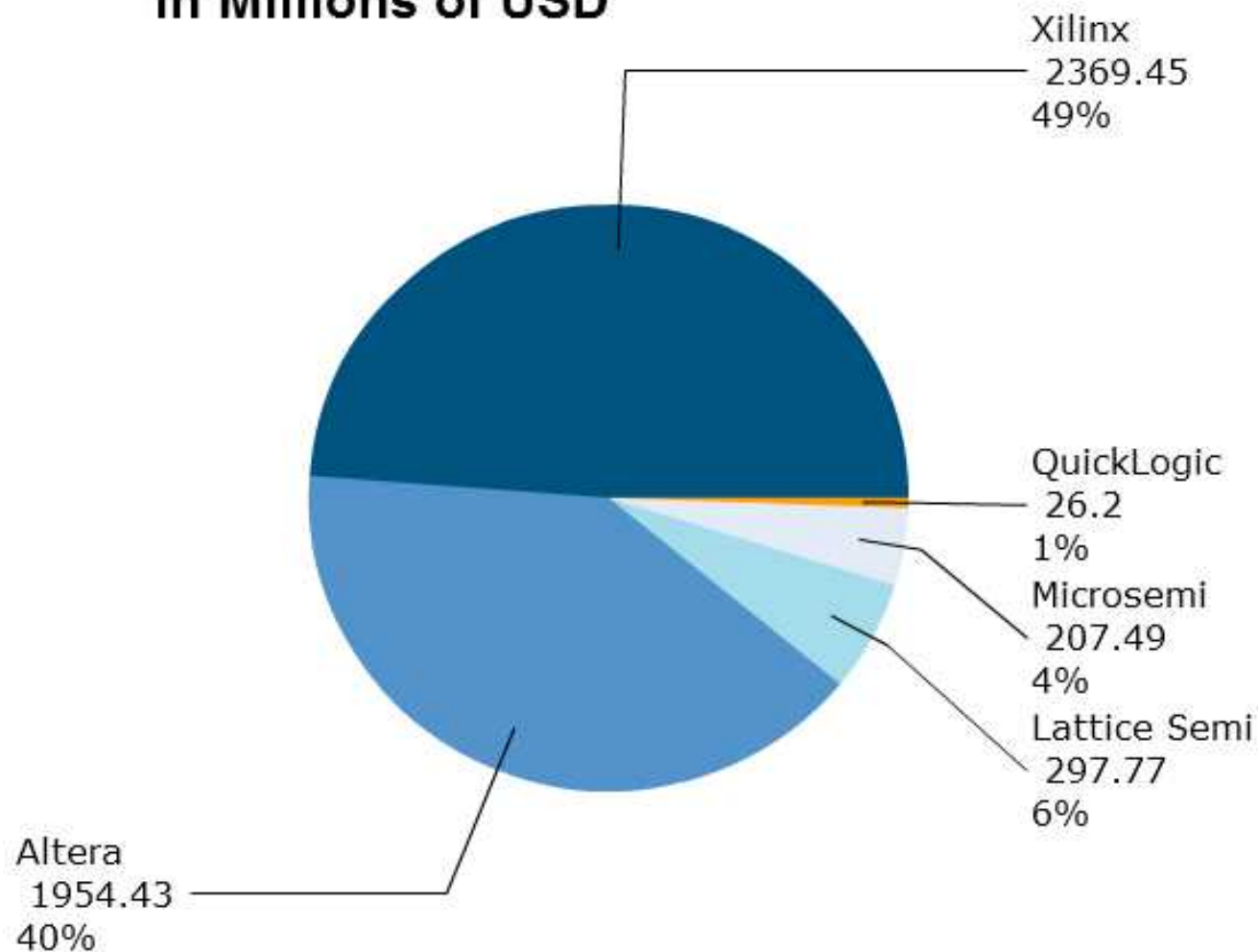
PLD Market Share





Market Share 2010

**FPGA Market Share by 2010 revenue
in Millions of USD**





Perfil Xilinx

É líder no mercado de FPGAs por muitos anos, Xilinx tem uma boa variedade de FPGAs em termos de custo e desempenho. Nos últimos anos, a série Spartan tornou-se bastante popular cobrindo o mercado de low-middle-end enquanto a série Virtex cobriu o high-end. Recentemente, Xilinx liberou a família "7" de FPGAs que são construídos em 28 nm processo e pela primeira vez, introduziu a Artex-7 e Kintex-série 7 que proporcionam uma melhor cobertura das aplicações mais low e mid-end, anteriormente cobertas pela série Spartan . O Kintex-7 recentemente ganhou o "Prêmio Altamente recomendável" Semiconductor do ano para 2011



Perfil Altera

Os FPGAs Altera cobrem os mercados low, middle e high end com as famílias da serie Cyclone, Arria e Stratix respectivamente. A oferta mais recente da Altera é o Cyclone-V, Arria-V e Stratix-V, todos construídos com 28-nm de tecnologia no processo.

Maior do que a Xilinx em valor de mercado, a Altera tem feito grandes progressos na conquista de quotas de mercado nos últimos anos. Muitas pessoas diriam que suas ferramentas de software são muito melhores que as da Xilinx, que provavelmente isto tenha sido um fator importante no seu sucesso.



Perfil Lattice

Lattice Semiconductor é focada no mercado de baixo consumo e baixo custo para FPGAs. Seus produtos são considerados tendo uma boa relação desempenho por custo, tidos como o "high value FPGAs" da indústria. Com a explosão em eletrônicos portáteis, esta tem sido uma boa estratégia para Lattice. A Lattice alega ter o FPGA com menor consumo de energia da indústria.



Perfil Microsemi

Microsemi é especializada em FPGAs de baixa potência e de mixed-signal. Segundo a Microsemi ela fabrica:

- O FPGA com menor consumo de potência: o IGLOO.
- Única FPGA da indústria o microcontrolador 32-bit ARMCortex-M3 hardcore: o SmartFusion.



Perfil QuickLogic

QuickLogic é focada nos dispositivos móveis com baixíssimo consumo de energia, embalagem de formato pequeno, e high security design. Ao invés de vender seus produtos com "FPGA", eles chamam de "semicondutores personalizável". Você não vai encontrar a palavra "FPGA" na primeira página do seu site.

"Nossa tecnologia de interconexão ViaLink ® patenteada permite QuickLogic ter FPGAs com menor consumo de energia, e mais roteáveis na indústria".



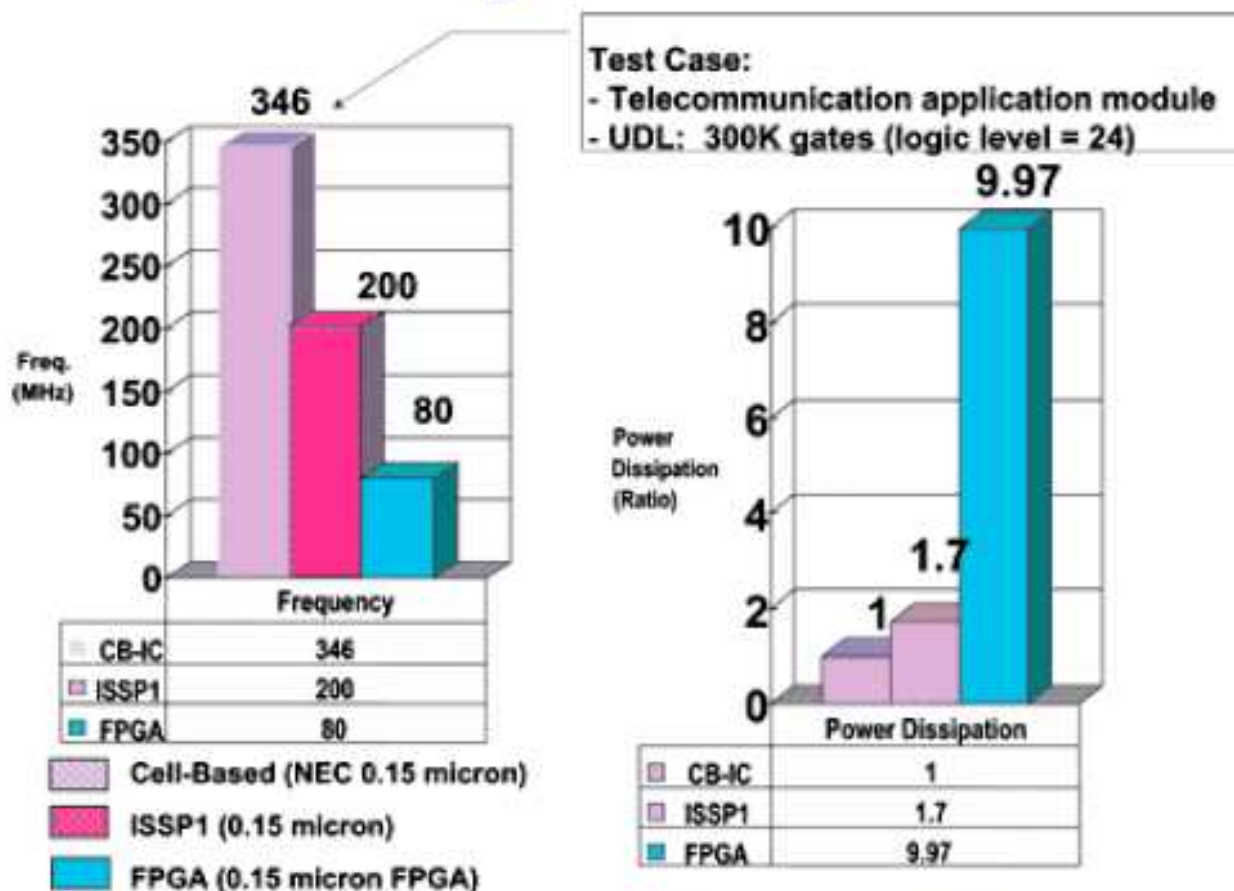
Ferramentas EDA

Electronics Design Automation é uma categoria de ferramentas de software para projetar sistemas eletrônicos, tais como placas de circuito impresso e circuitos integrados. As ferramentas trabalham juntas em um fluxo de projeto que permitem aos projetistas de chips ou placas de circuitos impressos, projetar, analisar, simular e depurar o projeto antes da confecção física do mesmo.



Ferramentas EDA

► FPGAs versus Soluções *Masked*



<http://www.chipdesignmag.com/display.php?articleId=115&issueId=11> (2005)

Transparência de F. Moraes (PUCRS)



Ferramentas EDA

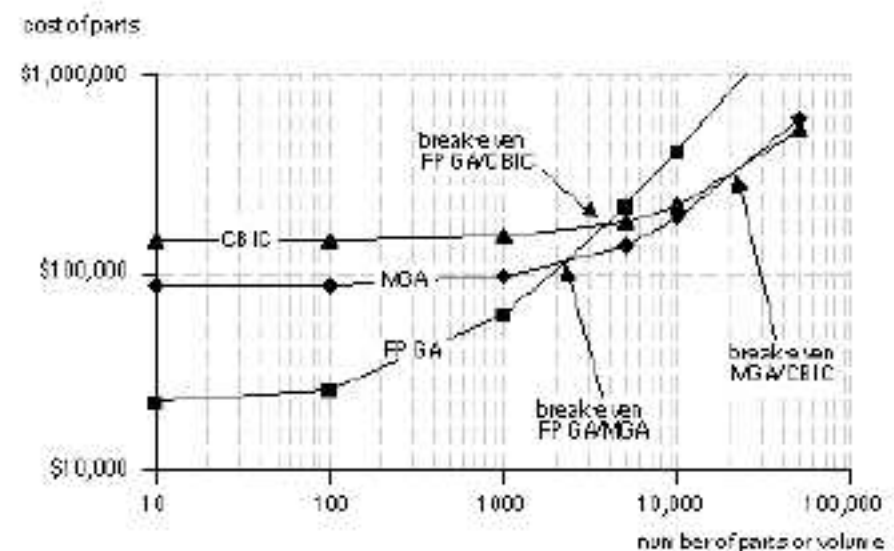
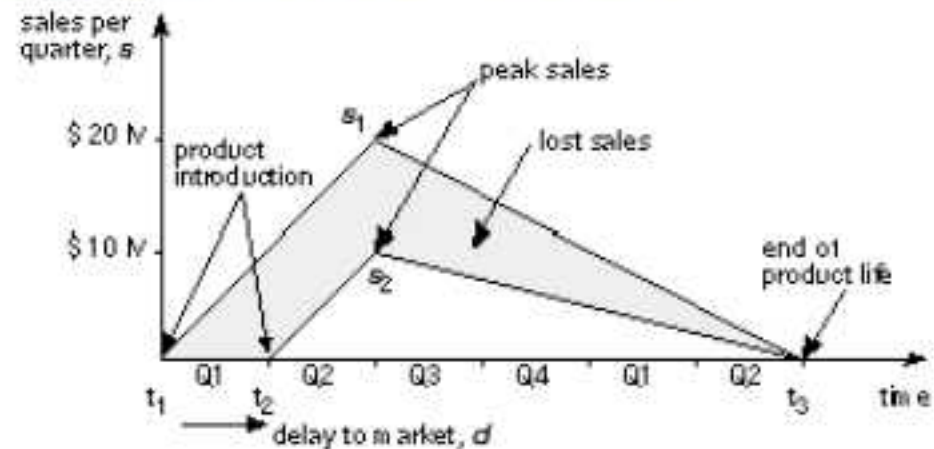
► FPGAs versus Soluções *Masked* (ASICs)

Desvantagens dos FPGAs

- Consomem mais energia
- São mais lentos (frequência de operação menor)

Vantagens dos FPGAs

- Menor *time-to-market*
- Muito flexíveis
- Permitem implementar SoCs complexos (>5 Mgates)
- Permitem implementar funções de telecomunicação para protocolos rápidos (> Gbps)
- Menor custo de engenharia (NRE)
- Menor custo que ASIC se volume <30.000 peças/ano (2006)





Ferramentas EDA

► **FPGAs: Fatores Limitantes**

- **Frequência de operação**
 - Altera: 500 MHz
 - É um problema? (Pode-se tentar contornar através do paralelismo...)
- **Consumo de energia (potência dissipada)**
 - Ainda impedem FPGAs em produtos eletrônicos que usam bateria
 - Altera: controle de consumo de potência através de múltiplas alimentações
- **Circuitos analógicos**
 - É um problema!
 - Xilinx introduziu conversão A/D e D/A nas Virtex5
- **Custo para alto volume**



Ferramentas EDA

▶ Ainda Assim FPGAs são Usados em Todas as Áreas

- **Telecomunicação**
 - um dos maiores mercados para FPGA
 - inclusive wireless
- **Automação e Controle**
- **Consumer**
 - HDTV
- **Automotivo**
 - Xilinx Automotive (XA) family
- **Espacial** (satélites e veículos de exploração)
 - radiation tolerant reconfigurable FPGAs
- **Supercomputação** (Cray)



Quartus II

- Fully-integrated development tool
 - Multiple design entry methods
 - Logic synthesis
 - Place & route
 - Simulation
 - Timing & power analysis
 - Device programming

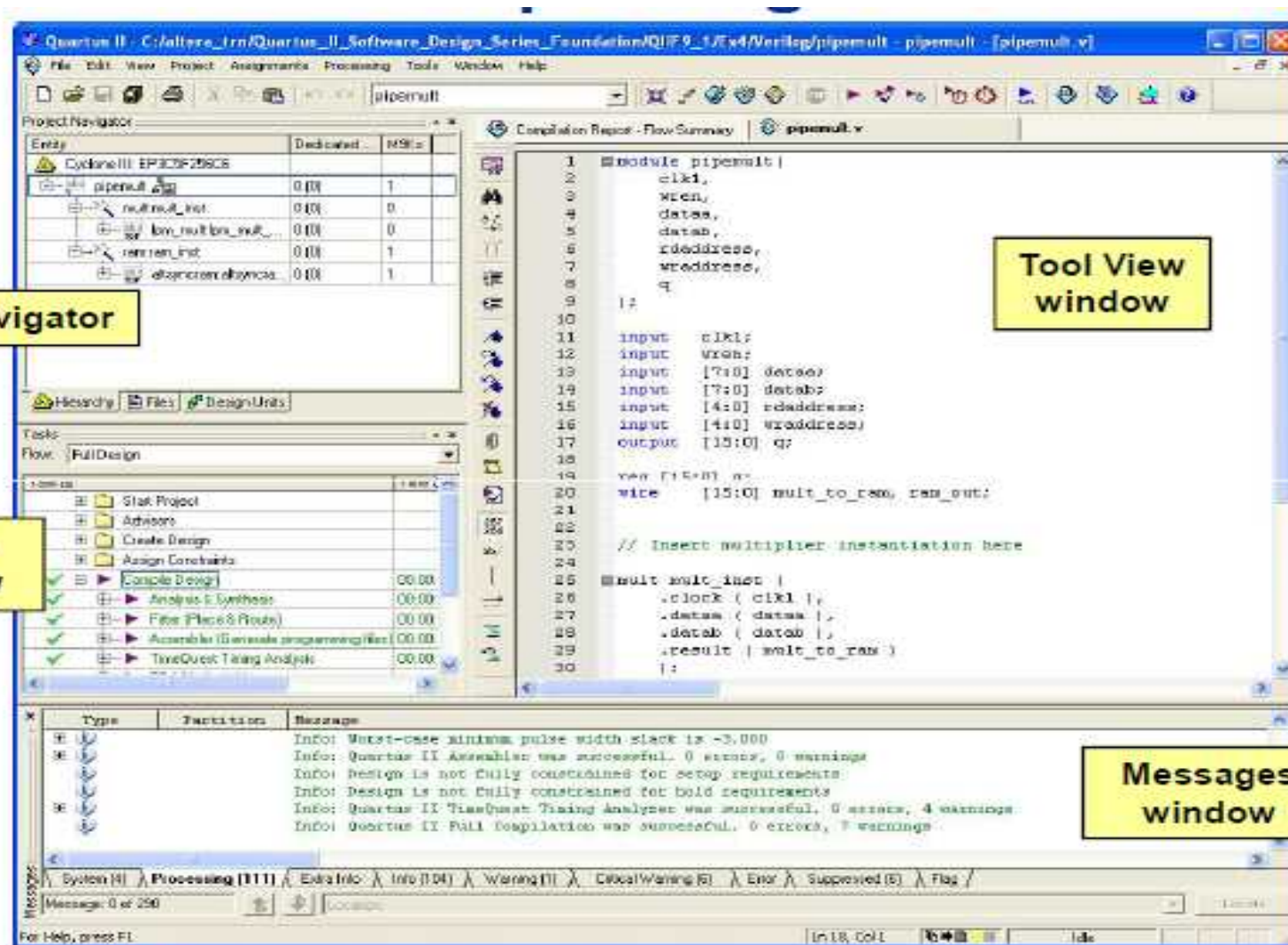


Quartus II

- MegaWizard® Plug-In Manager & SOPC Builder design tools
- TimeQuest Timing Analyzer
- Incremental compilation feature
- PowerPlay Power Analyzer
- NativeLink® 3rd-party EDA tool integration
- Debugging capabilities
 - From HDL to device in-system
- 32 & 64-bit Windows & Linux support
- Multi-processor support
- Node-locked & network licensing options



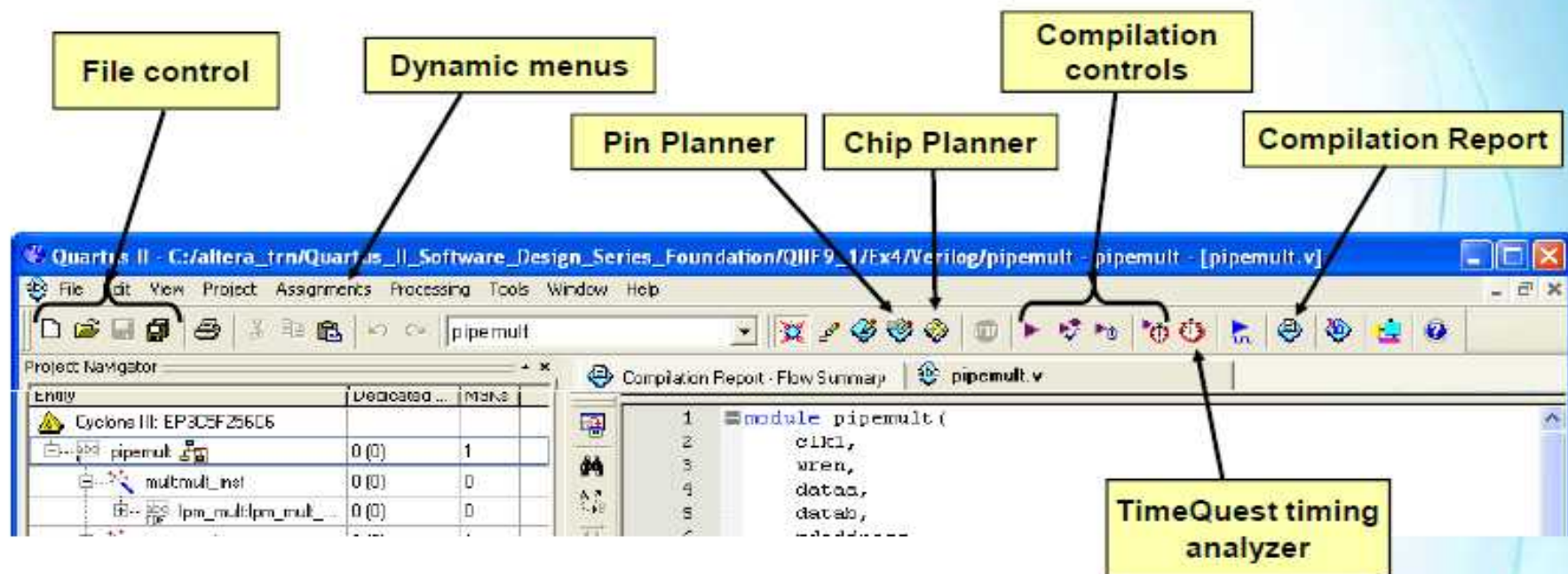
Quartus II IDE





Quartus II - Barra de ferramentas

Main Toolbar



To reset views:

1. Tools ⇒ Customize ⇒ Toolbars ⇒ Reset All
2. Restart Quartus II



Quartus II - Barra de ferramentas

Tips & Tricks Advisor

Help menu ⇒ Tips & Tricks

Get an Early Timing Estimate

Recommendation	You can get an early timing estimate without running a full compilation.
Description	You can use the Start Early Timing Estimate command on the Processing menu to get a full timing report based on estimated delays for the design. This command can run the Fitter up to ten times faster than a full fit and produces estimated delays within 20% of what a full compilation can achieve.
Action	Use the Start Early Timing Estimate command on the Processing menu to run an early timing estimate. You can specify settings for the early timing estimate in the Settings dialog box when a project is open. Open Settings dialog box - Early Timing Estimate page

Provides useful instructions on using the Quartus II software & links to settings.

Available sections include:

- New features in current release
- Helpful features and project settings available to designers

For Help, press F1



Quartus II - Barra de ferramentas

Built-In Help System

Quartus II Help Version 9.1 - Mozilla Firefox

File Edit View History Bookmarks Tools Help

Quartus II Help Version 9.1

Contents Index Search Forums

Shortcut to Altera forums

Welcome > Quartus II Introduction

ADTERA

Show All

Quickly expand all topics

Web browser-based allows for easy search in page

Quartus II Introduction

What's New in Quartus II

Getting Started with Quartus II

Managing Projects

Using Project Revisions

Archiving Projects

Project Database File Export and Import

Using Advisers for Design Options

Viewing Reports and Messages

Creating Designs

Using HDL with the Quartus II Software

Using Altera Megafunctions

Creating System-Level Designs

Assigning Constraints

Compiling Designs

Simulating Designs

Running Timing Analysis

Achieving Timing Closure

Power Estimation and Analysis

Signal Integrity Analysis

Designing with LogicLock Regions

Optimizing Designs with Design Assistant

Engineering Change Management

Using the Netlist Viewer

Using the State Machine Editor

Using the Design Assistant

Programming & Configuring Devices

Debugging & Optimization

Integrating Other EDA Tools

Devices and Adapters

Logic Options

API Functions for Tcl

Quartus II Scripting Support

Shortcuts

Welcome to the Quartus II Software

The Quartus II development software provides a complete design environment for system-on-a-programmable-chip (SoPC) design. Regardless of whether you use a personal computer or a Linux workstation, the Quartus II software ensures easy design entry, fast processing, and straightforward device programming. The following sections describe the general capabilities and design flows of the Quartus II software.

Quartus II Highlights:

Design Capabilities:

NativeLink Integration with other EDA Tools:

Click any of the following flow icons for more information about that part of the design flow.

Design Entry

Synthesis

Place & Route

Simulation

Timing Analysis

Power Analysis

Debugging

Engineering Change Management



Quartus II - Barra de ferramentas

Interactive Tutorial

Help menu ⇒ **Getting Started Tutorial**
or from the **Getting Started** window

The screenshot displays the Quartus II Interactive Tutorial within a Mozilla Firefox browser window. The browser's address bar shows the URL for the tutorial. The tutorial's left sidebar lists various modules, with 'Module 1: Quartus II Overview' and 'Getting Started' highlighted. The main content area of the browser shows the 'QUARTUS II TUTORIAL' title and instructions to create a new project by opening the New Project wizard. A yellow callout box points to the 'Help menu' and 'Getting Started Tutorial' options. The Quartus II software window is also visible, showing the 'File' menu with 'New Project Wizard' selected. A green callout box points to this option. The Quartus II window also shows the 'QUARTUS II' title and 'Version' information. At the bottom of the Quartus II window, there is a 'Show Me' button, a 'Guide Me' button, and a 'Test Me' button, all highlighted with a red box.



Quartus II - Barra de ferramentas

New Project Wizard

The image shows the 'New Project Wizard: Directory, Name, Top-Level Entity' dialog box in Quartus II. The dialog has three main input fields: 'What is the working directory for this project?' (with a browse button), 'What is the name of this project?' (with a browse button), and 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' (with a browse button). Below these fields is a checkbox labeled 'Use Existing Project Settings ...'. At the bottom are buttons for '< Back', 'Next >', 'Finish', and 'Cancel'. Annotations include: 'File menu' pointing to the 'New Project Wizard...' option in the Quartus II File menu; 'Tasks' pointing to the 'Open New Project Wizard' task in the Task pane; 'Select working directory' pointing to the first input field; 'Name of project can be any name; recommend using top-level file name' pointing to the second input field; 'Top-level entity does not need to be the same name as top-level file name' pointing to the third input field; 'Create a new project based on an existing project & settings' pointing to the 'Use Existing Project Settings ...' checkbox; and a terminal window at the bottom left showing the command 'Tcl: project_new <project_name>'.

File menu

Tasks

Select working directory

Name of project can be any name; recommend using top-level file name

Top-level entity does not need to be the same name as top-level file name

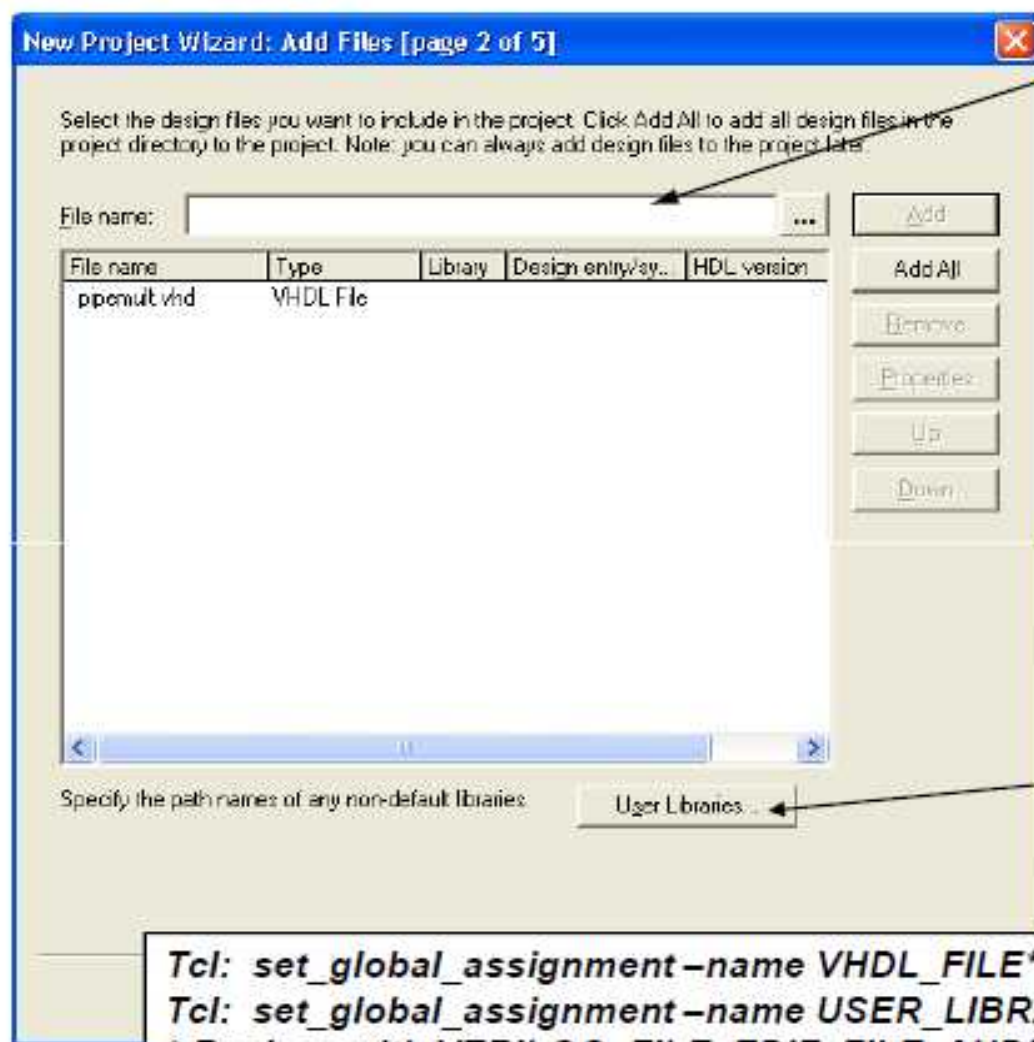
Create a new project based on an existing project & settings

Tcl: project_new <project_name>



Quartus II - Barra de ferramentas

Add Files



Add design files

- Graphic (.BDF)
- VHDL
- Verilog or SystemVerilog
- EDIF
- VQM

Notes:

- Files in project directory do not need to be added
- Add top-level file if filename & entity name are not the same
- Absolute & relative paths are supported

Add user library pathnames

- User libraries (any directory containing files)
- MegaCore®/AMPPSM libraries
- Pre-compiled VHDL packages

```
Tcl: set_global_assignment -name VHDL_FILE* <filename.vhd>
Tcl: set_global_assignment -name USER_LIBRARIES <library_path_name>
* Replace with VERILOG_FILE, EDIF_FILE, AHDL_FILE or BDF_FILE
```




Quartus II - Barra de ferramentas

Device Selection

New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family:
Family: Cyclone III
Devices: All

Target device:
☒ Auto device selected by the Fitter
☐ Specific device selected in Available devices list

Show in 'Available devices' list:
Package: FBGA
Pin count: 256
Speed grade: Fastest
☒ Show advanced devices
☐ HardCopy compatible only

Available devices:

Name	Core v...	LEs	User I/	Memory	Embed	PLL
EP3C3F25606	1.2V	5136	183	423936	46	2
EP3C10F25606	1.2V	10320	183	423936	46	2
EP3C10F25606	1.2V	10408	183	516096	112	4
EP3C25F25606	1.2V	24624	157	608256	132	4

Comparison device:
New device:
☒ Unit DSP & RAM to HardCopy/device resources

< Back Next > Finish Cancel

Choose device family and filter results

Advanced information on future devices

Choose specific part number from list or let Fitter choose smallest, fastest device based on filter criteria

```
Tcl: set_global_assignment -name FAMILY "device family name"  
Tcl: set_global_assignment -name DEVICE <part_number>
```



Quartus II - Barra de ferramentas

EDA Tool Settings

**Choose EDA tools
& file formats**

**Add or change
settings later**

New Project Wizard: EDA Tool Settings [page 4 of 5]

Specify the other EDA tools -- in addition to the Quartus II software -- used with the project.

Design Entry/Synthesis

Tool name: Synplify Pro

Format: VQM

☐ Run this tool automatically to synthesize the current design

Simulation

Tool name: ModelSim-Atera

Format: Verilog HDL

☒ Run gate: VHDL, Verilog HDL

Timing Analysis

Tool name: PrimeTime

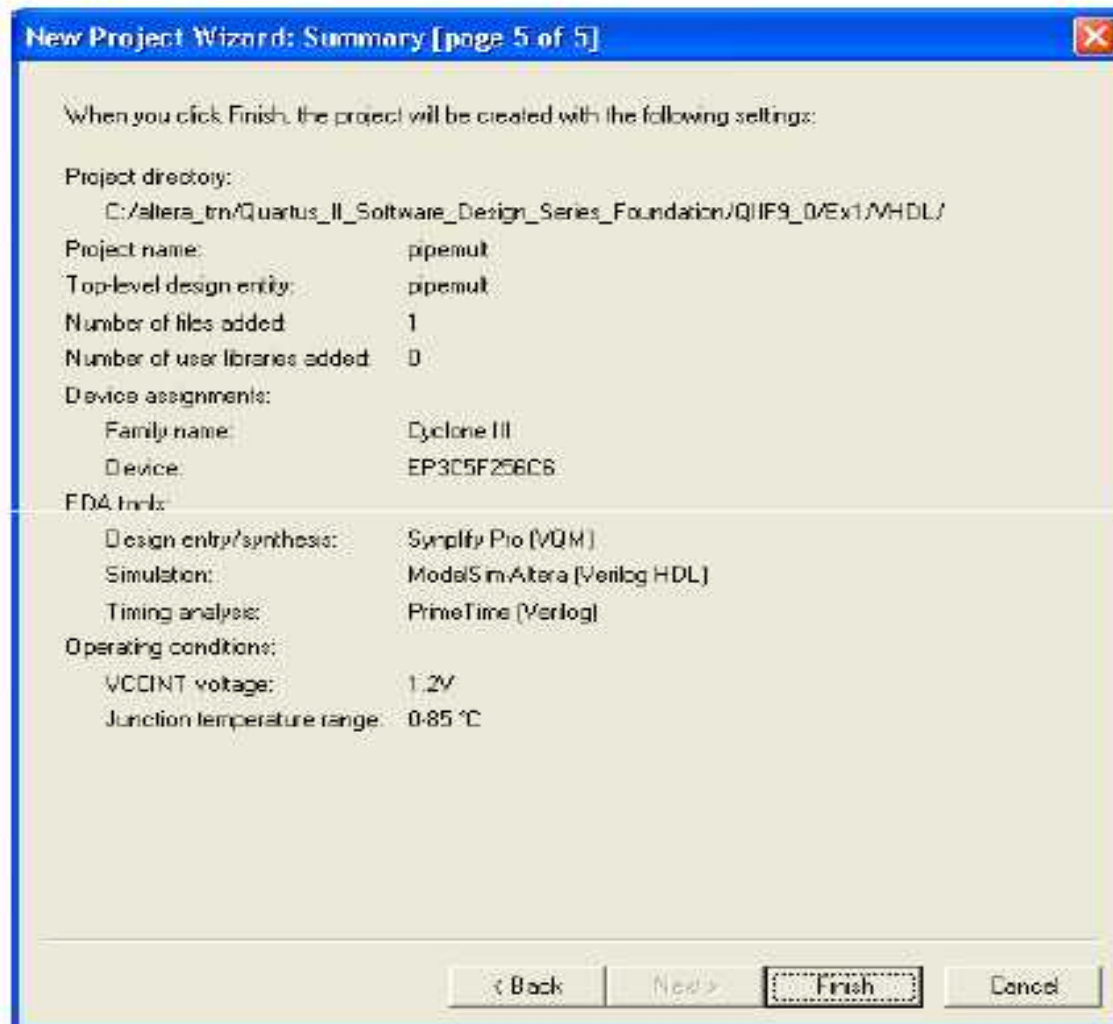
Format: Verilog HDL

☐ Run this tool automatically after compilation

< Back Next > Finish Cancel



Quartus II - Barra de ferramentas **Done!**



**Review results &
click Finish**



Referências

- Curso oficial da Altera "Quartus II Design Foundations"
- Aula do curso "ECE 448 - FPGA and ASIC" Design with HDL" George Manson University;
- <http://www.fpgadeveloper.com/2011/07/list-and-comparison-of-fpga-companies.html>