Chengxiang Ge

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25 | Anhui
Career Objective: Digital IC Design Engineer (Shanghai)

EDUCATION

Shanghai University 211 Double 1st-Class Sep 2020 - Jun 2023

Electronic Information Engineering Master School of Communication and Information Engineering

- Research Area: Wireless Communication IC Design
- Academic Performance: Top 10%
- Master's Thesis: "FPGA-Based Realization of Pivotal Technologies for LTE-V2X Baseband Chip"

Shanghai University 211 Double 1st-Class Sep 2016 - Jun 2020

Electronic Information Engineering Bachelor School of Communication and Information Engineering

Personal skills

- Proficient in Verilog programming, with some experience in algorithm RTL implementation, verification, and synthesis.
- Familiar with creating RTL reference models using Matlab and C++, and well-versed in System Verilog and UVM verification processes, including the extraction of validation points, validation cases, and assertion.
- Familiar with Python, Perl, and Shell scripting, with the ability to use ChatGPT to assist in quickly writing scripts.
- Familiar with Vivado, Quartus, ModelSim, VCS, Spyglass, Linux, and Gvim.
- Able to fluently read English research papers and technical manuals.
- Having independently designed key IPs such as FIR, CORDIC, and 2048-point FFT, and I also gained experience in RTL design for outsourced tapeout projects.

Work and internship experience

GigaDevice (Completed the work handover, available to start immediately) Jul 2023 - Nov 2023

Logical Design Verification Engineer Flash design verification department Hefei

1. Completed the company's new employee training program and provided a comprehensive summary report. Acquired fundamental knowledge and skills required in the field of chip design and verification. This encompassed chip design and manufacturing processes, the principles of various storage devices, RTL design and synthesis techniques, Linux and Vim operations, script writing, usage of VCS and software, UVM verification processes.
2. Studied the fundamental principles, applications, and comparisons of DRAM, NOR Flash, and NAND Flash. This included specific implementation solutions for RTL and circuit portions. Acquired knowledge about relevant design and verification documents, RTL code, circuit structures, state machines, and timing diagrams.
3. Participated in a NAND flash project, be responsible for the verification of various voltage control signals during NAND read, write, and erase operations. Wrote checklists based on design documents, supplemented and modified UVM test cases, analyzed the reasons for monitor errors, and performed validation of checklist verification points.

Internship: Qualcomm(3 days a week) Jun 2022 - Sep 2022

Design verification intern Validation team Shanghai

1.Studied the basics of SystemVerilog (SV) and Universal Verification Methodology (UVM), learned the verification process, and configured the server environment. Rebuilt a simple UVM verification environment by referencing other projects, debugged and resolved various errors. Developed UVM components, connected them to the DUT and generated stimuli.

3. Participated in a variety of intern training programs offered by Qualcomm, including career planning, workplace skill enhancement, and English email writing techniques.

PROJECT EXPERIENCE

Work Project: NAND Flash Pump Control Signal Verification Sep 2023 - Nov 2023

- Project Description: The new project involves verifying various voltage control signals applied to the storage

array of NAND Flash chips when receiving different user and test commands to ensure compliance with design requirements.

- Main Responsibilities: Under the guidance of my mentor, I delved into the principles of voltage control functions in NAND Flash under various operating conditions. Based on reference to previous documents, I extracted validation points, wrote and modified test cases, and configured and traversed various parameter combinations. I used simulation tools to check waveform and assertion trigger conditions, analyzed the reasons for assertion errors, and examined the verification environment for potential vulnerabilities in RTL and circuit design. During my work, I identified minor issues related to netlist port connections, documents, and assertion. To address port connection issues, I wrote a Python script that used a training set to verify the accuracy of port connections.

School Laboratory Project: LTE-V IP Design Work (CORDIC, FFT/IFFT IP Design) Aug 2022 - Dec 2022

- Project Description: Due to a future SOC chip tapeout plan, I was responsible for the design and implementation of CORDIC, FFT, and IFFT IPs.
- Main Responsibilities: I referenced Xilinx official manuals and related materials to design and implement the CORDIC, FFT, and IFFT IPs using Verilog. The CORDIC module supports both the sincos calculation the phase rotation. The FFT and IFFT modules are designed with the pipeline structure, featuring 11 stages of butterfly computation and the capability to configure cyclic prefix. These three IPs exhibit accuracy with an error less than 0.4% in configurations with the same quantization bit width. Their computation delay remains consistent with the original Xilinx IP, achieving a synthesis frequency of approximately 400MHz. They have successfully passed extensive on-board testing and meet the requirements of the LTE-V system.

Outsourced Project Undertaken by the Laboratory: DDC Design Project May 2022 - Jul 2023

- Project Description: Design the digital down-conversion module for a high-speed ADC chip, achieving a sampling rate of 500MHz. This module is required to support 8 different operating modes.
- Main Responsibilities: Responsible for all RTL code development. Implemented mixing and FIR decimation filtering functional modules based on C++ algorithm models. Completed RTL-level design and simulation, passing extensive simulation testing. Supported multiple operating modes and custom functions as required by the client. Verification work was outsourced, and it also passed their verification. The client's final feedback indicated that the functionality achieved was similar to that of a chip from TI.

School Laboratory Project: FPGA-Based LTE-V Receiver Synchronization System Sep 2020 - Dec 2020

- Project Description: Hardware implementation of the synchronization algorithm for the LTE-V protocol's physical layer receiver.
- Main Responsibilities: Responsible for all RTL code development for the LTE-V receiver synchronization module, detecting synchronization signal positions and marking wireless frame headers while performing frequency offset estimation and compensation. Completed simulation with multiple sets of test vectors and conducted long-term testing on Xilinx FPGA boards. Currently, LTE-V receiver synchronization works reliably in indoor and outdoor testing, enabling stable video transmission between two Xilinx FPGA boards.

Scientific research achievements and certificates during the school period

A Resource- and Power-Efficient Implementation of PSS Synchronization on FPGA in Vehicular Networks. (Accepted, EAI IoTaaS 2022 Conferences)	2022
FPGA-based system and method for LTE-V terminal CCH channel de-rate matching application number: 202210180518.2	2022
Method and System for FPGA-Based LTE-V Receiver Synchronization, Application Number: 202111208064.7	2021
Shanghai University Graduate Scholarship for Academic Excellence (First Class)	2021 and 2022
Second Prize in the TI Cup undergraduate Electronics Design Contest in Shanghai	2019
Second Prize in the TI Cup undergraduate Electronics Design Contest in Shanghai	2018

Self-evaluation

Resilient | Strong sense of responsibility | Optimistic | Enjoys teamwork | Good communication skills

Other

Have a wide range of interests and hobbies, participated in the college's Student Union, Sports Department, and Basketball Team.