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HUF76629D3ST-F085

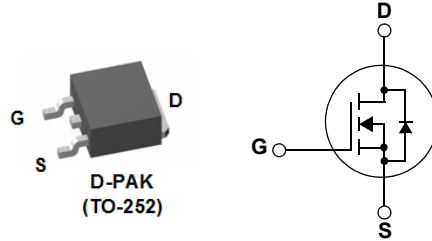
N-Channel Logic Level UltraFET® Power MOSFET
100V, 20A, 52mΩ

Features

- Typ $r_{DS(on)} = 41m\Omega$ at $V_{GS} = 10V$, $I_D = 20A$
- Typ $Q_{g(tot)} = 39nC$ at $V_{GS} = 10V$, $I_D = 20A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 16	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	20	A
	Pulsed Drain Current	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	231	mJ
P_D	Power Dissipation	150	W
	Derate above $25^\circ C$	1	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance Junction to Case	1	$^\circ C/W$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	52	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
HUF76629D3ST	HUF76629D3ST-F085	D-PAK(TO-252)	13"	12mm	2500 units

Notes:

1: Current is limited by bondwire configuration.

2: Starting $T_J = 25^\circ C$, $L = 1.8mH$, $I_{AS} = 16A$, $V_{DD} = 100V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche

3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

HUF76629D3ST-F085 N-Channel Logic Level UltraFET® Power MOSFET

Electrical Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	100	-	-	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 100\text{V}$, $T_J = 25^{\circ}\text{C}$ $V_{GS} = 0\text{V}$, $T_J = 175^{\circ}\text{C}$ (Note 4)	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 16\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1.0	1.6	3.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 20\text{A}$, $T_J = 25^{\circ}\text{C}$	-	41	52	$\text{m}\Omega$
		$V_{GS} = 10\text{V}$, $T_J = 175^{\circ}\text{C}$ (Note 4)	-	102	128	$\text{m}\Omega$
		$I_D = 20\text{A}$, $T_J = 25^{\circ}\text{C}$	-	47	55	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}$, $T_J = 175^{\circ}\text{C}$ (Note 4)	-	115	135	$\text{m}\Omega$

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz		-	1280	-	pF
C _{oss}	Output Capacitance			-	214	-	pF
C _{rss}	Reverse Transfer Capacitance			-	33	-	pF
R _g	Gate Resistance	f = 1MHz		-	2.5	-	Ω
Q _{g(ToT)}	Total Gate Charge	V _{GS} = 0 to 10V	V _{DD} = 50V I _D = 20A	-	39	43	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 2V		-	2.3	3	nC
Q _{gs}	Gate to Source Gate Charge			-	3.5	-	nC
Q _{gd}	Gate to Drain “Miller” Charge			-	11	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 50\text{V}$, $I_D = 20\text{A}$, $V_{GS} = 10\text{V}$, $R_{GEN} = 8.2\Omega$	-	-	27	ns
$t_{d(on)}$	Turn-On Delay Time		-	7	-	ns
t_r	Rise Time		-	12	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	38	-	ns
t_f	Fall Time		-	5	-	ns
t_{off}	Turn-Off Time		-	-	47	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 20\text{A}$, $V_{GS} = 0\text{V}$	-	-	1.25	V
		$I_{SD} = 10\text{A}$, $V_{GS} = 0\text{V}$	-	-	1.0	V
T_{rr}	Reverse Recovery Time	$I_F = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$, $V_{DD} = 80\text{V}$	-	77	99	ns
Q_{rr}	Reverse Recovery Charge		-	221	305	nC

Notes:

4: The maximum value is specified by design at $T_J = 175^{\circ}\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

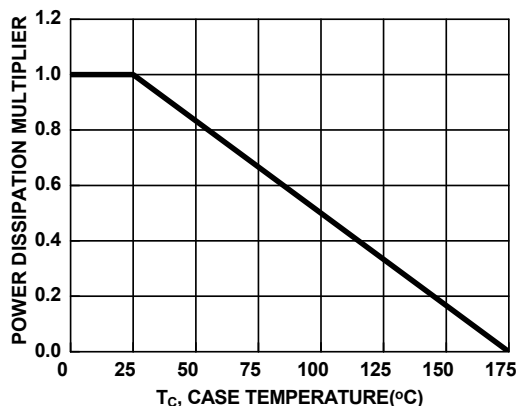


Figure 1. Normalized Power Dissipation vs Case Temperature

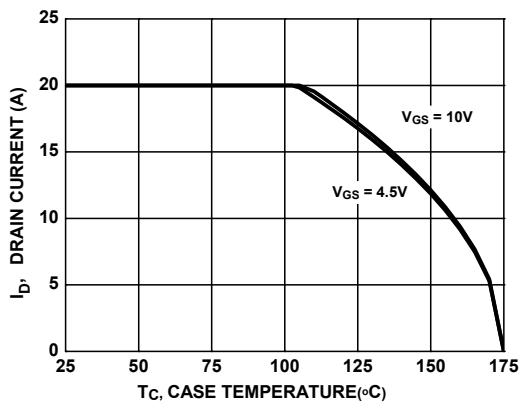


Figure 2. Maximum Continuous Drain Current vs Case Temperature

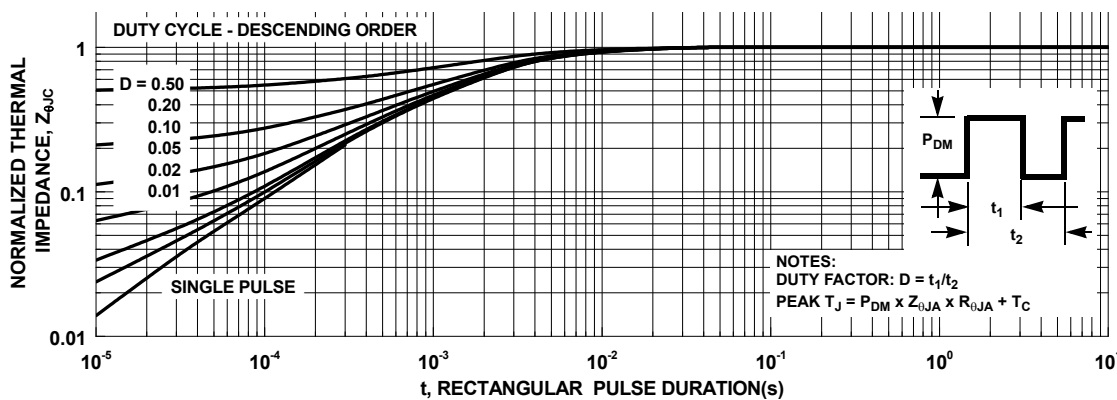


Figure 3. Normalized Maximum Transient Thermal Impedance

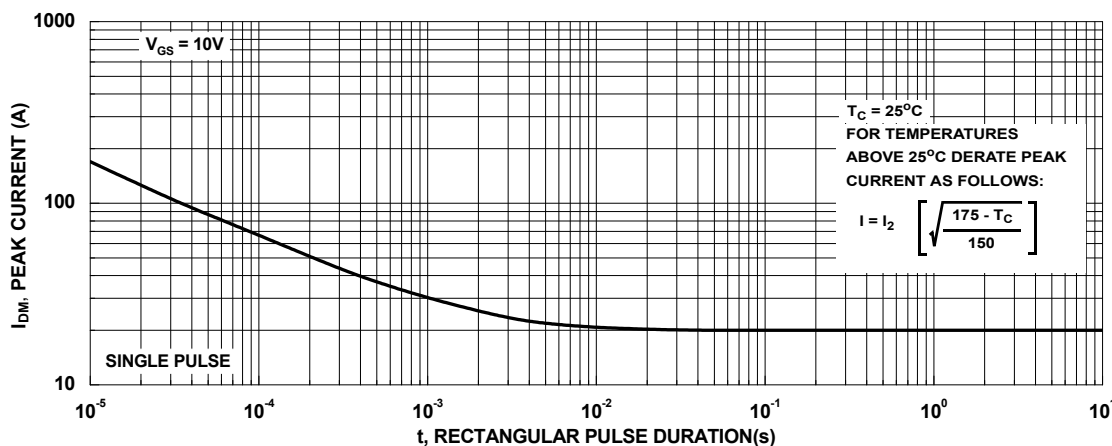


Figure 4. Peak Current Capability

Typical Characteristics

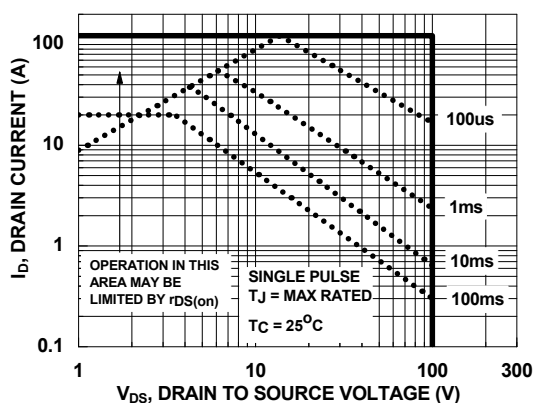
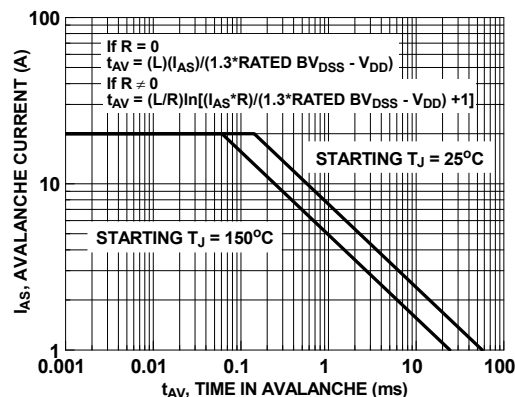


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to On Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

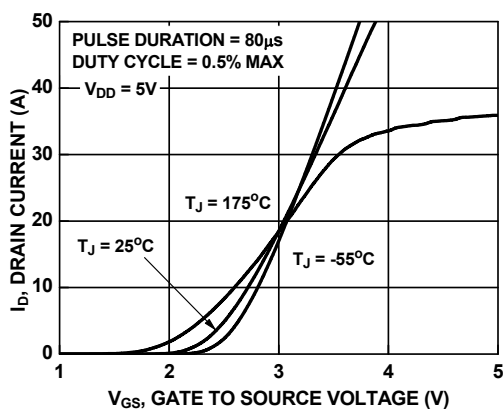


Figure 7. Transfer Characteristics

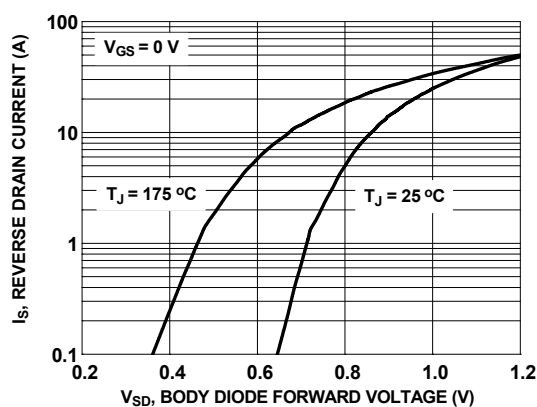


Figure 8. Forward Diode Characteristics

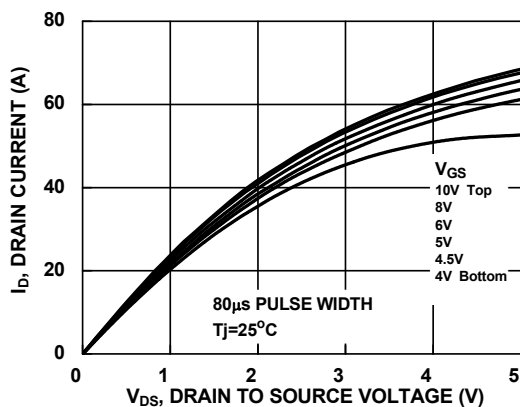


Figure 9. Saturation Characteristics

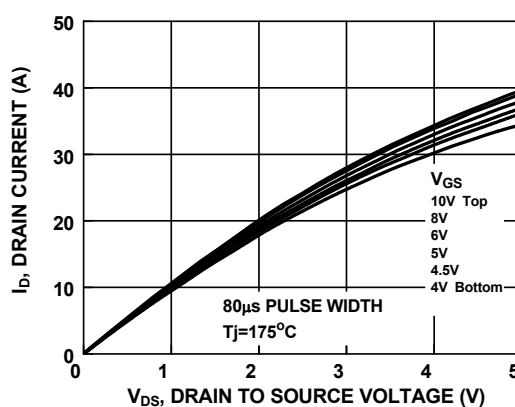


Figure 10. Saturation Characteristics

Typical Characteristics

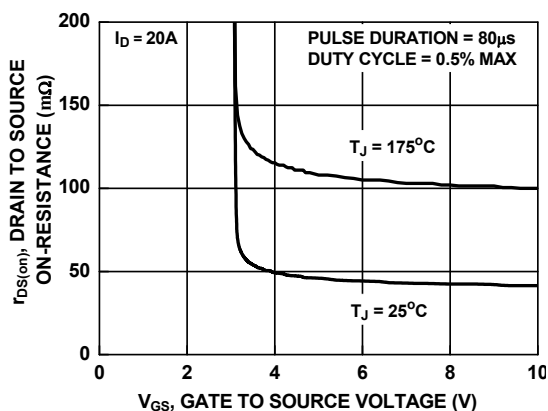


Figure 11. $R_{ds(on)}$ vs Gate Voltage

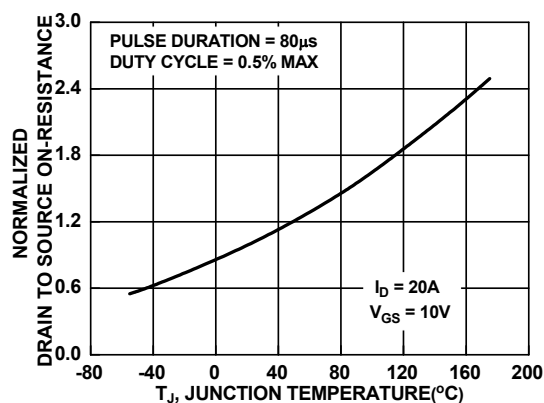


Figure 12. Normalized $R_{ds(on)}$ vs Junction Temperature

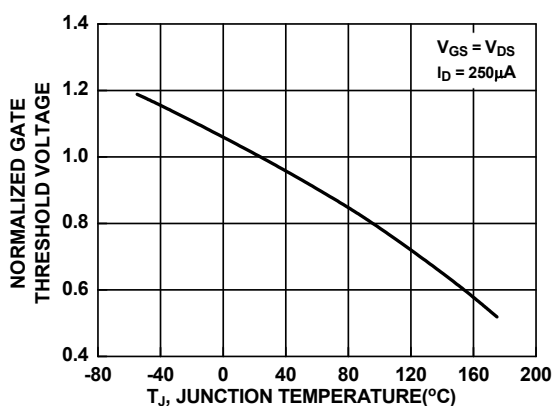


Figure 13. Normalized Gate Threshold Voltage vs Temperature

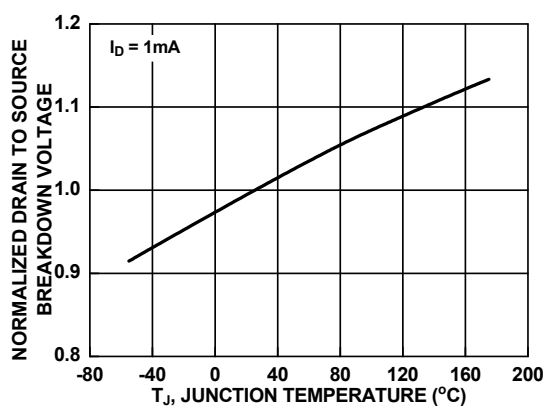


Figure 14. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

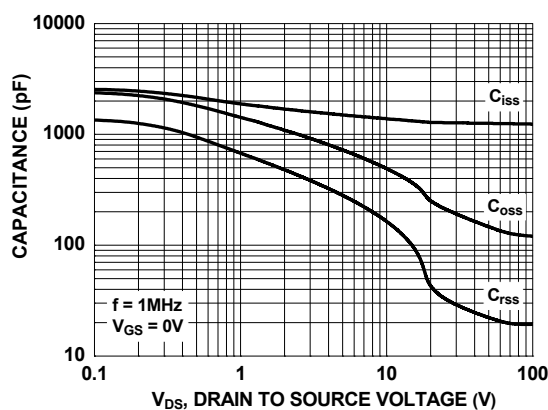


Figure 15. Capacitance vs Drain to Source Voltage

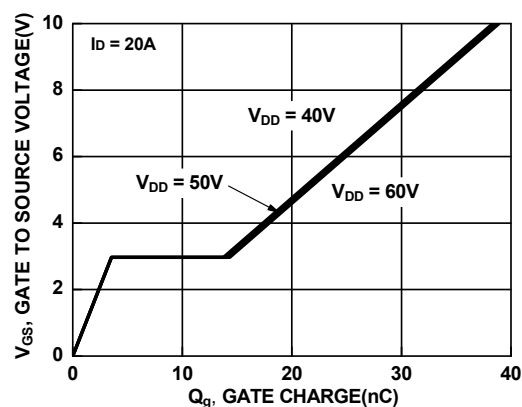



Figure 16. Gate Charge vs Gate to Source Voltage

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