Lab 1 Report

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1. Spike model and co-sim

1.1 Spike model (with Risc-V pk) execution correctness

The program for test is a simple C program that calculates the sum from 1 to 9.

```c
//
//  main.c
//  test
//
//  Created by 许昊 on 2022/10/14.
//

#include <stdio.h>

int main(int argc, const char * argv[]) {
    int a = 0;
    for ( int i = 0; i < 10; ++i){
        a += i;
    }
    printf("%d\n",a);
    return 0;
}
```

The result using Spike with PK is as follows:

```
[xuhao@server1 workspace]$ spike $PK test
bbl loader
45
[xuhao@server1 workspace]$
```

1.2 GreenRio core RTL execution correctness

Load the hex elf file in the memory:

```
dpram64 #(
    .SIZE(1<<16), // byte
    .mem_clear(1'b1),
    .memfile("isatest/rv64ui-p-andi.hex")
) magicmemory(
    .clk(clk),
    .we(s1_we),
    .din(s1_wdat),
    .waddr(s1_adr),
    .raddr(s1_adr),
    .dout(s1_rdat)
);
```

Simulate:

```
RTLPATH = ../rtl/lab_1/src \
    ../rtl/lab_1/src/cache \
    ../rtl/lab_1/src/cache/cacheblock \
    ../rtl/lab_1/src/core_empty \
    ../rtl/lab_1/src/core_empty/lsu \
    ../rtl/lab_1/src/core_empty/pipeline \
    ../rtl/lab_1/src/core_empty/units \
    .

RTLFILE += $(foreach p,$(RTLPATH),$(wildcard $(p)/*.v $(p)/*.sv))
CFILE = plug.cpp

VCSFLAG = -full64 +v2k -kdb -debug_access+all +define+DUMPON+CPLUG \
    -sverilog +vcs+lic+wait +vc+list +vpi \
    -timescale=1ns/1ps -v2k_generate +incdir+../rtl/lab_1/src


compile:
    vcs $(VCSFLAG) $(RTLFILE) $(CFILE) -top tb_hehe
```

```
Parsing design file './tb_hehe.v'
Parsing design file './dpram64.sv'
Parsing design file './wb_arb.sv'
Parsing design file './wb_interconnect.sv'
Top Level Modules:
       tb_hehe
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...

8 modules and 0 UDP read.
recompiling module l1dcache
recompiling module l1icache_32
recompiling module backend
recompiling module counter_rob
recompiling module csr
recompiling module tb_hehe
recompiling module dpram64
recompiling module wb_interconnect
All of 8 modules done
make[1]: Entering directory '/work/stu/xuhao/workspace/CPULAB/riosclass_template/verilog/NewTop/csrc'
make[1]: Leaving directory '/work/stu/xuhao/workspace/CPULAB/riosclass_template/verilog/NewTop/csrc'
make[1]: Entering directory '/work/stu/xuhao/workspace/CPULAB/riosclass_template/verilog/NewTop/csrc'
```

Run the simulation result:

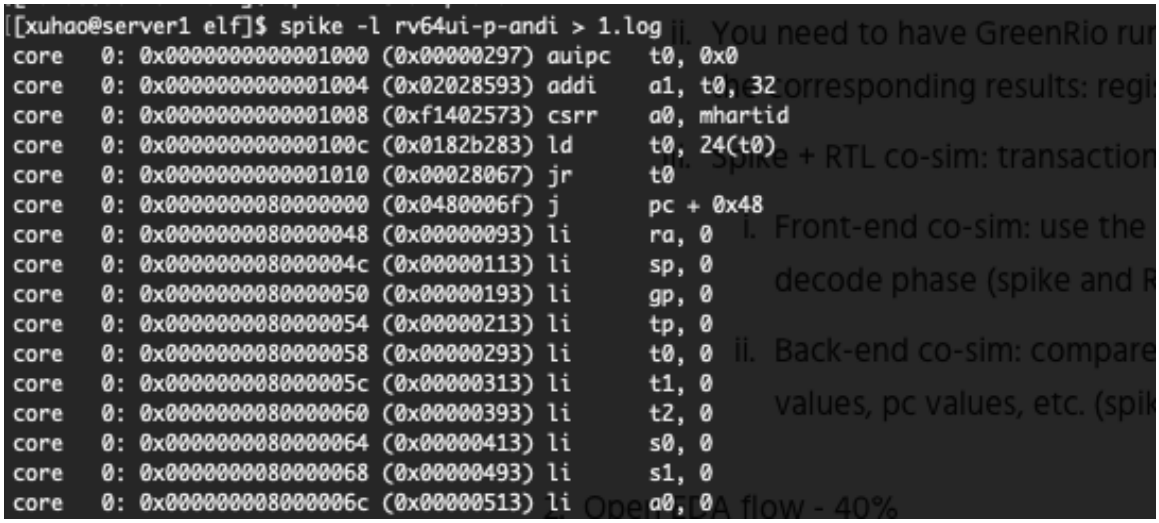
```
[xuhao@server1 NewTop]$ ./simv
Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP2_Full64; Runtime version Q-2020.03-SP2_Full64;  Oct 25 21:57 2022
Preloading tb_hehe.magicmemory from isatest/rv64ui-p-andi.hex
VCD+ Writer Q-2020.03-SP2_Full64 Copyright (c) 1991-2020 by Synopsys Inc.
*Verdi* Loading libsscore_vcs202003.so
FSDB Dumper for VCS, Release Verdi_Q-2020.03-SP2, Linux x86_64/64bit, 08/31/2020
(C) 1996 - 2020 by Synopsys, Inc.
*Verdi* : Create FSDB file 'novas.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : Enable +all dumping.
*Verdi* : End of traversing.
*Verdi* : fsdbDumpon - All FSDB files at 0 ps.
0x00000000
0x80000000
0x80000048
x1 <- 0
0x8000004C
x2 <- 0
```

```
x31 <- 11
0x8000001C
0x8000003C
x30 <- -2147479492
pass test
$finish called from file "./tb_hehe.v", line 119.
$finish at simulation time            18055000
           V C S   S i m u l a t i o n   R e p o r t
Time: 18055000 ps
CPU Time:      0.920 seconds;       Data structure size:   0.1Mb
Tue Oct 25 21:57:27 2022
[xuhao@server1 NewTop]$
```

1.3 Spike model + GreenRio RTL co-simulation system

1.3.1 Run the elf file on the spike emulator and print the log

The result with log is as follows:



1.3.2 Have GreenRio run the risc-v elf in an RTL simulation environment and get the corresponding results

2. Open EDA flow

2.1 GreenRio core logic synthesis by yosys

Configure the OpenLane environment and test:

```
[xuhao@server1 OpenLane]$ make test
cd /work/stu/xuhao/tools/OpenLane && \
        docker run --rm -v /work/stu/xuhao/tools/OpenLane:/openlane -v /work/stu/xuhao/tools/OpenLane/designs:/openlane/install -v /w
k/stu/xuhao/tools/OpenLane/pdks -e PDK=sky130A  --user 10215:1001 -e DISPLAY= -v /tmp/.X11-unix:/tmp/.X11-unix -v /work/stu/xuhao/.Xa
d7947cf9f-amd64 sh -c "./flow.tcl -design spm -tag openlane_test -overwrite"
OpenLane e3a5189a1b0fc4290686fcf2ae46cd6d7947cf9f
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Available under the Apache License, version 2.0. See the LICENSE file for more details.

[INFO]: Using configuration in 'designs/spm/config.json'...
[INFO]: PDK Root: /work/stu/xuhao/tools/OpenLane/pdks
[INFO]: Process Design Kit: sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library: sky130_fd_sc_hd
[INFO]: Run Directory: /openlane/designs/spm/runs/openlane_test
[INFO]: Removing existing /openlane/designs/spm/runs/openlane_test...
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis (log: designs/spm/runs/openlane_test/logs/synthesis/1-synthesis.log)...
```

```
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: Current core area is too small for a power grid. The power grid will be minimized.

Basic test passed
```

GreenRio core logic synthesis:

```
[OpenLane Container (e3a5189):/openlane$ ./flow.tcl -design hehe
OpenLane e3a5189a1b0fc4290686fcf2ae46cd6d7947cf9f
All rights reserved. (c) 2020-2022 Efabless Corporation and contributors.
Available under the Apache License, version 2.0. See the LICENSE file for more details.

[INFO]: Using configuration in 'designs/hehe/config.tcl'...
[INFO]: PDK Root: /work/stu/xuhao/tools/OpenLane/pdks
[INFO]: Process Design Kit: sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library: sky130_fd_sc_hd
[INFO]: Run Directory: /openlane/designs/hehe/runs/RUN_2022.10.26_14.33.51
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[STEP 1]
[INFO]: Running Synthesis (log: designs/hehe/runs/RUN_2022.10.26_14.33.51/logs/synthesis/1-synthesis.log)...
```

Use a different lib:

```
tools > OpenLane > pdks > sky130A > libs.tech > openlane > sky130_fd_sc_hd >  ≡ config.tcl
1   set current_folder [file dirname [file normalize [info script]]]
2   # Technology lib
3
4   set ::env(LIB_SYNTH) "$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd__tt_100C_1v80.lib"
5   set ::env(LIB_FASTEST) "$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd__ff_100C_1v95.lib"
6   set ::env(LIB_SLOWEST) "$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd__ss_100C_1v40.lib"
```

2.2 GreenRio core gate level netlist + Spike co-sim execution correctness

Get the gate level netlist file

(the file path is as follows: RUN_2022.10.26_15.05.51/results/synthesis/hehe.v)