[System Architecture](#h.h98c2qbs3qjk)

[Hardware Architecture](#h.x534mnp37c8o)

[Firmware Architecture](#h.i5bxigg37hib)

# System Architecture

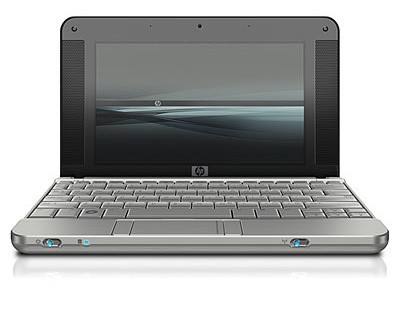
1234

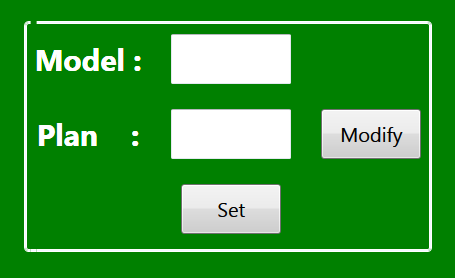
12341234

ABCDEFGH

PLAN

ACTUAL





ETHERNET CABLE

230V, AC INPUT

ABCDEFGH

1234

# Hardware Architecture

[PCB DESIGN](https://github.com/jjyothilinga/PCB_ASB_RANGSONS/)

DATA

PORTJ

PIC18F8722

1234

1234

MACHINE INPUT

SINGLE

CHANNEL

RELAY MODULE

DIGIT

SELECTION

PORTJ

B0

PORTC

UART

INTERFACE

PORTF

PORTE

PORTD

DIGIT

SELECTION

ROW SELECTION

COLOUMN

SELECTION

Decoder

Board

PIC18F67J60

ABCDEFGH

TCP/IP

INPUT

# Firmware Architecture

1. **PIC18F67J60**

[FIRMWARE](https://github.com/jjyothilinga/tcpip_to_uart/)

UART

TCP/IP STACK

COMMUNICATION

BERKELY SERVER

1. **PIC18F8722**

[FIRMWARE](https://github.com/jjyothilinga/Rangsons/)

EEPROM

APP

COMMUNICATION

DIGIT DISPALY

MMD

UART