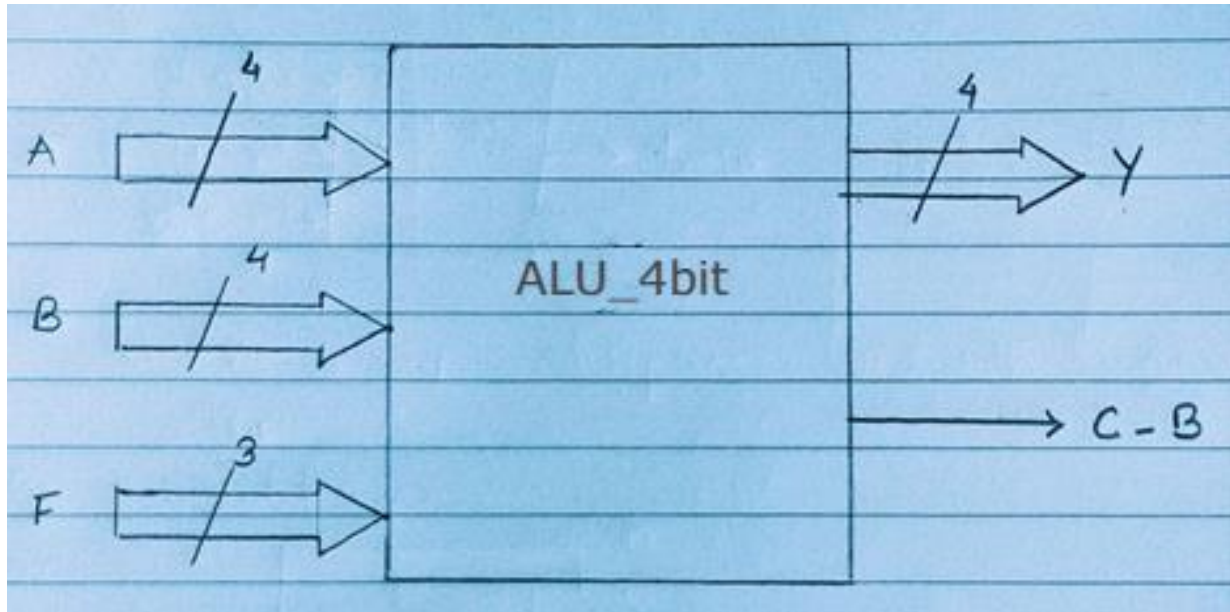


Class	:	
Batch	:	
Roll. No	:	
ABC ID	:	
Assignment No.	:	A.1
Assignment Name	:	4-Bit A.L.U (8 Operations : 6 Logical , 2 Arithmetic)
Date Of Performance	:	

BLOCK DIAGRAM



FUNCTION TABLE

F			Y	C_B
F ₂	F ₁	F ₀		
0	0	0	$A \cdot B$	x
0	0	1	$\overline{A \cdot B}$	x
0	1	0	$A + B$	x
0	1	1	$A \oplus B$	x
1	0	0	$\overline{A \odot B}$	x
1	0	1	$\overline{A + B}$	x
1	1	0	$A + B$	carry
1	1	1	$A - B$	borrow

MAIN VHDL MODEL (MVM)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity ALU_4bit is
  Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
        B : in  STD_LOGIC_VECTOR (3 downto 0);
        F : in  STD_LOGIC_VECTOR (2 downto 0);
        Y : out STD_LOGIC_VECTOR (3 downto 0);
        C_B : out STD_LOGIC
        );
end ALU_4bit;

architecture ALU_4bit_arch of ALU_4bit is

  signal result:STD_LOGIC_VECTOR(4 downto 0):="00000";

begin

  process(A,B,F)

  begin

    CASE F IS

      when "000" =>
        result <= '0' & (A AND B);

      when "001" =>
        result <= '0' & (A NAND B);

      when "010" =>
        result <= '0' & (A OR B);

      when "011" =>
        result <= '0' & (A XOR B);

      when "100" =>
        result <= '0' & (A XNOR B);

      when "101" =>
        result <= '0' & (A NOR B);

      when "110" =>
        result <= ('0' & A)+('0' & B);
```

```

when others =>
  if A < B then
    result <= '0' & (NOT B);
    result <= result+1;
    result <= ('0' & A) + result;
    result <= (NOT result) +1;
    result <= (NOT(('0' & A) + ('0' &(NOT B)) + 1))+1;
  else
    result <=('0' & A)-('0' & B);
  end if ;

end CASE;

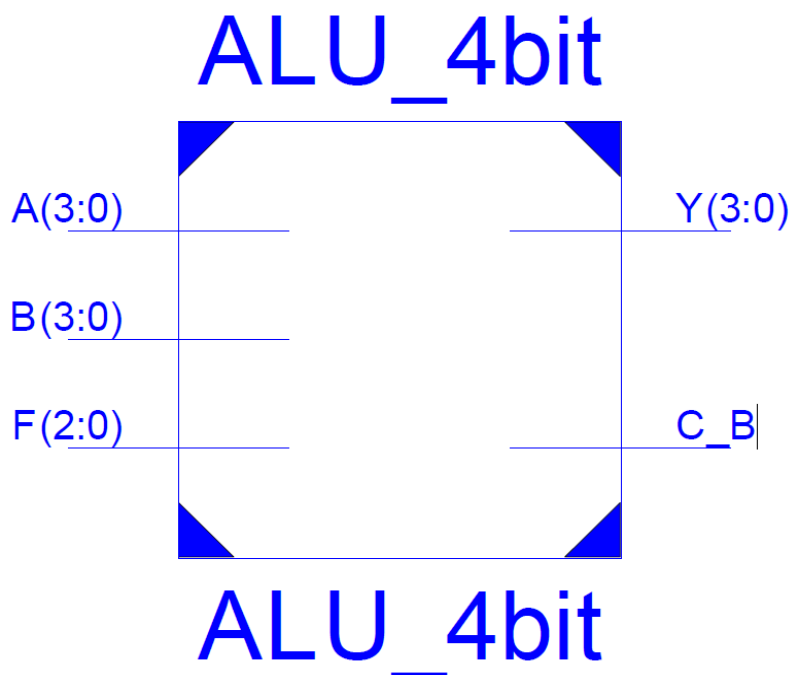
end process;

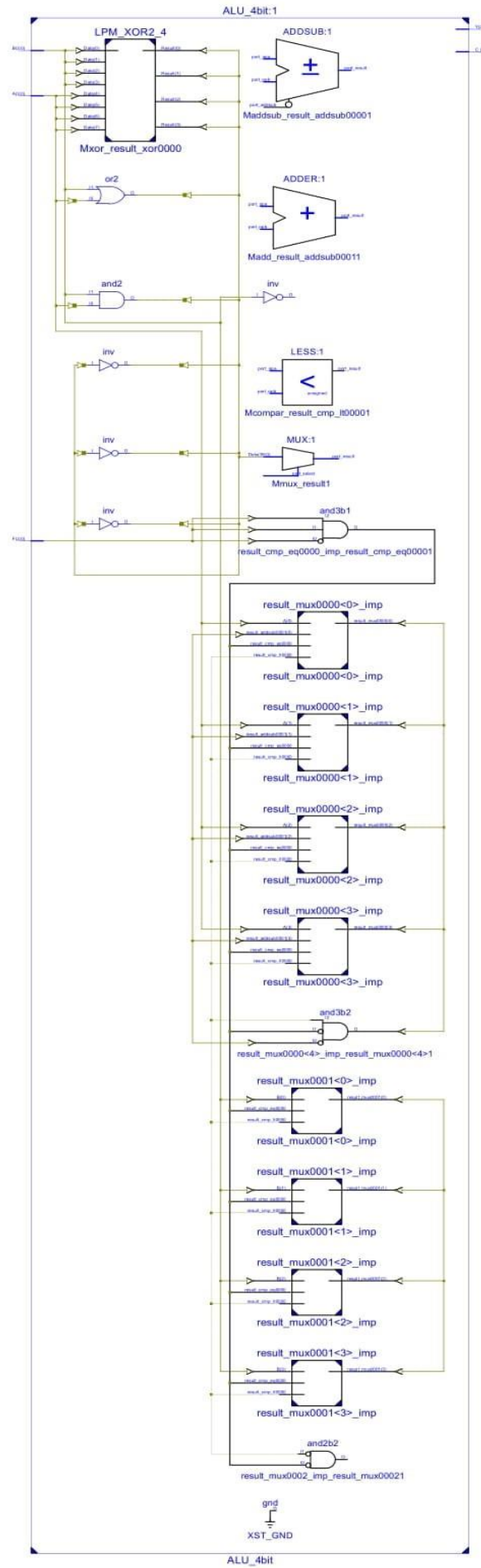
Y <= result(3 downto 0);
C_B <= result(4);

end ALU_4bit_arch;

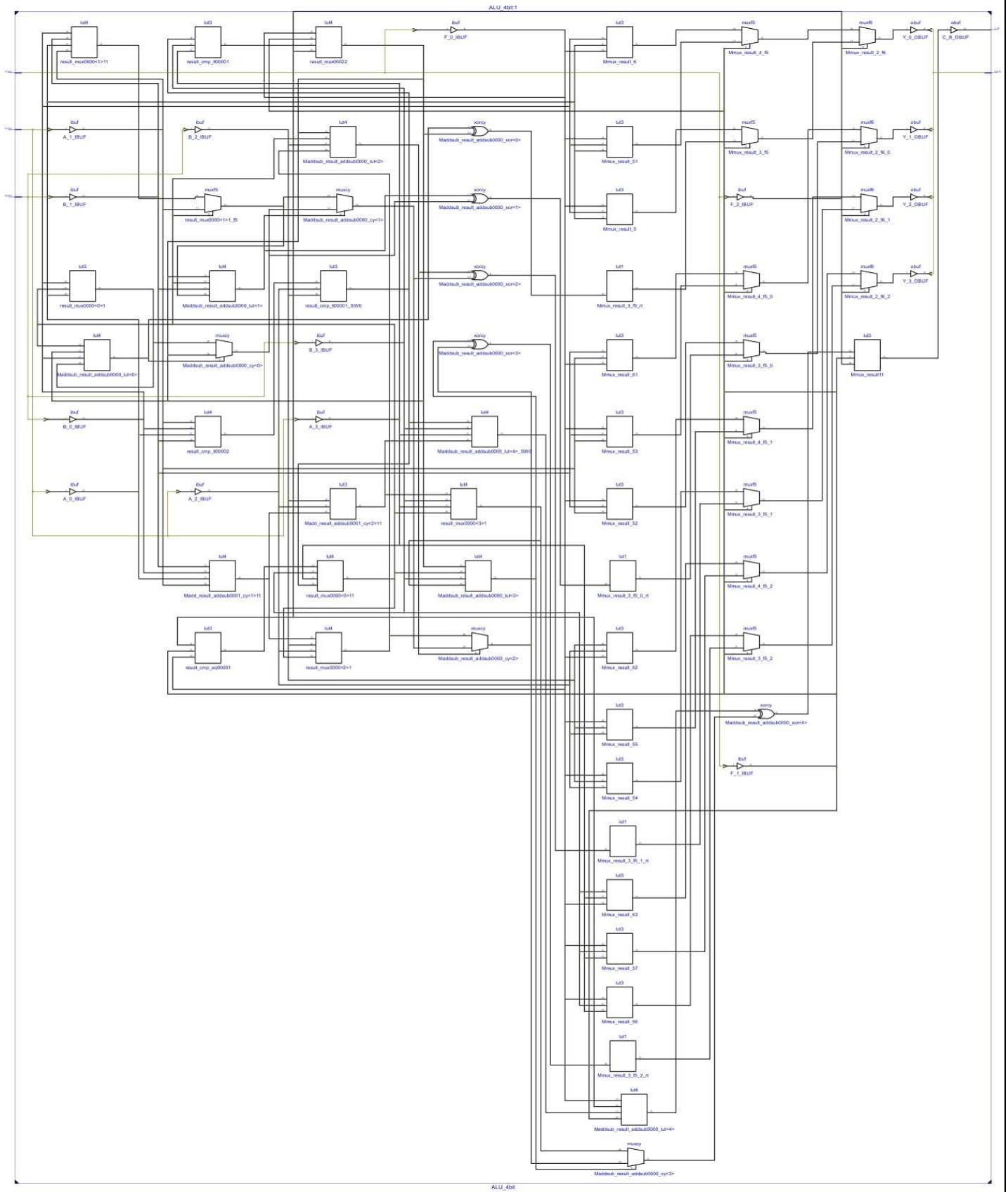
```

RTL SCHEMATIC:





TECHNOLOGY SCHEMATIC



SYNTHESIS REPORT

a) Device Utilization Summary:

=====

*	Final Report	*
---	--------------	---

=====

Final Results

RTL Top Level Output File Name : ALU_4bit.ngr

Top Level Output File Name : ALU_4bit

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 16

Cell Usage :

BELS : 57

LUT1 : 4

LUT3 : 18

LUT4 : 13

MUXCY : 4

MUXF5 : 9

MUXF6 : 4

XORCY : 5

IO Buffers : 16

IBUF : 11

OBUF :

=====

Device utilization summary:

=====

Selected Device : 3s250epq208-5

Number of Slices: 19 out of 2448 0%

Number of 4 input LUTs: 35 out of 4896 0%

Number of IOs: 16

Number of bonded IOBs: 16 out of 158 10%

b) TIMING REPORT:

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -5

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 13.714ns

Timing Detail:

All values displayed in nanoseconds (ns)

TESTBENCH VHDL MODEL (TVM)

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY ALU_4bit_tb IS
END ALU_4bit_tb;

ARCHITECTURE behavior OF ALU_4bit_tb IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT ALU_4bit
    PORT(
        A : IN  std_logic_vector(3 downto 0);
        B : IN  std_logic_vector(3 downto 0);
        F : IN  std_logic_vector(2 downto 0);
        Y : OUT std_logic_vector(3 downto 0);
        C_B : OUT std_logic
    );
    END COMPONENT;

    --Inputs
    signal A : std_logic_vector(3 downto 0) := "0010";
    signal B : std_logic_vector(3 downto 0) := "1111";
    signal F : std_logic_vector(2 downto 0) := (others => '1');

    --Outputs
    signal Y : std_logic_vector(3 downto 0);
    signal C_B : std_logic;
    -- No clocks detected in port list. Replace <clock> below with
    -- appropriate port name

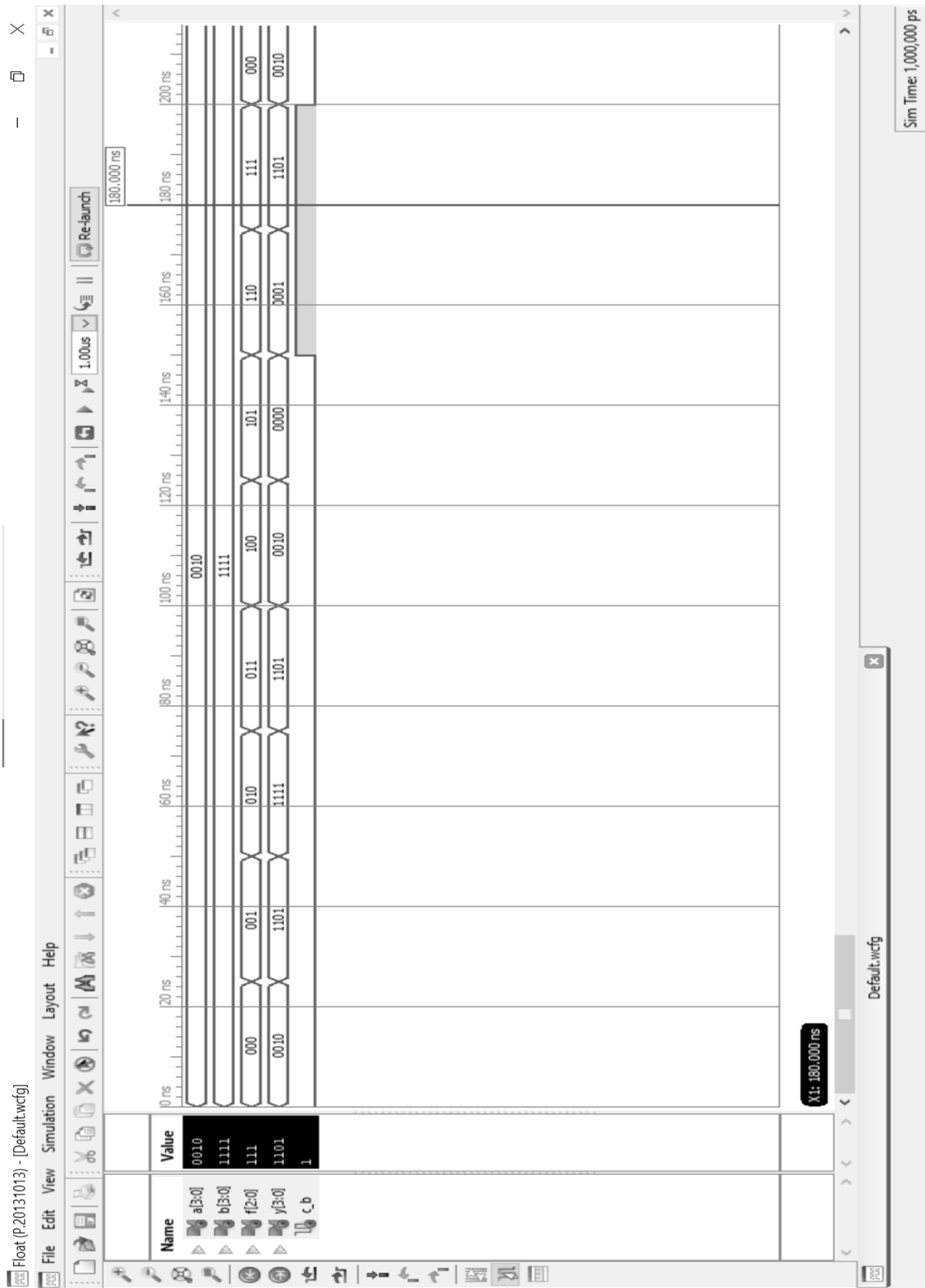
    BEGIN

    uut: ALU_4bit PORT MAP (
        A => A,
        B => B,
        F => F,
        Y => Y,
        C_B => C_B
    );

    stim_proc_F: process
    begin
        F <= F + 1;
        wait for 25 ns;

    end process;
END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

PlanAhead Generated physical constraints

NET "A[3]" LOC = P205;
NET "A[2]" LOC = P206;
NET "A[1]" LOC = P203;
NET "A[0]" LOC = P200;
NET "B[3]" LOC = P192;
NET "B[2]" LOC = P193;
NET "B[1]" LOC = P189;
NET "B[0]" LOC = P190;
NET "F[2]" LOC = P179;
NET "F[1]" LOC = P180;
NET "F[0]" LOC = P177;
NET "Y[3]" LOC = P165;
NET "Y[2]" LOC = P167;
NET "Y[1]" LOC = P163;
NET "Y[0]" LOC = P164;
NET "C_B" LOC = P153;

CONCLUSION

Thus, we have:

- 1) Modeled a 4-Bit ALU using Behavioral Modeling Style.
- 2) Observed following Schematics: **RTL & Technology Schematics** generated **Post-Synthesis**.
- 3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
- 4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency, setup time, hold time.
- 5) Written a TESTBENCH to verify the functionality of 4-Bit ALU & verified the functionality as per the FUNCTION-TABLE, by observing ISIM Waveforms.
- 6) Used PlanAhead Editor for pin-locking.
- 7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4-Bit ALU & verified its operation by giving suitable input combinations.