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CS 475 Parallel Programming

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Project #4: Vectorized Array Multiplication/Reduction using SSE

1. What machine you ran this on
   - I ran this on the flip server.
2. Show the table of performances for each array size and the corresponding speedups

Arraysize	Non-SIMD Mul	SIMD Mul	Mul Speed-Up	Non-SIMD Red	SIMD Red	Red Speed-Up
1000000	221.13	999.66	4.52	233.39	1791.19	7.67
2000000	220.91	878.02	3.97	228.37	1433.65	6.28
3000000	213.32	856.92	4.02	226.96	1302.62	5.74
4000000	220.58	873.15	3.96	225.46	1307.17	5.8
5000000	221.62	864.85	3.9	226.77	1303.76	5.75
6000000	220.42	872.89	3.96	227.34	1337.48	5.88
7000000	220.47	729.91	3.31	225.04	1262.45	5.61
8000000	219.25	855.14	3.9	225.62	1342.58	5.95

3. Show the graph of SIMD/non-SIMD speedup versus array size (one curve only)

Red Speed-Up
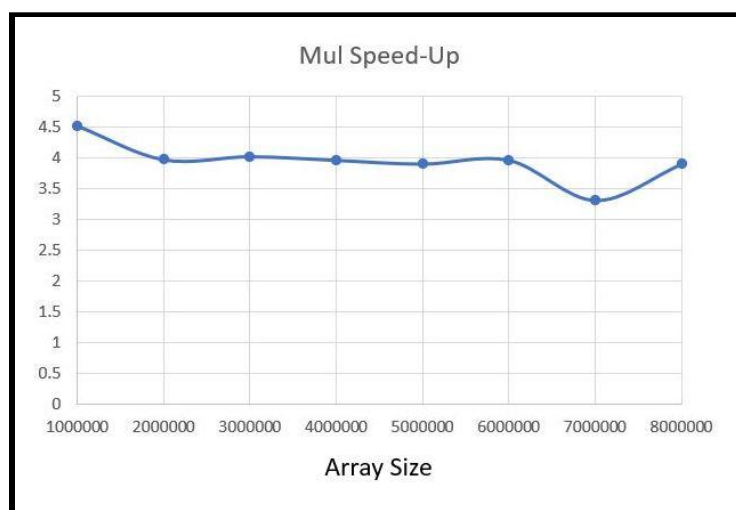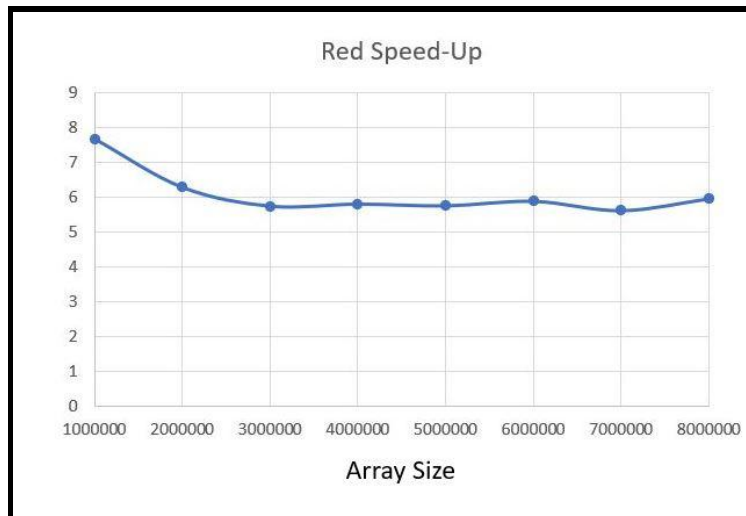
4. What patterns are you seeing in the speedups?
   - At first glance, the array multiplication speedup is on average smaller than the array reduction speedup. Moreover, its change in speedup over the array sizes also seem to be smaller. Despite the obvious differences in speedup, however, both speedup graphs appear to roughly follow the same pattern/curve, featuring a dip after 1000000 array size and remaining relatively stable for the following array sizes.
5. Are they consistent across a variety of array sizes?
   - Both the array multiplication and reduction speedups are relatively consistent after array size of 1000000, with the former maintaining approximately 4X speedup and the latter maintaining approximately 6X speedup.
6. Why or why not, do you think?
   - I think the reason why both speedups are consistent is because the array multiplication and reduction sections of the code improved by SSE may be approaching their theoretical maximum speedup given the array sizes. The roughly 4X speedup from the array multiplication SIMD graph almost appears to match the SSE_WIDTH of 4. Even though the speedup from the array reduction SIMD is roughly 6X, it may be the case that the operation is more performant and may require even larger array sizes to reach the theoretical maximum speedup.