诚尚Micro™

Abacus 1 Minicomputer
Instruction Reference Card

Control Instructions

```
nop
out
hlt
```

Accumulator Instructions

```
add A/V
sub A/V
xor A/V
and A/V
or A/V
not
```

Data Transfer Instructions

```
lda A/V
ldi I
sta A/V
ldf
```

Branching Instructions

```
jmp A/L
jc A/L
jz A/L
```

Notation	Meaning
A	Address
I	Integer *[1]*
V	Variable
L	Label *[2]*
/	Many types accepted

[1] Integer values must be in the range 0x000 to 0xfff (0-4095).

[2] Labels used as operands must be defined elsewhere in the program.

Access DB parts list goes here.

Abacus 1 System
Schematics Redacted

MOTOROLA

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

SN54/74LS160A
SN54/74LS161A
SN54/74LS162A
SN54/74LS163A

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

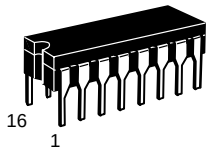
LOW POWER SCHOTTKY

The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary.)

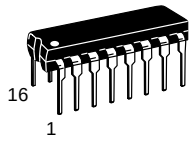
The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

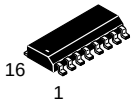
- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts


16
1

J SUFFIX
CERAMIC
CASE 620-09


16
1

N SUFFIX
PLASTIC
CASE 648-08

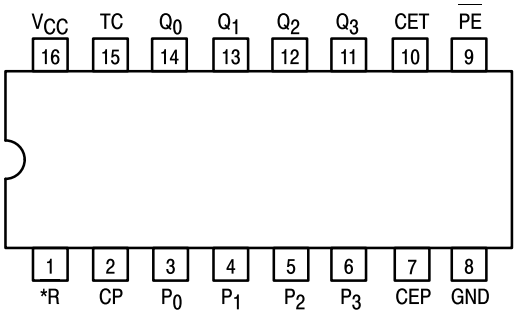

16
1

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

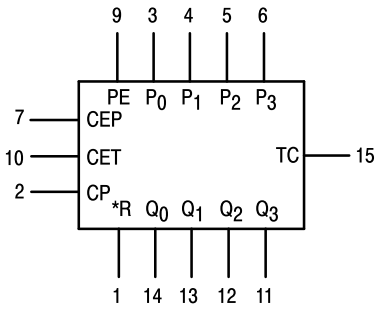
*MR for LS160A and LS161A
*SR for LS162A and LS163A

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
SR	Synchronous Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

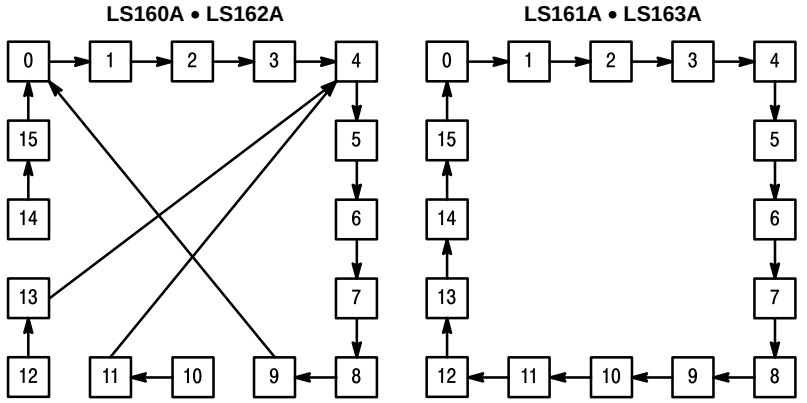
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

*MR for LS160A and LS161A
*SR for LS162A and LS163A

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = CEP • CET • PE

TC for LS160A & LS162A = CET • Q_0 • Q_1 • Q_2 • Q_3

TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3

Preset = PE • CP + (rising clock edge)

Reset = MR (LS160A & LS161A)

Reset = SR • CP + (rising clock edge)
(LS162A & LS163A)

NOTE:
The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and PE inputs are HIGH. When the PE is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET • CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the MR is LOW, it overrides all other input conditions and sets the outputs LOW. The MR pin should never be left open. If not used, the MR pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and PE, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD (P_n Q_n)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

FAIRCHILD SEMICONDUCTOR™

April 1988
Revised June 2002

74F189
64-Bit Random Access Memory with 3-STATE Outputs

General Description

The F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-STATE and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Features

- 3-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing

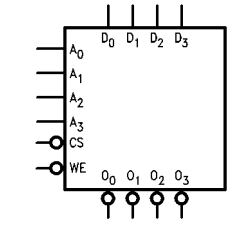
Ordering Code:

Order Number	Package Number	Package Description
74F189SC	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F189SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F189PC (Note 1)	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

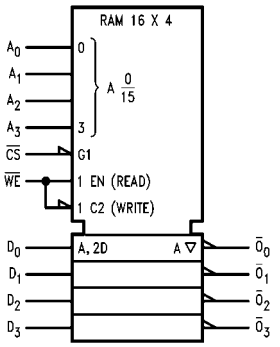
Devices also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

Note 1: This device not available in Tape and Reel.

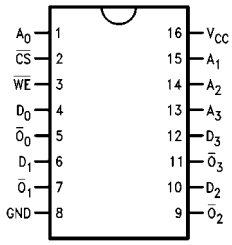
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

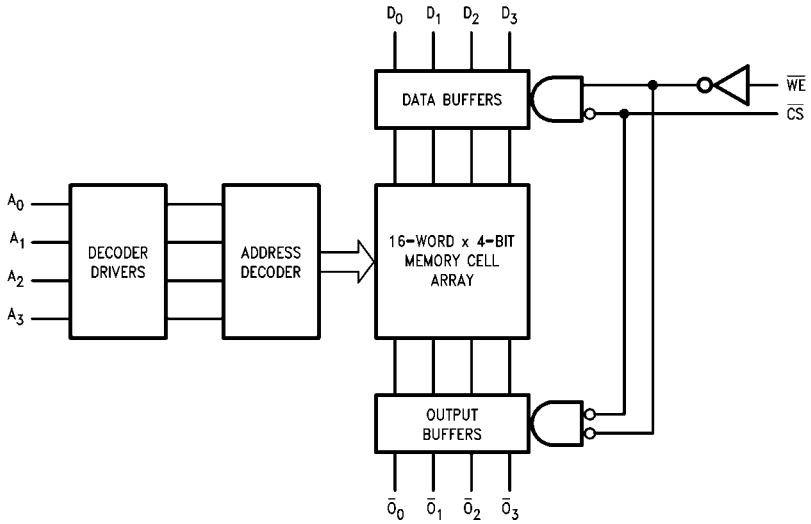
Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_3	Address Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 µA/–1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
D_0–D_3	Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{O}_0$–$\overline{O}_3$	Inverted Data Outputs	150/40 (33.3)	–3.0 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Features

- **Fast Read Access Time - 150 ns**
- **Fast Byte Write - 200 µs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **Internal Address and Data Latches**
  - **Internal Control Timer**
  - **Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **$\overline{\text{DATA}}$ POLLING**
- **Low Power**
  - **30 mA Active Current**
  - **100 µA CMOS Standby Current**
- **High Reliability**
  - **Endurance: 10^4 or 10^5 Cycles**
  - **Data Retention: 10 Years**
- **5V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Commercial and Industrial Temperature Ranges**

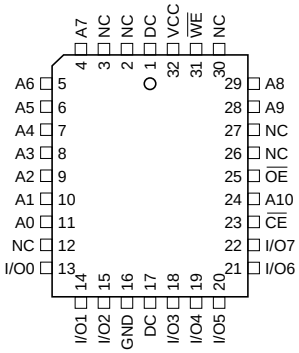
Description

The AT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C16 is a 16K memory organized as 2,048 words by 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology. *(continued)*

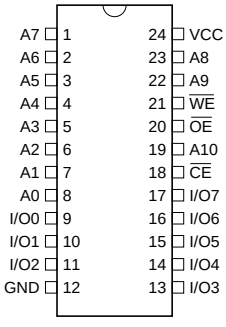
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

PLCC
Top View



PDIP, SOIC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

16K (2K x 8) Parallel EEPROMs

AT28C16

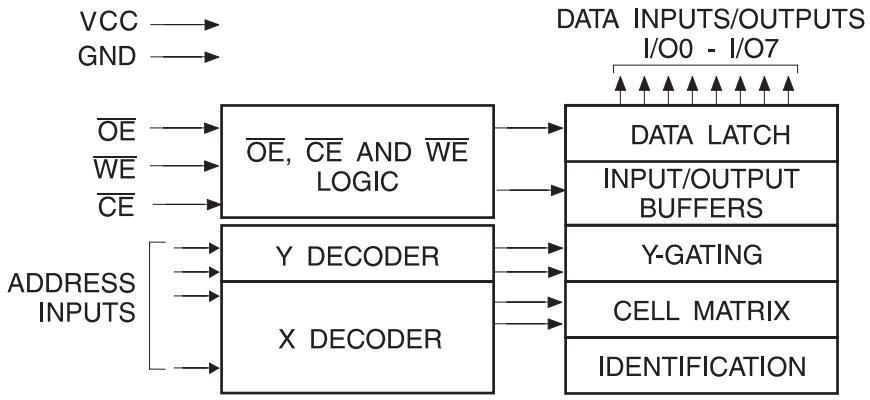
Rev. 0540B–10/98

The AT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{\text{DATA}}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Atmel's 28C16 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C16E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{\text{DATA}}$ POLLING: The AT28C16 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DATA SHEET

74F382
Arithmetic Logic Unit

Product specification

1990 Jul 12

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Arithmetic logic unit 74F382

FEATURES

- Performs six arithmetic and logic functions
- Selectable Low (clear) and High (preset) functions
- Low-input loading minimizes drive requirements
- Carry output for ripple expansion
- Overflow output for Two's Complement arithmetic

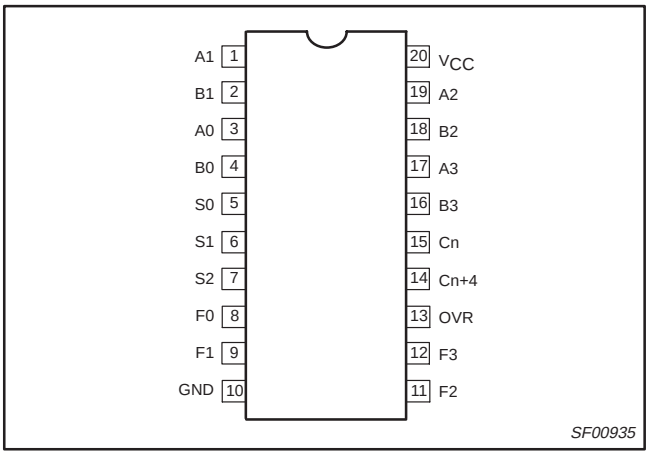
DESCRIPTION

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select (S0–S2) input codes force the Function outputs Low or High. An overflow output is provided for convenience in Two's Complement arithmetic.

A carry output is provided for ripple expansion. For high-speed expansion using a carry look-ahead generator, refer to the 74F381 data sheet.

Signals applied to the Select inputs, S0–S2, determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-HIgh or active-Low operands, with output levels in the same convention. In the subtract operating modes, it is necessary to force a carry (High for active-HIgh operands, Low for active-Low operands) into the Cn input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of Cn+3 and Cn+4; a High signal on OVR indicates overflow in Two's complement operation (See Table 2 for Two's complement arithmetic). Typical delays for Figure 1 are given in Table 1. When the 74F382 is cascaded to handle word lengths longer than 4 bits, only the most significant overflow (OVR) output is used.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0ns	54mA

ORDERING INFORMATION

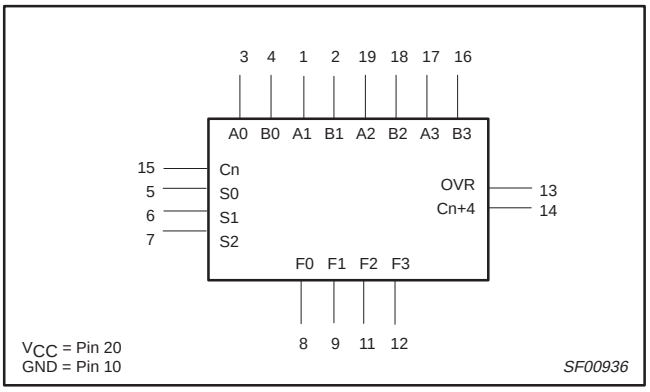
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
20-pin plastic DIP	N74F382N	SOT146-1
20-pin plastic SO	N74F382D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

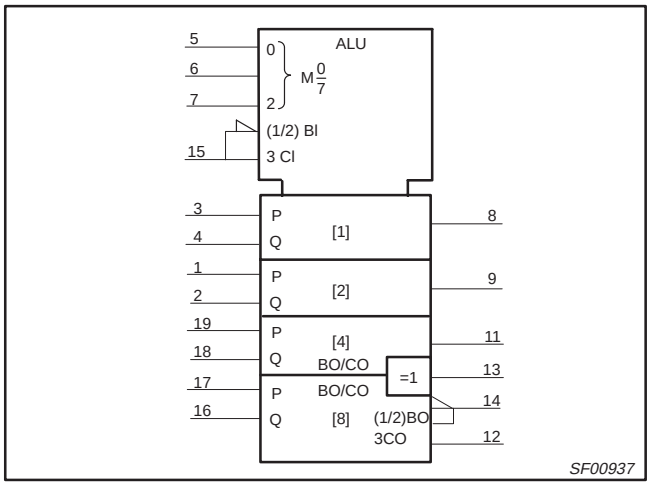
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A3	A operand inputs	1.0/4.0	20µA/2.4mA
B0 – B3	B operand inputs	1.0/4.0	20µA/2.4mA
S0 – S2	Function select inputs	1.0/1.0	20µA/0.6mA
Cn	Carry input	1.0/5.0	20µA/3.0mA
Cn+4	Carry output	50/33	1.0mA/20mA
OVR	Overflow output	50/33	1.0mA/20mA
F0–F3	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as 20µA in the High state and 0.6mA in the Low state.

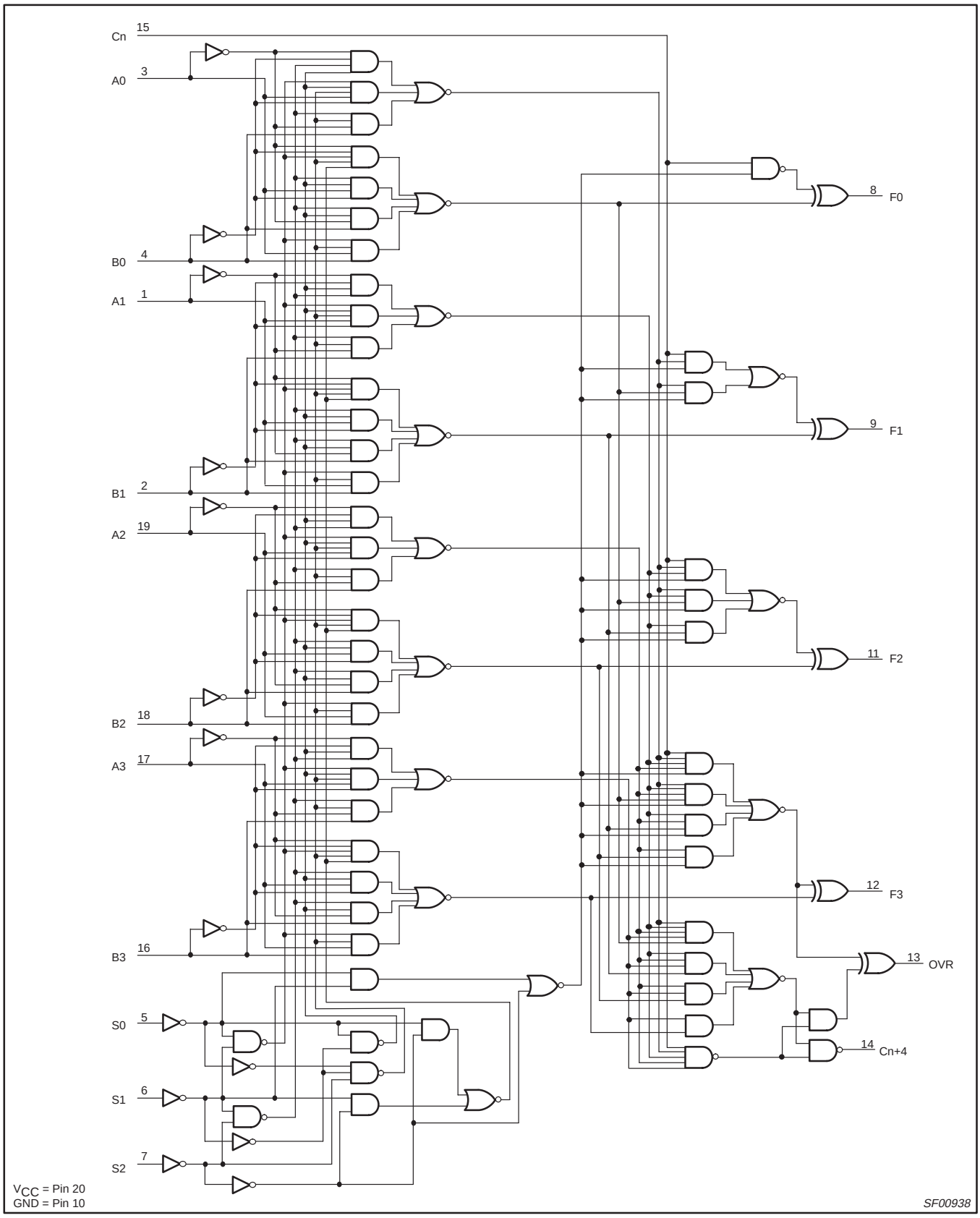
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS						OPERANDS	OPERATING MODE
S0	S1	S2	Cn	An	Bn	F0	F1	F2	F3	OVR	Cn+4		
L	L	L	L	X	X	L	L	L	L	H	H		Clear
L	L	L	H	X	X	L	L	L	L	H	H		
H	L	L	L	L	L	H	H	H	H	L	L	Active-Low	B minus A
H	L	L	L	L	H	L	H	H	H	L	H		
H	L	L	L	H	L	L	L	L	L	L	L		
H	L	L	L	H	H	H	H	H	H	L	L		
H	L	L	H	L	L	L	L	L	L	L	H	Active-High	
H	L	L	H	L	H	H	H	H	H	L	H		
H	L	L	H	H	L	H	L	L	L	L	L		
H	L	L	H	H	H	L	L	L	L	L	H		
L	H	L	L	L	L	H	H	H	H	L	L	Active-Low	A minus B
L	H	L	L	L	H	L	L	L	L	L	L		
L	H	L	L	H	L	L	H	H	H	L	H		
L	H	L	L	H	H	H	H	H	H	L	L		
L	H	L	H	L	L	L	L	L	L	L	H	Active-High	
L	H	L	H	L	H	H	L	L	L	L	L		
L	H	L	H	H	L	H	H	H	H	L	H		
L	H	L	H	H	H	L	L	L	L	L	H		
H	H	L	L	L	L	L	L	L	L	L	L		A Plus B
H	H	L	L	L	H	H	H	H	H	L	L		
H	H	L	L	H	L	H	H	H	H	L	L		
H	H	L	L	H	H	L	H	H	H	L	H		
H	H	L	H	L	L	H	L	L	L	L	L		
H	H	L	H	L	H	L	L	L	L	L	H		
H	H	L	H	H	L	L	L	L	L	L	H		
H	H	L	H	H	H	H	H	H	H	L	H		
L	L	H	X	L	L	L	L	L	L	L	L		A ⊕ B
L	L	H	X	L	H	H	H	H	H	L	L		
L	L	H	L	H	L	H	H	H	H	L	L		
L	L	H	X	H	H	L	L	L	L	H	H		
L	L	H	H	H	L	H	H	H	H	H	H		
H	L	H	X	L	L	L	L	L	L	L	L		A + B
H	L	H	X	L	H	H	H	H	H	L	L		
H	L	H	X	H	L	H	H	H	H	L	L		
H	L	H	L	H	H	H	H	H	H	L	L		
H	L	H	H	H	H	H	H	H	H	H	H		
L	H	H	X	L	L	L	L	L	L	H	H		AB
L	H	H	X	L	H	L	L	L	L	L	L		
L	H	H	X	H	L	L	L	L	L	H	H		
L	H	H	L	H	H	H	H	H	H	L	L		
L	H	H	H	H	H	H	H	H	H	H	H		
H	H	H	X	L	L	H	H	H	H	L	L		Preset
H	H	H	X	L	H	H	H	H	H	L	L		
H	H	H	X	H	L	H	H	H	H	L	L		
H	H	H	L	H	H	H	H	H	H	L	L		
H	H	H	H	H	H	H	H	H	H	H	H		

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S0	S1	S2	
L	L	L	Clear
H	L	L	B minus A
L	H	L	A minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
Ai or Bi to Cn+4	6.5ns	6.5ns
Cn to Cn+4	6.3ns	6.3ns
Cn to Cn+4	6.3ns	6.3ns
Cn to F	8.1ns	–
Cn to Cn+4, OVR	–	8.0ns
Total Delay	27.2ns	27.1ns

Table 2. Two's Complement Arithmetic

MSB			LSB	Numerical Values
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	–8
H	L	L	H	–7
H	L	H	L	–6
H	L	H	H	–5
H	H	L	L	–4
H	H	L	H	–3
H	H	H	L	–2
H	H	H	H	–1

H = High voltage level
L = Low voltage level

APPLICATION

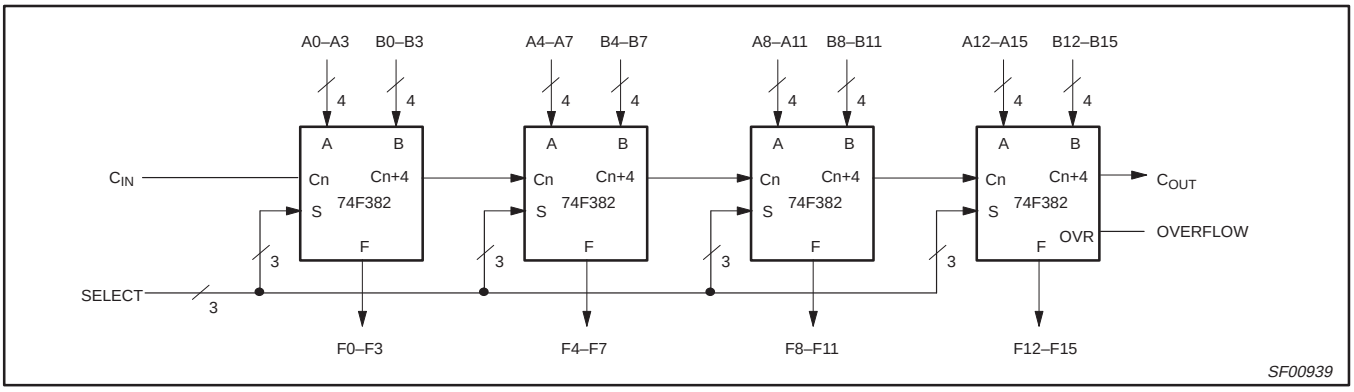


Figure 1. 16-bit Look-ahead Carry ALU Expansion

— FACSIMILE TRANSMISSION —

RETROGRADE TURING SYSTEMS
137 BERRINGA ROAD
VIC 3114, AUSTRALIA
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TO: **DATE:**

FROM: **NO. OF PAGES (INCL. THIS ONE):**

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