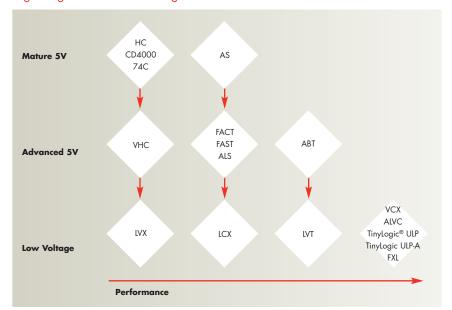


Logic Selection Guide

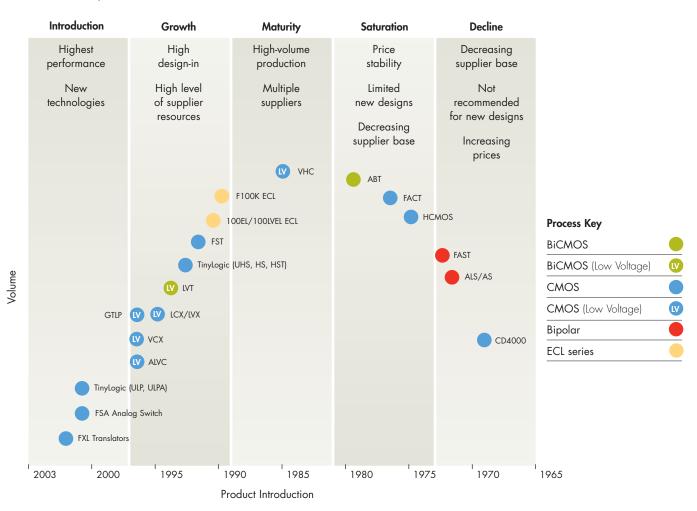
How to use this guide

The data on this page (page 2) give an historic overview of Fairchild's available logic families. The Quick Reference Attributes charts on page 3 may be a good first step if a particular type performance needs emphasis. The Family Specifications Comparison chart on page 4 lists general performance by operating voltage. Propagation Delay and Power Consumption are then further detailed in charts on page 5. The Product Portfolio and Description chart on page 6 summarizes the functions that are available within each of the logic families. The packaging table (page 7) provides dimensions for all packages, and their availability by logic family.

Logic Migration and Low-Voltage Transition



Product Life Cycle



Quick Reference Attributes for Logic

Process Tech.	High Speed	Low Noise	Low-Static Power	High Drive	Low Voltage	Board Space	Analog Signal Video Signal	Logic Level Translation
BICMOS 5V	ABT			ABT				
BICMOS 3V	LVT			LVT	LVT			
CMOS 5V	TinyLogic UHS	TinyLogic HS/HST	TinyLogic HS/HST			TinyLogic HS/HST		
			UHS					
		FACT QS	FACT					
	FACT	HC/HCT	FACT QS					
	FS	S VHC/VHCT						
		FST (Fairchild Switch)	VHC/VHCT					
		GTLP		GTLP		FXL Translators	FSA (Analog Switch)	FST (Fairchild Switch)
CMOS LV	VCX	LVX	LCX		LCX	TinyLogic UHS		FXL Translators
	LCX	TinyLogic HS	LVX		LVX			VCX Translators
	TinyLogic UHS		VCX		VCX			FXLP Translators
	TinyLogic ULP-A	TinyLogic ULP	TinyLogic HS/UHS		ALVC			
			TinyLogic ULP		TinyLogic ULP	TinyLogic ULP		
	GTLP	GTLP	TinyLogic ULP-A	GTLP	TinyLogic ULP-A	TinyLogic ULP-A		
Bipolar	FASTr	ALS		FASTr				
		FAST						
ECL	F100K FCI							
	F100K ECL							

Noise*

VHC

VHCT

НС

HCT

FASTr

FAST

AS

ALS

Bipolar

BiCMOS Notes 0.6 ABT -1.0 LVT/LVTH 3.3V 0.8 -0.8 '244 CMOS Quiet Output 1.8V ** VCX° (16) 1.8V 0.2 -0.2 HL or LH Transition 0.6 -0.6 0.8 -0.8 CROSSVOLT™ $V_{\text{OLP}} \\$ -0.3 LCX (16) 2.5V 0.3 3.3V 0.4 -0.5 LCX (8) 2.5V 0.5 -0.5 Quiet Output V_{OLV} 3.3V 0.7 -0.7 LVX 0.3 -0.2 AC 1.6 -1.5 '244 function, C_{LOAD}= 50pF, ACQ 0.9 -0.6 $R_L = 500 \Omega$, seven ACT -1.6 1.6 outputs switching, -0.5 ACTQ 0.9 minimum input

0.6

0.7

0.5

0.5

0.8

0.6

8.0

-0.6

-0.7

-0.3

-0.3

-0.8

-0.3

-1.4

-0.5

skew, typical

* No overshoot/ undershoot

oscilliscope

° C_{LOAD} = 30pF

‡ 16612 function

measurements

ringing evident for

values

VOLP (V) VOLV (V)

Quick Reference Attributes for Analog Switches

Part	Configuration	R _{ON} (Ω)	Supply Voltage (Vcc)	R _{ON} (Ω) Flatness		THD	Packages
FSA66	SPST	5.0	1.65V - 5.5V	6.0	250	0.011%	SC70, MicroPak, SOT23
FSAT66	SPST	7.0	1.65V - 5.5V	6.0	250	0.011%	SC70, MicroPak, SOT23
FSA3157	SPDT	5.0	1.65V - 5.5V	6.0	250	0.011%	SC70, MicroPak
FSA4157	SPDT	1.0	1.65V - 5.5V	0.2	350	0.003%	SC70, MicroPak
FSA266	Dual SPST	7.0	1.65V - 5.5V	6.0	300	0.016%	US8, MicroPak
FSAU3157	SPDT	5.0	1.65V - 5.5V	6.0	250	0.011%	SC70, MicroPak
FSA4684A	Dual SPDT	1.0	1.65V - 5.5V	0.2	350	0.003%	MicroPak
FSAV330	Quad SPDT Video Switch	7.0	4.0V - 5.5V		300		TSSOP, QSOP, SOIC
FSAL200	Quad 2:1 Mux/Demux (SPDT) LAN Switch	6.0	3.0V - 5.5V	3.0	300		QSOP, MLP
FSA3357	SP3T	6.0	1.65V - 5.5V	5.0	250	0.010%	US8, MicroPak
74VHC4051	8 Channel Mux	30.0	2.0V - 6.0V	N/A	35	0.008%	TSSOP, SOIC, PDIP
74VHC4052	Dual 4 Channel Mux	30.0	2.0V - 6.0V	N/A	35	0.008%	TSSOP, SOIC, PDIP
74VHC4051	Triple 2 Channel Mux	30.0	2.0V - 6.0V	N/A	35	0.008%	TSSOP, SOIC, PDIP
74VHC4066	Quad SPST	30.0	2.0V - 12.0V	N/A	100	0.008%	TSSOP, SOIC, PDIP

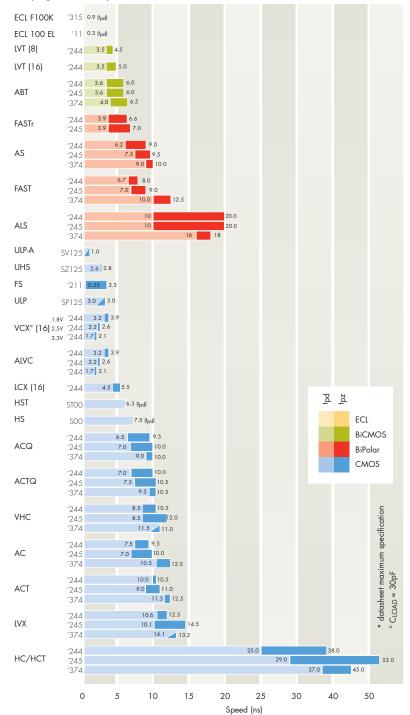
Family Specification Comparison*

	Technology	Specified Power Supply**	Speed †	Drive ††	Supply Current †
		Nominal V _{CC}	† _{PD}	lol / loh	Icc
Sub 3 Volt					
TinyLogic® ULP ◊◊	CMOS	0.9 / 1.2 / 1.5 / 1.8 / 2.5 / 3.3V	7ns	-2.6μΑ / 2.6μΑ	5μΑ
TinyLogic® ULP-A ↔	CMOS	0.9 / 1.2 / 1.5 / 1.8 / 2.5 / 3.3V	3ns	-24µA / 24µA	5μΑ
VCX ◊◊◊	CMOS	1.2 / 1.5 / 1.8 / 2.5 / 3.3V	2.5 / 3.2ns	-24mA / 24mA	20μΑ
ALVC	CMOS	1.8 / 2.5 / 3.3V	3.Ons	-24µA / 24µA	20μΑ
3 Volt					
TinyLogic® UHS ◊◊	CMOS	1.65 / 2.5 / 3.3 / 5V	4.5ns	-32mA / 32mA	20μΑ
LCX (8)	CMOS	2.5 / 3.3V	6.5ns	-24mA / 24mA	10μΑ
LCX (16)	CMOS	2.5 / 3.3V	4.5ns	-24mA / 24mA	20µA
LVT (8)	BiCMOS	3.3V	3.5ns	-32mA / 64mA	5mA
LVT (16)	BiCMOS	3.3V	3.5ns	-32mA / 64mA	5mA
LVX (8)	CMOS	3.3V	12.0ns	-4mA / 4mA	40μΑ
3Volt - 5 Volt					
VHC	CMOS	3.3 / 5V	8.5ns	-8mA / 8mA	40µA
HC	CMOS	2 / 4.5 / 6V	25ns	-6mA / 6mA	80µA
TinyLogic® HS ◊◊	CMOS	2.0 / 3.0 / 4.5 / 6V°°°	21ns	-2.6mA / 2.6mA	10µA
AC	CMOS	3.3 / 5V	7.5ns	-24mA / 24mA	80μΑ
ACQ	CMOS	3.3 / 5V	6.5ns	-24mA / 24mA	80μΑ
GTLP	CMOS	3.3 / 5V		-48mA / 48mA	5mA
F. W. h.					
5 Volt VHCT	CMOS	5V	9.5ns	-8mA / 8mA	40μΑ
HCT	CMOS	5V	25ns	-6mA / 6mA	80μΑ
FST Fairchild Switch	CMOS	4.0 - 5.5V	0.25ns	N/A	ЗμΑ
FASTr™	BiPolar	5V	3.9ns	-15mA / 64mA	75mA
FAST®	BiPolar	5V	6.5ns	-15mA / 64mA	90mA
AS	BiPolar	5V	6.2ns	-15mA / 64mA	90mA
ALS	BiPolar	5V	1 Ons	-15mA / 24mA	27mA
F100K	ECL	-5.7 to -4.2V	1.55ns	-1.8V into 50Ω	-65mA
100 EVL	ECL	-5.5 to -4.2V	0.385ns	-1.8V into 50Ω	-36mA
100 LVEL	ECL	-3.0 to -3.8V	0.435ns	-1.8V into 50Ω	-30mA
ACT	CMOS	5V	10.0ns	-24mA / 24mA	80μΑ
ACTQ	CMOS	5V	7.0ns	-24mA / 24mA	80μΑ
ABT	BiCMOS	5V	3.6ns	-32mA / 64mA	30mA
TinyLogic® HST ↔	CMOS	4.5 / 5 / 5.5V	30ns	-2.0mA / 2.0mA	10μΑ
15 Volt					
15 Volt 74C	CMOS	3 - 15V	70ns	-14mA / 12mA	300µA

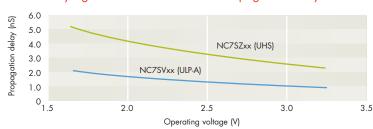
Notes

- * '244 function used unless otherwise noted
- ** except for ECL and HC
- ‡ input levels recognized by the device
- ‡‡ input levels the device is capable of driving
- maximum specification at maximum specified V_{CC}
- †† at maximum specified V_{CC}
- ° 7407 used for specifications
- ° CD4010 used for specifications
- ♦♦ NAND Gate (00) function for data
- $\Diamond\Diamond\Diamond C_{LOAD} = 30pF$

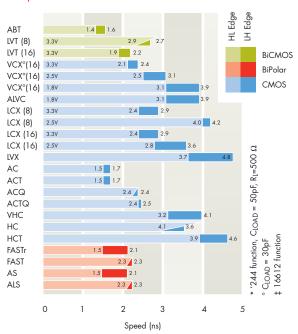
Propagation Delay*



TinyLogic ULP-A and UHS Series Propagation Delay



Output Rise and Fall Time*



Dynamic Current Consumption* (mA)

BICMOS ABT 19.7 43.8 115.9 266.0 303.3 LVT (8) 11.0 29.3 75.8 133.4 170.2 LVT (16) 12.5 90.1 246.2 494.3 580.1 CMOS VCX (16) 9.9 61.9 146.8 253.7 312.7 ALVC 9.9 61.9 146.8 253.7 312.7 LCX (8) 2.2 20.9 64.8 146.6 163.1 LCX (16) 6.7 61.9 160.0 294.4 375.1 LVX 2.0 19.4 64.0 100.1 106.3 AC 3.9 38.9 105.5 352.8 404.2 ACQ 5.4 52.3 139.5 206.0 218.5 VHC 3.1 30.8 103.0 180.7 192.1 HC 3.8 37.9 132.0 181.5 — Bipolar FAST 42.9 69.4 136.6 221.1 246.8 FASTr 38.6 58.0 94.5 198.2 232.4 ALS 14.1 41.0 126.7 240.2 393.8
LVT (8) 11.0 29.3 75.8 133.4 170.2 LVT (16) 12.5 90.1 246.2 494.3 580.1 CMOS
LVT (16) 12.5 90.1 246.2 494.3 580.1 CMOS
CMOS
VCX (16) 9.9 61.9 146.8 253.7 312.7 ALVC 9.9 61.9 146.8 253.7 312.7 LCX (8) 2.2 20.9 64.8 146.6 163.1 LCX (16) 6.7 61.9 160.0 294.4 375.1 LVX 2.0 19.4 64.0 100.1 106.3 AC 3.9 38.9 105.5 352.8 404.2
ALVC 9.9 61.9 146.8 253.7 312.7 LCX (8) 2.2 20.9 64.8 146.6 163.1 LCX (16) 6.7 61.9 160.0 294.4 375.1 LVX 2.0 19.4 64.0 100.1 106.3 AC 3.9 38.9 105.5 352.8 404.2
LCX (8) 2.2 20.9 64.8 146.6 163.1 LCX (16) 6.7 61.9 160.0 294.4 375.1 LVX 2.0 19.4 64.0 100.1 106.3 AC 3.9 38.9 105.5 352.8 404.2
LCX (16) 6.7 61.9 160.0 294.4 375.1 LVX 2.0 19.4 64.0 100.1 106.3 AC 3.9 38.9 105.5 352.8 404.2
LVX 2.0 19.4 64.0 100.1 106.3 AC 3.9 38.9 105.5 352.8 404.2
AC 3.9 38.9 105.5 352.8 404.2
ACQ 5.4 52.3 139.5 206.0 218.5
VHC 3.1 30.8 103.0 180.7 192.1
HC 3.8 37.9 132.0 181.5 —
Bipolar
FAST 42.9 69.4 136.6 221.1 246.8
FASTr 38.6 58.0 94.5 198.2 232.4
ALS 14.1 41.0 126.7 240.2 393.8

Dynamic Current Consumption* (mA) TinyLogic Families

	10MHz	30MHz	50MHz	70MHz	90MHz	
CMOS						
ULP	0.31	0.81	1.18	1.58	1.98	2
ULP-A	0.56	1.52	2.37	3.16	4.07	
HS	0.31	0.93	1.53	_	_	-
UHS	0.86	2.59	4.25	5.91	7.56	
HST	0.29	0.88	1.48	_	_	

* '244 function, multiple outputs switching @ 50pF, C_{LOAD} All figures represent typical performance values.

Product Portfolio and Description

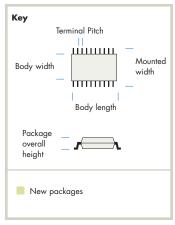
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BiCM																				
ABT		•	•	•	•				•							•	•	•		• High speed, high drive and low noise for superior system performance
LVT		•	•	•	•												•	•		• High-speed, high-drive logic for 3.3V applications
СМО	5																			
	VCX	•	•	•	•							•					•	•	**	 High-speed CMOS enables interoperability between 3.3V and 2.5V systems, with 3.6V-tolerant inputs and outputs
м.ДЛ	ALVC	•	•	•	•							•					•	•		Alternative to VCX
CROSSVOLT™	LCX	•	•	•	•		•			•		•	•				•	•	**	5V-tolerant inputs and outputs Ideal for 3.3V applications requiring balanced drive capability, high speed, and low noise
	LVX	•	•	•	•	•	•			•		•	•		•			•		 5V input tolerance allows 5V CMOS to interface with 3.3V systems. Includes specialized, dual-voltage translators and bus switch devices.
FACT	M AC/ACT	•	•	•	•	•	•	•	•	•	•	•	•					•		General-purpose/broad-portfolio ACMOS family
ACQ/	Quiet Series™ 'ACTQ	•	•	•	•				•			•				•	•	•		Family extension specifically designed for noise-sensitive applications. Proprietary circuitry guarantees low EMI and low device-generated noise.
(FST/FS	d Switch SA)						•					•	•		•		•	•	•	High-speed, high-impedance, low-resistance, undershoot-protected switches Low R _{ON} Analog Switches
VHC/	VHCT	•	•	•	•	•	•			•		•						•	**	The natural migration for HCMOS users who need more speed for their low-power, low-noise, low-drive applications Offered in fine-pitch packages
HC/H	СТ	•	•	•	•	•	•	•			•	•						•	**	Low CMOS device-generated noise and EMI available in the moderate-speed performance range Not recommended for new designs
74C		•		•	•	•	•			•		•						•		Application-specific, high-voltage CMOS products for high-noise environments
CD4K		•		•	•	•	•			•		•						•		• Standard high-voltage CMOS products for high-noise environments
	HS	•		•			•					•							•	General-purpose single-, dual- and triple-gate logic
gic®	HST											•							•	• TIL-compatible single-, dual- and triple-gate logic
TinyLogic®	UHS	•		•	•		•					•			•				•	 High-performance single- and dual-gate logic with 5V over-voltage tolerance on inputs and outputs
	ULP / ULP-A	•		•	•		•												•	Ultra-low power/voltage single-, dual- and triple-gate logic
FXL Tre	anslators													•			•	•	•	• Logic level translation within range 0.9V - 3.6V
GTLP		•	•										•							• Single-ended, open-drain transceiver technology for heavily loaded backplanes
Bipol	ar																			
FASTr1	тм	•	•	•	•									•			•	•		Fast TTL logic available A speed-improved, design-enhanced version of FAST®
FAST®		•	•	•	•	•	•	•	•	•	•	•		•				•		Optimal speed-to-power portfolio of Advanced Schottky TTL families
AS		•	•	•	•	•	•		•		•	•						•		A high-speed, high-drive TTL family Not recommended for new designs
ALS		•	•	•	•	•	•	•		•		•						•		Low-output noise and low power consumption for an advanced TTL logic family
ECL																				
F100k	Series	•	•	•	•	•	•		•	•		•	•					•		ECL with low power and excellent price/performance Socket replacement of F100K 100 Series
100EL Series	/ LVEL	•	•										•	•						1.0 - 2.0 GHZ Specified as EcLINPS™* replacement

^{*} Trademark of ON Semiconductor

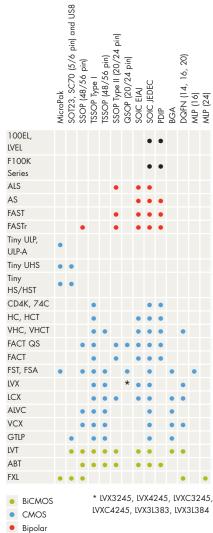
** See TinyLogic HS, UHS and ULP-A for 1-bit families with similar performance to HC, VHC, LCX and VCX.

Packaging

					Units: Milli	meters (Inches)		
Actual size		Package (Code)	Mounted width	Body width	Body length	Overall height	Terminal Pitch	Mounted Area
H	5	SOT23 (M5)	2.84 (0.112)	1.60 (0.063)	2.92 (0.115)	1.1 (0.043)	0.95 (0.037)	8.29 (0.012)
#	5/6	SC70 (P5) (P6)	2.10 (0.083)	1.25 (0.049)	2.0 (0.079)	0.90 (0.035)	0.65 (0.026)	4.20 (0.007)
B	6	MicroPak (XX)	1.0 (0.039)	1.0 (0.039)	1.45 (0.057)	0.55 (0.021)	0.50 (0.020)	1.45 (0.002)
	8	US8 (K8)	3.10 (0.122)	2.30 (0.09)	2.0 (0.079)	0.70 (0.027)	0.50 (0.020)	6.20 (0.009)
H	8	MicroPak (L8)	1.60 (0.062)	1.60 (0.062)	1.60 (0.062)	0.55 (0.021)	0.50 (0.020)	2.56 (0.003)
	10	MicroPak (L10)	1.60 (0.062)	1.60 (0.062)	2.10 (0.083)	0.55 (0.021)	0.50 (0.020)	3.36 (0.005)
	14	SOIC (M)	6.0 (0.231)	3.85 (0.153)	8.60 (0.340)	1.50 (0.061)	1.27 (0.050)	51.60 (0.078)
	14	TSSOP (MTC)	6.40 (0.252)	4.40 (0.173)	5.0 (0.197)	1.20 (0.047)	0.65 (0.026)	32.0 (0.050)
	14	DQFN (BQ)	2.5 (0.098)	2.5 (0.098)	3.0 (0.118)	0.80 (0.031)	0.50 (0.020)	7.50 (0.011)
	16	SOIC (M)	6.0 (0.231)	3.85 (0.153)	9.90 (0.390)	1.50 (0.061)	1.27 (0.050)	59.40 (0.090)
	16	TSSOP (MTC)	6.40 (0.252)	4.40 (0.173)	5.0 (0.197)	1.10 (0.043)	0.65 (0.026)	32.0 (0.050)
	16	QSOP (QSC)		1.35 (0.053)	4.90 (0.193)	1.60 (0.063)	0.63 (0.025)	29.35 (0.045)
	16	DQFN (BQ)		2.50 (0.098)	3.0 (0.118)	0.80 (0.031)	0.50 (0.020)	8.75 (0.013)
	16	MLP (MP)	3.0 (0.118)	3.0 (0.118)	3.0 (0.118)	1.0 (0.039)	0.50 (0.020)	9.0 (0.014)
	20	SOIC JEDEC (WM)	10.36 (0.408)	7.49 (0.295)	12.80 (0.504)	2.64 (0.104)	1.27 (0.050)	132.70 (0.206)
	20	TSSOP Type1 (MTC)	6.40 (0.252)	4.39 (0.173)	6.60 (0.260)	1.10 (0.104)	0.65 (0.025)	132.70 (0.206)
	20	SSOP Type II (MSA)	7.80 (0.307)	5.31 (0.209)	7.19 (0.283)	2.05 (0.081)	.065 (0.025)	56.08 (0.087)
	20	QSOP (QSC)	5.99 (0.236)	3.94 (0.155)	8.69 (0.342)	1.60 (0.063)	0.64 (0.025)	52.05 (0.087)
	20	DQFN (BQ)	2.5 (0.098)	2.5 (0.098)	4.50 (0.177)	0.80 (0.063)	0.50 (0.020)	11.25 (0.017)
	24	SOIC (WM)	10.30 (0.40)	7.50 (0.295)	15.40 (0.60)	2.50 (0.098)	1.27 (0.050)	158.62 (0.240)
	24	QSOP (QSC)	5.99 (0.236)	3.89 (0.153)	8.66 (0.341)	1.45 (0.057)	0.63 (0.025)	51.87 (0.080)
	24	TSSOP (MTC)	6.40 (0.252)	4.40 (0.173)	7.80 (0.307)	1.10 (0.043)	0.65 (0.026)	49.92 (0.077)
	24	MLP (MP)	3.50 (0.138)	3.50 (0.138)	4.50 (0.177)	0.80 (0.063)	0.50 (0.020)	15.75 (0.621)
	28	SOIC (WM)	10.30 (0.40)	7.49 (0.295)	18.10 (0.770)	2.5 (0.098)	1.27 (0.050)	186.43 (0.308)
	40	QVSOP (QSP)	6.0 (0.236)	3.90 (0.153)	9.90 (0.389)	2.0 (0.078)	0.50 (0.019)	59.40 (0.092)
	48	TSSOP (MTD)	8.10 (0.319)	6.10 (0.240)	12.50 (0.492)	1.10 (0.043)	0.50 (.020)	101.25 (0.157)
000000000000000000000000000000000000000	54	BGA54 (G)	8.0 (0.315)	8.0 (0.315)	5.50 (0.217)	1.40 (0.055)	0.80 (0.031)	44.0 (0.683)
	56	TSSOP (MTD)	8.10 (0.319)	6.10 (0.240)	14.0 (0.551)	1.10 (0.043)	0.50 (.020)	113.0 (0.175)
	80	QVSOP (QSP)	6.0 (0.236)	3.90 (0.153)	20.5 (0.807)	2.0 (0.078)	0.50 (0.019)	123.0 (0.190)
000000000000000000000000000000000000000	96	BGA96 (G)	5.50 (0.216)	5.50 (0.216)	13.50 (0.531)	1.40 (0.055)	0.80 (0.031)	74.25 (0.115)
000000000000000000000000000000000000000	114	BGA114 (G)	5.50 (0.216)	5.50 (0.216)	16.0 (0.630)	1.40 (0.055)	0.80 (0.031)	88.0 (0.136)



Package Availability



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