COMPARISON OF LOGIC FAMILIES USING NAND GATE

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Abstract

A digital circuit is constructed from small electronic circuits called logic gates that can be used to create combinational logic. A logic gate is an idealized or physical device which implements a Boolean function. It is an arrangement of electrically controlled switches, known as transistors. They are the fundamental building block for high performance data path circuits. The monolithic digital integrated circuit devices can be constructed using several different designs methods which use different logic families. In this paper different logic circuit families are compared. Power, delay and power-delay product are some of the performance parameters used for comparison.

Keywords- *CMOS, power, delay, power-delay product.*

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1 INTRODUCTION

A logic gate performs a logical operation on one or more logic inputs and produces a single logic output. Logic gates are primarily implemented using diodes or transistors but can also be constructed using electromagnetic relays, fluidic logic, pneumatic logic, or even mechanical elements. In the present work, NAND gate is implemented using RTL, DTL, TTL and CMOS structures.

2 LOGIC FAMILIES

2.1 RTL

RTL stands for Resistor Transistor Logic. In RTL logic, transistor is used in conjunction with resistors to create a logic circuit. The NPN transistor used in RTL logic acts as an inverter circuit. When high (Logic '1') input is applied at gate, then transistor turns 'ON' and low (logic 0') output is obtained. The RTL NAND gate is shown in figure 1.
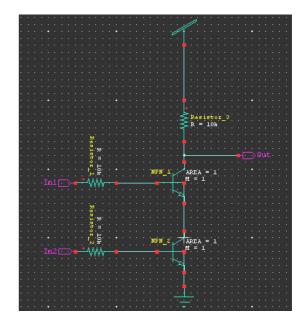

Fig. 1 RTL NAND gate

An RTL NAND gate circuit consists of two transistors Q1 and Q2 connected as shown in figure 1. When both of input In1 or In2 is driven high, corresponding transistor goes to saturation and output is pulled to low value. When both the inputs In1 and In2 are driven low, corresponding transistor goes to OFF state and output is pulled to high value.

2.2 DTL

DTL stands for Diode Transistor Logic. In DTL, the logic function is implemented using diodes and transistors. Each of the input is associated with one diode. Figure 2 shows DTL NAND logic circuit. Here diode acts as 'AND' circuit and is

connected to a transistor inverter which acts as 'NOT' circuit. According to inputs going high value, the corresponding diode conducts current, through the resistor. This turns 'ON' the transistor. The transistor act as short circuit and is grounded. At the output, low value is obtained. If input In1 and In2 are Low, the diodes do not conduct and thus output is at High value.
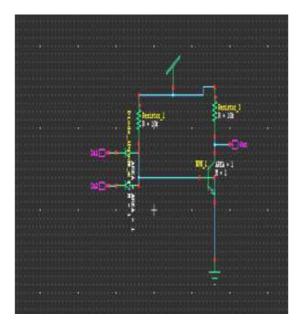

Fig. 2 DTL NAND gate

2.3 TTL

TTL stands for Transistor-Transistor Logic. Figure 3 shows the TTL NAND gate.
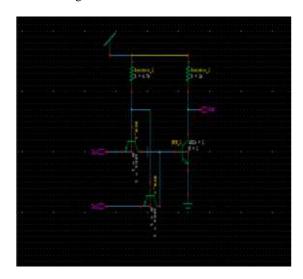

Fig. 3 TTL NAND gate

When one of the inputs is high, the output is high; otherwise, the output is low. When both inputs In1 and In2 are high, the two transistors on the left are in reverse active state. A current flows through the resistor through the base and collector of these transistors, and then through the base of the transistor on the right, saturating it and bringing the output down near ground When both inputs In1 and In2 are low, the easiest path to ground through the resistor is through the base of the transistors on the left to the inputs. This brings their collector voltages low enough so that very little current can flow through the base of the transistor on the right. This keeps that transistor off, bringing the output to high. When only one of the inputs is low, that input provides the easiest path to ground, through its corresponding transistor. This keeps the transistor on the right switched off.

2.4 CMOS

CMOS stands for complementary Metal Oxide Semiconductor. It uses complementary arrangements of N-channel and P-channel Field Effect Transistor. Since the initial devices used oxide-isolated metal gates, they are called CMOS. CMOS NAND gate is shown in figure 4.
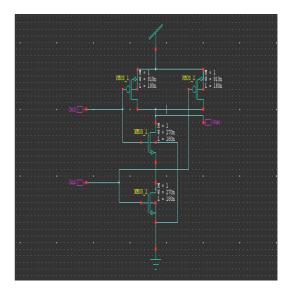

Fig. 4 CMOS NAND gate

3 RESULTS & DISSCUSSION

The output waveforms are shown in figure 5. The x axis shows the voltage level in volts and y axis shows time in seconds. The input voltage level is given by V(in1) and V(in2). The corresponding NAND logic output can be observed from V(out). Thus it can be seen that if both of the two inputs are at high logic level, the corresponding output shows logic '1' and if both the inputs are low, then output is at logic '1'. Simulations have been performed for RTL, DTL,

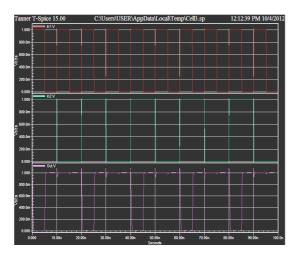TTL and CMOS NAND logic. The output waveform shown in fig 5 is of CMOS NAND logic.

Fig. 5 Output Waveforms

Table 1 shows the comparison between RTL, DTL, TTL and CMOS logic families. The simulation had been carried out at power supply voltage value of 3 V. Power, delay, and power-delay products are few of the performance parameters considered here for comparison between various logic families.

Table 1 Comparison of different logic families

length	Power	Delay	Power-Delay Product
RTL	4.43E-04	3.11E+01	1.38E-02
DTL	9.59E-04	7.69E+01	7.37E-02
TTL	3.59E-03	3.06E+01	1.10E-01
CMOS	4.62E-06	6.91E+01	3.19E-04

It can be observed from Table 1 that power dissipation in CMOS logic is least as compared to all the logic families. The power delay product which shows the figure of merit is least for CMOS technology and hence CMOS logic family outperforms all the logic families.

Figure 6 shows the graphical representation of power consumption in different logic families. It can be seen that TTL logic families consume highest power and minimum power dissipation is in CMOS logic family.
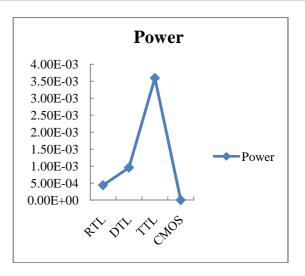

Fig. 6 Power dissipation in various logic families

Figure 7 shows the graphical representation of delay in different logic families. It is observed that DTL logic family has the maximum delay compared to CMOS logic family.
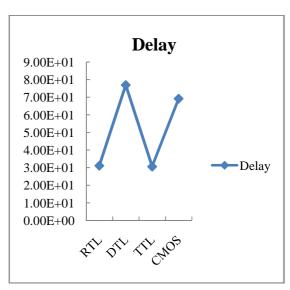

Fig. 7 Delay in various logic families

Figure 8 shows the graphical representation of power-delay product in different logic families. It can be seen that though delay in CMOS is high than TTL, but power-delay product of CMOS is minimum compared to other logic families. Thus overall performance of CMOS logic family is better in comparison with other logic families.
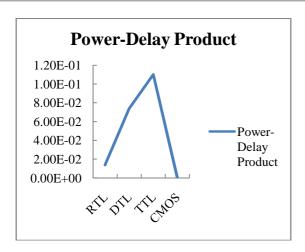
Fig. 8 Power dissipation product in various logic families

CONCLUSIONS

This paper provides comparison of different logic families in terms of power, delay and power-delay product. It has been observed that delay in CMOS logic family is high as compared to TTL logic family. The power consumption and power-delay product of CMOS logic families are minimum. Thus CMOS outperforms in performance parameters as compared to other logic families.

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