R/M \\ Mod	00	01	10	11
000	[AX]	[AX + Disp8]	[AX + Disp16]	Reg AL/AX
001	[BX]	[BX + Disp8]	[BX + Disp16]	Reg BL/BX
010	[CX]	[CX + Disp8]	[CX + Disp16]	Reg CL/CX
011	[DX]	[DX + Disp8]	[DX + Disp16]	Reg DL/DX
100	[EX]	[EX + Disp8]	[EX + Disp16]	Reg AH/EX
101	[FX]	[FX + Disp8]	[FX + Disp16]	Reg BH/FX
110	[SP]	[SP + Disp8]	[SP + Disp16]	Reg CH/SP
111	[BP]	[BP + Disp8]	[BP + Disp16]	Reg DH/BP
	[Reg16]	*[Reg16 + Disp8]*	*[Reg16 + Disp16]*	*Reg8/Reg16*
XXX	[Disp16]	Imm8	Imm16	[Disp8]

Mod	R/M	Reg
2 b	*3 b*	*3 b*

Mod	Meaning
00	Register indirect.
01	Register indirect with 8bit displacement.
10	Register indirect with 16bit displacement.
11	Register direct.

Reg defines the *src* or *dst* register.

Mod & R/M define the other *src* or *dst* register/memory location.

~~[Reg8]~~ ~~Load from zero page *(addr in reg8)*~~

[Disp8] Load from zero page *(addr in imm8)*

[Disp16] Load from anywhere *(addr in imm16)*

Imm8 Load immediate from *imm8*

Imm16 Load immediate from *imm16*

Address	8 Bit Op.	16 Bit Op.
000	AL	AX
001	BL	BX
010	CL	CX
011	DL	DX
100	AH	EX*
101	BH	FX*
110	CH	SP**
111	DH	BP**

*16 bit only register.
**Stack pointers.

Register		Use
AH	AL	*GP, Arguments, Returns*
BH	BL	*GP, Arguments*
CH	CL	*GP, Counters*
DH	DL	*GP*
EX		*GP*
FX		*GP, Relative data offset for PIC?*
SP		*Stack*
BP		*Stack*

Byte 1	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**		
Opcode + Mod		*D/W R/M*	*Displacement*		*Immediate*			
Instruction / Opcode (Bits)								
Any Opcode						*Mod*		
Byte 1			**Byte 2**					
Opcode			*Mod*	*Size + Direction*		*R/M*	*Reg*	
Byte 1	**Byte 2**	**Byte 3**	~~**Byte 4**~~	**Byte 5**	**Byte 6**	**Byte 7**	**Byte 8**	
Instruction / Opcode		*Mod R/M*	~~*SIB*~~	*Displacement*		*Immediate*		
Instruction / Opcode (Bits)								
Any Opcode						*Size*	*Direction*	
Byte 1			**Byte 2**				~~**Byte 3**~~	
Opcode	*Size*	*Direction*	*Mod*	*Reg*	*R/M*	~~*Scale*~~	~~*Index*~~	~~*Base*~~