Priority	Category	Name	Code	Range	Size	Addressing			X̄	Opcode	Instruction	Mo
Core	Data Transfer	Move	MOV	–	8	Register8	←	Register8	H	00 3 0	0 0 0 0 0 0	1 1
								Immediate8	M	04 1 0	0 0 0 0 0 1	0 1
					16	Register16	←	Register16	H	00 3 1	0 0 0 0 0 0	1 1
								Immediate16	M	04 2 1	0 0 0 0 0 1	1 0
Low				Zero Page	8	Register8	←	[Disp8]	H	04 3 0	0 0 0 0 0 1	1 1
							→	[Disp8]	M	04 3 2	0 0 0 0 0 1	1 1
					16	Register16	←	[Disp8]	H	04 3 1	0 0 0 0 0 1	1 1
							→	[Disp8]	H	04 3 3	0 0 0 0 0 1	1 1
Low					8	Immediate8	→	[Disp8]	M	0C 3 2	0 0 0 0 1 1	1 1
					16	Immediate16	→	[Disp8]	M	0C 3 3	0 0 0 0 1 1	1 1
Core				Near	8	Register8	←	[Disp16]	M	04 0 0	0 0 0 0 0 1	0 0
								[Reg16]	H	00 0 0	0 0 0 0 0 0	0 0
								[Reg16 + Disp8]	M	00 1 0	0 0 0 0 0 0	0 1
								[Reg16 + Disp16]	M	00 2 0	0 0 0 0 0 0	1 0
Core					16	Register16	←	[Disp16]	M	04 0 1	0 0 0 0 0 1	0 0
								[Reg16]	H	00 0 1	0 0 0 0 0 0	0 0
								[Reg16 + Disp8]	M	00 1 1	0 0 0 0 0 0	0 1
								[Reg16 + Disp16]	M	00 2 1	0 0 0 0 0 0	1 0
Med				Near	8	Immediate8	→	[Disp16]	M	0C 0 2	0 0 0 0 1 1	0 0
								[Reg16]	H	08 0 2	0 0 0 0 1 0	0 0
								[Reg16 + Disp8]	M	08 1 2	0 0 0 0 1 0	0 1
								[Reg16 + Disp16]	M	08 2 2	0 0 0 0 1 0	1 0
Core						Register8	→	[Disp16]	M	04 0 2	0 0 0 0 0 1	0 0
								[Reg16]	H	00 0 2	0 0 0 0 0 0	0 0
								[Reg16 + Disp8]	M	00 1 2	0 0 0 0 0 0	0 1
								[Reg16 + Disp16]	M	00 2 2	0 0 0 0 0 0	1 0
Med					16	Immediate16	→	[Disp16]	M	0C 0 3	0 0 0 0 1 1	0 0
								[Reg16]	M	08 0 3	0 0 0 0 1 0	0 0
								[Reg16 + Disp8]	M	08 1 3	0 0 0 0 1 0	0 1
								[Reg16 + Disp16]	M	08 2 3	0 0 0 0 1 0	1 0
Core						Register16	→	[Disp16]	M	04 0 3	0 0 0 0 0 1	0 0
								[Reg16]	H	00 0 3	0 0 0 0 0 0	0 0
								[Reg16 + Disp8]	M	00 1 3	0 0 0 0 0 0	0 1
								[Reg16 + Disp16]	M	00 2 3	0 0 0 0 0 0	1 0
Low		Move Flags	LDRF	–	8	Flags8	←	Register8	N	0C 1 0	0 0 0 0 1 1	0 1
					16	Flags16	←	Register16	N	0C 1 1	0 0 0 0 1 1	0 1
			STRF	–	8	Flags8	→	Register8	N	0C 1 2	0 0 0 0 1 1	0 1
					16	Flags16	→	Register16	N	0C 1 3	0 0 0 0 1 1	0 1
Med		Exchange	XCHG	–	8	Register8	↔	Register8	N	00 3 2	0 0 0 0 0 0	1 1
					16	Register16	↔	Register16	N	00 3 3	0 0 0 0 0 0	1 1
Core		Push	PUSH	–	8			Register8	H	20 3 2	0 0 1 0 0 0	1 1
								Immediate8	L	14 0 X	0 0 0 1 0 1	0 0
					16			Register16	H	20 3 3	0 0 1 0 0 0	1 1
								Immediate16	L	14 1 X	0 0 0 1 0 1	0 1
				Zero Page	8			[Disp8]	L	18 0 X	0 0 0 1 1 0	0 0
					16			[Disp8]	L	18 1 X	0 0 0 1 1 0	0 1
					8	Stack16	←	[Disp16]	M	18 2 X	0 0 0 1 1 0	1 0
								[Reg16]	M	20 0 2	0 0 1 0 0 0	0 0
				Near				[Reg16 + Disp8]	M	20 1 2	0 0 1 0 0 0	0 1
								[Reg16 + Disp16]	M	20 2 2	0 0 1 0 0 0	1 0
					16			[Disp16]	M	18 3 X	0 0 0 1 1 0	1 1
								[Reg16]	M	20 0 3	0 0 1 0 0 0	0 0
								[Reg16 + Disp8]	M	20 1 3	0 0 1 0 0 0	0 1
								[Reg16 + Disp16]	M	20 2 3	0 0 1 0 0 0	1 0
			PUSHF	–	16	Stack16	←	Flags16	L	14 2 3	0 0 0 1 0 1	1 0
Core		Pop	POP	–	8			Register8	H	20 3 0	0 0 1 0 0 0	1 1
					16			Register16	H	20 3 1	0 0 1 0 0 0	1 1
				Zero Page	8			[Disp8]	L	1C 0 X	0 0 0 1 1 1	0 0
					16			[Disp8]	L	1C 1 X	0 0 0 1 1 1	0 1
					8	Stack16	→	[Disp16]	M	1C 2 X	0 0 0 1 1 1	1 0
								[Reg16]	M	20 0 0	0 0 1 0 0 0	0 0
				Near				[Reg16 + Disp8]	M	20 1 0	0 0 1 0 0 0	0 1
								[Reg16 + Disp16]	M	20 2 0	0 0 1 0 0 0	1 0
					16			[Disp16]	M	1C 3 X	0 0 0 1 1 1	1 1
								[Reg16]	M	20 0 1	0 0 1 0 0 0	0 0
								[Reg16 + Disp8]	M	20 1 1	0 0 1 0 0 0	0 1
								[Reg16 + Disp16]	M	20 2 1	0 0 1 0 0 0	1 0

Priority	Instruction	Mnemonic	Range	Size	Operand1	Dir	Operand2	Flag	Code									
		POPF	–	16	Stack16	→	Flags16	L	14 2 1	0	0	0	1	0	1	1	0
High	In	IN	Near	8	Register8	←	Port(Disp8)	N	DC 1 X	1	1	0	1	1	1	0	1
High				16	Register16	←	Port(Disp8)	N	DC 2 X	1	1	0	1	1	1	1	0
High	Out	OUT	Near	8	Register8	→	Port(Disp8)	N	EC 1 X	1	1	1	0	1	1	0	1
High				16	Register16	→	Port(Disp8)	N	EC 2 X	1	1	1	0	1	1	1	0
Low	Load Effective Address	LEA	Short	8	Register8	←	Reg8 + Disp8	L	08 2 0	0	0	0	0	1	0	1	0
Low			Near	16	Register16	←	Reg16 + Disp8	L	08 1 0	0	0	0	0	1	0	0	1
						←	Reg16 + Disp16	L	08 2 1	0	0	0	0	1	0	1	0
Low	Sign Extend	CBW	–	8	Register8			N	24 3 0	0	0	1	0	0	1	1	1
High	Add	ADD	Zero Page	8	Register8	←+	[Disp8]	H	84 3 0	1	0	0	0	0	1	1	1
						+→	[Disp8]	M	84 3 2	1	0	0	0	0	1	1	1
Med				16	Register16	←+	[Disp8]	H	84 3 1	1	0	0	0	0	1	1	1
Med						+→	[Disp8]	H	84 3 3	1	0	0	0	0	1	1	1
				8	Immediate8	+→	[Disp8]	M	8C 3 2	1	0	0	0	1	1	1	1
				16	Immediate16	+→	[Disp8]	M	8C 3 3	1	0	0	0	1	1	1	1
Core			Near	8	Register8	←+	Immediate8	M	84 1 0	1	0	0	0	0	1	0	1
							Register8	M	80 3 0	1	0	0	0	0	0	1	1
							[Disp16]	M	84 0 0	1	0	0	0	0	1	0	0
							[Reg16]	H	80 0 0	1	0	0	0	0	0	0	0
							[Reg16 + Disp8]	M	80 1 0	1	0	0	0	0	0	0	1
High							[Reg16 + Disp16]	H	80 2 0	1	0	0	0	0	0	1	0
					Register8	+→	[Disp16]	M	84 0 2	1	0	0	0	0	1	0	0
							[Reg16]	M	80 0 2	0	0	0	0	0	1	1	1
							[Reg16 + Disp8]	M	80 1 2	1	0	0	0	0	0	0	1
							[Reg16 + Disp16]	M	80 2 2	1	0	0	0	0	0	1	0
					Immediate8	+→	[Disp16]	L	8C 0 2	1	0	0	0	1	1	0	0
							[Reg16]	L	88 0 2	1	0	0	0	1	0	0	0
							[Reg16 + Disp8]	L	88 1 2	1	0	0	0	1	0	0	1
							[Reg16 + Disp16]	L	88 2 2	1	0	0	0	1	0	1	0
Med				16	Register16	←+	Immediate16	M	84 2 1	1	0	0	0	0	1	1	0
							Register16	M	80 3 1	1	0	0	0	0	0	1	1
							[Disp16]	M	84 0 1	1	0	0	0	0	1	0	0
							[Reg16]	H	80 0 1	1	0	0	0	0	0	0	0
							[Reg16 + Disp8]	M	80 1 1	1	0	0	0	0	0	0	1
							[Reg16 + Disp16]	H	80 2 1	1	0	0	0	0	0	1	0
					Register16	+→	[Disp16]	M	84 0 3	1	0	0	0	0	1	0	0
							[Reg16]	M	80 0 3	1	0	0	0	0	0	0	0
							[Reg16 + Disp8]	M	80 1 3	1	0	0	0	0	0	0	1
							[Reg16 + Disp16]	M	80 2 3	1	0	0	0	0	0	1	0
					Immediate16	+→	[Disp16]	L	8C 0 3	1	0	0	0	1	1	0	0
							[Reg16]	L	88 0 3	1	0	0	0	1	0	0	0
							[Reg16 + Disp8]	L	88 1 3	1	0	0	0	1	0	0	1
							[Reg16 + Disp16]	L	88 2 3	1	0	0	0	1	0	1	0
High			Zero Page	8	Register8	←+	[Disp8]	M	94 3 0	1	0	0	1	0	1	1	1
						+→	[Disp8]	M	94 3 2	1	0	0	1	0	1	1	1
Med				16	Register16	←+	[Disp8]	M	94 3 1	1	0	0	1	0	1	1	1
Med						+→	[Disp8]	M	94 3 3	1	0	0	1	0	1	1	1
				8	Immediate8	+→	[Disp8]	M	9C 3 2	1	0	0	1	1	1	1	1
				16	Immediate16	+→	[Disp8]	M	9C 3 3	1	0	0	1	1	1	1	1
Core			Near	8	Register8	←+	Immediate8	L	94 1 0	1	0	0	1	0	1	0	1
							Register8	L	90 3 0	1	0	0	1	0	0	1	1
							[Disp16]	L	94 0 0	1	0	0	1	0	1	0	0
							[Reg16]	M	90 0 0	1	0	0	1	0	0	0	0
							[Reg16 + Disp8]	L	90 1 0	1	0	0	1	0	0	0	1
							[Reg16 + Disp16]	M	90 2 0	1	0	0	1	0	0	1	0
					Register8	+→	[Disp16]	L	94 0 2	1	0	0	1	0	1	0	0
							[Reg16]	L	90 0 2	1	0	0	1	0	0	0	0
							[Reg16 + Disp8]	L	90 1 2	1	0	0	1	0	0	0	1
High							[Reg16 + Disp16]	L	90 2 2	1	0	0	1	0	0	1	0
	Add with Carry	ADC			Immediate8	+→	[Disp16]	L	9C 0 2	1	0	0	1	1	1	0	0
							[Reg16]	L	98 0 2	1	0	0	1	1	0	0	0
							[Reg16 + Disp8]	L	98 1 2	1	0	0	1	1	0	0	1
			Near				[Reg16 + Disp16]	L	98 2 2	1	0	0	1	1	0	1	0
					Register16	←+	Immediate16	L	94 2 1	1	0	0	1	0	1	1	0
							Register16	L	90 3 1	1	0	0	1	0	0	1	1
							[Disp16]	L	94 0 1	1	0	0	1	0	1	0	0
							[Reg16]	M	90 0 1	1	0	0	1	0	0	0	0

Speed	Category	Operation	Mnemonic	Mode	Size	Operand	Dir	Addressing	X	Code								
Med					16			[Reg16 + Disp8]	L	90 1 1	1	0	0	1	0	0	0	1
								[Reg16 + Disp16]	M	90 2 1	1	0	0	1	0	0	1	0
						Register16	+→	[Disp16]	L	94 0 3	1	0	0	1	0	1	0	0
								[Reg16]	L	90 0 3	1	0	0	1	0	0	0	0
								[Reg16 + Disp8]	L	90 1 3	1	0	0	1	0	0	0	1
								[Reg16 + Disp16]	L	90 2 3	1	0	0	1	0	0	1	0
						Immediate16	+→	[Disp16]	L	9C 0 3	1	0	0	1	1	1	0	0
								[Reg16]	L	98 0 3	1	0	0	1	1	0	0	0
								[Reg16 + Disp8]	L	98 1 3	1	0	0	1	1	0	0	1
								[Reg16 + Disp16]	L	98 2 3	1	0	0	1	1	0	1	0
High		Subtract	SUB	Zero Page	8	Register8	←-	[Disp8]	H	44 3 0	0	1	0	0	0	1	1	1
							-→	[Disp8]	M	44 3 2	0	1	0	0	0	1	1	1
Med					16	Register16	←-	[Disp8]	H	44 3 1	0	1	0	0	0	1	1	1
Med							-→	[Disp8]	H	44 3 3	0	1	0	0	0	1	1	1
					8	Immediate8	-→	[Disp8]	M	4C 3 2	0	1	0	0	1	1	1	1
					16	Immediate16	-→	[Disp8]	M	4C 3 3	0	1	0	0	1	1	1	1
Core				Near	8	Register8	←-	Immediate8	L	44 1 0	0	1	0	0	0	1	0	1
								Register8	L	40 3 0	0	1	0	0	0	0	1	1
								[Disp16]	L	44 0 0	0	1	0	0	0	1	0	0
								[Reg16]	M	40 0 0	0	1	0	0	0	0	0	0
High								[Reg16 + Disp8]	L	40 1 0	0	1	0	0	0	0	0	1
								[Reg16 + Disp16]	M	40 2 0	0	1	0	0	0	0	1	0
						Register8	-→	[Disp16]	L	44 0 2	0	1	0	0	0	1	0	0
								[Reg16]	L	40 0 2	0	1	0	0	0	0	0	0
								[Reg16 + Disp8]	L	40 1 2	0	1	0	0	0	0	0	1
								[Reg16 + Disp16]	L	40 2 2	0	1	0	0	0	0	1	0
						Immediate8	-→	[Disp16]	L	4C 0 2	0	1	0	0	1	1	0	0
								[Reg16]	L	48 0 2	0	1	0	0	1	0	0	0
								[Reg16 + Disp8]	L	48 1 2	0	1	0	0	1	0	0	1
								[Reg16 + Disp16]	L	48 2 2	0	1	0	0	1	0	1	0
Med	Arithmetic				16	Register16	←-	Immediate16	L	44 2 1	0	1	0	0	0	1	1	0
								Register16	L	40 3 1	0	1	0	0	0	0	1	1
								[Disp16]	L	44 0 1	0	1	0	0	0	1	0	0
								[Reg16]	M	40 0 1	0	1	0	0	0	0	0	0
								[Reg16 + Disp8]	L	40 1 1	0	1	0	0	0	0	0	1
								[Reg16 + Disp16]	M	40 2 1	0	1	0	0	0	0	1	0
						Register16	-→	[Disp16]	L	44 0 3	0	1	0	0	0	1	0	0
								[Reg16]	L	40 0 3	0	1	0	0	0	0	0	0
								[Reg16 + Disp8]	L	40 1 3	0	1	0	0	0	0	0	1
								[Reg16 + Disp16]	L	40 2 3	0	1	0	0	0	0	1	0
						Immediate16	-→	[Disp16]	L	4C 0 3	0	1	0	0	1	1	0	0
								[Reg16]	L	48 0 3	0	1	0	0	1	0	0	0
								[Reg16 + Disp8]	L	48 1 3	0	1	0	0	1	0	0	1
								[Reg16 + Disp16]	L	48 2 3	0	1	0	0	1	0	1	0
High		Subtract with Borrow	SBB	Zero Page	8	Register8	←-	[Disp8]	M	54 3 0	0	1	0	1	0	1	1	1
							-→	[Disp8]	M	54 3 2	0	1	0	1	0	1	1	1
Med					16	Register16	←-	[Disp8]	M	54 3 1	0	1	0	1	0	1	1	1
Med							-→	[Disp8]	M	54 3 3	0	1	0	1	0	1	1	1
					8	Immediate8	-→	[Disp8]	M	5C 3 2	0	1	0	1	1	1	1	1
					16	Immediate16	-→	[Disp8]	M	5C 3 3	0	1	0	1	1	1	1	1
Core				Near	8	Register8	←-	Immediate8	L	54 1 0	0	1	0	1	0	1	0	1
								Register8	L	50 3 0	0	1	0	1	0	0	1	1
								[Disp16]	L	54 0 0	0	1	0	1	0	1	0	0
								[Reg16]	M	50 0 0	0	1	0	1	0	0	0	0
								[Reg16 + Disp8]	L	50 1 0	0	1	0	1	0	0	0	1
								[Reg16 + Disp16]	M	50 2 0	0	1	0	1	0	0	1	0
High					8	Register8	-→	[Disp16]	L	54 0 2	0	1	0	1	0	1	0	0
								[Reg16]	L	50 0 2	0	1	0	1	0	0	0	0
								[Reg16 + Disp8]	L	50 1 2	0	1	0	1	0	0	0	1
								[Reg16 + Disp16]	L	50 2 2	0	1	0	1	0	0	1	0
						Immediate8	-→	[Disp16]	L	5C 0 2	0	1	0	1	1	1	0	0
								[Reg16]	L	58 0 2	0	1	0	1	1	0	0	0
								[Reg16 + Disp8]	L	58 1 2	0	1	0	1	1	0	0	1
								[Reg16 + Disp16]	L	58 2 2	0	1	0	1	1	0	1	0
					16	Register16	←-	Immediate16	L	54 2 1	0	1	0	1	0	1	1	0
								Register16	L	50 3 1	0	1	0	1	0	0	1	1
								[Disp16]	L	54 0 1	0	1	0	1	0	1	0	0
								[Reg16]	M	50 0 1	0	1	0	1	0	0	0	0

Tier	Name	Mnem.	Mode	Size	Operand	Dir	Operand 2	Flag	Code	Bits
Med				16	Register16	-→	[Reg16 + Disp8]	L	50 1 1	0 1 0 1 0 0 0 1
							[Reg16 + Disp16]	M	50 2 1	0 1 0 1 0 0 1 0
							[Disp16]	L	54 0 3	0 1 0 1 0 1 0 0
							[Reg16]	L	50 0 3	0 1 0 1 0 0 0 0
							[Reg16 + Disp8]	L	50 1 3	0 1 0 1 0 0 0 1
							[Reg16 + Disp16]	L	50 2 3	0 1 0 1 0 0 1 0
					Immediate16	-→	[Disp16]	L	5C 0 3	0 1 0 1 1 1 0 0
							[Reg16]	L	58 0 3	0 1 0 1 1 0 0 0
							[Reg16 + Disp8]	L	58 1 3	0 1 0 1 1 0 0 1
							[Reg16 + Disp16]	L	58 2 3	0 1 0 1 1 0 1 0
Med	Increment	INC	Zero Page	8			[Disp8]	L	20 0 X	0 0 1 0 0 0 0 0
				16			[Disp8]	L	20 1 X	0 0 1 0 0 0 0 1
High			Near	8			Register8	M	24 3 0	0 0 1 0 0 1 1 1
Med							[Disp16]	L	20 2 X	0 0 1 0 0 0 1 0
							[Reg16]	L	24 0 0	0 0 1 0 0 1 0 0
							[Reg16 + Disp8]	L	24 1 0	0 0 1 0 0 1 0 1
							[Reg16 + Disp16]	L	24 2 0	0 0 1 0 0 1 1 0
Med				16			Register16	M	24 3 1	0 0 1 0 0 1 1 1
							[Disp16]	L	20 3 X	0 0 1 0 0 0 1 1
							[Reg16]	L	24 0 1	0 0 1 0 0 1 0 0
							[Reg16 + Disp8]	L	24 1 1	0 0 1 0 0 1 0 1
							[Reg16 + Disp16]	L	24 2 1	0 0 1 0 0 1 1 0
Med	Decrement	DEC	Zero Page	8			[Disp8]	L	C0 0 X	1 1 0 0 0 0 0 0
				16			[Disp8]	L	C0 1 X	1 1 0 0 0 0 0 1
High			Near	8			Register8	L	C4 3 0	1 1 0 0 0 1 1 1
Med							[Disp16]	N	C0 2 X	1 1 0 0 0 0 1 0
							[Reg16]	N	C4 0 0	1 1 0 0 0 1 0 0
							[Reg16 + Disp8]	N	C4 1 0	1 1 0 0 0 1 0 1
							[Reg16 + Disp16]	N	C4 2 0	1 1 0 0 0 1 1 0
Med				16			Register16	L	C4 3 1	1 1 0 0 0 1 1 1
							[Disp16]	N	C0 3 X	1 1 0 0 0 0 1 1
							[Reg16]	N	C4 0 1	1 1 0 0 0 1 0 0
							[Reg16 + Disp8]	N	C4 1 1	1 1 0 0 0 1 0 1
							[Reg16 + Disp16]	N	C4 2 1	1 1 0 0 0 1 1 0
Med	Negate	NEG	Zero Page	8			[Disp8]	N	30 0 X	0 0 1 1 0 0 0 0
				16			[Disp8]	N	30 1 X	0 0 1 1 0 0 0 1
High			Near	8			Register8	L	34 3 0	0 0 1 1 0 1 1 1
Med							[Disp16]	N	30 2 X	0 0 1 1 0 0 1 0
							[Reg16]	N	34 0 0	0 0 1 1 0 1 0 0
							[Reg16 + Disp8]	N	34 1 0	0 0 1 1 0 1 0 1
							[Reg16 + Disp16]	N	34 2 0	0 0 1 1 0 1 1 0
Med				16			Register16	L	34 3 1	0 0 1 1 0 1 1 1
							[Disp16]	N	30 3 X	0 0 1 1 0 0 1 1
							[Reg16]	N	34 0 1	0 0 1 1 0 1 0 0
							[Reg16 + Disp8]	N	34 1 1	0 0 1 1 0 1 0 1
							[Reg16 + Disp16]	N	34 2 1	0 0 1 1 0 1 1 0
High	Compare	CMP	Zero Page	8	Register8	←-	[Disp8]	M	64 3 0	0 1 1 0 0 1 1 1
						-→	[Disp8]	M	64 3 2	0 1 1 0 0 1 1 1
Med				16	Register16	←-	[Disp8]	M	64 3 1	0 1 1 0 0 1 1 1
						-→	[Disp8]	M	64 3 3	0 1 1 0 0 1 1 1
Med				8	Immediate8	-→	[Disp8]	M	6C 3 2	0 1 1 0 1 1 1 1
				16	Immediate16	-→	[Disp8]	M	6C 3 3	0 1 1 0 1 1 1 1
Core			Near	8	Register8	←-	Immediate8	M	64 1 0	0 1 1 0 0 1 0 1
							Register8	M	60 3 0	0 1 1 0 0 0 1 1
							[Disp16]	M	64 0 0	0 1 1 0 0 1 0 0
							[Reg16]	H	60 0 0	0 1 1 0 0 0 0 0
							[Reg16 + Disp8]	M	60 1 0	0 1 1 0 0 0 0 1
							[Reg16 + Disp16]	H	60 2 0	0 1 1 0 0 0 1 0
High					Register8	-→	[Disp16]	M	64 0 2	0 1 1 0 0 1 0 0
							[Reg16]	M	60 0 2	0 1 1 0 0 0 0 0
							[Reg16 + Disp8]	M	60 1 2	0 1 1 0 0 0 0 1
							[Reg16 + Disp16]	M	60 2 2	0 1 1 0 0 0 1 0
					Immediate8	-→	[Disp16]	L	6C 0 2	0 1 1 0 1 1 0 0
							[Reg16]	L	68 0 2	0 1 1 0 1 0 0 0
							[Reg16 + Disp8]	L	68 1 2	0 1 1 0 1 0 0 1
							[Reg16 + Disp16]	L	68 2 2	0 1 1 0 1 0 1 0
							Immediate16	M	64 2 1	0 1 1 0 0 1 1 0
							Register16	M	60 3 1	0 1 1 0 0 0 1 1

Category	Mnemonic	MNEMONIC	Mode	Size	Operand	Dir	Address	Flag	Hex	b7	b6	b5	b4	b3	b2	b1	b0
Med				16	Register16	←-	[Disp16]	M	64 0 1	0	1	1	0	0	1	0	0
							[Reg16]	H	60 0 1	0	1	1	0	0	0	0	0
							[Reg16 + Disp8]	M	60 1 1	0	1	1	0	0	0	0	1
							[Reg16 + Disp16]	H	60 2 1	0	1	1	0	0	0	1	0
					Register16	-→	[Disp16]	M	64 0 3	0	1	1	0	0	1	0	0
							[Reg16]	M	60 0 3	0	1	1	0	0	0	0	0
							[Reg16 + Disp8]	M	60 1 3	0	1	1	0	0	0	0	1
							[Reg16 + Disp16]	M	60 2 3	0	1	1	0	0	0	1	0
					Immediate16	-→	[Disp16]	L	6C 03	0	1	1	0	1	1	0	0
							[Reg16]	L	68 0 3	0	1	1	0	1	0	0	0
							[Reg16 + Disp8]	L	68 1 3	0	1	1	0	1	0	0	1
							[Reg16 + Disp16]	L	68 2 3	0	1	1	0	1	0	1	0
High	And	AND	Zero Page	8	Register8	←	[Disp8]	M	A4 3 0	1	0	1	0	0	1	1	1
						→	[Disp8]	M	A4 3 2	1	0	1	0	0	1	1	1
Med					Register16	←	[Disp8]	M	A4 3 1	1	0	1	0	0	1	1	1
						→	[Disp8]	M	A4 3 3	1	0	1	0	0	1	1	1
Med					Immediate8	→	[Disp8]	M	AC 3 2	1	0	1	0	1	1	1	1
					Immediate16	→	[Disp8]	M	AC 3 3	1	0	1	0	1	1	1	1
Core			Near	8	Register8	←	Immediate8	L	A4 1 0	1	0	1	0	0	1	0	1
							Register8	L	A0 3 0	1	0	1	0	0	0	1	1
							[Disp16]	L	A4 0 0	1	0	1	0	0	1	0	0
							[Reg16]	M	A0 0 0	1	0	1	0	0	0	0	0
							[Reg16 + Disp8]	L	A0 1 0	1	0	1	0	0	0	0	1
							[Reg16 + Disp16]	M	A0 2 0	1	0	1	0	0	0	1	0
High					Register8	→	[Disp16]	L	A4 0 2	1	0	1	0	0	1	0	0
							[Reg16]	L	A0 0 2	1	0	1	0	0	0	0	0
							[Reg16 + Disp8]	L	A0 1 2	1	0	1	0	0	0	0	1
							[Reg16 + Disp16]	L	A0 2 2	1	0	1	0	0	0	1	0
					Immediate8	→	[Disp16]	L	AC 0 2	1	0	1	0	1	1	0	0
							[Reg16]	L	A8 0 2	1	0	1	0	1	0	0	0
							[Reg16 + Disp8]	L	A8 1 2	1	0	1	0	1	0	0	1
							[Reg16 + Disp16]	L	A8 2 2	1	0	1	0	1	0	1	0
Med				16	Register16	←	Immediate16	L	A4 2 1	1	0	1	0	0	1	1	0
							Register16	L	A0 3 1	1	0	1	0	0	0	1	1
							[Disp16]	L	A4 0 1	1	0	1	0	0	1	0	0
							[Reg16]	M	A0 0 1	1	0	1	0	0	0	0	0
							[Reg16 + Disp8]	L	A0 1 1	1	0	1	0	0	0	0	1
							[Reg16 + Disp16]	M	A0 2 1	1	0	1	0	0	0	1	0
					Register16	→	[Disp16]	L	A4 0 3	1	0	1	0	0	1	0	0
							[Reg16]	L	A0 0 3	1	0	1	0	0	0	0	0
							[Reg16 + Disp8]	L	A0 1 3	1	0	1	0	0	0	0	1
							[Reg16 + Disp16]	L	A0 2 3	1	0	1	0	0	0	1	0
					Immediate16	→	[Disp16]	L	AC 0 3	1	0	1	0	1	1	0	0
							[Reg16]	L	A8 0 3	1	0	1	0	1	0	0	0
							[Reg16 + Disp8]	L	A8 1 3	1	0	1	0	1	0	0	1
							[Reg16 + Disp16]	L	A8 2 3	1	0	1	0	1	0	1	0
High			Zero Page	8	Register8	←	[Disp8]	M	D4 3 0	1	1	0	1	0	1	1	1
						→	[Disp8]	M	D4 3 2	1	1	0	1	0	1	1	1
Med					Register16	←	[Disp8]	M	D4 3 1	1	1	0	1	0	1	1	1
						→	[Disp8]	M	D4 3 3	1	1	0	1	0	1	1	1
Med					Immediate8	→	[Disp8]	M	DC 3 2	1	1	0	1	1	1	1	1
					Immediate16	→	[Disp8]	M	DC 3 3	1	1	0	1	1	1	1	1
Core				8	Register8	←	Immediate8	L	D4 1 0	1	1	0	1	0	1	0	1
							Register8	L	D0 3 0	1	1	0	1	0	0	1	1
							[Disp16]	L	D4 0 0	1	1	0	1	0	1	0	0
							[Reg16]	M	D0 0 0	1	1	0	1	0	0	0	0
							[Reg16 + Disp8]	L	D0 1 0	1	1	0	1	0	0	0	1
							[Reg16 + Disp16]	M	D0 2 0	1	1	0	1	0	0	1	0
High					Register8	→	[Disp16]	L	D4 0 2	1	1	0	1	0	1	0	0
							[Reg16]	L	D0 0 2	1	1	0	1	0	0	0	0
							[Reg16 + Disp8]	L	D0 1 2	1	1	0	1	0	0	0	1
							[Reg16 + Disp16]	L	D0 2 2	1	1	0	1	0	0	1	0
	Or	OR			Immediate8	→	[Disp16]	L	DC 0 2	1	1	0	1	1	1	0	0
							[Reg16]	L	D8 0 2	1	1	0	1	1	0	0	0
							[Reg16 + Disp8]	L	D8 1 2	1	1	0	1	1	0	0	1
							[Reg16 + Disp16]	L	D8 2 2	1	1	0	1	1	0	1	0
			Near				Immediate16	L	D4 2 1	1	1	0	1	0	1	1	0
							Register16	L	D0 3 1	1	1	0	1	0	0	1	1

Cat		Operation		AddrMode	Size	Operand1	Dir	Operand2		Code	b7	b6	b5	b4	b3	b2	b1	b0
Med	Logic				16	Register16	←	[Disp16]	L	D4 0 1	1	1	0	1	0	1	0	0
								[Reg16]	M	D0 0 1	1	1	0	1	0	0	0	0
								[Reg16 + Disp8]	L	D0 1 1	1	1	0	1	0	0	0	1
								[Reg16 + Disp16]	M	D0 2 1	1	1	0	1	0	0	1	0
						Register16	→	[Disp16]	L	D4 0 3	1	1	0	1	0	1	0	0
								[Reg16]	L	D0 0 3	1	1	0	1	0	0	0	0
								[Reg16 + Disp8]	L	D0 1 3	1	1	0	1	0	0	0	1
								[Reg16 + Disp16]	L	D0 2 3	1	1	0	1	0	0	1	0
						Immediate16	→	[Disp16]	L	DC 0 3	1	1	0	1	1	1	0	0
								[Reg16]	L	D8 0 3	1	1	0	1	1	0	0	0
								[Reg16 + Disp8]	L	D8 1 3	1	1	0	1	1	0	0	1
								[Reg16 + Disp16]	L	D8 2 3	1	1	0	1	1	0	1	0
High		Exclusive Or	XOR	Zero Page	8	Register8	←	[Disp8]	H	74 3 0	0	1	1	1	0	1	1	1
							→	[Disp8]	M	74 3 2	0	1	1	1	0	1	1	1
Med						Register16	←	[Disp8]	H	74 3 1	0	1	1	1	0	1	1	1
Med							→	[Disp8]	H	74 3 3	0	1	1	1	0	1	1	1
						Immediate8	→	[Disp8]	M	7C 3 2	0	1	1	1	1	1	1	1
Core						Immediate16	→	[Disp8]	M	7C 3 3	0	1	1	1	1	1	1	1
				Near	8	Register8	←	Immediate8	M	74 1 0	0	1	1	1	0	1	0	1
								Register8	M	70 3 0	0	1	1	1	0	0	1	1
								[Disp16]	M	74 0 0	0	1	1	1	0	1	0	0
High								[Reg16]	H	70 0 0	0	1	1	1	0	0	0	0
								[Reg16 + Disp8]	M	70 1 0	0	1	1	1	0	0	0	1
								[Reg16 + Disp16]	H	70 2 0	0	1	1	1	0	0	1	0
						Register8	→	[Disp16]	M	74 0 2	0	1	1	1	0	1	0	0
								[Reg16]	M	70 0 2	0	1	1	1	0	0	0	0
								[Reg16 + Disp8]	M	70 1 2	0	1	1	1	0	0	0	1
								[Reg16 + Disp16]	M	70 2 2	0	1	1	1	0	0	1	0
						Immediate8	→	[Disp16]	L	7C 0 2	0	1	1	1	1	1	0	0
								[Reg16]	L	78 0 2	0	1	1	1	1	0	0	0
								[Reg16 + Disp8]	L	78 1 2	0	1	1	1	1	0	0	1
								[Reg16 + Disp16]	L	78 2 2	0	1	1	1	1	0	1	0
					16	Register16	←	Immediate16	M	74 2 1	0	1	1	1	0	1	1	0
								Register16	M	70 3 1	0	1	1	1	0	0	1	1
								[Disp16]	M	74 0 1	0	1	1	1	0	1	0	0
								[Reg16]	H	70 0 1	0	1	1	1	0	0	0	0
								[Reg16 + Disp8]	M	70 1 1	0	1	1	1	0	0	0	1
								[Reg16 + Disp16]	H	70 2 1	0	1	1	1	0	0	1	0
Med						Register16	→	[Disp16]	M	74 0 3	0	1	1	1	0	1	0	0
								[Reg16]	M	70 0 3	0	1	1	1	0	0	0	0
								[Reg16 + Disp8]	M	70 1 3	0	1	1	1	0	0	0	1
								[Reg16 + Disp16]	M	70 2 3	0	1	1	1	0	0	1	0
						Immediate16	→	[Disp16]	L	7C 0 3	0	1	1	1	1	1	0	0
								[Reg16]	L	78 0 3	0	1	1	1	1	0	0	0
								[Reg16 + Disp8]	L	78 1 3	0	1	1	1	1	0	0	1
								[Reg16 + Disp16]	L	78 2 3	0	1	1	1	1	0	1	0
Med		Not	NOT	Zero Page	8	[Disp8]			N	28 0 X	0	0	1	0	1	0	0	0
					16	[Disp8]			N	28 1 X	0	0	1	0	1	0	0	1
Core				Near	8	Register8			L	2C 3 0	0	0	1	0	1	1	1	1
						[Disp16]			N	28 2 X	0	0	1	0	1	0	1	0
						[Reg16]			N	2C 0 0	0	0	1	0	1	1	0	0
High						[Reg16 + Disp8]			N	2C 1 0	0	0	1	0	1	1	0	1
						[Reg16 + Disp16]			N	2C 2 0	0	0	1	0	1	1	1	0
					16	Register16			L	2C 3 1	0	0	1	0	1	1	1	1
						[Disp16]			N	28 3 X	0	0	1	0	1	0	1	1
Med						[Reg16]			N	2C 0 1	0	0	1	0	1	1	0	0
						[Reg16 + Disp8]			N	2C 1 1	0	0	1	0	1	1	0	1
						[Reg16 + Disp16]			N	2C 2 1	0	0	1	0	1	1	1	0
High				Zero Page	8	Register8	←	[Disp8]	H	B4 3 0	1	0	1	1	0	1	1	1
							→	[Disp8]	M	B4 3 2	1	0	1	1	0	1	1	1
Med						Register16	←	[Disp8]	H	B4 3 1	1	0	1	1	0	1	1	1
Med							→	[Disp8]	H	B4 3 3	1	0	1	1	0	1	1	1
						Immediate8	→	[Disp8]	M	BC 3 2	1	0	1	1	1	1	1	1
						Immediate16	→	[Disp8]	M	BC 3 3	1	0	1	1	1	1	1	1
								Immediate8	M	B4 1 0	1	0	1	1	0	1	0	1
Core								Register8	M	B0 3 0	1	0	1	1	0	0	1	1
						Register8	←	[Disp16]	M	B4 0 0	1	0	1	1	0	1	0	0
								[Reg16]	H	B0 0 0	1	0	1	1	0	0	0	0

Tier	Category	Instruction	Mnemonic	Distance	Size	Operand 1	Dir	Operand 2	Code	Opcode	Bits
High		Test	TEST	Near				[Reg16 + Disp8]	M	B0 1 0	1 0 1 1 0 0 0 1
High								[Reg16 + Disp16]	H	B0 2 0	1 0 1 1 0 0 1 0
High					8	Register8	→	[Disp16]	M	B4 0 2	1 0 1 1 0 1 0 0
High								[Reg16]	M	B0 0 2	1 0 1 1 0 0 0 0
High								[Reg16 + Disp8]	M	B0 1 2	1 0 1 1 0 0 0 1
High								[Reg16 + Disp16]	M	B0 2 2	1 0 1 1 0 0 1 0
High						Immediate8	→	[Disp16]	L	BC 0 2	1 0 1 1 1 1 0 0
High								[Reg16]	L	B8 0 2	1 0 1 1 1 0 0 0
High								[Reg16 + Disp8]	L	B8 1 2	1 0 1 1 1 0 0 1
High								[Reg16 + Disp16]	L	B8 2 2	1 0 1 1 1 0 1 0
Med					16	Register16	←	Immediate16	M	B4 2 1	1 0 1 1 0 1 1 0
Med								Register16	M	B0 3 1	1 0 1 1 0 0 1 1
Med								[Disp16]	M	B4 0 1	1 0 1 1 0 1 0 0
Med								[Reg16]	H	B0 0 1	1 0 1 1 0 0 0 0
Med								[Reg16 + Disp8]	M	B0 1 1	1 0 1 1 0 0 0 1
Med								[Reg16 + Disp16]	H	B0 2 1	1 0 1 1 0 0 1 0
Med						Register16	→	[Disp16]	M	B4 0 3	1 0 1 1 0 1 0 0
Med								[Reg16]	M	B0 0 3	1 0 1 1 0 0 0 0
Med								[Reg16 + Disp8]	M	B0 1 3	1 0 1 1 0 0 0 1
Med								[Reg16 + Disp16]	M	B0 2 3	1 0 1 1 0 0 1 0
Med						Immediate16	→	[Disp16]	L	BC 0 3	1 0 1 1 1 1 0 0
Med								[Reg16]	L	B8 0 3	1 0 1 1 1 0 0 0
Med								[Reg16 + Disp8]	L	B8 1 3	1 0 1 1 1 0 0 1
Med								[Reg16 + Disp16]	L	B8 2 3	1 0 1 1 1 0 1 0
Core	Shift and Rotate	Rotate Left	ROL	–	8	Register8, Immediate3			N	24 0 0	0 0 1 0 0 1 0 0
Med					16	Register16, Immediate3			N	24 0 1	0 0 1 0 0 1 0 0
High		Rotate Right	ROR	–	8	Register8, Immediate3			N	24 0 2	0 0 1 0 0 1 0 0
Med					16	Register16, Immediate3			N	24 0 3	0 0 1 0 0 1 0 0
Core		Rotate Left through Carry	RCL	–	8	Register8, Immediate3			N	24 1 0	0 0 1 0 0 1 0 1
Med					16	Register16, Immediate3			N	24 1 1	0 0 1 0 0 1 0 1
High		Rotate Right through Carry	RCR	–	8	Register8, Immediate3			N	24 1 2	0 0 1 0 0 1 0 1
Med					16	Register16, Immediate3			N	24 1 3	0 0 1 0 0 1 0 1
Core		Shift Left	SHL	–	8	Register8, Immediate3			L	24 2 0	0 0 1 0 0 1 1 0
Med					16	Register16, Immediate3			L	24 2 1	0 0 1 0 0 1 1 0
High		Shift Logical Right	SHR	–	8	Register8, Immediate3			N	24 2 2	0 0 1 0 0 1 1 0
Med					16	Register16, Immediate3			N	24 2 3	0 0 1 0 0 1 1 0
High		Shift Arithmetic Right	SAR	–	8	Register8, Immediate3			N	24 3 2	0 0 1 0 0 1 1 1
Med					16	Register16, Immediate3			N	24 3 3	0 0 1 0 0 1 1 1
Core	Branching	Jump Unconditional	JMP	Near	–	Program16	←	Immediate16	H	C8 0 X	1 1 0 0 1 0 0 0
Core								[Disp16]	H	C8 1 X	1 1 0 0 1 0 0 1
High			JMPR	Short	–	Program16	←+	Immediate8	M	C8 3 X	1 1 0 0 1 0 1 1
Core				Near				Immediate16	H	C8 2 X	1 1 0 0 1 0 1 0
Core		Jump Overflow	JO	Near	–	Program16	←	Immediate16	M	E8 0 X	1 1 1 0 1 0 0 0
Core								[Disp16]	M	E8 1 X	1 1 1 0 1 0 0 1
High			JOR	Short	–	Program16	←+	Immediate8	L	E8 3 X	1 1 1 0 1 0 1 1
Core				Near				Immediate16	M	E8 2 X	1 1 1 0 1 0 1 0
Core		Jump Sign	JS	Near	–	Program16	←	Immediate16	M	E4 0 X	1 1 1 0 0 1 0 0
Core								[Disp16]	M	E4 1 X	1 1 1 0 0 1 0 1
High			JSR	Short	–	Program16	←+	Immediate8	L	E4 3 X	1 1 1 0 0 1 1 1
Core				Near				Immediate16	M	E4 2 X	1 1 1 0 0 1 1 0
Core		Jump Zero	JZ	Near	–	Program16	←	Immediate16	H	CC 0 X	1 1 0 0 1 1 0 0
Core								[Disp16]	H	CC 1 X	1 1 0 0 1 1 0 1
High			JZR	Short	–	Program16	←+	Immediate8	M	CC 3 X	1 1 0 0 1 1 1 1
Core				Near				Immediate16	H	CC 2 X	1 1 0 0 1 1 1 0
Med		Jump Not Zero	JNZ	Near	–	Program16	←	Immediate16	H	F0 0 X	1 1 1 1 0 0 0 0
Med								[Disp16]	H	F0 1 X	1 1 1 1 0 0 0 1
Med			JNZR	Short	–	Program16	←+	Immediate8	M	F0 3 X	1 1 1 1 0 0 1 1
Med				Near				Immediate16	H	F0 2 X	1 1 1 1 0 0 1 0
Core		Jump Carry	JC	Near	–	Program16	←	Immediate16	M	E0 0 X	1 1 1 0 0 0 0 0
Core								[Disp16]	M	E0 1 X	1 1 1 0 0 0 0 1
High			JCR	Short	–	Program16	←+	Immediate8	L	E0 3 X	1 1 1 0 0 0 1 1
Core				Near				Immediate16	M	E0 2 X	1 1 1 0 0 0 1 0
Med		Jump Not Carry	JNC	Near	–	Program16	←	Immediate16	N	F4 0 X	1 1 1 1 0 1 0 0
Med								[Disp16]	N	F4 1 X	1 1 1 1 0 1 0 1
Med			JNCR	Short	–	Program16	←+	Immediate8	N	F4 3 X	1 1 1 1 0 1 1 1
Med				Near				Immediate16	N	F4 2 X	1 1 1 1 0 1 1 0
High		Jump Parity	JP	Near	–	Program16	←	Immediate16	M	EC 0 X	1 1 1 0 1 1 0 0
High								[Disp16]	M	EC 1 X	1 1 1 0 1 1 0 1

Priority	Category	Operation	Mnemonic			Target		Operand	Type	Opcode	b7	b6	b5	b4	b3	b2	b1	b0
Med		Jump Parity	JPR	Short	–	Program16	←+	Immediate8	L	EC 3 X	1	1	1	0	1	1	1	1
High				Near				Immediate16	M	EC 2 X	1	1	1	0	1	1	1	0
Core	Subroutines	Call	CALL	Near	–	Program16	←	Immediate16	H	10 0 X	0	0	0	1	0	0	0	0
Core								[Disp16]	H	10 1 X	0	0	0	1	0	0	0	1
High			CALLR	Short	–	Program16	←+	Immediate8	M	10 3 X	0	0	0	1	0	0	1	1
Core				Near				Immediate16	H	10 2 X	0	0	0	1	0	0	1	0
Core		Return	RET	–	–	–			L	04 0 X	0	0	0	0	0	1	0	0
High				–	–	Immediate8			N	04 1 X	0	0	0	0	0	1	0	1
Core		Interrupt	INT	–	–	Immediate8			N	00 1 X	0	0	0	0	0	0	0	1
Med		Breakpoint	BRK	–	–	–			N	00 0 X	0	0	0	0	0	0	0	0
Core		Interrupt Return	IRET	–	–	–			N	04 2 X	0	0	0	0	0	1	1	0
Med	Flag Manipulation	Clear Flag	CLF	–	–	Immediate8			N	DC 2 X	1	1	0	1	1	1	1	0
Med		Set Flag	STF	–	–	Immediate8			N	DC 1 X	1	1	0	1	1	1	0	1
Low		Complement Flag	CMF	–	–	Immediate8			N	7C 1 X	0	1	1	1	1	1	0	1
High	Processor Control	Identification	CPUID	–	–	–			N	04 3 0	0	0	0	0	0	1	1	1
High		No Operation	NOP	–	–	–			N	00 2 X	0	0	0	0	0	0	1	0
Core		Halt	HLT	–	–	–			N	04 3 3	0	0	0	0	0	1	1	1
Med		Wait	WAIT	–	–	Immediate4			N	04 3 2	0	0	0	0	0	1	1	1
Med	Expansion Instructions	Reserved for Expansion	–	–	–	–			–	00 3 X	0	0	0	0	0	0	1	1
High		Maths Coprocessor	–	–	–	–			–	40 3 X	0	1	0	0	0	0	1	1
High	Floating Point Instructions	FPU NOP	FNOP	–	–				L	40 3 0	0	1	0	0	0	0	1	1
High		Convert to Integer	FIXS	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			FIXD	–	–				M	40 3 0	0	1	0	0	0	0	1	1
High		Convert to Floating Point	FLTS	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			FLTD	–	–				M	40 3 0	0	1	0	0	0	0	1	1
High		Change Sign	CHSS	–	–				L	40 3 1	0	1	0	0	0	0	1	1
			CHSD	–	–				L	40 3 0	0	1	0	0	0	0	1	1
			CHSF	–	–				L	40 3 0	0	1	0	0	0	0	1	1
High		Exchange Stack	XCHS	–	–				L	40 3 1	0	1	0	0	0	0	1	1
			XCHD	–	–				L	40 3 0	0	1	0	0	0	0	1	1
			XCHF	–	–				L	40 3 0	0	1	0	0	0	0	1	1
Core		Pop FPU Stack	POPS						L	40 3 1	0	1	0	0	0	0	1	1
			POPD						L	40 3 0	0	1	0	0	0	0	1	1
			POPF						L	40 3 0	0	1	0	0	0	0	1	1
Core		Push FPU Stack	PTOS						L	40 3 1	0	1	0	0	0	0	1	1
			PTOD						L	40 3 0	0	1	0	0	0	0	1	1
			PTOF						L	40 3 0	0	1	0	0	0	0	1	1
Med			PUPI	–	–				L	40 3 0	0	1	0	0	0	0	1	1
Med		Integer Functions (16 bit)	SADD	–	–				M	40 3 1	0	1	0	0	0	0	1	1
			SSUB	–	–				M	40 3 1	0	1	0	0	0	0	1	1
			SMUL	–	–				M	40 3 1	0	1	0	0	0	0	1	1
			SMUU	–	–				M	40 3 1	0	1	0	0	0	0	1	1
			SDIV	–	–				M	40 3 1	0	1	0	0	0	0	1	1
Med		Integer Functions (32 bit)	DADD	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			DSUB	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			DMUL	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			DMUU	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			DDIV	–	–				M	40 3 0	0	1	0	0	0	0	1	1
Core		Floating Point Functions	FADD	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			FSUB	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			FMUL	–	–				M	40 3 0	0	1	0	0	0	0	1	1
			FDIV	–	–				M	40 3 0	0	1	0	0	0	0	1	1
High		Trigonometric Functions	SIN	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			COS	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			TAN	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			ASIN	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			ACOS	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			ATAN	–	–				H	40 3 0	0	1	0	0	0	0	1	1
High		Exponential & Logarithmic Functions	SQRT	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			LOG	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			LN	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			EXP	–	–				H	40 3 0	0	1	0	0	0	0	1	1
			PWR	–	–				H	40 3 0	0	1	0	0	0	0	1	1