## Comparison of IC Logic Families

Chapter	r · April 2017		
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## **Comparison of Logic Families**

	Logic Family (Sil	licon Technology)	Introduction	Features	Limitations
Transistor Logic Families (Bipolar Transistor Technology)	Saturated Logic Families  (ON — Saturation Mode)  (OFF — Cut Off Mode)	1. RTL (Resistor Transistor Logic)	<ul> <li>In common use before the development of ICs. Common Emitter Configuration.</li> <li>Logic 1: 1-3.6 V and Logic 0: 0.2V</li> </ul>	- First logic family, require minimum number of transistors.	<ul><li>Low speed, high power dissipation</li><li>Low fan out, poor noise immunity</li><li>Operating speed &lt;4MHz.</li></ul>
		2. DCTL	- Direct coupled transistors.	- Simpler than RTL, easy to fabricate.	- Small logic swing, poor noise margin.
		(Direct Coupled Transistor Logic)	- Base resistors of RTL are removed.	- Fewer components hence economical.	- Current hogging
		3. DTL (Diode Transistor Logic)	<ul><li>Use diodes and transistors.</li><li>Input is fed through diodes followed by transistor at the output side.</li></ul>	<ul> <li>First circuit configuration designed into IC.</li> <li>Very small in size and high reliability at very low price.</li> <li>Greater fan out and improved noise margins.</li> </ul>	- No low and constant output impedance in both states.
		4. TTL (Transistor-Transistor Logic)	- Use all transistors totem pole output.	- Fast switching time, larger fan out.	- Large current spike when switching
			- Function of diodes in DTL is performed	- Reduced silicon chip area.	from low to high.
			by multi-emitter transistor at input	- Easy to interface with other logic families.	- Less noise immunity (0.4V)
		5. IIL (Integrated Injection Logic)	<ul> <li>Merged Transistor Logic (MTL).</li> <li>Both PNP and NPN transistors are used.</li> <li>Designed around multi-collector inverting transistors.</li> </ul>	<ul><li>High component density, less power dissipation.</li><li>Low metal interconnection.</li><li>Used in MSI and LSI designs.</li></ul>	- Poor noise immunity.
	Non-Saturated Logic  ON — Active Mode OFF — Cut Off Mode	6.ECL (Emitter Coupled Logic)	<ul> <li>Non saturated logic/Current mode logic.</li> <li>Compliment output/eliminates the need of inverter.</li> <li>Logic 1: -0.8 and Logic 0: -1.7</li> </ul>	<ul><li>Fastest logic family</li><li>Used in very high frequency applications.</li><li>No noise spikes, large fan out.</li></ul>	<ul> <li>Require large silicon area, high power dissipation (high cost).</li> <li>Inconvenient voltage levels.</li> <li>Low noise margins.</li> </ul>
	IOS Logic Families or Transistor Technology)	7.MOS Logic (Metal Oxide Semiconductor Logic)	<ul> <li>Use pMOS, nMOS or both with high packaging density.</li> <li>Easy to design and fabricate</li> <li>Less power drawn due to gate dielectric.</li> </ul>	<ul><li>Lower power dissipation.</li><li>Shorter rise and fall times.</li><li>Large fan-out.</li></ul>	<ul><li>Larger propagation due to high output impedance.</li><li>Noise margin is around 1V.</li></ul>

Parameter	RTL	IIL	DTL	HTL	TTL	ECL	MOS	CMOS
Basic Gate	NOR	NOR	NAND	NAND	NAND	OR-NOR	NAND	NOR-NAND
Fan Out	5	Depends on Injector Current	8	10	10-20	25	20	20-50
Power Dissipation	12 mW	6 nW – 70 uW	8-12 mW	55 mW	10 mW	40-55 mW	0.2-10 mW	0.025-1.01 mW
Noise Immunity	Nominal	Poor	Good	Excellent	Very Good	Poor	Good	Very Good
<b>Propagation Delay</b>	12 nSec	25-30 nSec	30 nSec	4 nSec	10 nSec	1-2 nSec	300 nSec	70 nSec
Clock Rate	8 MHz	-	72 MHz	4 MHz	35 MHz	+60 MHz	2 MHz	10 MHz
Speed X Power	144	Less than 1	300	-	100	100	60	70

