Priority	Category	Name	Code	Range	Size	Addressing			⧖	Opcode	Instruction							Mo		D	S	R/M	Reg	Byte 3	Byte 4	Byte 5	Byte 6
Core	*Data Transfer*	Move	MOV	–	8	Register8	←	Register8	H	00 3 0	0	0	0	0	0	0	**1**	**1**	0	0	Source	Dest				
								Immediate8	M	04 1 0	0	0	0	0	0	**1**	0	**1**	0	0		Dest	Immediate8			
					16	Register16	←	Register16	H	00 3 1	0	0	0	0	0	0	**1**	**1**	0	**1**	Source	Dest				
								Immediate16	M	04 2 1	0	0	0	0	0	**1**	**1**	0	0	**1**		Dest	Immediate16			
Low				Zero Page	8	Register8	←	[Disp8]	H	04 3 0	0	0	0	0	0	**1**	**1**	**1**	0	0		Dest	Disp8			
							→	[Disp8]	M	04 3 2	0	0	0	0	0	**1**	**1**	**1**	**1**	0		Source	Disp8			
					16	Register16	←	[Disp8]	H	04 3 1	0	0	0	0	0	**1**	**1**	**1**	0	**1**		Dest	Disp8			
							→	[Disp8]	H	04 3 3	0	0	0	0	0	**1**	**1**	**1**	**1**	**1**		Source	Disp8			
Low					8	Immediate8	→	[Disp8]	M	0C 3 2	0	0	0	0	**1**	**1**	**1**	**1**	**1**	0			Disp8	Immediate8		
					16	Immediate16	→	[Disp8]	M	0C 3 3	0	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**			Disp8	Immediate16		
Core				Near	8	Register8	←	[Disp16]	M	04 0 0	0	0	0	0	0	**1**	0	0	0	0		Dest	Disp16			
								[Reg16]	H	00 0 0	0	0	0	0	0	0	0	0	0	0	Base	Dest				
								[Reg16 + Disp8]	M	00 1 0	0	0	0	0	0	0	0	**1**	0	0	Base	Dest	Disp8			
								[Reg16 + Disp16]	M	00 2 0	0	0	0	0	0	0	**1**	0	0	0	Base	Dest	Disp16			
Core					16	Register16	←	[Disp16]	M	04 0 1	0	0	0	0	0	**1**	0	0	0	**1**		Dest	Disp16			
								[Reg16]	H	00 0 1	0	0	0	0	0	0	0	0	0	**1**	Base	Dest				
								[Reg16 + Disp8]	M	00 1 1	0	0	0	0	0	0	0	**1**	0	**1**	Base	Dest	Disp8			
								[Reg16 + Disp16]	M	00 2 1	0	0	0	0	0	0	**1**	0	0	**1**	Base	Dest	Disp16			
Med				Near	8	Immediate8	→	[Disp16]	M	0C 0 2	0	0	0	0	**1**	**1**	0	0	**1**	0			Disp16	Immediate8		
								[Reg16]	H	08 0 2	0	0	0	0	**1**	0	0	0	**1**	0	Base		Immediate8			
								[Reg16 + Disp8]	M	08 1 2	0	0	0	0	**1**	0	0	**1**	**1**	0	Base		Disp8	Immediate8		
								[Reg16 + Disp16]	M	08 2 2	0	0	0	0	**1**	0	**1**	0	**1**	0	Base		Disp16	Immediate8		
Core						Register8	→	[Disp16]	M	04 0 2	0	0	0	0	0	**1**	0	0	**1**	0		Source	Disp16			
								[Reg16]	H	00 0 2	0	0	0	0	0	0	0	0	**1**	0	Base	Source				
								[Reg16 + Disp8]	M	00 1 2	0	0	0	0	0	0	0	**1**	**1**	0	Base	Source	Disp8			
								[Reg16 + Disp16]	M	00 2 2	0	0	0	0	0	0	**1**	0	**1**	0	Base	Source	Disp16			
Med					16	Immediate16	→	[Disp16]	M	0C 0 3	0	0	0	0	**1**	**1**	0	0	**1**	**1**			Disp16	Immediate16		
								[Reg16]	M	08 0 3	0	0	0	0	**1**	0	0	0	**1**	**1**	Base		Immediate16			
								[Reg16 + Disp8]	M	08 1 3	0	0	0	0	**1**	0	0	**1**	**1**	**1**	Base		Disp8	Immediate16		
								[Reg16 + Disp16]	M	08 2 3	0	0	0	0	**1**	0	**1**	0	**1**	**1**	Base		Disp16	Immediate16		
Core						Register16	→	[Disp16]	M	04 0 3	0	0	0	0	0	**1**	0	0	**1**	**1**		Source	Disp16			
								[Reg16]	H	00 0 3	0	0	0	0	0	0	0	0	**1**	**1**	Base	Source				
								[Reg16 + Disp8]	M	00 1 3	0	0	0	0	0	0	0	**1**	**1**	**1**	Base	Source	Disp8			
								[Reg16 + Disp16]	M	00 2 3	0	0	0	0	0	0	**1**	0	**1**	**1**	Base	Source	Disp16			
Low		Move Flags	LDRF	–	8	Flags8	←	Register8	N	0C 1 0	0	0	0	0	**1**	**1**	0	**1**	0	0		Source				
					16	Flags16	←	Register16	N	0C 1 1	0	0	0	0	**1**	**1**	0	**1**	0	**1**		Source				
			STRF	–	8	Flags8	→	Register8	N	0C 1 2	0	0	0	0	**1**	**1**	0	**1**	**1**	0		Dest				
					16	Flags16	→	Register16	N	0C 1 3	0	0	0	0	**1**	**1**	0	**1**	**1**	**1**		Dest				
Med		Exchange	XCHG	–	8	Register8	↔	Register8	N	00 3 2	0	0	0	0	0	0	**1**	**1**	**1**	0	Source	Dest				
					16	Register16	↔	Register16	N	00 3 3	0	0	0	0	0	0	**1**	**1**	**1**	**1**	Source	Dest				
Core		Push	PUSH	–	8	Register8	←	Register8	H	20 3 2	0	0	**1**	0	0	0	**1**	**1**	**1**	0		Source				
								Immediate8	L	14 0 X	0	0	0	**1**	0	**1**	0	0	Immediate8						
					16			Register16	H	20 3 3	0	0	**1**	0	0	0	**1**	**1**	**1**	**1**		Source				
								Immediate16	L	14 1 X	0	0	0	**1**	0	**1**	0	**1**	Immediate16						
				Zero Page	8	Stack16		[Disp8]	L	18 0 X	0	0	0	**1**	**1**	0	0	0	Disp8						
					16			[Disp8]	L	18 1 X	0	0	0	**1**	**1**	0	0	**1**	Disp8						
				Near	8			[Disp16]	M	18 2 X	0	0	0	**1**	**1**	0	**1**	0	Disp16						
								[Reg16]	M	20 0 2	0	0	**1**	0	0	0	0	0	**1**	0	Base	Source				
								[Reg16 + Disp8]	M	20 1 2	0	0	**1**	0	0	0	0	**1**	**1**	0	Base	Source	Disp8			
								[Reg16 + Disp16]	M	20 2 2	0	0	**1**	0	0	0	**1**	0	**1**	0	Base	Source	Disp16			
					16			[Disp16]	M	18 3 X	0	0	0	**1**	**1**	0	**1**	**1**	Disp16						
								[Reg16]	M	20 0 3	0	0	**1**	0	0	0	0	0	**1**	**1**	Base	Source				
								[Reg16 + Disp8]	M	20 1 3	0	0	**1**	0	0	0	0	**1**	**1**	**1**	Base	Source	Disp8			
								[Reg16 + Disp16]	M	20 2 3	0	0	**1**	0	0	0	**1**	0	**1**	**1**	Base	Source	Disp16			
			PUSHF	–	16	Stack16	←	Flags16	L	14 2 3	0	0	0	**1**	0	**1**	**1**	0	**1**	**1**						
Core		Pop	POP	–	8	Stack16	→	Register8	H	20 3 0	0	0	**1**	0	0	0	**1**	**1**	0	0		Dest				
					16			Register16	H	20 3 1	0	0	**1**	0	0	0	**1**	**1**	0	**1**		Dest				
				Zero Page	8			[Disp8]	L	1C 0 X	0	0	0	**1**	**1**	**1**	0	0	Disp8						
					16			[Disp8]	L	1C 1 X	0	0	0	**1**	**1**	**1**	0	**1**	Disp8						
				Near	8			[Disp16]	M	1C 2 X	0	0	0	**1**	**1**	**1**	**1**	0	Disp16						
								[Reg16]	M	20 0 0	0	0	**1**	0	0	0	0	0	0	0	Base	Source				
								[Reg16 + Disp8]	M	20 1 0	0	0	**1**	0	0	0	0	**1**	0	0	Base	Source	Disp8			
								[Reg16 + Disp16]	M	20 2 0	0	0	**1**	0	0	0	**1**	0	0	0	Base	Source	Disp16			
					16			[Disp16]	M	1C 3 X	0	0	0	**1**	**1**	**1**	**1**	**1**	Disp16						
								[Reg16]	M	20 0 1	0	0	**1**	0	0	0	0	0	0	**1**	Base	Source				
								[Reg16 + Disp8]	M	20 1 1	0	0	**1**	0	0	0	0	**1**	0	**1**	Base	Source	Disp8			
								[Reg16 + Disp16]	M	20 2 1	0	0	**1**	0	0	0	**1**	0	0	**1**	Base	Source	Disp16			
			POPF	–	16	Stack16	→	Flags16	L	14 2 1	0	0	0	**1**	0	**1**	**1**	0	0	**1**						
High		In	IN	Near	8	Register8	←	Port(Disp8)	N	DC 1 X	**1**	**1**	0	**1**	**1**	**1**	0	**1**					Disp8			
					16	Register16	←	Port(Disp8)	N	DC 2 X	**1**	**1**	0	**1**	**1**	**1**	**1**	0					Disp8			
High		Out	OUT	Near	8	Register8	→	Port(Disp8)	N	EC 1 X	**1**	**1**	**1**	0	**1**	**1**	0	**1**					Disp8			
					16	Register16	→	Port(Disp8)	N	EC 2 X	**1**	**1**	**1**	0	**1**	**1**	**1**	0					Disp8			
Low		Load Effective Address	LEA	Short	8	Register8	←	Reg8 + Disp8	L	08 2 0	0	0	0	0	**1**	0	**1**	0	0	0	Base	Dest	Disp8			
				Near	16	Register16	←	Reg16 + Disp8	L	08 1 0	0	0	0	0	**1**	0	0	**1**	0	0	Base	Dest	Disp8			
								Reg16 + Disp16	L	08 2 1	0	0	0	0	**1**	0	**1**	0	0	**1**	Base	Dest	Disp16			
Low		Sign Extend	CBW	–	8	Register8			N	24 3 0	0	0	**1**	0	0	**1**	**1**	**1**	0	0		Reg				
High		Add	ADD	Zero Page	8	Register8	←+	[Disp8]	H	84 3 0	**1**	0	0	0	0	**1**	**1**	**1**	0	0		Dest	Disp8			
							+→	[Disp8]	M	84 3 2	**1**	0	0	0	0	**1**	**1**	**1**	**1**	0		Source	Disp8			
Med					16	Register16	←+	[Disp8]	H	84 3 1	**1**	0	0	0	0	**1**	**1**	**1**	0	**1**		Dest	Disp8			
							+→	[Disp8]	H	84 3 3	**1**	0	0	0	0	**1**	**1**	**1**	**1**	**1**		Source	Disp8			
Med					8	Immediate8	+→	[Disp8]	M	8C 3 2	**1**	0	0	0	**1**	**1**	**1**	**1**	**1**	0			Disp8	Immediate8		
					16	Immediate16	+→	[Disp8]	M	8C 3 3	**1**	0	0	0	**1**	**1**	**1**	**1**	**1**	**1**			Disp8	Immediate16		
Core				Near	8	Register8	←+	Immediate8	M	84 1 0	**1**	0	0	0	0	**1**	0	**1**	0	0		Dest	Immediate8			
								Register8	M	80 3 0	**1**	0	0	0	0	0	**1**	**1**	0	0	Source	Dest				
								[Disp16]	M	84 0 0	**1**	0	0	0	0	**1**	0	0	0	0		Dest	Disp16			
								[Reg16]	H	80 0 0	**1**	0	0	0	0	0	0	0	0	0	Base	Dest				
								[Reg16 + Disp8]	M	80 1 0	**1**	0	0	0	0	0	0	**1**	0	0	Base	Dest	Disp8			
								[Reg16 + Disp16]	H	80 2 0	**1**	0	0	0	0	0	**1**	0	0	0	Base	Dest	Disp16			
High						Register8	+→	[Disp16]	M	84 0 2	**1**	0	0	0	0	**1**	0	0	**1**	0		Source	Disp16			
								[Reg16]	M	80 0 2	**1**	0	0	0	0	0	0	0	**1**	0	Base	Source				
								[Reg16 + Disp8]	M	80 1 2	**1**	0	0	0	0	0	0	**1**	**1**	0	Base	Source	Disp8			
								[Reg16 + Disp16]	M	80 2 2	**1**	0	0	0	0	0	**1**	0	**1**	0	Base	Source	Disp16			
						Immediate8		[Disp16]	L	8C 0 2	**1**	0	0	0	**1**	**1**	0	0	**1**	0			Disp16	Immediate8		
								[Reg16]	L	88 0 2	**1**	0	0	0	**1**	0	0	0	**1**	0	Base		Immediate8			
								[Reg16 + Disp8]	L	88 1 2	**1**	0	0	0	**1**	0	0	**1**	**1**	0	Base		Disp8	Immediate8		
								[Reg16 + Disp16]	L	88 2 2	**1**	0	0	0	**1**	0	**1**	0	**1**	0	Base		Disp16	Immediate8		
Med					16	Register16	←+	Immediate16	M	84 2 1	**1**	0	0	0	0	**1**	**1**	0	0	**1**		Dest	Immediate16			
								Register16	M	80 3 1	**1**	0	0	0	0	0	**1**	**1**	0	**1**	Source	Dest				
								[Disp16]	M	84 0 1	**1**	0	0	0	0	**1**	0	0	0	**1**		Dest	Disp16			
								[Reg16]	H	80 0 1	**1**	0	0	0	0	0	0	0	0	**1**	Base	Dest				
								[Reg16 + Disp8]	M	80 1 1	**1**	0	0	0	0	0	0	**1**	0	**1**	Base	Dest	Disp8			
								[Reg16 + Disp16]	H	80 2 1	**1**	0	0	0	0	0	**1**	0	0	**1**	Base	Dest	Disp16			
					16	Register16	+→	[Disp16]	M	84 0 3	**1**	0	0	0	0	**1**	0	0	**1**	**1**		Source	Disp16			
								[Reg16]	M	80 0 3	**1**	0	0	0	0	0	0	0	**1**	**1**	Base	Source				
								[Reg16 + Disp8]	M	80 1 3	**1**	0	0	0	0	0	0	**1**	**1**	**1**	Base	Source	Disp8			
								[Reg16 + Disp16]	M	80 2 3	**1**	0	0	0	0	0	**1**	0	**1**	**1**	Base	Source	Disp16			
						Immediate16	+→	[Disp16]	L	8C 0 3	**1**	0	0	0	**1**	**1**	0	0	**1**	**1**			Disp16	Immediate16		
								[Reg16]	L	88 0 3	**1**	0	0	0	**1**	0	0	0	**1**	**1**	Base		Immediate16			
								[Reg16 + Disp8]	L	88 1 3	**1**	0	0	0	**1**	0	0	**1**	**1**	**1**	Base		Disp8	Immediate16		
								[Reg16 + Disp16]	L	88 2 3	**1**	0	0	0	**1**	0	**1**	0	**1**	**1**	Base		Disp16	Immediate16		
High				Zero	8	Register8	←+	[Disp8]	M	94 3 0	**1**	0	0	**1**	0	**1**	**1**	**1**	0	0		Dest	Disp8			
							+→	[Disp8]	M	94 3 2	**1**	0	0	**1**	0	**1**	**1**	**1**	**1**	0		Source	Disp8			
					16		←+	[Disp8]	M	94 3 1	**1**	0	0	**1**	0	**1**	**1**	**1**	0	**1**		Dest	Disp8			

Priority	Category	Operation	Mnemonic	Mode	Size	Operand	Dir	Operand	Cost	Hex	Bits	Field	Field	Byte 1	Byte 2	Byte 3
	Arithmetic	Add with Carry	ADC	Page	16	Register16	+→	[Disp8]	M	94 3 3	10010111 11		Source	Disp8		
Med					8	Immediate8	+→	[Disp8]	M	9C 3 2	10011111 10			Disp8	Immediate8	
					16	Immediate16	+→	[Disp8]	M	9C 3 3	10011111 11			Disp8	Immediate16	
Core				Near	8	Register8	←+	Immediate8	L	94 1 0	10010101 00		Dest	Immediate8		
								Register8	L	90 3 0	10010011 00	Source	Dest			
								[Disp16]	L	94 0 0	10010100 00		Dest	Disp16		
								[Reg16]	M	90 0 0	10010000 00	Base	Dest			
High								[Reg16 + Disp8]	L	90 1 0	10010001 00	Base	Dest	Disp8		
								[Reg16 + Disp16]	M	90 2 0	10010010 00	Base	Dest	Disp16		
						Register8	+→	[Disp16]	L	94 0 2	10010100 10		Source	Disp16		
								[Reg16]	L	90 0 2	10010000 10	Base	Source			
								[Reg16 + Disp8]	L	90 1 2	10010001 10	Base	Source	Disp8		
								[Reg16 + Disp16]	L	90 2 2	10010010 10	Base	Source	Disp16		
						Immediate8	+→	[Disp16]	L	9C 0 2	10011100 10			Disp16		Immediate8
								[Reg16]	L	98 0 2	10011000 10	Base		Immediate8		
								[Reg16 + Disp8]	L	98 1 2	10011001 10	Base		Disp8	Immediate8	
								[Reg16 + Disp16]	L	98 2 2	10011010 10	Base		Disp16		Immediate8
Med					16	Register16	←+	Immediate16	L	94 2 1	10010110 01		Dest	Immediate16		
								Register16	L	90 3 1	10010011 01	Source	Dest			
								[Disp16]	L	94 0 1	10010100 01		Dest	Disp16		
								[Reg16]	M	90 0 1	10010000 01	Base	Dest			
								[Reg16 + Disp8]	L	90 1 1	10010001 01	Base	Dest	Disp8		
								[Reg16 + Disp16]	M	90 2 1	10010010 01	Base	Dest	Disp16		
						Register16	+→	[Disp16]	L	94 0 3	10010100 11		Source	Disp16		
								[Reg16]	L	90 0 3	10010000 11	Base	Source			
								[Reg16 + Disp8]	L	90 1 3	10010001 11	Base	Source	Disp8		
								[Reg16 + Disp16]	L	90 2 3	10010010 11	Base	Source	Disp16		
						Immediate16	+→	[Disp16]	L	9C 0 3	10011100 11			Disp16		Immediate16
								[Reg16]	L	98 0 3	10011000 11	Base		Immediate16		
								[Reg16 + Disp8]	L	98 1 3	10011001 11	Base		Disp8	Immediate16	
								[Reg16 + Disp16]	L	98 2 3	10011010 11	Base		Disp16		Immediate16
High		Subtract	SUB	Zero Page	8	Register8	←-	[Disp8]	H	44 3 0	01000111 00		Dest	Disp8		
							-→	[Disp8]	M	44 3 2	01000111 10		Source	Disp8		
Med					16	Register16	←-	[Disp8]	H	44 3 1	01000111 01		Dest	Disp8		
							-→	[Disp8]	H	44 3 3	01000111 11		Source	Disp8		
Med					8	Immediate8	-→	[Disp8]	M	4C 3 2	01001111 10			Disp8	Immediate8	
					16	Immediate16	-→	[Disp8]	M	4C 3 3	01001111 11			Disp8	Immediate16	
Core				Near	8	Register8	←-	Immediate8	L	44 1 0	01000101 00		Dest	Immediate8		
								Register8	L	40 3 0	01000011 00	Source	Dest			
								[Disp16]	L	44 0 0	01000100 00		Dest	Disp16		
								[Reg16]	M	40 0 0	01000000 00	Base	Dest			
High								[Reg16 + Disp8]	L	40 1 0	01000001 00	Base	Dest	Disp8		
								[Reg16 + Disp16]	M	40 2 0	01000010 00	Base	Dest	Disp16		
						Register8	-→	[Disp16]	L	44 0 2	01000100 10		Source	Disp16		
								[Reg16]	L	40 0 2	01000000 10	Base	Source			
								[Reg16 + Disp8]	L	40 1 2	01000001 10	Base	Source	Disp8		
								[Reg16 + Disp16]	L	40 2 2	01000010 10	Base	Source	Disp16		
						Immediate8	-→	[Disp16]	L	4C 0 2	01001100 10			Disp16		Immediate8
								[Reg16]	L	48 0 2	01001000 10	Base		Immediate8		
								[Reg16 + Disp8]	L	48 1 2	01001001 10	Base		Disp8	Immediate8	
								[Reg16 + Disp16]	L	48 2 2	01001010 10	Base		Disp16		Immediate8
Med					16	Register16	←-	Immediate16	L	44 2 1	01000110 01		Dest	Immediate16		
								Register16	L	40 3 1	01000011 01	Source	Dest			
								[Disp16]	L	44 0 1	01000100 01		Dest	Disp16		
								[Reg16]	M	40 0 1	01000000 01	Base	Dest			
								[Reg16 + Disp8]	L	40 1 1	01000001 01	Base	Dest	Disp8		
								[Reg16 + Disp16]	M	40 2 1	01000010 01	Base	Dest	Disp16		
						Register16	-→	[Disp16]	L	44 0 3	01000100 11		Source	Disp16		
								[Reg16]	L	40 0 3	01000000 11	Base	Source			
								[Reg16 + Disp8]	L	40 1 3	01000001 11	Base	Source	Disp8		
								[Reg16 + Disp16]	L	40 2 3	01000010 11	Base	Source	Disp16		
						Immediate16	-→	[Disp16]	L	4C 0 3	01001100 11			Disp16		Immediate16
								[Reg16]	L	48 0 3	01001000 11	Base		Immediate16		
								[Reg16 + Disp8]	L	48 1 3	01001001 11	Base		Disp8	Immediate16	
								[Reg16 + Disp16]	L	48 2 3	01001010 11	Base		Disp16		Immediate16
High		Subtract with Borrow	SBB	Zero Page	8	Register8	←-	[Disp8]	M	54 3 0	01010111 00		Dest	Disp8		
							-→	[Disp8]	M	54 3 2	01010111 10		Source	Disp8		
Med					16	Register16	←-	[Disp8]	M	54 3 1	01010111 01		Dest	Disp8		
							-→	[Disp8]	M	54 3 3	01010111 11		Source	Disp8		
Med					8	Immediate8	-→	[Disp8]	M	5C 3 2	01011111 10			Disp8	Immediate8	
					16	Immediate16	-→	[Disp8]	M	5C 3 3	01011111 11			Disp8	Immediate16	
Core				Near	8	Register8	←-	Immediate8	L	54 1 0	01010101 00		Dest	Immediate8		
								Register8	L	50 3 0	01010011 00	Source	Dest			
								[Disp16]	L	54 0 0	01010100 00		Dest	Disp16		
								[Reg16]	M	50 0 0	01010000 00	Base	Dest			
High								[Reg16 + Disp8]	L	50 1 0	01010001 00	Base	Dest	Disp8		
								[Reg16 + Disp16]	M	50 2 0	01010010 00	Base	Dest	Disp16		
						Register8	-→	[Disp16]	L	54 0 2	01010100 10		Source	Disp16		
								[Reg16]	L	50 0 2	01010000 10	Base	Source			
								[Reg16 + Disp8]	L	50 1 2	01010001 10	Base	Source	Disp8		
								[Reg16 + Disp16]	L	50 2 2	01010010 10	Base	Source	Disp16		
						Immediate8	-→	[Disp16]	L	5C 0 2	01011100 10			Disp16		Immediate8
								[Reg16]	L	58 0 2	01011000 10	Base		Immediate8		
								[Reg16 + Disp8]	L	58 1 2	01011001 10	Base		Disp8	Immediate8	
								[Reg16 + Disp16]	L	58 2 2	01011010 10	Base		Disp16		Immediate8
Med					16	Register16	←-	Immediate16	L	54 2 1	01010110 01		Dest	Immediate16		
								Register16	L	50 3 1	01010011 01	Source	Dest			
								[Disp16]	L	54 0 1	01010100 01		Dest	Disp16		
								[Reg16]	M	50 0 1	01010000 01	Base	Dest			
								[Reg16 + Disp8]	L	50 1 1	01010001 01	Base	Dest	Disp8		
								[Reg16 + Disp16]	M	50 2 1	01010010 01	Base	Dest	Disp16		
						Register16	-→	[Disp16]	L	54 0 3	01010100 11		Source	Disp16		
								[Reg16]	L	50 0 3	01010000 11	Base	Source			
								[Reg16 + Disp8]	L	50 1 3	01010001 11	Base	Source	Disp8		
								[Reg16 + Disp16]	L	50 2 3	01010010 11	Base	Source	Disp16		
						Immediate16	-→	[Disp16]	L	5C 0 3	01011100 11			Disp16		Immediate16
								[Reg16]	L	58 0 3	01011000 11	Base		Immediate16		
								[Reg16 + Disp8]	L	58 1 3	01011001 11	Base		Disp8	Immediate16	
								[Reg16 + Disp16]	L	58 2 3	01011010 11	Base		Disp16		Immediate16
Med		Increment	INC	Zero Page	8	[Disp8]			L	20 0 X	00100000	Disp8				
					16	[Disp8]			L	20 1 X	00100001	Disp8				
High				Near	8	Register8			M	24 3 0	00100111 00		Reg			
						[Disp16]			L	20 2 X	00100010		Disp16			
Med						[Reg16]			L	24 0 0	00100100 00	Base				
						[Reg16 + Disp8]			L	24 1 0	00100101 00	Base		Disp8		
						[Reg16 + Disp16]			L	24 2 0	00100110 00	Base		Disp16		
Med					16	Register16			M	24 3 1	00100111 01		Reg			
						[Disp16]			L	20 3 X	00100011		Disp16			
						[Reg16]			L	24 0 1	00100100 01	Base				
						[Reg16 + Disp8]			L	24 1 1	00100101 01	Base		Disp8		
						[Reg16 + Disp16]			L	24 2 1	00100110 01	Base		Disp16		
Med				Zero Page	8	[Disp8]			L	C0 0 X	11000000	Disp8				
					16	[Disp8]			L	C0 1 X	11000001	Disp8				
High						Register8			L	C4 3 0	11000111 00		Reg			
						[Disp16]			N	C0 2 X	11000010		Disp16			

Priority	Operation	Mnemonic	Mode	Size	Operand	Dir	Operand	Level	Opcode	Bits	Field	Field	Operand bytes	Extra bytes
	Decrement	DEC	Near	8	[Reg16]			N	C4 0 0	1 1 0 0 0 1 0 0 0 0	Base			
Med					[Reg16 + Disp8]			N	C4 1 0	1 1 0 0 0 1 0 1 0 0	Base		Disp8	
					[Reg16 + Disp16]			N	C4 2 0	1 1 0 0 0 1 1 0 0 0	Base		Disp16	
				16	Register16			L	C4 3 1	1 1 0 0 0 1 1 1 0 1		Reg		
					[Disp16]			N	C0 3 X	1 1 0 0 0 0 1 1			Disp16	
Med					[Reg16]			N	C4 0 1	1 1 0 0 0 1 0 0 0 1	Base			
					[Reg16 + Disp8]			N	C4 1 1	1 1 0 0 0 1 0 1 0 1	Base		Disp8	
					[Reg16 + Disp16]			N	C4 2 1	1 1 0 0 0 1 1 0 0 1	Base		Disp16	
Med	Negate	NEG	Zero Page	8	[Disp8]			N	30 0 X	0 0 1 1 0 0 0 0			Disp8	
				16	[Disp8]			N	30 1 X	0 0 1 1 0 0 0 1			Disp8	
			Near	8	Register8			L	34 3 0	0 0 1 1 0 1 1 1 0 0		Reg		
High					[Disp16]			N	30 2 X	0 0 1 1 0 0 1 0			Disp16	
					[Reg16]			N	34 0 0	0 0 1 1 0 1 0 0 0 0	Base			
Med					[Reg16 + Disp8]			N	34 1 0	0 0 1 1 0 1 0 1 0 0	Base		Disp8	
					[Reg16 + Disp16]			N	34 2 0	0 0 1 1 0 1 1 0 0 0	Base		Disp16	
				16	Register16			L	34 3 1	0 0 1 1 0 1 1 1 0 1		Reg		
					[Disp16]			N	30 3 X	0 0 1 1 0 0 1 1			Disp16	
Med					[Reg16]			N	34 0 1	0 0 1 1 0 1 0 0 0 1	Base			
					[Reg16 + Disp8]			N	34 1 1	0 0 1 1 0 1 0 1 0 1	Base		Disp8	
					[Reg16 + Disp16]			N	34 2 1	0 0 1 1 0 1 1 0 0 1	Base		Disp16	
High	Compare	CMP	Zero Page	8	Register8	←-	[Disp8]	M	64 3 0	0 1 1 0 0 1 1 1 0 0		Dest	Disp8	
						-→	[Disp8]	M	64 3 2	0 1 1 0 0 1 1 1 1 0		Source	Disp8	
Med				16	Register16	←-	[Disp8]	M	64 3 1	0 1 1 0 0 1 1 1 0 1		Dest	Disp8	
						-→	[Disp8]	M	64 3 3	0 1 1 0 0 1 1 1 1 1		Source	Disp8	
Med				8	Immediate8	-→	[Disp8]	M	6C 3 2	0 1 1 0 1 1 1 1 1 0			Disp8	Immediate8
				16	Immediate16	-→	[Disp8]	M	6C 3 3	0 1 1 0 1 1 1 1 1 1			Disp8	Immediate16
			Near	8	Register8	←-	Immediate8	M	64 1 0	0 1 1 0 0 1 0 1 0 0		Dest	Immediate8	
Core							Register8	M	60 3 0	0 1 1 0 0 0 1 1 0 0	Source	Dest		
							[Disp16]	M	64 0 0	0 1 1 0 0 1 0 0 0 0		Dest	Disp16	
							[Reg16]	H	60 0 0	0 1 1 0 0 0 0 0 0 0	Base	Dest		
							[Reg16 + Disp8]	M	60 1 0	0 1 1 0 0 0 0 1 0 0	Base	Dest	Disp8	
							[Reg16 + Disp16]	H	60 2 0	0 1 1 0 0 0 1 0 0 0	Base	Dest	Disp16	
					Register8	-→	[Disp16]	M	64 0 2	0 1 1 0 0 1 0 0 1 0		Source	Disp16	
							[Reg16]	M	60 0 2	0 1 1 0 0 0 0 0 1 0	Base	Source		
High							[Reg16 + Disp8]	M	60 1 2	0 1 1 0 0 0 0 1 1 0	Base	Source	Disp8	
							[Reg16 + Disp16]	M	60 2 2	0 1 1 0 0 0 1 0 1 0	Base	Source	Disp16	
					Immediate8	-→	[Disp16]	L	6C 0 2	0 1 1 0 1 1 0 0 1 0			Disp16	Immediate8
							[Reg16]	L	68 0 2	0 1 1 0 1 0 0 0 1 0	Base		Immediate8	
							[Reg16 + Disp8]	L	68 1 2	0 1 1 0 1 0 0 1 1 0	Base		Disp8	Immediate8
							[Reg16 + Disp16]	L	68 2 2	0 1 1 0 1 0 1 0 1 0	Base		Disp16	Immediate8
				16	Register16	←-	Immediate16	M	64 2 1	0 1 1 0 0 1 1 0 0 1		Dest	Immediate16	
							Register16	M	60 3 1	0 1 1 0 0 0 1 1 0 1	Source	Dest		
							[Disp16]	M	64 0 1	0 1 1 0 0 1 0 0 0 1		Dest	Disp16	
							[Reg16]	H	60 0 1	0 1 1 0 0 0 0 0 0 1	Base	Dest		
							[Reg16 + Disp8]	M	60 1 1	0 1 1 0 0 0 0 1 0 1	Base	Dest	Disp8	
							[Reg16 + Disp16]	H	60 2 1	0 1 1 0 0 0 1 0 0 1	Base	Dest	Disp16	
Med					Register16	-→	[Disp16]	M	64 0 3	0 1 1 0 0 1 0 0 1 1		Source	Disp16	
							[Reg16]	M	60 0 3	0 1 1 0 0 0 0 0 1 1	Base	Source		
							[Reg16 + Disp8]	M	60 1 3	0 1 1 0 0 0 0 1 1 1	Base	Source	Disp8	
							[Reg16 + Disp16]	M	60 2 3	0 1 1 0 0 0 1 0 1 1	Base	Source	Disp16	
					Immediate16	-→	[Disp16]	L	6C 0 3	0 1 1 0 1 1 0 0 1 1			Disp16	Immediate16
							[Reg16]	L	68 0 3	0 1 1 0 1 0 0 0 1 1	Base		Immediate16	
							[Reg16 + Disp8]	L	68 1 3	0 1 1 0 1 0 0 1 1 1	Base		Disp8	Immediate16
							[Reg16 + Disp16]	L	68 2 3	0 1 1 0 1 0 1 0 1 1	Base		Disp16	Immediate16
High	And	AND	Zero Page	8	Register8	←	[Disp8]	M	A4 3 0	1 0 1 0 0 1 1 1 0 0		Dest	Disp8	
						→	[Disp8]	M	A4 3 2	1 0 1 0 0 1 1 1 1 0		Source	Disp8	
Med					Register16	←	[Disp8]	M	A4 3 1	1 0 1 0 0 1 1 1 0 1		Dest	Disp8	
						→	[Disp8]	M	A4 3 3	1 0 1 0 0 1 1 1 1 1		Source	Disp8	
Med					Immediate8	→	[Disp8]	M	AC 3 2	1 0 1 0 1 1 1 1 1 0			Disp8	Immediate8
					Immediate16	→	[Disp8]	M	AC 3 3	1 0 1 0 1 1 1 1 1 1			Disp8	Immediate16
			Near	8	Register8	←	Immediate8	L	A4 1 0	1 0 1 0 0 1 0 1 0 0		Dest	Immediate8	
Core							Register8	L	A0 3 0	1 0 1 0 0 0 1 1 0 0	Source	Dest		
							[Disp16]	L	A4 0 0	1 0 1 0 0 1 0 0 0 0		Dest	Disp16	
							[Reg16]	M	A0 0 0	1 0 1 0 0 0 0 0 0 0	Base	Dest		
							[Reg16 + Disp8]	L	A0 1 0	1 0 1 0 0 0 0 1 0 0	Base	Dest	Disp8	
							[Reg16 + Disp16]	M	A0 2 0	1 0 1 0 0 0 1 0 0 0	Base	Dest	Disp16	
					Register8	→	[Disp16]	L	A4 0 2	1 0 1 0 0 1 0 0 1 0		Source	Disp16	
							[Reg16]	L	A0 0 2	1 0 1 0 0 0 0 0 1 0	Base	Source		
High							[Reg16 + Disp8]	L	A0 1 2	1 0 1 0 0 0 0 1 1 0	Base	Source	Disp8	
							[Reg16 + Disp16]	L	A0 2 2	1 0 1 0 0 0 1 0 1 0	Base	Source	Disp16	
					Immediate8	→	[Disp16]	L	AC 0 2	1 0 1 0 1 1 0 0 1 0			Disp16	Immediate8
							[Reg16]	L	A8 0 2	1 0 1 0 1 0 0 0 1 0	Base		Immediate8	
							[Reg16 + Disp8]	L	A8 1 2	1 0 1 0 1 0 0 1 1 0	Base		Disp8	Immediate8
							[Reg16 + Disp16]	L	A8 2 2	1 0 1 0 1 0 1 0 1 0	Base		Disp16	Immediate8
				16	Register16	←	Immediate16	L	A4 2 1	1 0 1 0 0 1 1 0 0 1		Dest	Immediate16	
							Register16	L	A0 3 1	1 0 1 0 0 0 1 1 0 1	Source	Dest		
							[Disp16]	L	A4 0 1	1 0 1 0 0 1 0 0 0 1		Dest	Disp16	
							[Reg16]	M	A0 0 1	1 0 1 0 0 0 0 0 0 1	Base	Dest		
							[Reg16 + Disp8]	L	A0 1 1	1 0 1 0 0 0 0 1 0 1	Base	Dest	Disp8	
							[Reg16 + Disp16]	M	A0 2 1	1 0 1 0 0 0 1 0 0 1	Base	Dest	Disp16	
Med					Register16	→	[Disp16]	L	A4 0 3	1 0 1 0 0 1 0 0 1 1		Source	Disp16	
							[Reg16]	L	A0 0 3	1 0 1 0 0 0 0 0 1 1	Base	Source		
							[Reg16 + Disp8]	L	A0 1 3	1 0 1 0 0 0 0 1 1 1	Base	Source	Disp8	
							[Reg16 + Disp16]	L	A0 2 3	1 0 1 0 0 0 1 0 1 1	Base	Source	Disp16	
					Immediate16	→	[Disp16]	L	AC 0 3	1 0 1 0 1 1 0 0 1 1			Disp16	Immediate16
							[Reg16]	L	A8 0 3	1 0 1 0 1 0 0 0 1 1	Base		Immediate16	
							[Reg16 + Disp8]	L	A8 1 3	1 0 1 0 1 0 0 1 1 1	Base		Disp8	Immediate16
							[Reg16 + Disp16]	L	A8 2 3	1 0 1 0 1 0 1 0 1 1	Base		Disp16	Immediate16
High	Or	OR	Zero Page	8	Register8	←	[Disp8]	M	D4 3 0	1 1 0 1 0 1 1 1 0 0		Dest	Disp8	
						→	[Disp8]	M	D4 3 2	1 1 0 1 0 1 1 1 1 0		Source	Disp8	
Med					Register16	←	[Disp8]	M	D4 3 1	1 1 0 1 0 1 1 1 0 1		Dest	Disp8	
						→	[Disp8]	M	D4 3 3	1 1 0 1 0 1 1 1 1 1		Source	Disp8	
Med					Immediate8	→	[Disp8]	M	DC 3 2	1 1 0 1 1 1 1 1 1 0			Disp8	Immediate8
					Immediate16	→	[Disp8]	M	DC 3 3	1 1 0 1 1 1 1 1 1 1			Disp8	Immediate16
			Near	8	Register8	←	Immediate8	L	D4 1 0	1 1 0 1 0 1 0 1 0 0		Dest	Immediate8	
Core							Register8	L	D0 3 0	1 1 0 1 0 0 1 1 0 0	Source	Dest		
							[Disp16]	L	D4 0 0	1 1 0 1 0 1 0 0 0 0		Dest	Disp16	
							[Reg16]	M	D0 0 0	1 1 0 1 0 0 0 0 0 0	Base	Dest		
							[Reg16 + Disp8]	L	D0 1 0	1 1 0 1 0 0 0 1 0 0	Base	Dest	Disp8	
							[Reg16 + Disp16]	M	D0 2 0	1 1 0 1 0 0 1 0 0 0	Base	Dest	Disp16	
					Register8	→	[Disp16]	L	D4 0 2	1 1 0 1 0 1 0 0 1 0		Source	Disp16	
							[Reg16]	L	D0 0 2	1 1 0 1 0 0 0 0 1 0	Base	Source		
High							[Reg16 + Disp8]	L	D0 1 2	1 1 0 1 0 0 0 1 1 0	Base	Source	Disp8	
							[Reg16 + Disp16]	L	D0 2 2	1 1 0 1 0 0 1 0 1 0	Base	Source	Disp16	
					Immediate8	→	[Disp16]	L	DC 0 2	1 1 0 1 1 1 0 0 1 0			Disp16	Immediate8
							[Reg16]	L	D8 0 2	1 1 0 1 1 0 0 0 1 0	Base		Immediate8	
							[Reg16 + Disp8]	L	D8 1 2	1 1 0 1 1 0 0 1 1 0	Base		Disp8	Immediate8
							[Reg16 + Disp16]	L	D8 2 2	1 1 0 1 1 0 1 0 1 0	Base		Disp16	Immediate8
					Register16	←	Immediate16	L	D4 2 1	1 1 0 1 0 1 1 0 0 1		Dest	Immediate16	
							Register16	L	D0 3 1	1 1 0 1 0 0 1 1 0 1	Source	Dest		
							[Disp16]	L	D4 0 1	1 1 0 1 0 1 0 0 0 1		Dest	Disp16	
							[Reg16]	M	D0 0 1	1 1 0 1 0 0 0 0 0 1	Base	Dest		
							[Reg16 + Disp8]	L	D0 1 1	1 1 0 1 0 0 0 1 0 1	Base	Dest	Disp8	
							[Reg16 + Disp16]	M	D0 2 1	1 1 0 1 0 0 1 0 0 1	Base	Dest	Disp16	
Med				16			[Disp16]	L	D4 0 3	1 1 0 1 0 1 0 0 1 1		Source	Disp16	

Priority	Group	Instruction	Mnemonic	Mode	Size	Operand	Dir	Operand	Class	Opcode	Bits	Field	Field	Encoding
Med					16	Register16	→	[Reg16]	L	D0 0 3	11010000 11	Base	Source	
								[Reg16 + Disp8]	L	D0 1 3	11010001 11	Base	Source	Disp8
								[Reg16 + Disp16]	L	D0 2 3	11010010 11	Base	Source	Disp16
						Immediate16	→	[Disp16]	L	DC 0 3	11011100 11			Disp16, Immediate16
								[Reg16]	L	D8 0 3	11011000 11	Base		Immediate16
								[Reg16 + Disp8]	L	D8 1 3	11011001 11	Base		Disp8, Immediate16
								[Reg16 + Disp16]	L	D8 2 3	11011010 11	Base		Disp16, Immediate16
High		Exclusive Or	XOR	Zero Page	8	Register8	←	[Disp8]	H	74 3 0	01110111 00		Dest	Disp8
							→	[Disp8]	M	74 3 2	01110111 10		Source	Disp8
Med						Register16	←	[Disp8]	H	74 3 1	01110111 01		Dest	Disp8
							→	[Disp8]	H	74 3 3	01110111 11		Source	Disp8
Med						Immediate8	→	[Disp8]	M	7C 3 2	01111111 10			Disp8, Immediate8
						Immediate16	→	[Disp8]	M	7C 3 3	01111111 11			Disp8, Immediate16
	Logic			Near	8	Register8	←	Immediate8	M	74 1 0	01110101 00		Dest	Immediate8
Core								Register8	M	70 3 0	01110011 00	Source	Dest	
								[Disp16]	M	74 0 0	01110100 00		Dest	Disp16
								[Reg16]	H	70 0 0	01110000 00	Base	Dest	
								[Reg16 + Disp8]	M	70 1 0	01110001 00	Base	Dest	Disp8
								[Reg16 + Disp16]	H	70 2 0	01110010 00	Base	Dest	Disp16
						Register8	→	[Disp16]	M	74 0 2	01110100 10		Source	Disp16
								[Reg16]	M	70 0 2	01110000 10	Base	Source	
High								[Reg16 + Disp8]	M	70 1 2	01110001 10	Base	Source	Disp8
								[Reg16 + Disp16]	M	70 2 2	01110010 10	Base	Source	Disp16
						Immediate8	→	[Disp16]	L	7C 0 2	01111100 10			Disp16, Immediate8
								[Reg16]	L	78 0 2	01111000 10	Base		Immediate8
								[Reg16 + Disp8]	L	78 1 2	01111001 10	Base		Disp8, Immediate8
								[Reg16 + Disp16]	L	78 2 2	01111010 10	Base		Disp16, Immediate8
					16	Register16	←	Immediate16	M	74 2 1	01110110 01		Dest	Immediate16
								Register16	M	70 3 1	01110011 01	Source	Dest	
								[Disp16]	M	74 0 1	01110100 01		Dest	Disp16
								[Reg16]	H	70 0 1	01110000 01	Base	Dest	
								[Reg16 + Disp8]	M	70 1 1	01110001 01	Base	Dest	Disp8
								[Reg16 + Disp16]	H	70 2 1	01110010 01	Base	Dest	Disp16
Med						Register16	→	[Disp16]	M	74 0 3	01110100 11		Source	Disp16
								[Reg16]	M	70 0 3	01110000 11	Base	Source	
								[Reg16 + Disp8]	M	70 1 3	01110001 11	Base	Source	Disp8
								[Reg16 + Disp16]	M	70 2 3	01110010 11	Base	Source	Disp16
						Immediate16	→	[Disp16]	L	7C 0 3	01111100 11			Disp16, Immediate16
								[Reg16]	L	78 0 3	01111000 11	Base		Immediate16
								[Reg16 + Disp8]	L	78 1 3	01111001 11	Base		Disp8, Immediate16
								[Reg16 + Disp16]	L	78 2 3	01111010 11	Base		Disp16, Immediate16
Med		Not	NOT	Zero Page	8			[Disp8]	N	28 0 X	00101000			Disp8
					16			[Disp8]	N	28 1 X	00101001			Disp8
				Near	8			Register8	L	2C 3 0	00101111 00		Reg	
Core								[Disp16]	N	28 2 X	00101010			Disp16
								[Reg16]	N	2C 0 0	00101100 00	Base		
High								[Reg16 + Disp8]	N	2C 1 0	00101101 00	Base		Disp8
								[Reg16 + Disp16]	N	2C 2 0	00101110 00	Base		Disp16
					16			Register16	L	2C 3 1	00101111 01		Reg	
								[Disp16]	N	28 3 X	00101011			Disp16
Med								[Reg16]	N	2C 0 1	00101100 01	Base		
								[Reg16 + Disp8]	N	2C 1 1	00101101 01	Base		Disp8
								[Reg16 + Disp16]	N	2C 2 1	00101110 01	Base		Disp16
High		Test	TEST	Zero Page	8	Register8	←	[Disp8]	H	B4 3 0	10110111 00		Dest	Disp8
							→	[Disp8]	M	B4 3 2	10110111 10		Source	Disp8
Med						Register16	←	[Disp8]	H	B4 3 1	10110111 01		Dest	Disp8
							→	[Disp8]	H	B4 3 3	10110111 11		Source	Disp8
Med						Immediate8	→	[Disp8]	M	BC 3 2	10111111 10			Disp8, Immediate8
						Immediate16	→	[Disp8]	M	BC 3 3	10111111 11			Disp8, Immediate16
				Near	8	Register8	←	Immediate8	M	B4 1 0	10110101 00		Dest	Immediate8
Core								Register8	M	B0 3 0	10110011 00	Source	Dest	
								[Disp16]	M	B4 0 0	10110100 00		Dest	Disp16
								[Reg16]	H	B0 0 0	10110000 00	Base	Dest	
								[Reg16 + Disp8]	M	B0 1 0	10110001 00	Base	Dest	Disp8
								[Reg16 + Disp16]	H	B0 2 0	10110010 00	Base	Dest	Disp16
						Register8	→	[Disp16]	M	B4 0 2	10110100 10		Source	Disp16
								[Reg16]	M	B0 0 2	10110000 10	Base	Source	
High								[Reg16 + Disp8]	M	B0 1 2	10110001 10	Base	Source	Disp8
								[Reg16 + Disp16]	M	B0 2 2	10110010 10	Base	Source	Disp16
						Immediate8	→	[Disp16]	L	BC 0 2	10111100 10			Disp16, Immediate8
								[Reg16]	L	B8 0 2	10111000 10	Base		Immediate8
								[Reg16 + Disp8]	L	B8 1 2	10111001 10	Base		Disp8, Immediate8
								[Reg16 + Disp16]	L	B8 2 2	10111010 10	Base		Disp16, Immediate8
					16	Register16	←	Immediate16	M	B4 2 1	10110110 01		Dest	Immediate16
								Register16	M	B0 3 1	10110011 01	Source	Dest	
								[Disp16]	M	B4 0 1	10110100 01		Dest	Disp16
								[Reg16]	H	B0 0 1	10110000 01	Base	Dest	
								[Reg16 + Disp8]	M	B0 1 1	10110001 01	Base	Dest	Disp8
								[Reg16 + Disp16]	H	B0 2 1	10110010 01	Base	Dest	Disp16
Med						Register16	→	[Disp16]	M	B4 0 3	10110100 11		Source	Disp16
								[Reg16]	M	B0 0 3	10110000 11	Base	Source	
								[Reg16 + Disp8]	M	B0 1 3	10110001 11	Base	Source	Disp8
								[Reg16 + Disp16]	M	B0 2 3	10110010 11	Base	Source	Disp16
						Immediate16	→	[Disp16]	L	BC 0 3	10111100 11			Disp16, Immediate16
								[Reg16]	L	B8 0 3	10111000 11	Base		Immediate16
								[Reg16 + Disp8]	L	B8 1 3	10111001 11	Base		Disp8, Immediate16
								[Reg16 + Disp16]	L	B8 2 3	10111010 11	Base		Disp16, Immediate16
Core		Rotate Left	ROL	–	8			Register8, Immediate3	N	24 0 0	00100100 00	Imm3	Dest	
Med					16			Register16, Immediate3	N	24 0 1	00100100 01	Imm3	Dest	
High		Rotate Right	ROR	–	8			Register8, Immediate3	N	24 0 2	00100100 10	Imm3	Dest	
Med					16			Register16, Immediate3	N	24 0 3	00100100 11	Imm3	Dest	
Core		Rotate Left through Carry	RCL	–	8			Register8, Immediate3	N	24 1 0	00100101 00	Imm3	Dest	
Med					16			Register16, Immediate3	N	24 1 1	00100101 01	Imm3	Dest	
High	*Shift and Rotate*	Rotate Right through Carry	RCR	–	8			Register8, Immediate3	N	24 1 2	00100101 10	Imm3	Dest	
Med					16			Register16, Immediate3	N	24 1 3	00100101 11	Imm3	Dest	
Core		Shift Left	SHL	–	8			Register8, Immediate3	L	24 2 0	00100110 00	Imm3	Dest	
Med					16			Register16, Immediate3	L	24 2 1	00100110 01	Imm3	Dest	
High		Shift Logical Right	SHR	–	8			Register8, Immediate3	N	24 2 2	00100110 10	Imm3	Dest	
Med					16			Register16, Immediate3	N	24 2 3	00100110 11	Imm3	Dest	
High		Shift Arithmetic Right	SAR	–	8			Register8, Immediate3	N	24 3 2	00100111 10	Imm3	Dest	
Med					16			Register16, Immediate3	N	24 3 3	00100111 11	Imm3	Dest	
Core		Jump Unconditional	JMP	Near	–	Program16	←	Immediate16	H	C8 0 X	11001000			Disp16
Core								[Disp16]	H	C8 1 X	11001001			Disp16
High			JMPR	Short	–	Program16	←+	Immediate8	M	C8 3 X	11001011			Disp8
Core				Near				Immediate16	H	C8 2 X	11001010			Disp16
Core		Jump Overflow	JO	Near	–	Program16	←	Immediate16	M	E8 0 X	11101000			Disp16
Core								[Disp16]	M	E8 1 X	11101001			Disp16
High			JOR	Short	–	Program16	←+	Immediate8	L	E8 3 X	11101011			Disp8
Core				Near				Immediate16	M	E8 2 X	11101010			Disp16
Core		Jump Sign	JS	Near	–	Program16	←	Immediate16	M	E4 0 X	11100100			Disp16
Core								[Disp16]	M	E4 1 X	11100101			Disp16
High			JSR	Short	–	Program16	←+	Immediate8	L	E4 3 X	11100111			Disp8
Core				Near				Immediate16	M	E4 2 X	11100110			Disp16
Core		Jump Zero	JZ	Near	–	Program16	←	Immediate16	H	CC 0 X	11001100			Disp16
Core								[Disp16]	H	CC 1 X	11001101			Disp16

High	Branching	Jump Zero	JZR	Short	–	Program16	←+	Immediate8	M	CC 3 X	1 1 0 0 1 1 1 1	Disp8
Core				Near				Immediate16	H	CC 2 X	1 1 0 0 1 1 1 0	Disp16
Med		Jump Not Zero	JNZ	Near	–	Program16	←	Immediate16	H	F0 0 X	1 1 1 1 0 0 0 0	Disp16
								[Disp16]	H	F0 1 X	1 1 1 1 0 0 0 1	Disp16
Med			JNZR	Short	–	Program16	←+	Immediate8	M	F0 3 X	1 1 1 1 0 0 1 1	Disp8
				Near				Immediate16	H	F0 2 X	1 1 1 1 0 0 1 0	Disp16
Core		Jump Carry	JC	Near	–	Program16	←	Immediate16	M	E0 0 X	1 1 1 0 0 0 0 0	Disp16
Core								[Disp16]	M	E0 1 X	1 1 1 0 0 0 0 1	Disp16
High			JCR	Short	–	Program16	←+	Immediate8	L	E0 3 X	1 1 1 0 0 0 1 1	Disp8
Core				Near				Immediate16	M	E0 2 X	1 1 1 0 0 0 1 0	Disp16
Med		Jump Not Carry	JNC	Near	–	Program16	←	Immediate16	N	F4 0 X	1 1 1 1 0 1 0 0	Disp16
								[Disp16]	N	F4 1 X	1 1 1 1 0 1 0 1	Disp16
Med			JNCR	Short	–	Program16	←+	Immediate8	N	F4 3 X	1 1 1 1 0 1 1 1	Disp8
Med				Near				Immediate16	N	F4 2 X	1 1 1 1 0 1 1 0	Disp16
High		Jump Parity	JP	Near	–	Program16	←	Immediate16	M	EC 0 X	1 1 1 0 1 1 0 0	Disp16
High								[Disp16]	M	EC 1 X	1 1 1 0 1 1 0 1	Disp16
Med			JPR	Short	–	Program16	←+	Immediate8	L	EC 3 X	1 1 1 0 1 1 1 1	Disp8
High				Near				Immediate16	M	EC 2 X	1 1 1 0 1 1 1 0	Disp16
Core	Subroutines	Call	CALL	Near	–	Program16	←	Immediate16	H	10 0 X	0 0 0 1 0 0 0 0	Disp16
Core								[Disp16]	H	10 1 X	0 0 0 1 0 0 0 1	Disp16
High			CALLR	Short	–	Program16	←+	Immediate8	M	10 3 X	0 0 0 1 0 0 1 1	Disp8
Core				Near				Immediate16	H	10 2 X	0 0 0 1 0 0 1 0	Disp16
Core		Return	RET	–	–			–	L	04 0 X	0 0 0 0 0 1 0 0	X X
High								Immediate8	N	04 1 X	0 0 0 0 0 1 0 1	Immediate7 0
Core		Interrupt	INT	–	–			Immediate8	N	00 1 X	0 0 0 0 0 0 0 1	Interrupt7 0
Med		Breakpoint	BRK	–	–			–	N	00 0 X	0 0 0 0 0 0 0 0	X X
Core		Interrupt Return	IRET	–	–			–	N	04 2 X	0 0 0 0 0 1 1 0	X X
Med	Flag Manipulation	Clear Flag	CLF	–	–			Immediate8	N	DC 2 X	1 1 0 1 1 1 1 0	Flags8
Med		Set Flag	STF	–	–			Immediate8	N	DC 1 X	1 1 0 1 1 1 0 1	Flags8
Low		Complement Flag	CMF	–	–			Immediate8	N	7C 1 X	0 1 1 1 1 1 0 1	Flags8
High	Processor Control	Identification	CPUID	–	–			–	N	04 3 0	0 0 0 0 0 1 1 1	0 0
High		No Operation	NOP	–	–			–	N	00 2 X	0 0 0 0 0 0 1 0	X X
Core		Halt	HLT	–	–			–	N	04 3 3	0 0 0 0 0 1 1 1	1 1
Med		Wait	WAIT	–	–			Immediate4	N	04 3 2	0 0 0 0 0 1 1 1	1 0 Int4
Med	Expansion Instructions	Reserved for Expansion	–	–	–			–	–	00 3 X	0 0 0 0 0 0 1 1	X X
High		Maths Coprocessor	–	–	–			–	–	40 3 X	0 1 0 0 0 0 1 1	X X
High	Floating Point Instructions	FPU NOP	FNOP	–	–				L	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 0 0 0
High		Convert to Integer	FIXS	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 1 1 1
			FIXD	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 1 1 0
High		Convert to Floating Point	FLTS	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 1 0 1
			FLTD	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 1 0 0
High		Change Sign	CHSS	–	–				L	40 3 1	0 1 0 0 0 0 1 1	0 1 1 1 0 1 0 0
			CHSD	–	–				L	40 3 0	0 1 0 0 0 0 1 1	0 0 1 1 0 1 0 0
			CHSF	–	–				L	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 0 1 0 1
High		Exchange Stack	XCHS	–	–				L	40 3 1	0 1 0 0 0 0 1 1	0 1 1 1 1 0 0 1
			XCHD	–	–				L	40 3 0	0 1 0 0 0 0 1 1	0 0 1 1 1 0 0 1
			XCHF	–	–				L	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 0 0 1
Core		Pop FPU Stack	POPS						L	40 3 1	0 1 0 0 0 0 1 1	0 1 1 1 1 0 0 0
			POPD						L	40 3 0	0 1 0 0 0 0 1 1	0 0 1 1 1 0 0 0
			POPF						L	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 0 0 0
Core		Push FPU Stack	PTOS						L	40 3 1	0 1 0 0 0 0 1 1	0 1 1 1 0 1 1 1
			PTOD						L	40 3 0	0 1 0 0 0 0 1 1	0 0 1 1 0 1 1 1
			PTOF						L	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 0 1 1 1
Med			PUPI	–	–				L	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 1 0 1 0
Med		Integer Functions (16 bit)	SADD	–	–				M	40 3 1	0 1 0 0 0 0 1 1	0 1 1 0 1 1 0 0
			SSUB	–	–				M	40 3 1	0 1 0 0 0 0 1 1	0 1 1 0 1 1 0 1
			SMUL	–	–				M	40 3 1	0 1 0 0 0 0 1 1	0 1 1 0 1 1 1 0
			SMUU	–	–				M	40 3 1	0 1 0 0 0 0 1 1	0 1 1 1 0 1 1 0
			SDIV	–	–				M	40 3 1	0 1 0 0 0 0 1 1	0 1 1 0 1 1 1 1
Med		Integer Functions (32 bit)	DADD	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 1 0 1 1 0 0
			DSUB	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 1 0 1 1 0 1
			DMUL	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 1 0 1 1 1 0
			DMUU	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 1 1 0 1 1 0
			DDIV	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 1 0 1 1 1 1
Core		Floating Point Functions	FADD	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 0 0 0 0
			FSUB	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 0 0 0 1
			FMUL	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 0 0 1 0
			FDIV	–	–				M	40 3 0	0 1 0 0 0 0 1 1	0 0 0 1 0 0 1 1
High		Trigonometric Functions	SIN	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 0 1 0
			COS	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 0 1 1
			TAN	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 1 0 0
			ASIN	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 1 0 1
			ACOS	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 1 1 0
			ATAN	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 1 1 1
High		Exponential & Logarithmic Functions	SQRT	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 0 0 0 1
			LOG	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 1 0 0 0
			LN	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 1 0 0 1
			EXP	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 1 0 1 0
			PWR	–	–				H	40 3 0	0 1 0 0 0 0 1 1	0 0 0 0 1 0 1 1