${\bf Project~Carbon-JC~Series~Bus}$

	Description	Pin	В	Α	Pin	Description		
	+5 V DC power	+5V	B1	A1	GND	Ground		
	Machine cycle 1 indicator	/M1	В2	A2	/RESET	Primary reset		
	Interrupt request	/INT	В3	А3	CLK	Primary clock		
	Memory request	/MREQ	В4	A4	Α0			
	I/O request	/IORQ	В5	A5	A1		JC-40 (Standard)	
	Write strobe	/WR	В6	A6	A2			
	Read strobe	/RD	В7	A7	A3			
æ	–12 V DC power	-12V	В8	A8	A4			
arc	Serial transmit	TX	В9	A9	A5			
and	Serial receive	RX	B10	A10	A6			
(St	+12 V DC power	+12V	B11	A11	A7			
JC-40 (Standard)		D0	B12	A12	A8	16-bit address bus		
بخ	8-bit data bus	D1	B13	A13	A9			
		D2	B14	A14	A10			
		D3	B15	A15	A11	·······		
		D4	B16	A16	A12	·······		
		D5	B17	A17	A13	·······		
		D6	B18	A17	A14			
		D7	B19	A10	A14			
ŀ		+5V	B20	A19 A20	GND	Ground		
	+5 V DC power	+3V +12V		!		Ground	+	
	+12 V DC power		B21	A21	GND		-	
ŀ	+3.3 V DC power	+3.3V	B22	A22	GND	Ground		
İ	Secondary serial transmit	TX2	B23	A23	A16		JC-	
ed)	Secondary serial receive	RX2	B24	A24	A17			
anc	Non-maskable interrupt	/NMI	B25	A25	A18		4	
JC-64 (Enhanced)	CPU wait request	/WAIT	B26	A26	A19	24-bit address bus	JC-64 (Enhanced)	
† (E	CPU halt indicator	/HALT	B27	A27	A20			
9-	Bus request	/BUSREQ	B28	A28	A21			
ĕ	Bus acknowledge	/BUSACK	B29	A29	A22			
	Secondary clock	CLK2	B30	A30	A23		_	
ļ	Secondary reset	/RESET2	B31	A31	/RFSH	Refresh cycle indicator		
	+5 V DC power	+5V	B32	A32	GND	Ground		
	Trap breakpoint	/TRAP	B33	A33	GND	Ground		
ਓ	Address latch enable	ALE	B34	A34	GND	Ground	<u></u>	
nced)	Zilog direct memory access	/BAI	B35	A35	IEI	7ilog interrupt requests	JC-80	
JC-80 (Advai	Znog unect memory access	/BAO	B36	A36	IEO	Zilog interrupt requests		
₹		/DREQ0	B37	A37	/IRQ0		(Advanced)	
80	Direct memory access	/DACK0	B38	A38	/IRQ1			
۲		/DREQ1	B39	A39	/IRQ2	Interrupt requests		
		/DACK1	B40	A40	/IRQ3	········		
	Direct memory access	/DREQ2	B41	A41	/IRQ4		JC-100 (Ultimate)	
		/DACK2	B42	A42	/IRQ5			
<u>a</u>		/DREQ3	B43	A43	/IRQ6	Interrupt requests		
nate		/DACK3	B44	A44	/IRQ7			
JC-100 (Ultimate)	(Unassigned)	(NC)	B45	A45	(NC)	(Unassigned)	00 (
9	(Unassigned)	(NC)	B46	A46	(NC)	(Unassigned)	Į.	
100	Bus lock	/LOCK	B47	A47	VMA	Valid memory address	ij	
<u>ن</u>	Program store enable	/PSEN	B48	A48	/FIRQ	Fast interrupt request	ate)	
7	+12 V DC power	+12V	B49	A49	GND	Ground	7	
	+5 V DC power	+5V	B50	A50	GND	Ground		
-	+3 V DC power	+3V D8	B51					
	16-bit data bus 	D9	B52	A51	/BHE	Byte high enable		
				A52	(RES)	(Reserved)		
Jed		D10	B53	A53	(NC)	(Unassigned)	JC-120 (eXtended)	
enc		D11	B54	A54	(NC)	(Unassigned)		
JC-120 (eXtended)		D12	B55	A55	(NC)	(Unassigned)		
		D13	B56	A56	(NC)	(Unassigned)		
		D14	B57	A57	(NC)	(Unassigned)	ıde	
		D15	B58	A58	(NC)	(Unassigned)	<u>e</u>	
	+3.3 V DC power	+3.3V	B59	A59	GND	Ground	_	
	+5 V DC power	+5V	B60	A60	GND	Ground		