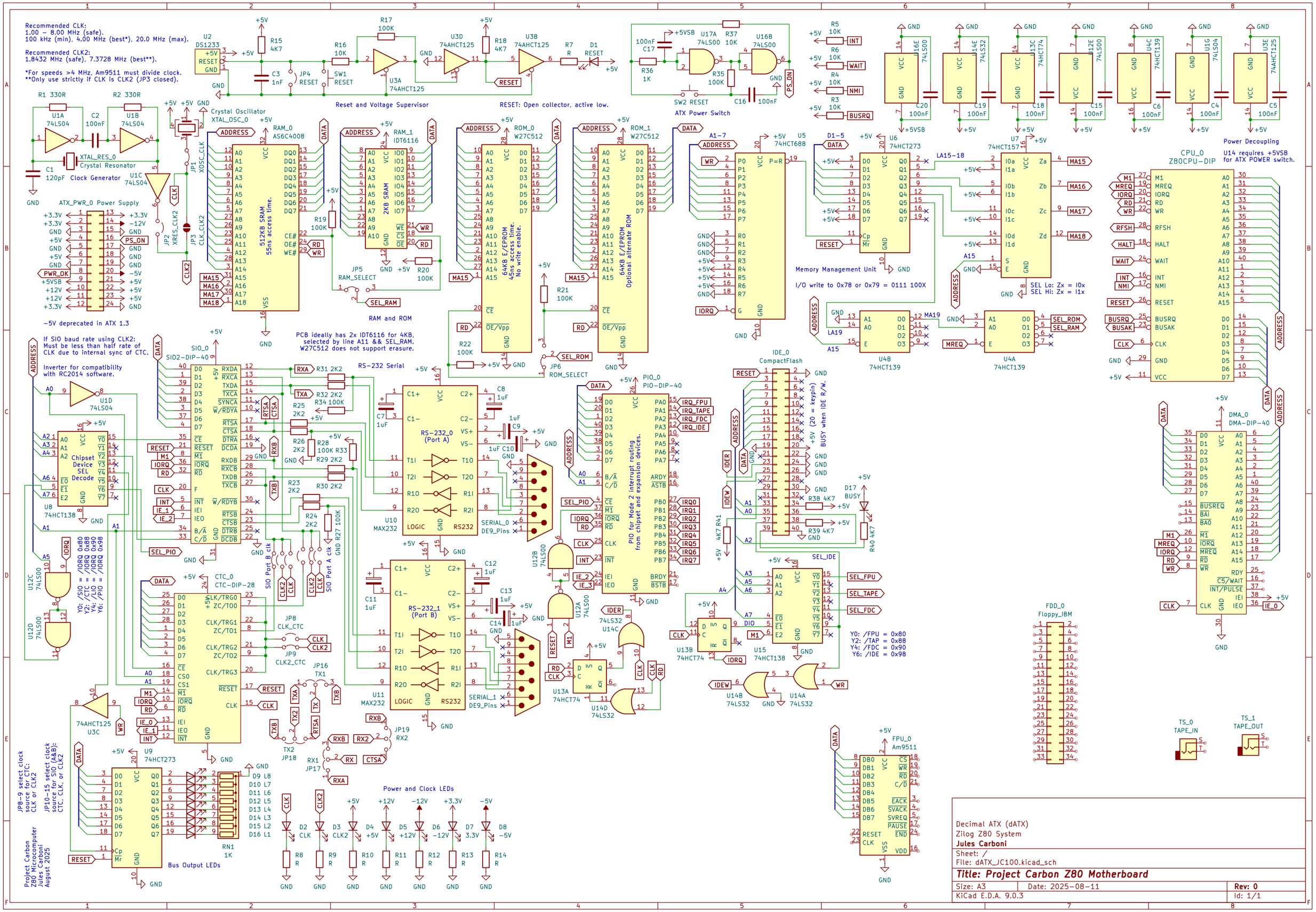
Recommended CLK:
1.00 – 8.00 MHz (safe).
100 kHz (min), 4.00 MHz (best*), 20.0 MHz (max).
Recommended CLK2:
1.8432 MHz (safe), 7.3728 MHz (best**).
*For speeds >4 MHz, Am9511 must divide clock.
**Only use strictly if CLK is CLK2 (JP3 closed).
Reset and Voltage Supervisor
RESET: Open collector, active low.
ATX Power Switch
Power Decoupling
U14 requires +5VSB for ATX POWER switch.
Crystal Oscillator
XTAL_OSC_0
Crystal Resonator
Clock Generator
ATX_PWR_0 Power Supply
−5V deprecated in ATX 1.3
RAM_0
AS6C4008
512KB SRAM
55ns access time.
RAM_1
IDT6116
2KB SRAM
RAM and ROM
ROM_0
W27C512
64KB E/EPROM
45ns access time.
No write enable.
ROM_1
64KB E/EPROM
Optional alternate ROM
PCB ideally has 2x IDT6116 for 4KB,
selected by line A11 && SEL_RAM.
W27C512 does not support erasure.
74HCT688
74HCT273
Memory Management Unit
I/O write to 0x78 or 0x79 = 0111 100X
74HCT157
SEL Lo: Zx = I0x
SEL Hi: Zx = I1x
74HCT139
CPU_0
Z80CPU-DIP
If SIO baud rate using CLK2:
Must be less than half rate of
CLK due to internal sync of CTC.
Inverter for compatibility
with RC2014 software.
SIO_0
SIO2-DIP-40
RS-232 Serial
Chipset
Device
SEL
Decode
74HCT138
RS-232_0
(Port A)
RS-232_1
(Port B)
MAX232
PIO_0
PIO-DIP-40
PIO for Mode 2 interrupt routing
and expansion devices.
IDE_0
CompactFlash
DMA_0
DMA-DIP-40
CTC_0
CTC-DIP-28
SIO Port B Clk
SIO Port A clk
CLK_CTC
CLK2_CTC
SEL_IDE
FDD_0
Floppy_IBM
TAPE_IN
TAPE_OUT
FPU_0
Am9511
Y0: /FPU = 0x80
Y2: /TAP = 0x88
Y4: /FDC = 0x90
Y6: /IDE = 0x98
JP8–9 select clock
source for CTC:
CLK or CLK2
JP10–15 select clock
source for SIO (A&B):
CTC, CLK, or CLK2
Bus Output LEDs
Power and Clock LEDs
Project Carbon
Z80 Microcomputer
Jules Carboni
August 2025
Decimal ATX (dATX)
Zilog Z80 System
Jules Carboni
Sheet: /
File: dATX_JC100.kicad_sch
Title: Project Carbon Z80 Motherboard
Size: A3
Date: 2025-08-11
Rev: 0
KiCad E.D.A. 9.0.3
Id: 1/1