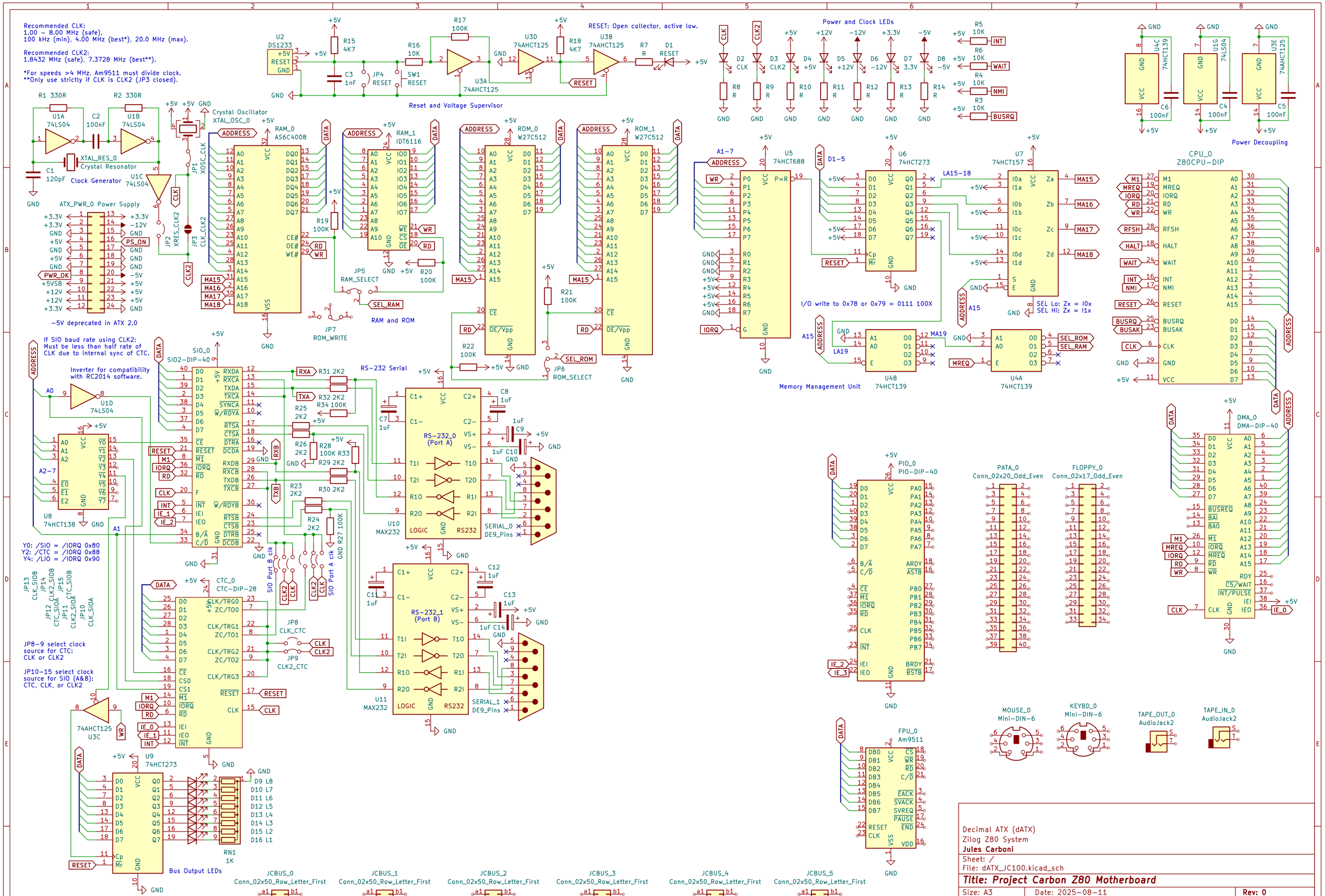
Recommended CLK:
1.00 – 8.00 MHz (safe).
100 kHz (min), 4.00 MHz (best*), 20.0 MHz (max).
Recommended CLK2:
1.8432 MHz (safe), 7.3728 MHz (best**).
*For speeds >4 MHz, Am9511 must divide clock.
**Only use strictly if CLK is CLK2 (JP3 closed).
Reset and Voltage Supervisor
RESET: Open collector, active low.
Power and Clock LEDs
Power Decoupling
Clock Generator
Crystal Oscillator
ATX_PWR_0 Power Supply
–5V deprecated in ATX 2.0
RAM and ROM
Memory Management Unit
I/O write to 0x78 or 0x79 = 0111 100X
SEL Lo: Zx = I0x
SEL Hi: Zx = I1x
RS-232 Serial
If SIO baud rate using CLK2:
Must be less than half rate of
CLK due to internal sync of CTC.
Inverter for compatibility
with RC2014 software.
Y0: /SIO = /IORQ 0x80
Y2: /CTC = /IORQ 0x88
Y4: /LIO = /IORQ 0x90
JP8–9 select clock
source for CTC:
CLK or CLK2
JP10–15 select clock
source for SIO (A&B):
CTC, CLK, or CLK2
Bus Output LEDs
Decimal ATX (dATX)
Zilog Z80 System
Jules Carboni
Sheet: /
File: dATX_JC100.kicad_sch
Title: Project Carbon Z80 Motherboard
Size: A3
Date: 2025-08-11
Rev: 0
KiCad E.D.A. 9.0.3
Id: 1/1