${\bf Project~Carbon-JC~Series~Bus}$

| | Description | Pin | В | Α | Pin | Description | |
|-------------------|-------------------------------------|--------------------------|--------------------------|--------------------------|--------------------------|---------------------------------|-------------------|
| | +5 V DC power | +5V | B1 | A 1 | GND | Ground | |
| | Machine cycle 1 indicator | /M1 | B2 | A2 | /RESET | Primary reset | |
| | Interrupt request | /INT | В3 | A3 | CLK | Primary clock | |
| | Memory request | /MREQ | В4 | A4 | A0 | 16-bit address bus Ground | |
| | I/O request | /IORQ | В5 | A5 | A1 | | |
| | Write strobe | /WR | В6 | A6 | A2 | | |
| | Read strobe | /RD | В7 | A7 | A3 | | |
| | −12 V DC power | -12V | В8 | A8 | A4 | | _ ا |
| JC-40 (Standard) | Serial transmit | TX | В9 | A9 | A5 | | JC-40 (Standard) |
| p - | Serial receive | RX | B10 | A10 | A6 | | |
| Sta | +12 V DC power | +12V | B11 | A11 | A7 | | |
| 6 | +12 V DC power | D0 | B12 | A11 | A8 | | nda |
| <u>č</u> | 8-bit data bus | | | | | | ď |
| 1 | | D1 | B13 | A13 | A9 | | |
| | | D2 | B14 | A14 | A10 | | |
| | | D3 | B15 | A15 | A11 | | |
| | | D4 | B16 | A16 | A12 | | |
| | | D5 | B17 | A17 | A13 | | |
| | | D6 | B18 | A18 | A14 | | |
| | | D7 | B19 | A19 | A15 | | |
| | +5 V DC power | +5 V | B20 | A20 | GND | | |
| | +12 V DC power | +12V | B21 | A21 | GND | Ground | |
| | +3.3 V DC power | +3.3V | B22 | A22 | GND | Ground | |
| JC-64 (Enhanced) | Secondary serial transmit | TX2 | B23 | A23 | A16 | 24-bit address bus | |
| | Secondary serial receive | RX2 | B24 | A24 | A17 | | _ |
| | Non-maskable interrupt | /NMI | B25 | A25 | A18 | | Ó |
| | CPU wait request | /WAIT | B26 | A26 | A19 | | 4 (F) |
| | CPU halt indicator | /HALT | B27 | A27 | A20 | | n |
| 4 | Bus request | | B28 | A28 | A21 | | anc |
| 2 | | | ••••• | | | | JC-64 (Enhanced) |
| | Bus acknowledge | /BUSACK | B29 | A29 | A22 | | |
| | Secondary clock | CLK2 | B30 | A30 | A23 | Pafrach cycle indicator | |
| | Secondary reset | /RESET2 | B31 | A31 | /RFSH | Refresh cycle indicator | |
| | +5 V DC power | +5V | B32 | A32 | GND | Ground | |
| | Trap breakpoint | /TRAP | B33 | A33 | GND | Ground | |
| (pa | Address latch enable | ALE | B34 | A34 | GND | Ground | JC-80 |
| Suc | Zilog direct memory access | /BAI | B35 | A35 | IEI | Zilog interrupt requests | |
| JC-80 (Advanced) | , | /BAO | | A36 | IEO | Interrupt requests | |
| | Direct memory access | /DREQ0 | B37 | A37 | /IRQ0 | | Va |
| 86 | | /DACK0 | B38 | A38 | /IRQ1 | | (Advanced) |
| 2 | | /DREQ1 | B39 | A39 | /IRQ2 | | |
| | | /DACK1 | B40 | A40 | /IRQ3 | | |
| | Direct memory access | /DREQ2 | B41 | A41 | /IRQ4 | Interrupt requests (Unassigned) | |
| | | /DACK2 | B42 | A42 | /IRQ5 | | |
| JC-100 (Ultimate) | | /DREQ3 | B43 | A43 | /IRQ6 | | _ |
| | | /DACK3 | B44 | A44 | /IRQ7 | | 12 |
| | (Unassigned) | (NC) | B45 | A45 | (NC) | | |
| | (Unassigned) | (NC) | B46 | A46 | (NC) | (Unassigned) | JC-100 (Ultimate) |
| | Bus lock | /LOCK | B47 | A47 | VMA | Valid memory address | |
| | Program store enable | /PSEN | B48 | A48 | /FIRQ | Fast interrupt request | e e |
| | +12 V DC power | •••••• | | A49 | GND | Ground | |
| | | +12V | B49 | l | | | |
| | +5 V DC power | +5V | B50 | A50 | GND | | |
| | | D8 | B51 | A51 | A24 | | |
| - 1 | | D9 | B52 | A52 | A25 | | . |
| | | _ | | A F 2 | A26 | | ~ |
| ed) | | D10 | B53 | A53 | | | 1.50 |
| ended) | 16-hit data hus: | D11 | B54 | A54 | A27 | 32-hit address hus | 71.7 |
| (Xtended) | 16-bit data bus | | | | | 32-bit address bus | 120 (e |
|) (eXtended) | 16-bit data bus | D11 | B54 | A54 | A27 | 32-bit address bus | :-120 (exte |
| 120 (eXtended) | 16-bit data bus | D11 D12 | B54 B55 | A54 A55 | A27 A28 | 32-bit address bus | -120 (eXtend |
| JC-120 (eXtended) | 16-bit data bus | D11 D12 D13 | B54 B55 B56 | A54 A55 A56 | A27 A28 A29 | 32-bit address bus | :-120 (eXtended) |
| JC-120 (eXtended) | 16-bit data bus | D11 D12 D13 D14 | B54 B55 B56 B57 | A54 A55 A56 A57 | A27 A28 A29 A30 | 32-bit address bus | JC-120 (eXtended) |