${\bf Project~Carbon-JC~Series~Bus}$

	Description	Pin	В		Α	Pin	Description	
JC-40 (Standard)	+5 V DC power	+5 V	В1	>>	A1	GND	Ground	JC-40 (Standard)
	Machine cycle 1 indicator	/M1	B2	70.00 22	A2	/RESET	Primary reset	
	Interrupt request	/INT	В3	<,<,	А3	CLK	Primary clock	
	Memory request	/MREQ	B4	//	A4	Α0	16-bit address bus	
	I/O request	/IORQ	B5		A5	A1		
	Write strobe	/WR	B6	/ /	A6	A2		
		/RD	B7		A7	A3		
	Read strobe							
	–12 V DC power	-12V	В8		A8	A4		
	Serial transmit	TX	В9		A9	A5		
	Serial receive	RX	B10		A10	A6		
	+12 V DC power	+12V	B11		A11	A7		
	 8-bit data bus 	D0	B12	11	A12	A8		
		D1	B13	111	A13	A9		
		D2	B14	<<	A14	A10		
		D3	B15	//	A15	A11		
Ì		D4	B16		A16	A12		
		D5		t. d 	A17	A13		
		D6	B18		A18	A14		
				d. d				
ļ		D7	B19		A19	A15		
	+5 V DC power	+5V	B20	-	A20	GND	Ground	
JC-64 (Enhanced)	+12 V DC power	+12V	B21	 .2 2	A21	GND	Ground	JC-64 (Enhanced)
	+3.3 V DC power	+3.3V	B22	<u>, ;</u>	A22	GND	Ground	
	Secondary serial transmit	TX2	B23	44	A23	A16		
	Secondary serial receive	RX2	B24	//	A24	A17		
	Non-maskable interrupt	/NMI	B25	//	A25	A18		
	CPU wait request	/WAIT	B26	77	A26	A19		
	CPU halt indicator	/HALT		77 77		A20		
	Bus request		B28		A28	A21		
	Bus acknowledge	/BUSACK	B29	<u></u>	A29	A22		
	Secondary clock	CLK2		<u> </u>	A30	A23		
	Secondary reset	/RESET2	B31	<u> </u>	A31	/RFSH	Refresh cycle indicator	
	+5 V DC power	+5V	B32	<u> </u>	A32	GND	Ground	
JC-80 (Advanced)	Trap breakpoint	/TRAP	B33	//	A33	GND	Ground	JC-80 (Advanced)
	Address latch enable	ALE	B34		A34	GND	Ground	
	→	/BAI	B35	//	A35	IEI	Zilog interrupt requests	
	Zilog direct memory access	/BAO	B36	//	A36	IEO		
PA T	Direct memory access	/DREQ0	B37		A37	/IRQ0	Interrupt requests	
00		/DACK0	B38		A38	/IRQ1		anc
JC			B39	-4 4 	A39			ed
		/DREQ1		<u>.</u>		/IRQ2		
		/DACK1	B40	22	A40	/IRQ3		
JC-100 (Ultimate)	Direct memory access	/DREQ2	B41	~~	A41	/IRQ4	Interrupt requests	
		/DACK2	B42	,,	A42	/IRQ5		į
		/DREQ3	B43	// 	A43	/IRQ6		JC
		/DACK3	B44	//	A44	/IRQ7		-10
	(Unassigned)	(NC)	B45	77	A45	(NC)	(Unassigned)	JC-100 (Ultimate)
	(Unassigned)	(NC)	B46		A46	(NC)	(Unassigned)	
	Bus lock	/LOCK	B47		A47	VMA	Valid memory address	
	Program store enable	/PSEN			A48	/FIRQ	Fast interrupt request	
	+12 V DC power	+12V			A49	GND	Ground	
JC-120 (eXtended)	+5 V DC power	+5V			A50	GND	Ground	
		D8		// \\	A51	/BHE	Byte high enable	JC-120 (eXtended)
	 16-bit data bus 	D9		//	A52	(RES)	(Reserved)	
		D10	B53	//	A53	(NC)	(Unassigned)	
		D11	B54	//	A54	(NC)	(Unassigned)	
		D12	B55	!! !!	A55	(NC)	(Unassigned)	
		D13	B56	22	A56	(NC)	(Unassigned)	
		D14	B57	··(-(<	A57	(NC)	(Unassigned)	
		D15	B58	,','	A58	(NC)	(Unassigned)	
	+3.3 V DC power	+3.3V	B59	44	A59	GND	Ground	
		•••••						
	+5 V DC power	+5V	B60	11	A60	GND	Ground	