	Description	Pin	В	Α	Pin	Description	
	+5 V DC power	+5V	B1	A1	GND	Ground	JC-64 (8 Bit)
	+12 V DC power	+12V	В2	A2	GND	Ground	
	−12 V DC power	–12V	В3	А3	GND	Ground	
	+3.3 V DC power	+3.3V	В4	A4	GND	Ground	
	Secondary clock	CLK2	В5	A5	TX2	Secondary serial transmit	
	Secondary reset	/RESET2	В6	A6	RX2	Secondary serial receive	
	Primary clock	CLK	В7	A7	TX	Serial transmit	
	Primary reset	/RESET	В8	A8	RX	Serial receive	
	Memory request	/MREQ	В9	A9	Α0	16-bit address bus	
	I/O request	/IORQ	B10	A10	A1		
	Write strobe	/WR	B11	A11	A2		
	Read strobe	/RD	B12	A12	A3		
	Machine cycle 1 indicator	/M1	B13	A13	A4		
	Interrupt request	/INT	B14	A14	A5		
Bit)	Non-maskable interrupt	/NMI	B15	A15	A6		
JC-64 (8 B	CPU wait request	/WAIT	B16	A16			
	CPU halt indicator	/HALT		A17			
	Bus request	/BUSREQ		A18	A9		
	Bus acknowledge	/BUSACK		4	A10		
	Refresh cycle indicator	/RFSH	B20	·	A11		
	Interrupt requests	/IRQ0	B21	A21	A12		
		/IRQ1	B22	. 	A13		
		/IRQ2		. 	A14		
		/IRQ3	B24	. 	A15		
	8-bit data bus	D0	B25	·	A16	24-bit address bus	
		D1	B26		A17		
		D2	B27		A18		
		D3	B28	·	A19		
		D4	B29		A20		
			B30	·	A21		
			B31	A31	A22		
			B32		A23		
	16-bit data bus	D8		i	A24	32-bit address bus	JC-100 (16 Bit)
		D9	B34	+	A25		
JC-100 (16 Bit)			B35	. 	A26		
		D11	B36	4	A27		
		D12		. 	A28		
		D13	B38	4	A29		
		D14		ļ	A30		
		D15		. 	A31		
	Interrupt requests	/IRQ4		A41	/DREQ0	Direct memory access	
		/IRQ5		A42	/DACK0		
10			B43	A43	/DREQ1		
<u>'</u>		/IRQ7	B44	A44	/DACK1		
1	Direct memory access—	/DREQ4		A45	/DREQ2	Direct memory access	
		/DACK4		A46	/DACK2		
		/DREQ5		A47	/DREQ3		
		/DACK5		A48	/DACK3		
	+5 V DC power	+5V		A49		Ground	
	+12 V DC power	+12V		A50		Ground	
	TIZ V DC power	TIZV	טכם	730	מוזט	Ground	i