	Description	Pin	В	Α	Pin	Description	
	+5 V DC power	+5 <b>V</b>	B1	<b>A</b> 1	GND	Ground	
	Machine cycle 1 indicator	/M1	В2	A2	/RESET	Primary reset Primary clock	
	Interrupt request	/INT	В3	<b>A</b> 3	CLK		
	Memory request	/MREQ	В4	A4	A0		
	I/O request	/IORQ	В5	A5	A1		
	Write strobe	/WR	В6	A6	A2		
	Read strobe	/RD	В7	A7	A3		
ਉ	–12 V DC power	-12V	В8	A8	A4		RC-40 (Standard)
<u>م</u>	Serial transmit	TX	В9	A9	A5		
au	Serial receive	RX	B10	A10	A6		6
St	+12 V DC power	+12V	B11	A11	A7		šta
RC-40 (Standard)		D0	B12	A12	A8	16-bit address bus	nd
Ü	8-bit data bus	D1	B13	A13	A9		arc
~		D2	B14	A14	A10		5
		D3	B15	A15	A11		
		D3	B16	A16	A11		
		D5	B17	A17	A13		
		······		A17			
		D6	B18		A14		
		D7	B19	A19	A15		
	+5 V DC power	+5V	B20	A20	GND	Ground	
	+12 V DC power	+12V	B21	A21	GND	Ground	
RC-64 (Enhanced)	+3.3 V DC power	+3.3V	B22	A22	GND	Ground	
	Secondary serial transmit	TX2	B23	A23	A16		찟
	Secondary serial receive	RX2	B24	A24	A17		RC-64 (Enhanced)
an	Non-maskable interrupt	/NMI	B25	A25	A18		4
u u	CPU wait request	/WAIT	B26	A26	A19		<u> </u>
<b>9</b>	CPU halt indicator	/HALT	B27	A27	A20		ha
64	Bus request		B28	A28	A21		ınc
RC-	Bus acknowledge	/BUSACK	B29	A29	A22		ed
	Secondary clock	CLK2	B30	A30	A23		$\sim$
	Secondary reset	/RESET2	B31	A31	/RFSH	Refresh cycle indicator	
	+5 V DC power	+5 <b>V</b>	B32	A32	GND	Ground	
_	Trap breakpoint	/TRAP	B33	A33	GND	Ground	_
eq	Address latch enable	ALE	B34	A34	GND	Ground	RC-80 (Advan
RC-80 (Advanced)	Zilog direct memory access	/BAI	B35	A35	IEI	Zilog interrupt requests	80
N S		/BAO	B36	A36	IEO		≨
4	Direct memory access-	/DREQ0	B37	A37	/IRQ0	Interrupt requests	ď
00		/DACK0	B38	A38	/IRQ1		an
٥		/DREQ1	B39	A39	/IRQ2		ced)
~		/DACK1	B40	A40	/IRQ3		9
		/DREQ2	B41	A41	/IRQ4		
	Direct memory access	/DACK2	B42	A42	/IRQ5	<del></del>	
te)		/DREQ3	B43	A43	/IRQ6	Interrupt requests	RC
RC-100 (Ultimate)		/DACK3	B44	A44	/IRQ7		RC-100 (Ultimate)
章	(Unassigned)	(NC)	B45	A44	(NC)	(Unassigned)	8
3	(Unassigned)		B45 B46	A45	(NC)	(Unassigned)	<b>a</b>
8		(NC)			VMA		<b>=</b>
5	Bus lock	/LOCK	B47	A47		Valid memory address	na
RC	Program store enable	/PSEN	B48	A48	/FIRQ	Fast interrupt request	
	+12 V DC power	+12V	B49	A49	GND	Ground	
	+5 V DC power	+5V	B50	A50	GND	Ground	
	16-bit data bus	D8	B51	A51	A24		
RC-120 (eXtended)		D9	B52	A52	A25		₽
		D10	B53	A53	A26		2
		D11	B54	A54	A27		RC-120 (eXtended)
		D12	B55	A55	A28		e
		D13	B56	A56	A29		Xt
		D14	B57	A57	A30		en
2				··I			0
C-12		D15	B58	A58	A31		<u>@</u>
RC-12	+3.3 V DC power	D15 +3.3V	B58 B59	A58 A59	GND	Ground	ed)