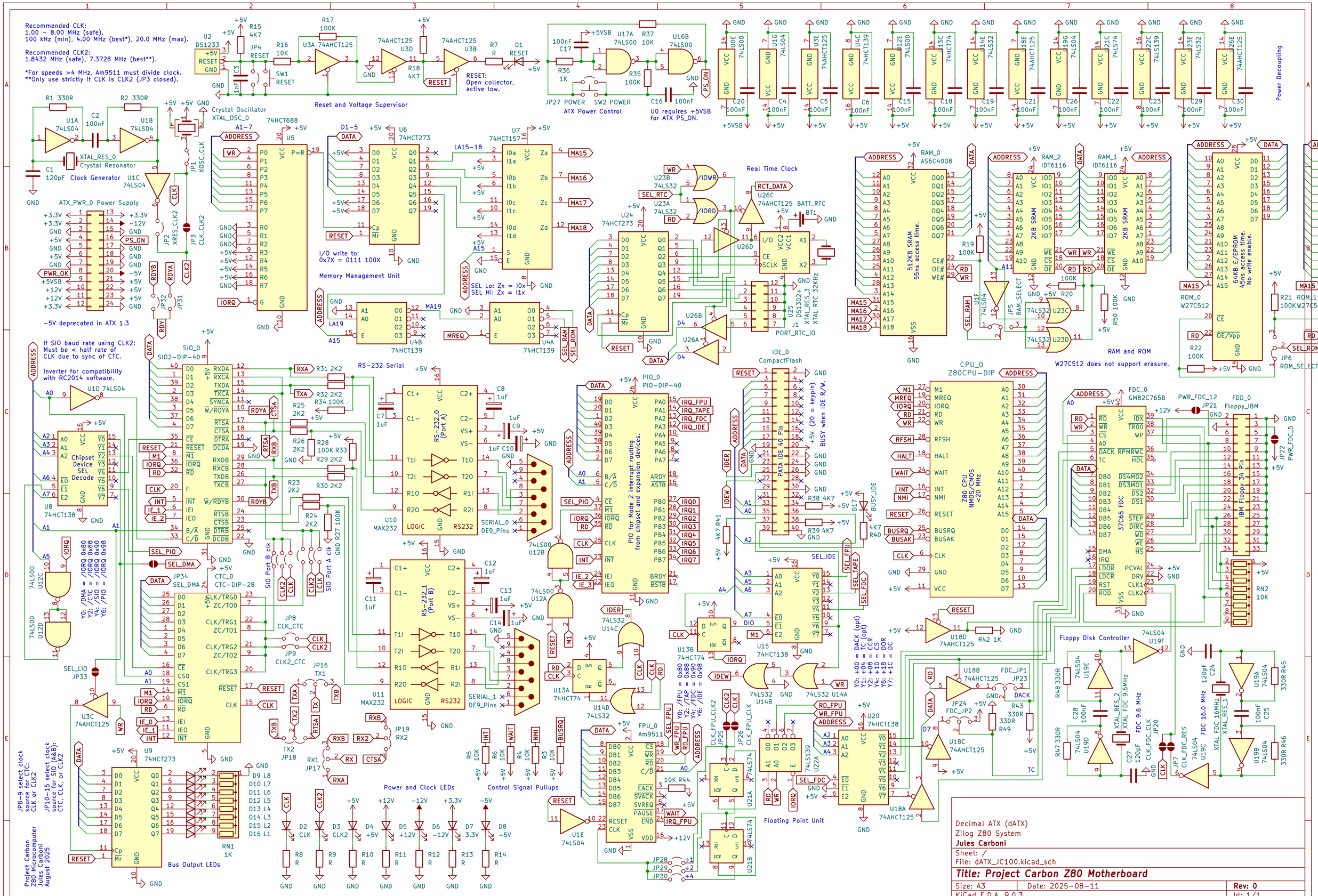
Recommended CLK:
1.00 – 8.00 MHz (safe).
100 kHz (min), 4.00 MHz (best*), 20.0 MHz (max).
Recommended CLK2:
1.8432 MHz (safe), 7.3728 MHz (best**).
*For speeds >4 MHz, Am9511 must divide clock.
**Only use strictly if CLK is CLK2 (JP3 closed).
Reset and Voltage Supervisor
RESET: Open collector, active low.
ATX Power Control
U0 requires +5VSB for ATX PS_ON.
Power Decoupling
Crystal Oscillator
Clock Generator
ATX_PWR_0 Power Supply
−5V deprecated in ATX 1.3
Memory Management Unit
I/O write to: 0x7X = 0111 100X
SEL Lo: Zx = I0x
SEL Hi: Zx = I1x
Real Time Clock
RAM_0 AS6C4008
512KB SRAM 55ns access time.
RAM_2 IDT6116
RAM_1 IDT6116
2KB SRAM
ROM_0 W27C512
64KB E/EPROM 45ns access time. No write enable.
RAM and ROM
W27C512 does not support erasure.
If SIO baud rate using CLK2: Must be < half rate of CLK due to sync of CTC.
Inverter for compatibility with RC2014 software.
RS-232 Serial
Chipset Device SEL Decode
PIO for Mode 2 interrupt routing from chipset and expansion devices.
IDE_0 CompactFlash
CPU_0 Z80CPU-DIP
Z80 CPU NMOS/CMOS <20 MHz
FDC_0 GM82C765B
37C65 FDC
Floppy Disk Controller
Floppy_IBM
IBM Floppy 34 Pin
Floating Point Unit
FPU_0 Am9511
Bus Output LEDs
Power and Clock LEDs
Control Signal Pullups
Project Carbon Z80 Motherboard
Jules Carboni
August 2025
Decimal ATX (dATX)
Zilog Z80 System
Jules Carboni
Sheet: /
File: dATX_JC100.kicad_sch
Title: Project Carbon Z80 Motherboard
Size: A3
Date: 2025-08-11
Rev: 0
KiCad E.D.A. 9.0.3
Id: 1/1