

Project Carbon — JC-Series Bus

<i>Description</i>	<i>Pin</i>	<i>B</i>	<i>A</i>	<i>Pin</i>	<i>Description</i>
+5 V DC power	+5V	B1	A1	GND	Ground
Machine cycle 1 indicator	/M1	B2	A2	/RESET	Primary reset
Interrupt request	/INT	B3	A3	CLK	Primary clock
Memory request	/MREQ	B4	A4	A0	16-bit address bus
Write strobe	/WR	B5	A5	A1	
Read strobe	/RD	B6	A6	A2	
I/O request	/IORQ	B7	A7	A3	
−12 V DC power	−12V	B8	A8	A4	
Serial transmit	TX	B9	A9	A5	
Serial receive	RX	B10	A10	A6	
+12 V DC power	+12V	B11	A11	A7	
8-bit data bus	D0	B12	A12	A8	
	D1	B13	A13	A9	
	D2	B14	A14	A10	
	D3	B15	A15	A11	
	D4	B16	A16	A12	
	D5	B17	A17	A13	
	D6	B18	A18	A14	
	D7	B19	A19	A15	
+5 V DC power	+5V	B20	A20	GND	Ground
+12 V DC power	+12V	B21	A21	GND	Ground
+3.3 V DC power	+3.3V	B22	A22	GND	Ground
Secondary serial transmit	TX2	B23	A23	A16	24-bit address bus
Secondary serial receive	RX2	B24	A24	A17	
Non-maskable interrupt	/NMI	B25	A25	A18	
CPU wait request	/WAIT	B26	A26	A19	
CPU halt indicator	/HALT	B27	A27	A20	
Bus request	/BUSREQ	B28	A28	A21	
Bus acknowledge	/BUSACK	B29	A29	A22	
Secondary clock	CLK2	B30	A30	A23	
Secondary reset	/RESET2	B31	A31	/RFSH	Refresh cycle indicator
+5 V DC power	+5V	B32	A32	GND	Ground
Trap breakpoint	/TRAP	B33	A33	GND	Ground
Address latch enable	ALE	B34	A34	GND	Ground
Zilog direct memory access	/BAI	B35	A35	IEI	Zilog interrupt requests
	/BAO	B36	A36	IEO	
Direct memory access	/DREQ0	B37	A37	/IRQ0	Interrupt requests
	/DACK0	B38	A38	/IRQ1	
	/DREQ1	B39	A39	/IRQ2	
	/DACK1	B40	A40	/IRQ3	
Direct memory access	/DREQ2	B41	A41	/IRQ4	Interrupt requests
	/DACK2	B42	A42	/IRQ5	
	/DREQ3	B43	A43	/IRQ6	
	/DACK3	B44	A44	/IRQ7	
(Unassigned)	(NC)	B45	A45	(NC)	(Unassigned)
(Unassigned)	(NC)	B46	A46	(NC)	(Unassigned)
+5 V DC power	+5V	B47	A47	GND	Ground
+12 V DC power	+12V	B48	A48	GND	Ground
Program store enable	/PSEN	B49	A49	/FIRQ	Fast interrupt request
Valid memory address	VMA	B50	A50	(RES)	(Reserved)

