

SCREW1
2 -56 UNC

SCREW2
2 -56 UNC

Max 0.3A@12V

Front panel grounding

shield clips

8 user LEDs

Maximum current for +/- 13V supply over SCSI connector is +/- 100mA

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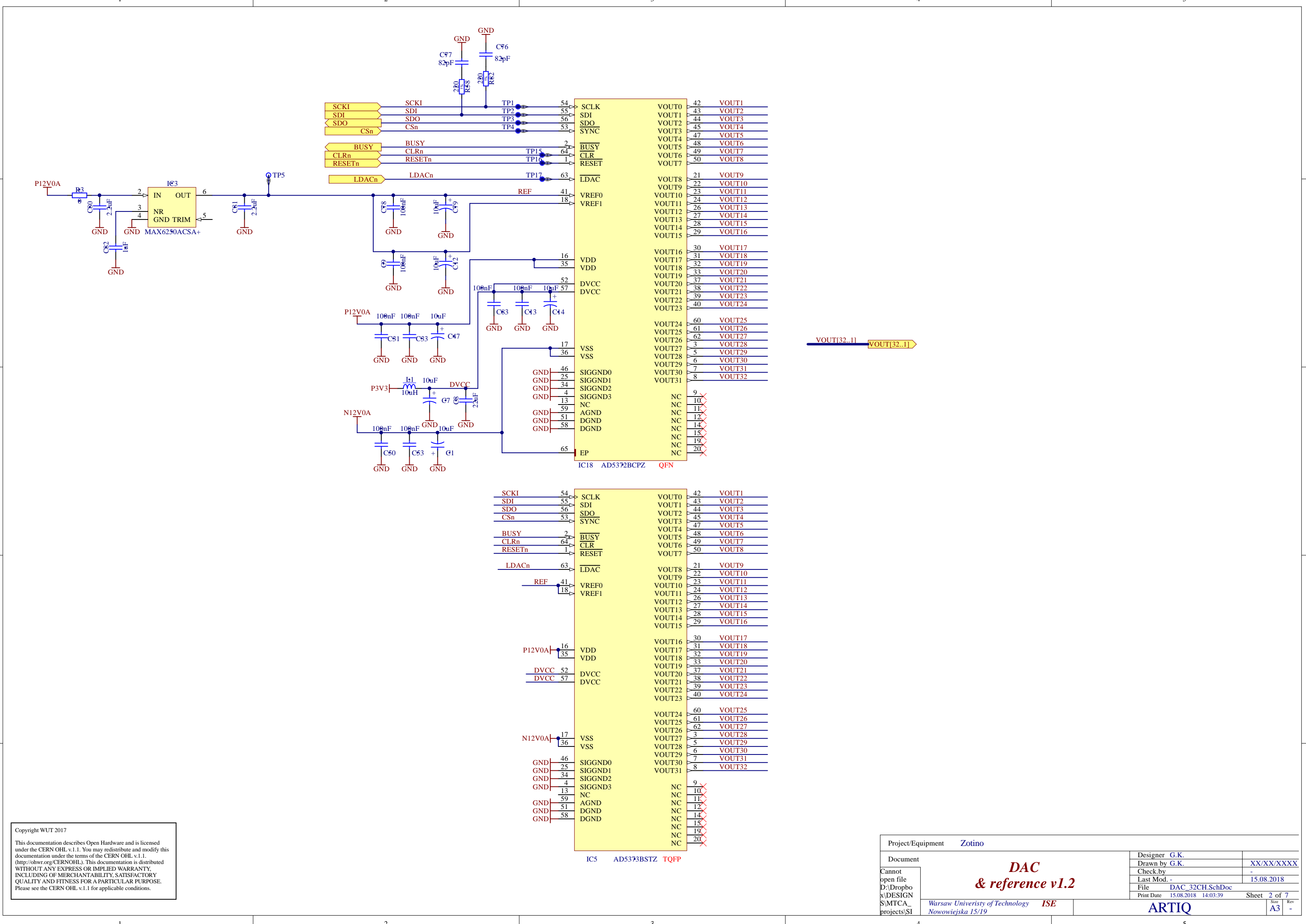
Project/Equipment		Zotino	
Document		Designer G.K.	
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		Check by	
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		File Zotino.schdoc	
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Zotino v1.2
32 channel 16 Bit DAC - TOP

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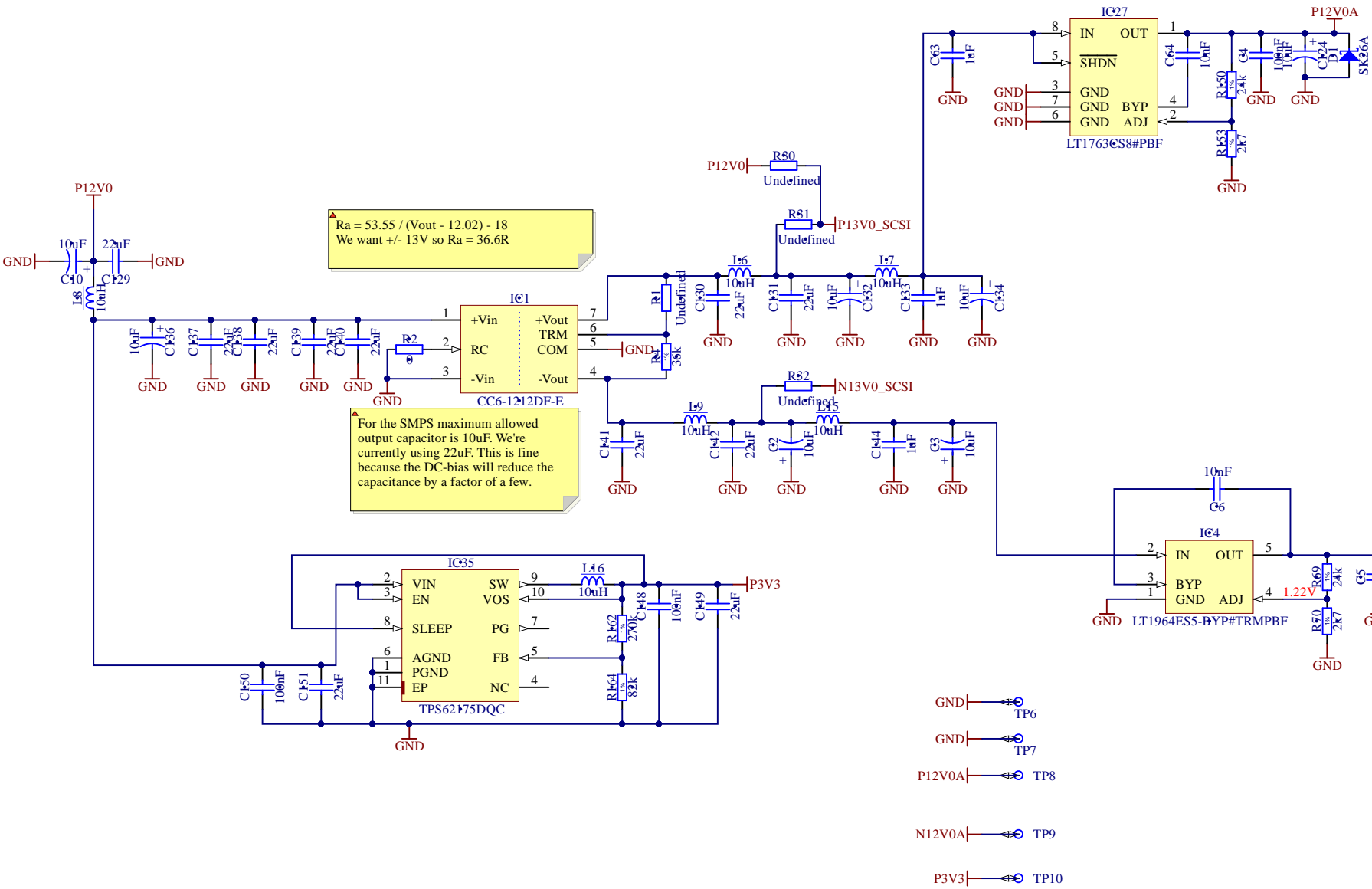
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Project/Equipment		Zotino	
Document		Designer	G.K.
Cannot open file D:\Dropbox\DESIGN\SI\MTCA_projects\SI	<i>Output filter v1.2</i>	Drawn by	G.K.
		Check by	-
		Last Mod. -	21.03.2018
		File	Output_channel.SchDoc
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Ra = 53.55 / (Vout - 12.02) - 18
We want +/- 13V so Ra = 36.6R

For the SMPS maximum allowed output capacitor is 10uF. We're currently using 22uF. This is fine because the DC-bias will reduce the capacitance by a factor of a few.

Power budget:			
opamp OPA197:	+13V rail	-13V rail	3.3V
32*1.5mA=48mA	48mA	48mA	
opam load 32*0.5mA	16mA	16mA	
DAC5373			
IDvcc 2mA 3.3V			2mA
Ivss -18mA -12V		18mA	
Ivdd 16mA 12V	16mA		
Reference	3mA		
SCSI connector	0mA	0mA	
LVDS interface 2x			330mA
LVDS load 4x24mA			96mA
Total load max	183mA	182mA	428mA
Total load min	64mA	63mA	250mA
Power max	2.3W	2.3W	1.4W
Power min	0.83	0.83	0.8
DC/DC converter losses	max: 0.92W; min:0.32		
Total power max (SCSI 2x 0mA + 0.5mA per out amp + 4 active LVDS outputs)			
Total power min (just supply current, 2 active LVDS)			
Power budget does not include TEC driver			

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Project/Equipment		Zotino	
Document		Designer	G.K.
		Drawn by	G.K.
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		Last Mod.	14.08.2018
		File	Supply_DAC.SchDoc
		Print Date	15.08.2018 14:03:40
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Zotino

Power supply v1.2

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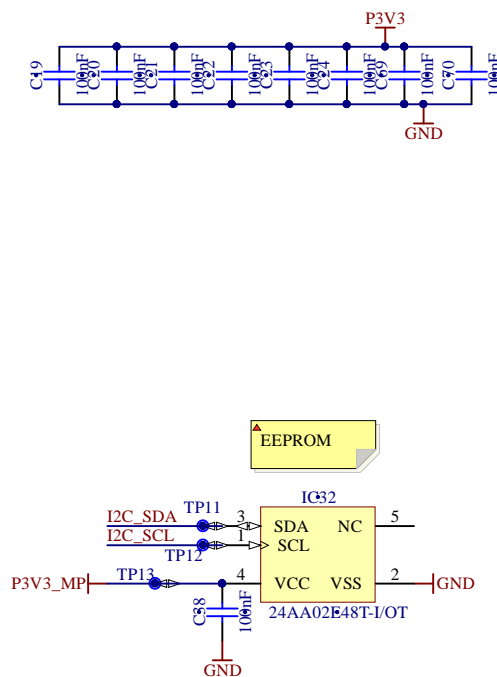
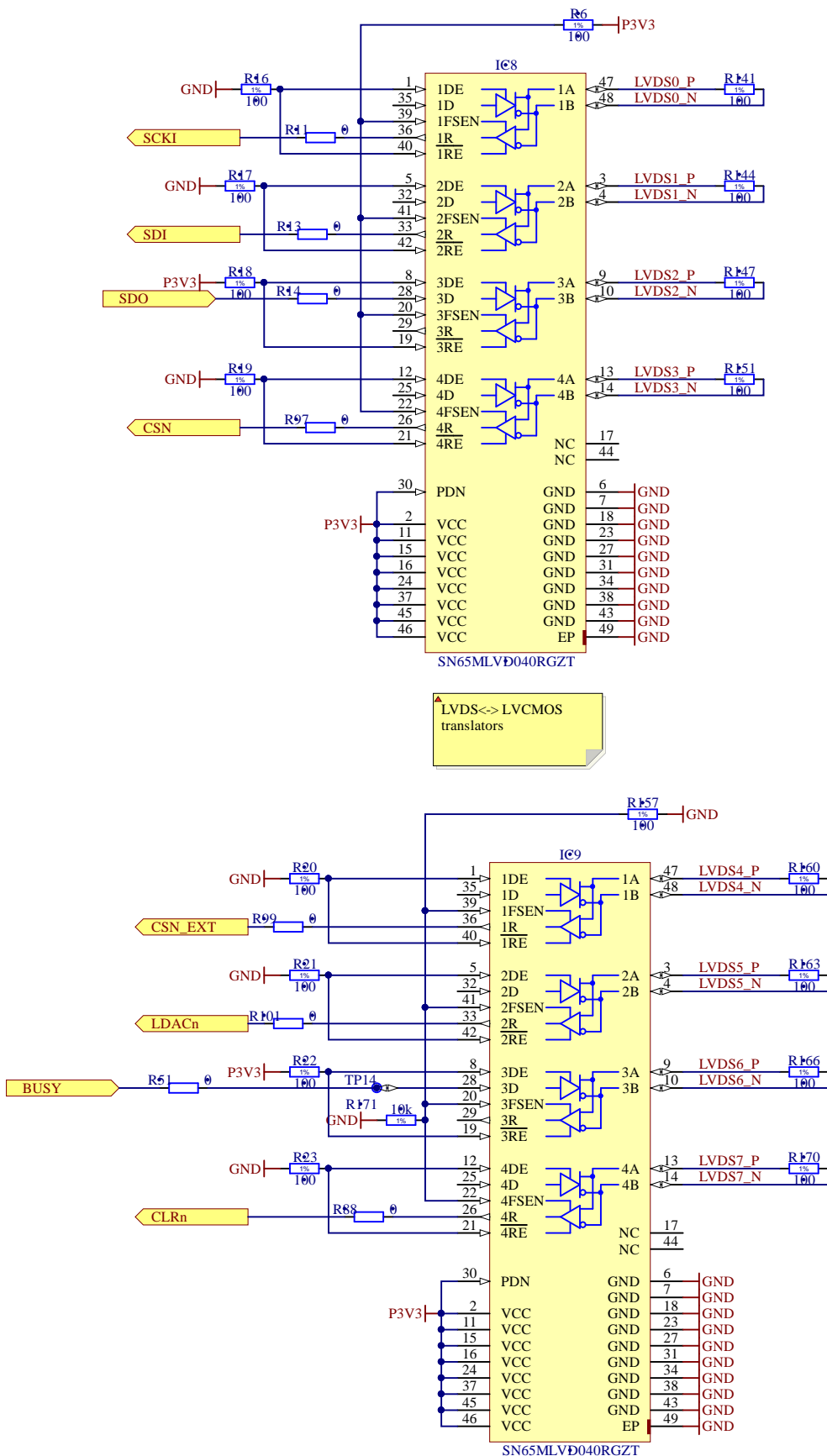
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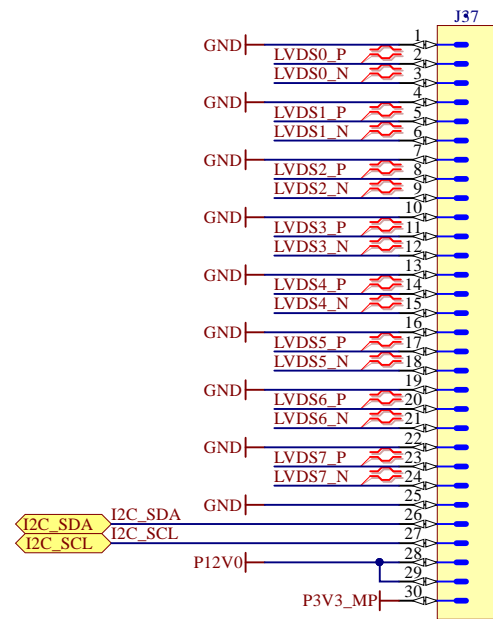
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EEM connector: IO are LVDS, I2C is 3V3 LVCMOS, P3V3_MP up to 20mA, P12V up to 1A.



Project/Equipment		Zotino	
Document	Designer		G.K.
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	Last Mod.		21.03.2018
	File		LVDS_IFC_DAC.SchDoc
Cannot open file D:\Dropbox\DESIGN\SI\MTCA_projects\SI	Print Date		15.08.2018 14:03:40
	Sheet		7 of 7
	Size		A3
	Rev		-
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