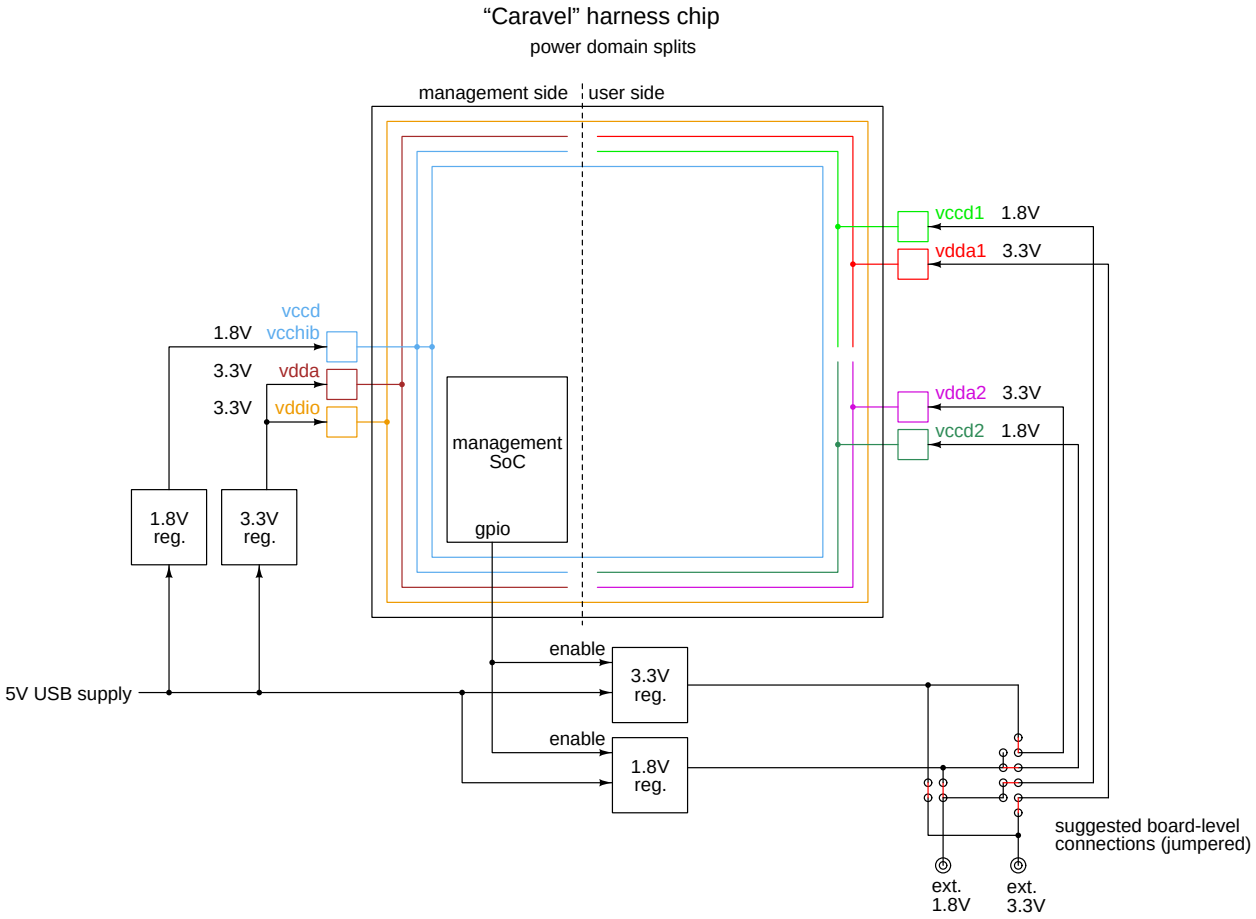
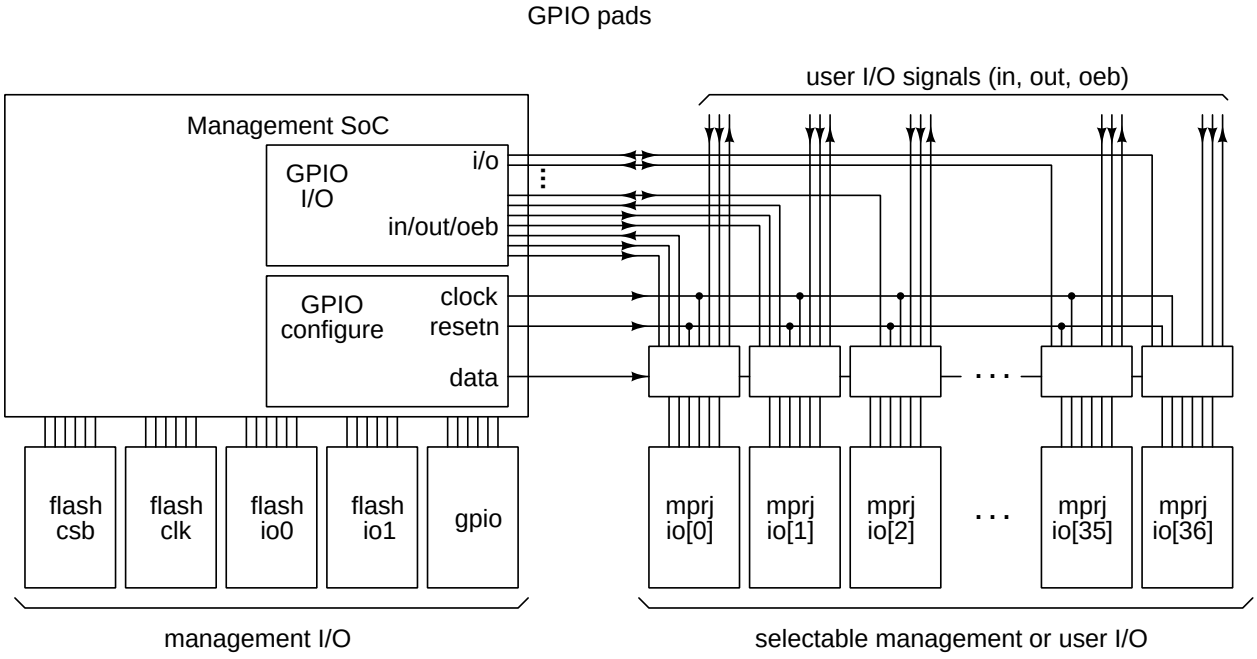
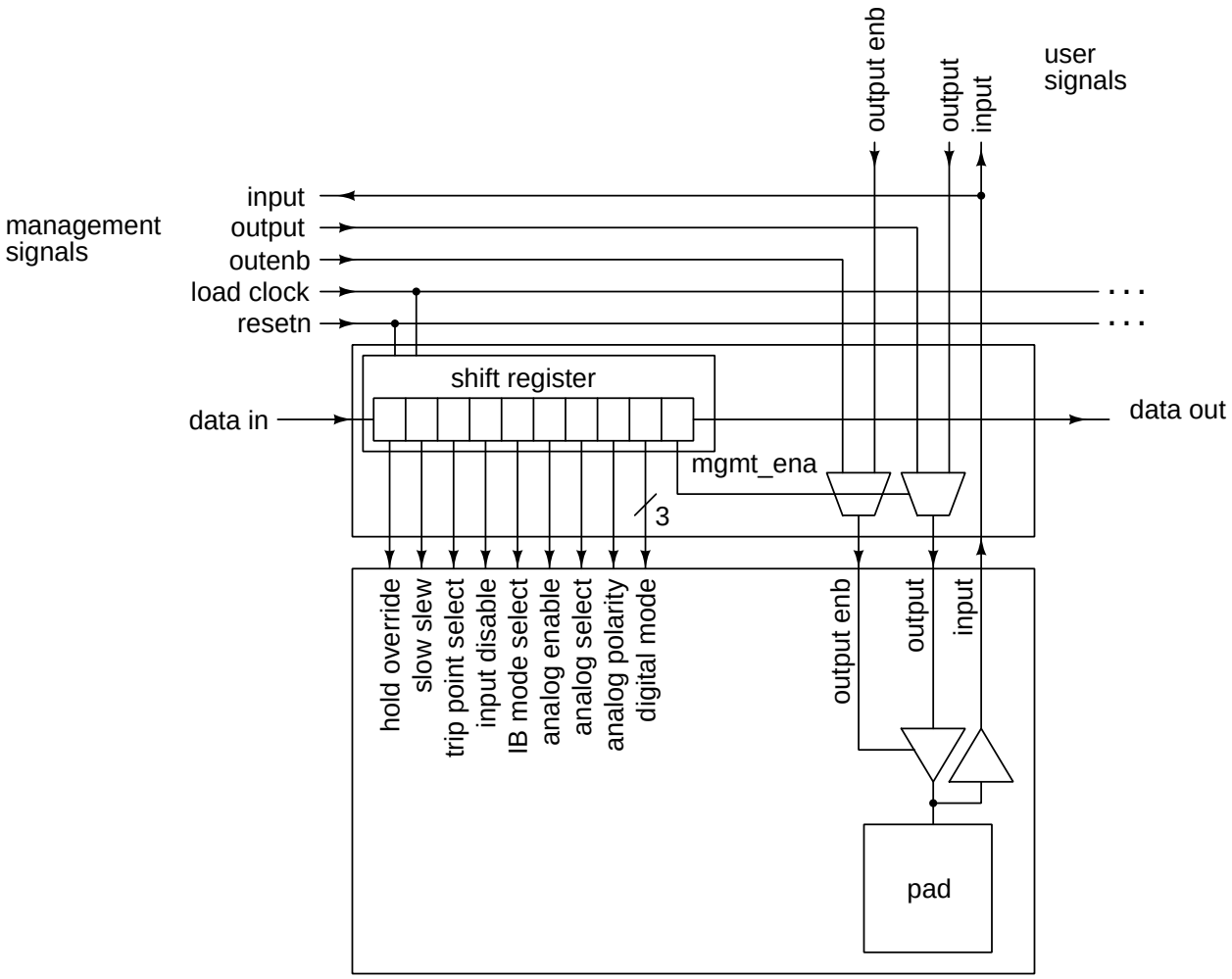

“Caravel” harness chip
power domain splits
management side
user side
vccd1 1.8V
vdda1 3.3V
vccd
1.8V vcchib
3.3V vdda
3.3V vddio
management SoC
gpio
vdda2 3.3V
vccd2 1.8V
1.8V reg.
3.3V reg.
enable
3.3V reg.
5V USB supply
enable
1.8V reg.
suggested board-level connections (jumpered)
ext. 1.8V
ext. 3.3V

“Caravel” harness chip

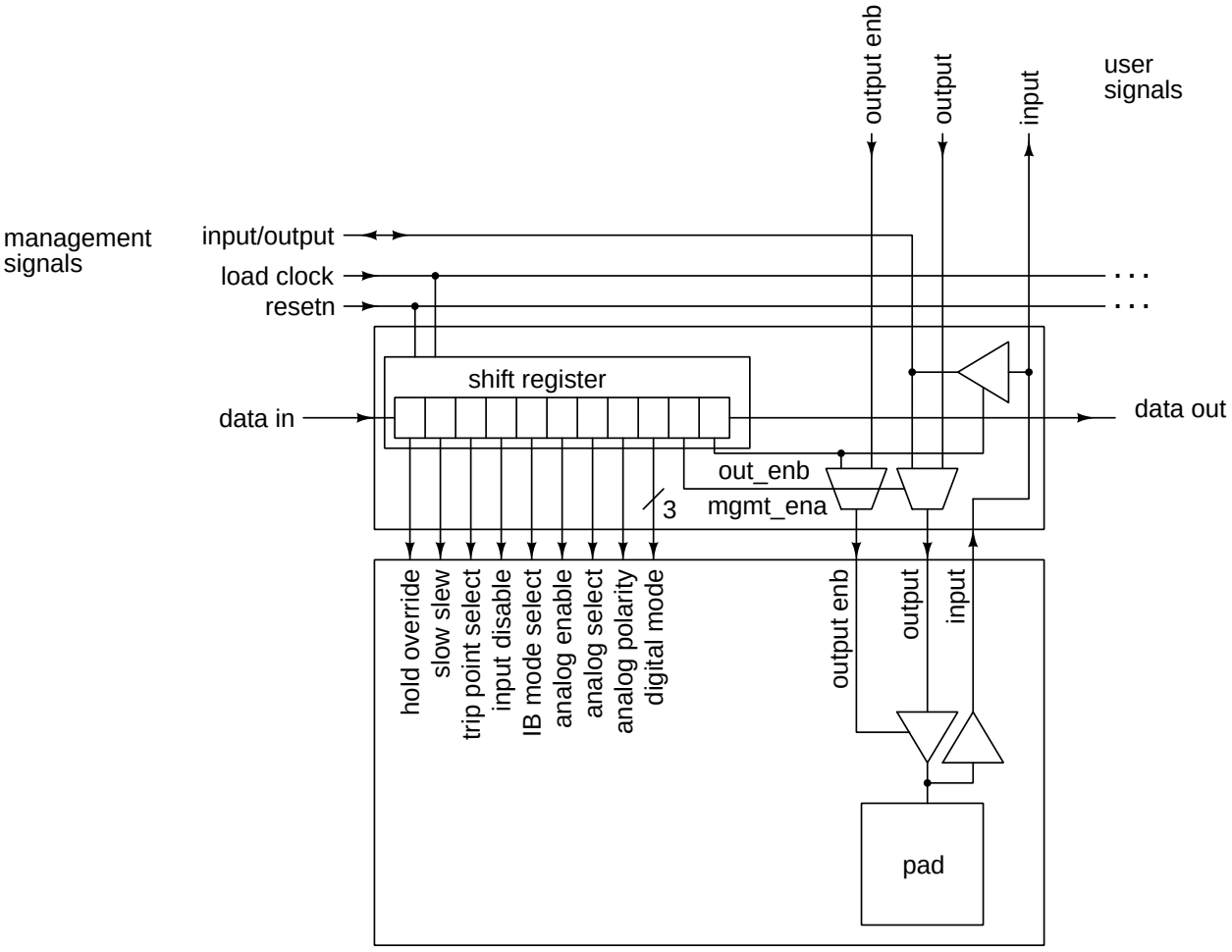


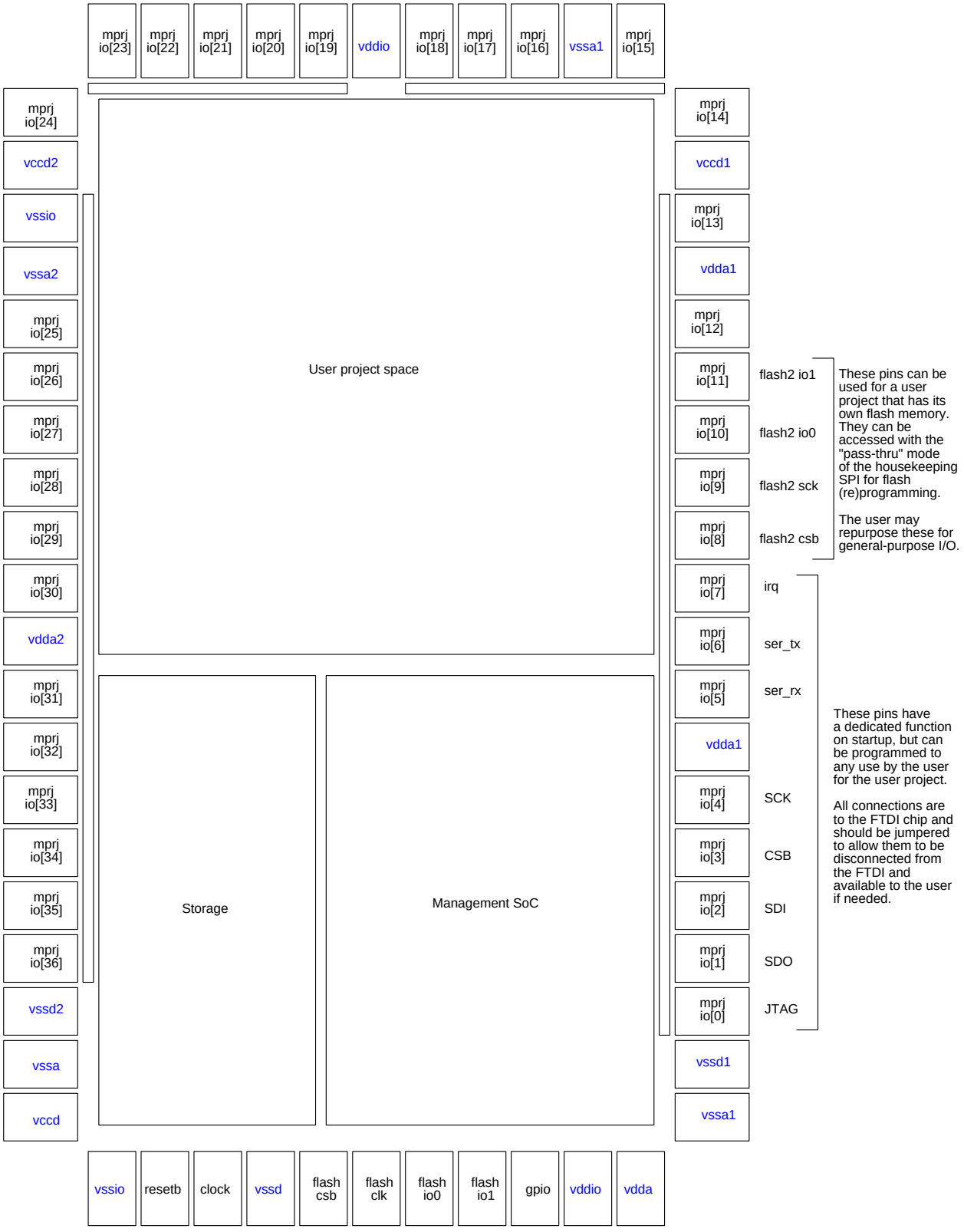
Single GPIO pad structure

Used for pad 0 (JTAG) and pad 1 (SDO)

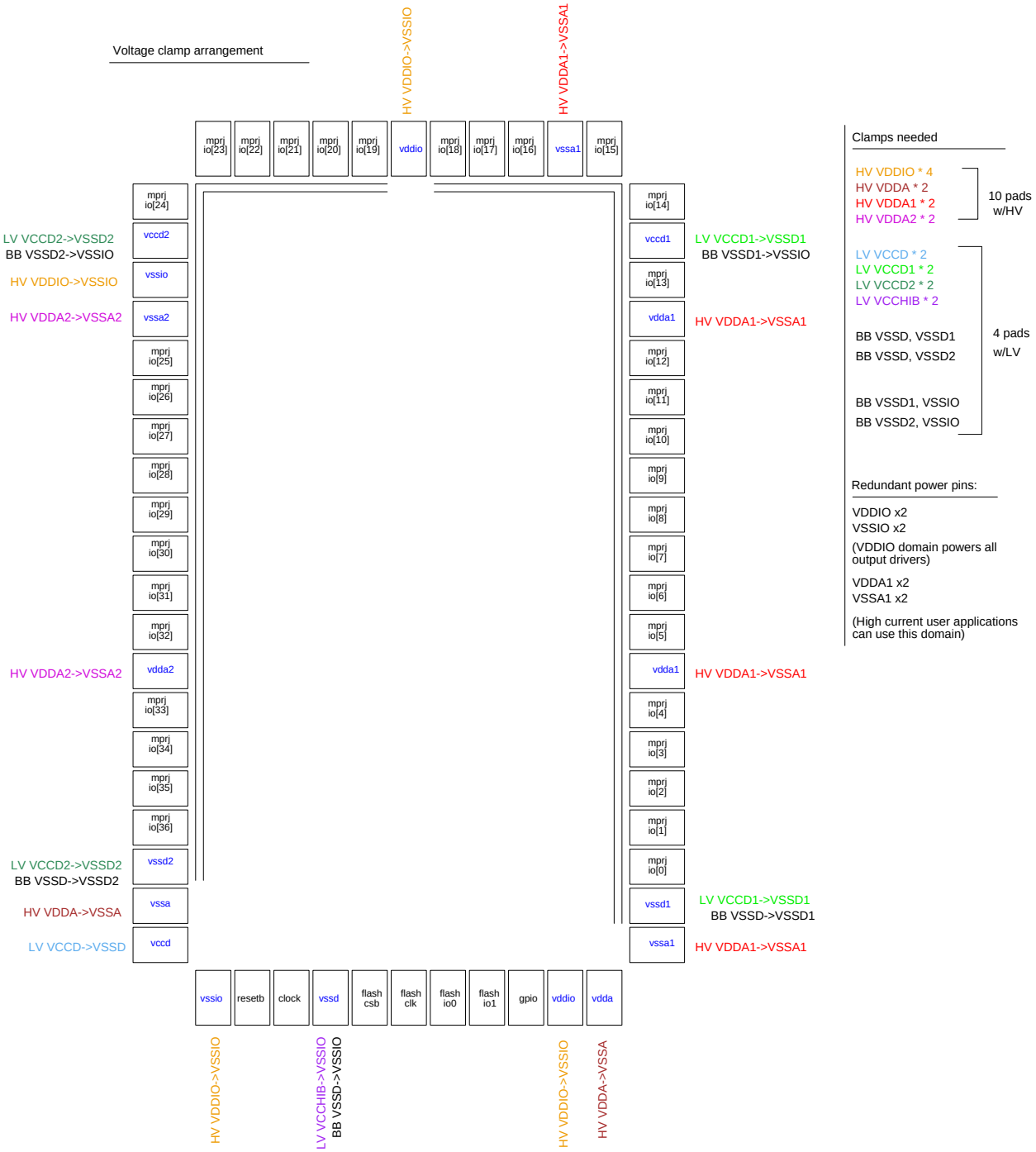


Single GPIO pad structure
Used for all pads except 0 and 1

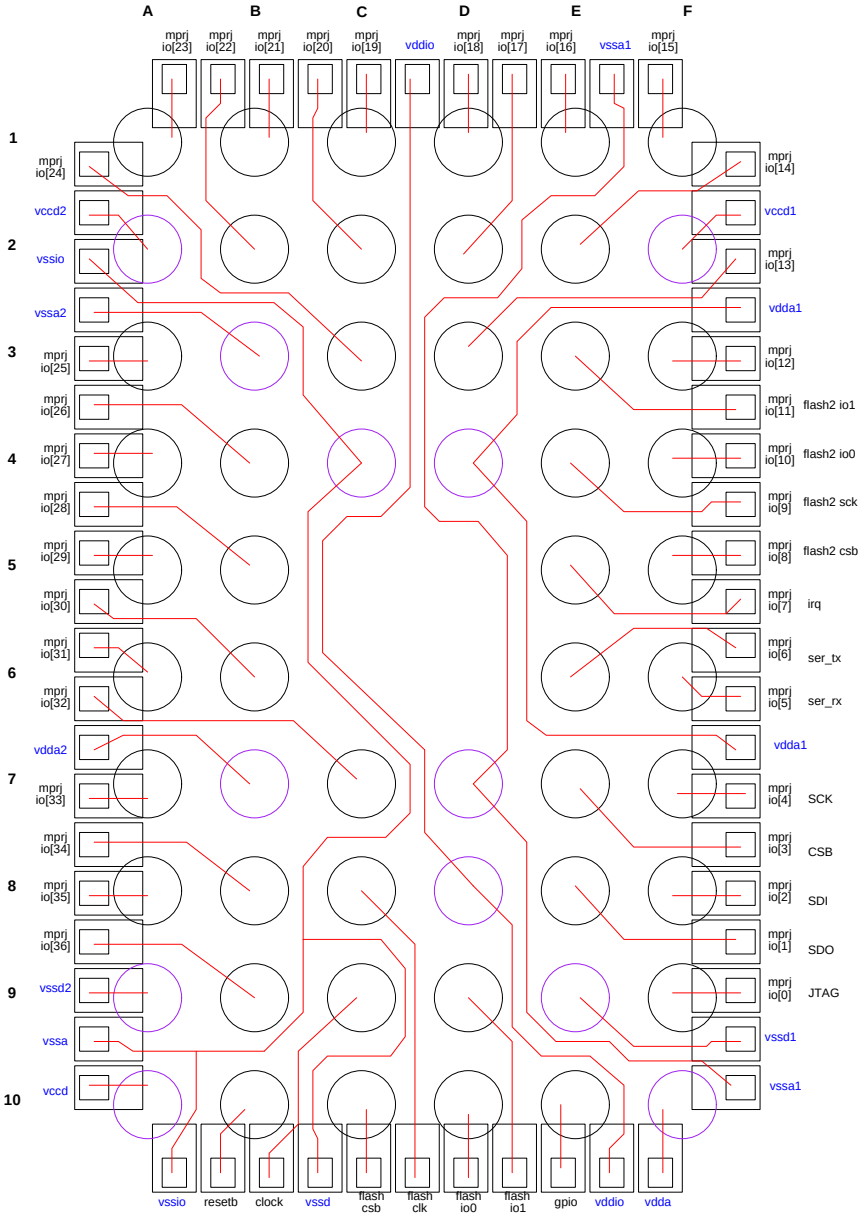




3.2 x 5.3 mm, 62 pins (20, 20, 11, and 11)


Voltage clamp arrangement
HV VDDIO->VSSIO
HV VDDA1->VSSA1
mprj io[23]
mprj io[22]
mprj io[21]
mprj io[20]
mprj io[19]
vddio
mprj io[18]
mprj io[17]
mprj io[16]
vssa1
mprj io[15]
mprj io[24]
vccd2
vssio
vssa2
mprj io[25]
mprj io[26]
mprj io[27]
mprj io[28]
mprj io[29]
mprj io[30]
mprj io[31]
mprj io[32]
vdda2
mprj io[33]
mprj io[34]
mprj io[35]
mprj io[36]
vssd2
vssa
vccd
mprj io[14]
vccd1
mprj io[13]
vdda1
mprj io[12]
mprj io[11]
mprj io[10]
mprj io[9]
mprj io[8]
mprj io[7]
mprj io[6]
mprj io[5]
vdda1
mprj io[4]
mprj io[3]
mprj io[2]
mprj io[1]
mprj io[0]
vssd1
vssa1
vssio
resetb
clock
vssd
flash csb
flash clk
flash io0
flash io1
gpio
vddio
vdda
LV VCCD2->VSSD2
BB VSSD2->VSSIO
HV VDDIO->VSSIO
HV VDDA2->VSSA2
HV VDDA2->VSSA2
LV VCCD2->VSSD2
BB VSSD->VSSD2
HV VDDA->VSSA
LV VCCD->VSSD
LV VCCD1->VSSD1
BB VSSD1->VSSIO
HV VDDA1->VSSA1
HV VDDA1->VSSA1
LV VCCD1->VSSD1
BB VSSD->VSSD1
HV VDDA1->VSSA1
HV VDDIO->VSSIO
LV VCCHIB->VSSIO
BB VSSD->VSSIO
HV VDDIO->VSSIO
HV VDDA->VSSA
Clamps needed
HV VDDIO * 4
HV VDDA * 2
HV VDDA1 * 2
HV VDDA2 * 2
10 pads w/HV
LV VCCD * 2
LV VCCD1 * 2
LV VCCD2 * 2
LV VCCHIB * 2
BB VSSD, VSSD1
BB VSSD, VSSD2
BB VSSD1, VSSIO
BB VSSD2, VSSIO
4 pads w/LV
Redundant power pins:
VDDIO x2
VSSIO x2
(VDDIO domain powers all output drivers)
VDDA1 x2
VSSA1 x2
(High current user applications can use this domain)

Bond plan Bumps at 0.5mm spacing, 350um diameter



44 signal pins
14 unique power pins
4 redundant power pins

58 pins

60 pad positions (6 x 10 array)

prefer to remove the 4 center pads for PCB routability

So, 56 pads.

Unique power domains:

vddio	vssio	Combine these into one pin
vdda	vssa	
vccd	vssd	
vdda1	vssa1	
vccd1	vssd1	
vdda2	vssa2	
vccd2	vssd2	

Total: 56 pins

Pinout

A1	mprj_io[23]	D1	mprj_io[18]
A2	vccd2	D2	mprj_io[17]
A3	mprj_io[25]	D3	mprj_io[13]
A4	mprj_io[27]	D4	vdda1
A5	mprj_io[29]		
A6	mprj_io[31]		
A7	mprj_io[33]	D7	vssa1
A8	mprj_io[35]	D8	vddio
A9	vssd2	D9	flash io1
A10	vccd	D10	flash io0
B1	mprj_io[21]	E1	mprj_io[16]
B2	mprj_io[22]	E2	mprj_io[14]
B3	vssa2	E3	mprj_io[11]/flash2 io1
B4	mprj_io[26]	E4	mprj_io[9]/flash2 sck
B5	mprj_io[28]	E5	mprj_io[7]/irq
B6	mprj_io[30]	E6	mprj_io[6]/ser_tx
B7	vdda2	E7	mprj_io[3]/CSB
B8	mprj_io[34]	E8	mprj_io[1]/SDO
B9	mprj_io[36]	E9	vssd1
B10	resetb	E10	gpio
C1	mprj_io[19]	F1	mprj_io[15]
C2	mprj_io[20]	F2	vccd1
C3	mprj_io[24]	F3	mprj_io[12]
C4	vssio/vssa/vssd	F4	mprj_io[10]/flash2 io0
		F5	mprj_io[8]/flash2 csb
		F6	mprj_io[5]/ser_rx
C7	mprj_io[32]	F7	mprj_io[4]/SCK
C8	flash clk	F8	mprj_io[2]/SDI
C9	clock	F9	mprj_io[0]/JTAG
C10	flash csb	F10	vdda

PCB route pattern