Julia DiTomas
Board 2 Report
ECEN 3730
Spring 2025

1. Plan of Record
    a. Block Diagram

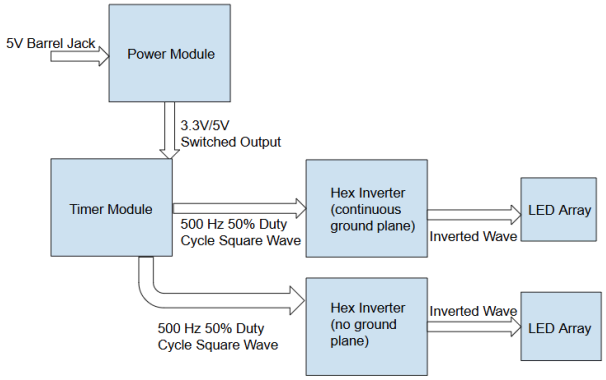


Figure 1: Board 2 block diagram. The power module takes 5V DC as an input from a barrel jack, and includes a switch to change the output between 3.3V and 5V DC. The timer block is a 555 timer configured as an astable oscillator that outputs a square wave of approximately 500 Hz with a duty cycle about 50%. Each hex inverter takes the square wave as 4 of its inputs, and ground and the power rail as the other two. The LED arrays each include 3 LEDs in series with 50 Ω resistors to draw current from the hex inverter.

    b. Parts
        i. LDO AMS1117: LCSC Part #C6186 (https://www.lcsc.com/datasheet/lcsc_datasheet_2410121508_Advanced-Monolithic-Systems-AMS1117-3-3_C6186.pdf)
        ii. Hex Inverter 74AHC14: LSCS Part #C6942 (https://www.lcsc.com/datasheet/lcsc_datasheet_2410122010_Texas-Instruments-SN74AHC14DR_C6942.pdf)
        iii. 555 Timer TI Part #LMC555CMX/NOPB (https://www.ti.com/general/docs/suppproductinfo.tsp?distId=10&gotoUrl=https%3A%2F%2Fwww.ti.com%2Flit%2Fgpn%2Flmc555)

    c. Requirements
        i. The board will take 5V input from a barrel jack, convert it to a 3.3V rail, and allow switching between the two voltage levels for powering the 555 timer and hex inverters.
        ii. The 555 timer will output a square wave about 50% duty cycle and 500 Hz.
        iii. For each hex inverter, the user will be able to measure its rail compression, switching time, and pin's output Thévenin equivalent source.
        iv. A switch will allow the user to see the difference between the LDO output with and without the filter capacitor.
        v. A switch will allow the user to see the difference between a close and far decoupling capacitor on the bad hex inverter circuit.

    d. Test Plan
        i. Test 1: Power
            1. Begin with all switches open. Plug in 5V power cable. Check that LEDs 1 and 2 light up.

2. Measure voltage at TP1 using the oscilloscope. Verify that it is 5V with tolerance of 10%.
3. Measure voltage at TP2 using the oscilloscope. Verify that it is 3.3V with tolerance of 10%. Measure amplitude of oscillations.
4. Close SW1. Measure amplitude of oscillation and note any changes.

ii. Test 2: Timer Circuit

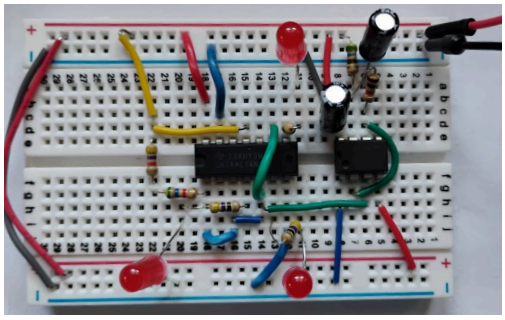
1. Close SW2 for 5V. Observe output at TP7. Verify that the wave has a frequency of 480 Hz and a duty cycle of 67% (both within tolerances of 5%).

iii. Test 3: Hex inverters (repeat for each)

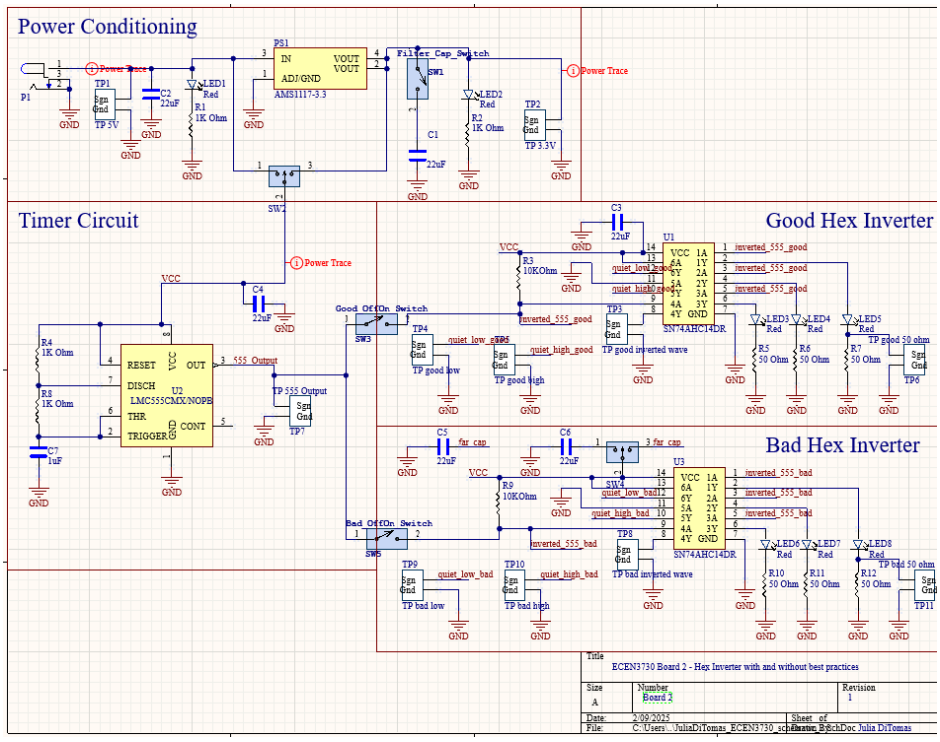
1. Close SW3 (or SW5). Measure outputs at TPs 3 and 6 (or 8 and 11). Calculate Thévenin equivalent circuit based on high voltages.
2. Measure outputs at TPs 3, 4, and 5 (or 8, 9 and 10). Calculate rail compression and measure rise/fall time.
    a. For the bad circuit only, close SW4 and repeat this step.

2. Board Progression

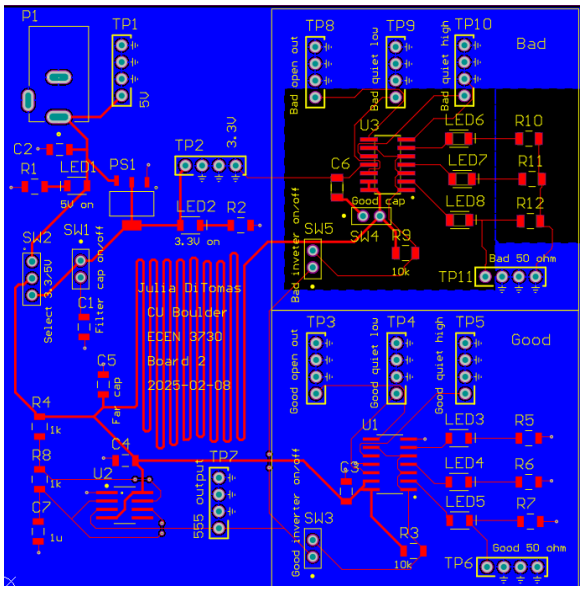
a. SBB



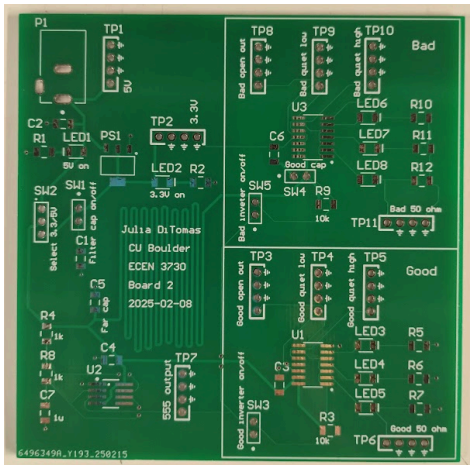
b. Schematic

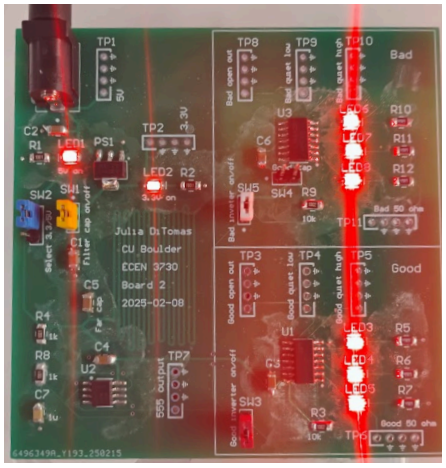


c. Layout



d. Bare Board and Assembled Board





3. Board Testing

After assembling my board, I plugged in the 5V barrel jack and watched LEDs 1 and 2 light up. I measured the voltage at TP1 as 5.2 V and that at TP2 (the LDO output) as 3.3 V. The noise at TP2 had a peak-to-peak amplitude of 40 mV without the filter capacitor, which reduced to 24 mV after closing SW1. The power test passed. I then closed SW2 to the 5V setting. Probing TP7 showed that the 555 timer output had a frequency of 484 Hz and a duty cycle of 66%. Thus, the timer test also passed.

Next I tested the “good” hex inverter circuit. I closed SW3 and measured TP3, which is on the open output of the hex inverter, and TP5, which is across one of the 47 Ω resistors. I measured the Thévenin voltage of the hex inverter output pin as 5.1 V. Assuming that the voltage drop across the LED was 1.9 V and observing 1.8 V across the resistor, I calculated the Thévenin resistance as $\frac{V_{TH}-1.9-1.8}{i} = (47)\frac{5.1-1.9-1.8}{1.8} = 36.6\,\Omega$.

Then, for each of the possible design configurations, and for each edge (rising and falling), I measured the rail collapse and the switching time. I took the rail collapse to be wherever the quiet high and quiet low traces were closest to each other; for example, in Figure 2, this is at about the 4 ns mark. I measured the switching time as the time between the initial drop and where the voltage began to settle to its final value. This is an important distinction especially for the falling edge on the bad layout with the far decoupling capacitor (Figure 3), for which I observed significant ringing. Though the oscilloscope only measured one of those falls as the fall time, I considered it to be the whole duration (approximately 80 ns in the case shown). After performing these measurements for each circuit at 5V, I repeated them powered at 3.3V. Because I was able to make all the required observations and calculations, the hex inverter test passed.

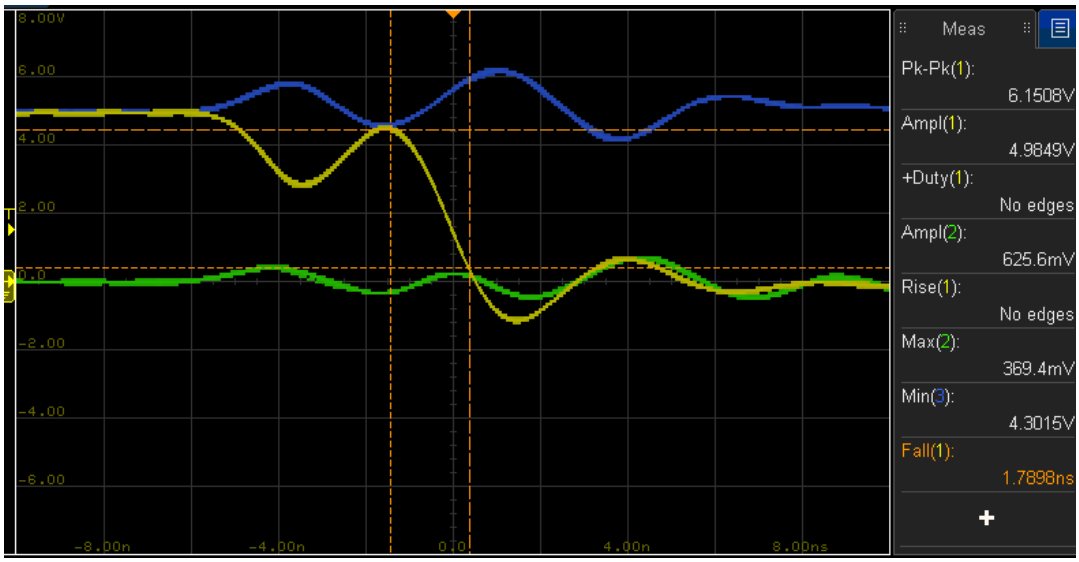


Figure 2: Falling edge on bad layout (no ground plane) with close decoupling capacitor.

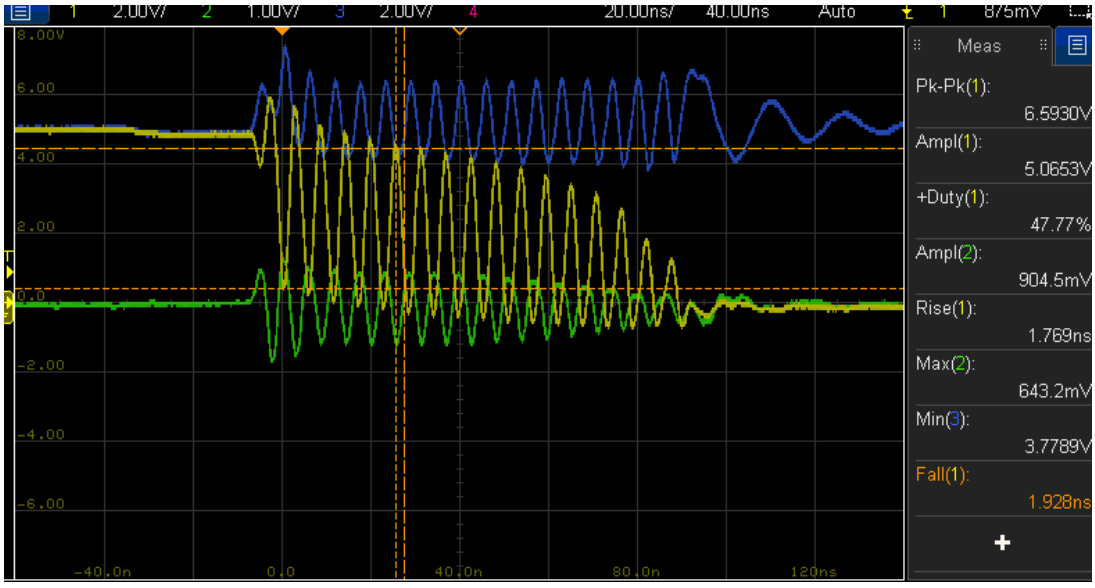


Figure 3: Falling edge on bad layout (no ground plane) with far decoupling capacitor.

4. Conclusions and Lessons

Figures 4 and 5 aggregate the measured results. To compare the rail collapse when powered with 5V versus 3.3V, I took each rail collapse as a percentage of Vcc in Figure 4. I found that when supplied with 5V, the rail collapse was much higher in all cases; reaching up to 43.9% for the bad circuit and far capacitor combination. For the rising edge cases, the rail compression consistently increases as the PCB design practices deteriorate. Interestingly, on the falling edges, the rail compression slightly decreased when the capacitor was switched to the far one. It should be noted that the measurements with ringing are more prone to error since it was difficult to judge at which point the maximum rail collapse occurred. I have also since learned about the math function built-in to the oscilloscope, which may have improved accuracy.

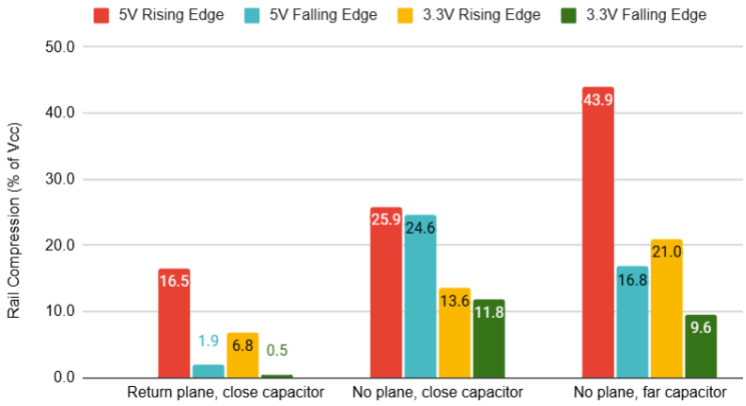


Figure 4: A comparison of rail compression with various PCB design practices, displayed as percentage of the supplied voltage.

The switching time increases with worse design practices in all cases. There is no significant difference between 5V and 3.3V, or between rising edge and falling edge, except for the last board layout, in which the fall time was up to 9x its matching rise time. There are drastic effects to performance for switching signals based on PCB practices. Because it is simple to include a continuous ground plane and decoupling capacitors, these are design principles that I will use for my future boards.

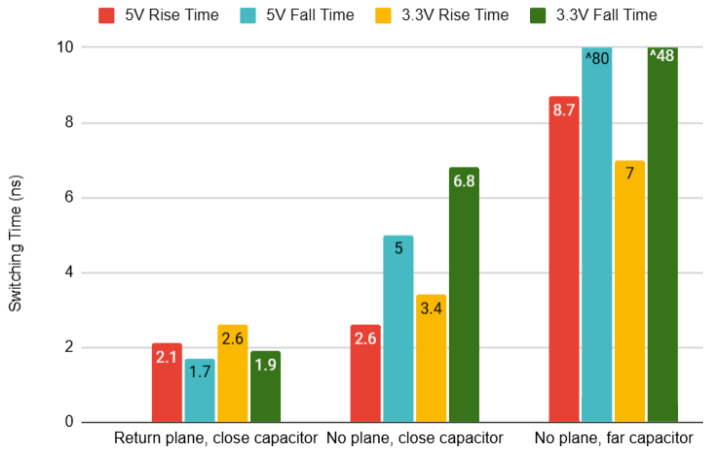


Figure 5: Comparing switching times with various PCB design practices and power supply voltages. Note that both fall times for the third case (no ground place and far decoupling capacitor) are not shown on this scale.