Amplifier Circuit Design in AWR Microwave Office

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I. Passive Circuits Exploration

A. Stop-band filter

We first designed a stop-band filter with an alternating pattern of high and low impedance quarter-wavelength sections of microstrip line. Using the tuner tool in AWR, we found that if both Z_{0h} and Z_{0l} are set to 50 Ω, then there is no reflection across all frequencies, as we expect. If either filter impedance is unmatched, a dip forms in the plot of S_{21} centered on 3 GHz, and it grows both deeper and wider as the impedances move further from 50 Ω. This indicates greater attenuation in the stop-band as well as a wider stop-band.

For our design, we chose $Z_{0h} = 57\ \Omega$ and $Z_{0l} = 37\ \Omega$. Using the TXLine tool in AWR, we calculated the necessary widths to achieve those impedances as $w_h = 1.204$ mm and $w_l = 2.400$ mm. $|S_{11}|$ and $|S_{21}|$ for our simulated microstrip filter are shown in Fig. 1. We found that the stop-band attenuation is -8.33 dB and the 3 dB bandwidth is 1.14 GHz. The roll-off has a slope of 0.141 dB/GHz. The insertion loss is -0.165 dB (at 2.1 GHz). Fig. 2 displays the layout of our design.

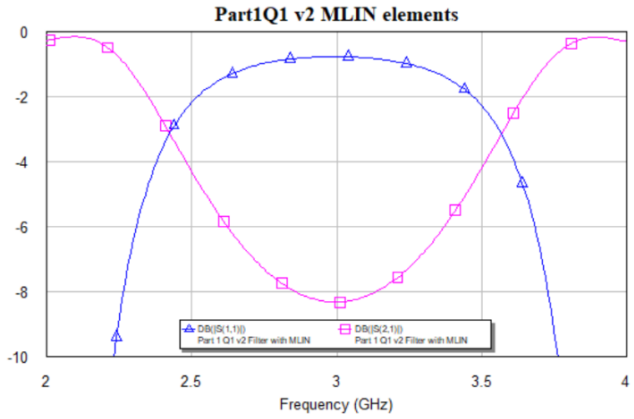

Fig. 1. S-parameter magnitudes for stop-band microstrip filter.

Fig. 2. Layout of microstrip stop-band filter generated by AWR.

B. Rat-race coupler

We designed a 3 dB rat-race coupler centered at 2.45 GHz, using microstrip line with impedance of $50\sqrt{2}\ \Omega$, which required width of 0.800 mm. At 2.45 GHz, we found that $|S_{21}| = |S_{41}| = -3.074$ dB and that the phase of S_{21} is 90° while that of S_{41} is −90°. We defined the band to be where the power to the coupled port was greater than -4.074 dB (where S_{21} was within 1 dB of its max), and we calculated the bandwidth to be 0.916 GHz.

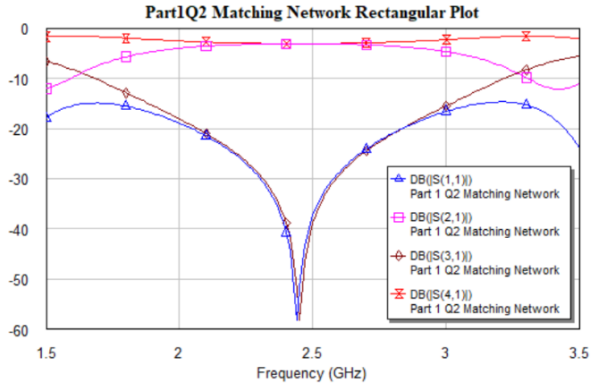

Fig. 3. Rat-race coupler magnitudes of S-parameters, all ports 50 Ω.

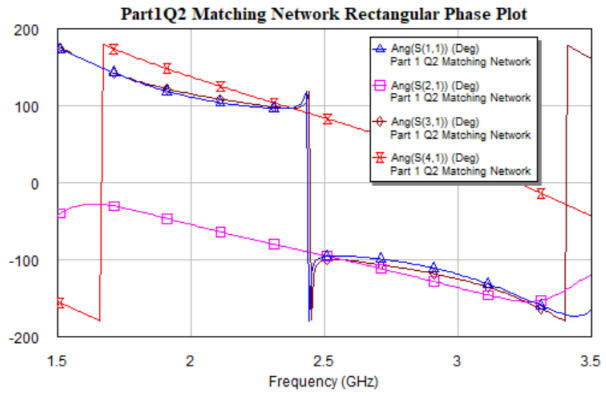

Fig. 4. Rat-race coupler angles of S-parameters, all ports 50 Ω.

We then investigated what happens if the coupled and through ports have unequal and unmatched loads. We found that varying the loads on ports 2 and 4 by up to 10% did not significantly impact the performance rat-race coupler, as the

power delivered to the coupled and through ports only slightly dropped. Fig. 5 shows the S-parameters with the impedances on both ports 2 and 4 changed to 45 Ω. We found that there was a higher reflection coefficient in this case, but it was still less than -25 dB, and we had $|S_{21}| = |S_{41}| = -3.087$ dB.

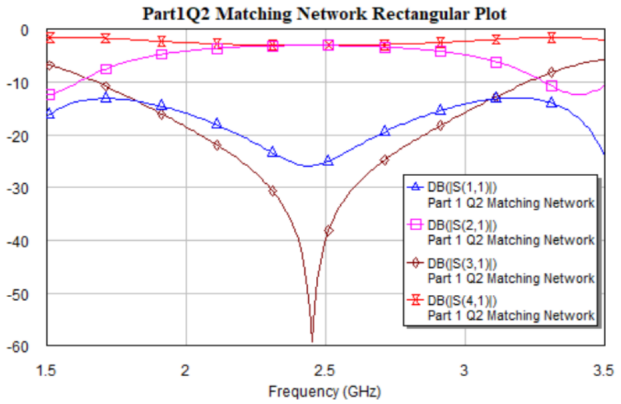

Fig. 5. Rat-race coupler magnitudes of S-parameters, 45 Ω impedance on ports 2 and 4.

Fig. 6 shows the magnitudes of the S-parameters with unequal loads on ports 2 and 4. In this case, we found that $|S_{31}|$ increased at the operating frequency, but that it was still less than -25 dB. We found $|S_{21}| = |S_{41}| = -3.086$ dB.

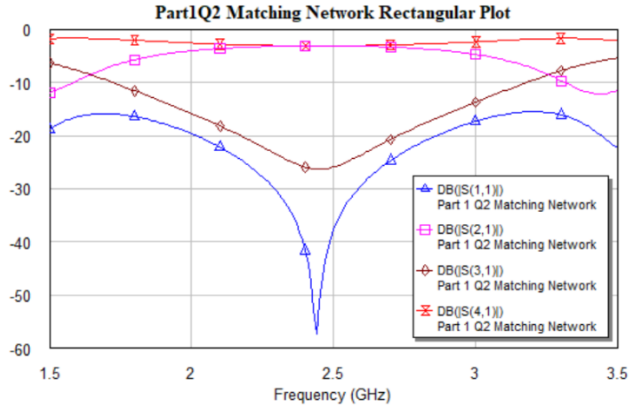

Fig. 6. Rat-race coupler magnitudes of S-parameters, 45 Ω impedance on port 2 and 55 Ω impedance on port 4.

In either case, we observed that the phases on the coupled and through ports changed by less than 1 degree, and that they were still 180 ° from each other.

C. Bias-tee network

Specifications for RF surface mount capacitors provided by manufacturers (and typical values) include capacitance (1 pF-100 nF), rated voltage (10-100 VDC), operating temperature range (-55°C-+125°C), temperature coefficient of capacitance (30-150000 ppm/°C), insulation resistance ($10^7 - 10^{11}\Omega$), mechanical dimensions (< 2 mm), and S-parameters.

For our design, we selected ATC's 500S100 SMT capacitor, which has a value of 10 pF and a self-resonant frequency of 20.68 GHz. We downloaded the S-parameters and compared simulations of an ideal 10 pF capacitor in series with 50 Ω transmission line and the actual device.

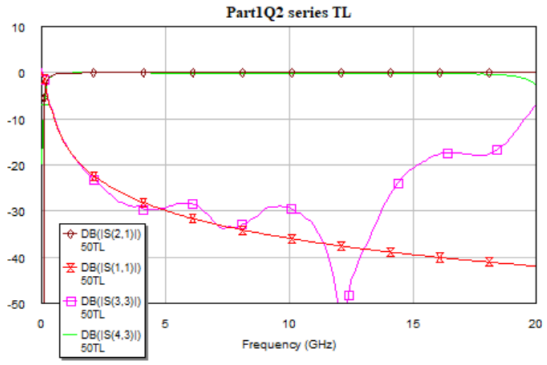

Fig. 7. Comparison of ideal 10 pF capacitor (ports 1 and 2) and ATC 500S100 (ports 3 and 4).

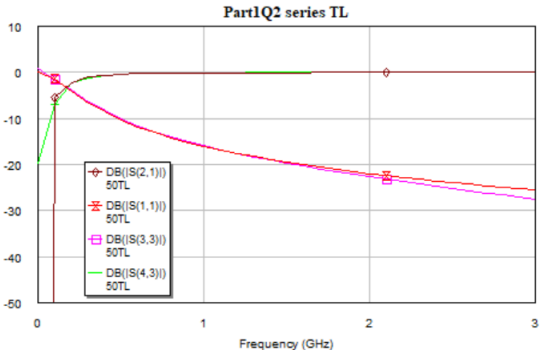

Fig. 8. Repetition of Fig. 7 plot zoomed in over frequencies of interest.

Figs. 7 and 8 show that while the S-parameters of the selected capacitor differ from those of an ideal capacitor at higher frequencies (especially as the self-resonant frequency is approached), at frequencies near our operating point, the 500S100 very closely resembles an ideal device.

We then researched inductors to design the RF choke. Specifications for RF inductors provided by manufacturers (and typical values) are inductance (1 nH-10 μH), maximum current (0.2-1A), DC resistance (0.1-5Ω), maximum frequency (10-50 GHz), self-resonant frequency (3-30 GHz), and S-parameters. Not all manufacturers provide Q and resonant frequency in their datasheets, but the highest values we saw were Q=30 for Piconics CC25T47K240G5-C, and SRF=32 GHz for AVX 506WLSN6R00KT236T.

For our design, we selected Coilcraft's 0201AF-330, which has an inductance of 33 nH and a self-resonant frequency of 3.4 GHz. We constructed our bias-tee network with the chosen components and a 1 mm long section of 50 Ω MLIN between each piece.

Fig. 9 shows the S-parameter magnitudes of the bias-tee network with realistic components. We found that the DC current is blocked from going into port 2 (the RF output port),

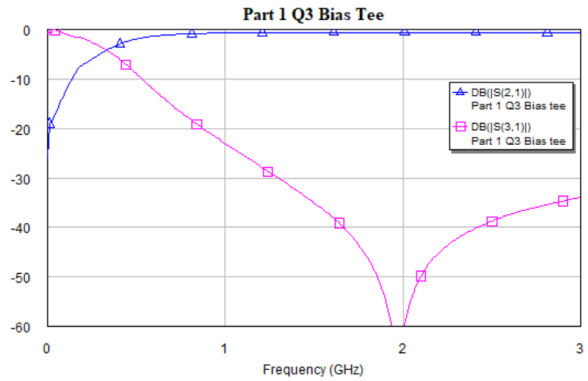

Fig. 9. Performance of bias-tee network with realistic components.

and that the RF signal does not go into port 3 (the DC input port). Compared to the same network with ideal components, this design does have a slightly lower $|S_{21}|$ at 2 GHz (-0.5503 dB vs -0.0123 dB) due to the parasitics.

II. Designing a Small-Signal Linear Amplifier

A. Unilateral matching networks for FET

We first characterized the FET by downloading the S-parameters from Qorvo and finding the input and output impedance at 2 GHz. Fig. 10 shows the normalized impedances on the Smith chart. Multiplying each by the characteristic impedance, we find that they are $Z_{in} = (3.61 - 4.73j)\Omega$ and $Z_{out} = (16.6 - 29.7j)\Omega$.

We then designed separate matching circuits for each port, using the Iowa Hills Smith chart, under the assumption that the other port was terminated in 50 Ω. We decided to utilize lumped element circuits for matching as they take up less space than transmission line stubs.

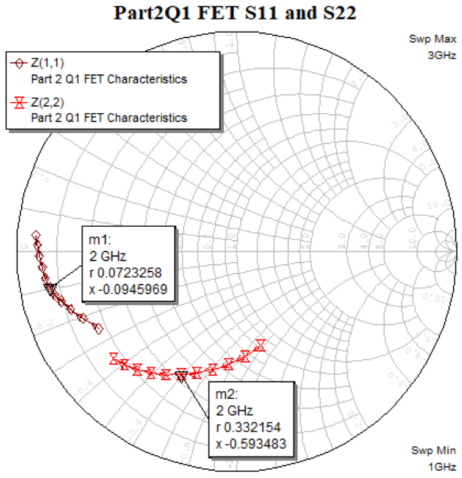

Fig. 10. Impedance at each FET port when other port terminated in 50 Ω.

Our input match was achieved with a 10 pF series capacitor (ATC 500S100) connected to the FET, then a 1 nH shunt inductance (2 0201DS-0N5 0.5 nH inductors from Coilcraft in series).

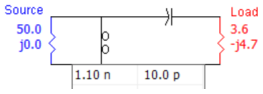

Fig. 11. Iowa Hills Smith chart tool schematic of input matching network. Note that the actual shunt inductance we used was 1 nH.

Our output match was achieved with a 0.5 nH series inductor (Coilcraft 0201DS-0N5) connected to the FET, then a 2.7 nH shunt inductance (0201DS-1N3 in series with 0201DS-1N4).

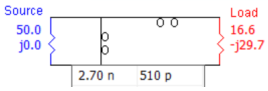

Fig. 12. Iowa Hills Smith chart tool schematic of output matching network. Note that the actual series inductance we used was 0.5 nH.

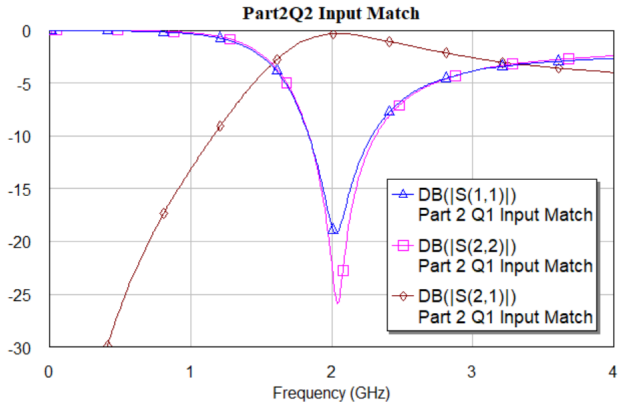

Fig. 13. Performance of input matching network.

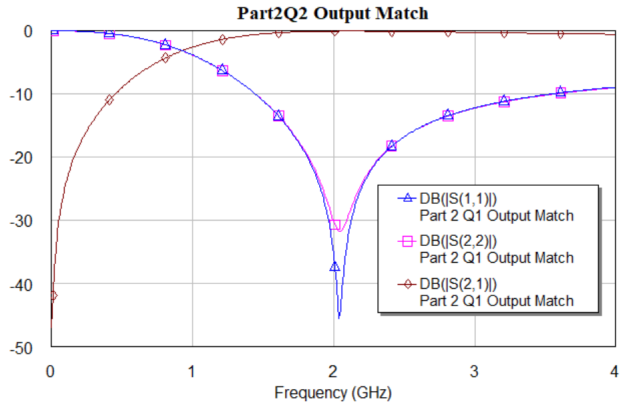

Fig. 14. Performance of output matching network.

B. Implement input match and output match

We then connected both the input and output matching networks from the previous section to the FET and simulated the performance (Fig. 15).

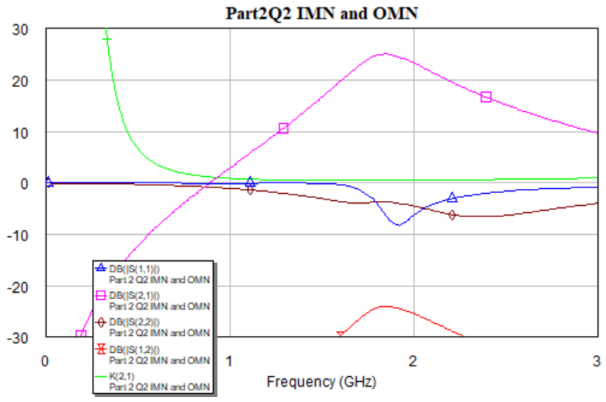

Fig. 15. S-parameters for FET connected to the two matching networks found in part II. A.

Fig. 15 shows a maximum S_{21} of 25.02 dB at 1.85 GHz. Although this solution achieved high gain somewhat close to our operating frequency, it wasn't centered on 2 GHz and it had a stability issue. (Its K-factor is less than 1 from 0.94 GHz to 3.08 GHz). We found that our unilateral matching networks did not match either port as efficiently once the system became bilateral.

C. Bilateral matching

We then designed a bilateral match using the tuning tool in AWR. We built the circuit out of ideal lumped elements initially, using the values from the separate input and output matching networks as a starting point. To increase the stability at lower frequencies, we also inserted a parallel RC circuit in series on the drain side, and a shunt resistor. We added the values for all of the elements as variables in the tuning tool, and configured them for maximum gain at 2 GHz while maintaining stability. After noticing a sharp dip in K to negative values around 6.6 GHz, we added a band stop filter at this frequency using the stepped impedance microstrip line approach from part I.A. Finally, we replaced each ideal inductor, capacitor, and resistor with a realistic component using manufacturer-provided s2p files.

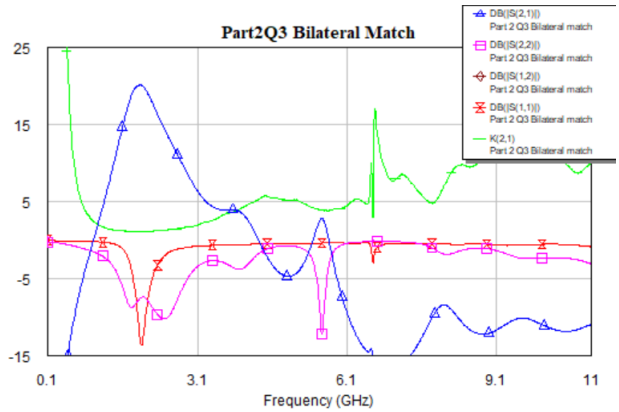

Fig. 16. S-parameters for bilateral matching with realistic components.

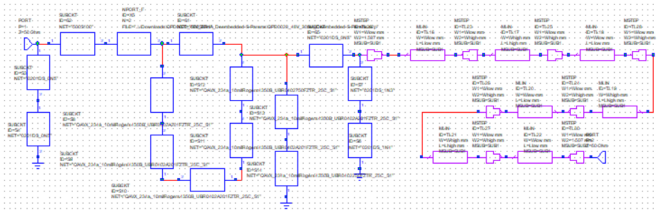

Fig. 17. Bilateral match schematic with realistic components.

S_{11} at 2 GHz	0.177 - 0.1293j
S_{21} at 2 GHz	-0.02137 - 0.02973j
S_{12} at 2 GHz	6.559 - 7.533j
S_{22} at 2 GHz	-0.2611 - 0.3405j
Gain at 2 GHz	20.01 dB
Minimum K-factor	1.136 at 2.07 GHz
3 dB Bandwidth	0.5 GHz (25%)

TABLE I
BILATERAL MATCH PERFORMANCE

We found that ensuring stability of our design over the entire frequency range of the device (0.1 GHz - 11 GHz) came at the cost of our S-parameters. Adding the resistors and the band stop filter decreased our gain and increased the magnitudes of our reflection coefficients.

D. Source inductance

After completing our bilateral matching network, we simulated the inductance on the ground lead of the Qorvo transistor. Our results are summarized in Table II. We found that including the source inductance decreased our gain, moved our maximum gain away from 2 GHz, and caused our design to be potentially unstable over large frequency intervals.

Inductance (nH)	$K < 1$ Frequency Interval (GHz)	Gain at 2 GHz
0.1	$[3.0 - 10.7]$	15.8 dB
0.5	$[2.2 - 11]$	7.6 dB
1	$[2.0 - 11]$	2.762 dB

TABLE II
BILATERAL MATCH PERFORMANCE

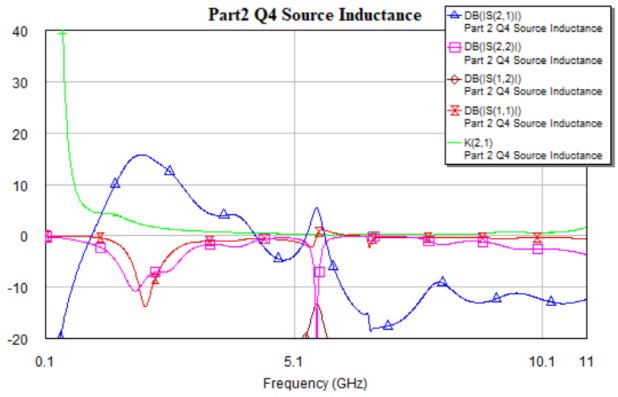

Fig. 18. Performance of bilateral match design with 0.1 nH source inductance.

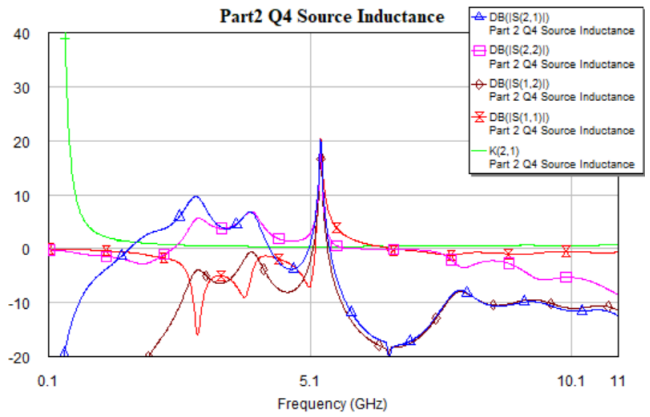

Fig. 19. Performance of bilateral match design with 1 nH source inductance.

Fig. 19 shows the performance with 1 nH source inductance, which has been severely degraded. In this case, there is high reflection on the output, and all four S-parameters have a sharp uptick at 5.3 GHz. The K-factor is less than 1 from 2 GHz to the end of the graph (11 GHz).

E. Implementing bias-tee network

Finally, we added our bias-tee network from part I.C. to our amplifier design. On the input side, we experimented with inserting it before and after the series capacitor. On the output side, we experimented with inserting it immediately after the FET, after the RC circuit, and immediately before the band stop filter. We set the DC voltage according to the recommended operating conditions from the QPD0020 datasheet (-2.7 V gate voltage, +48 V drain voltage). We found that changing the locations of the bias lines only slightly changed our results, but that the best performance was achieved with one bias-tee network before the capacitor on the input side, and the other immediately after the FET on the output side.

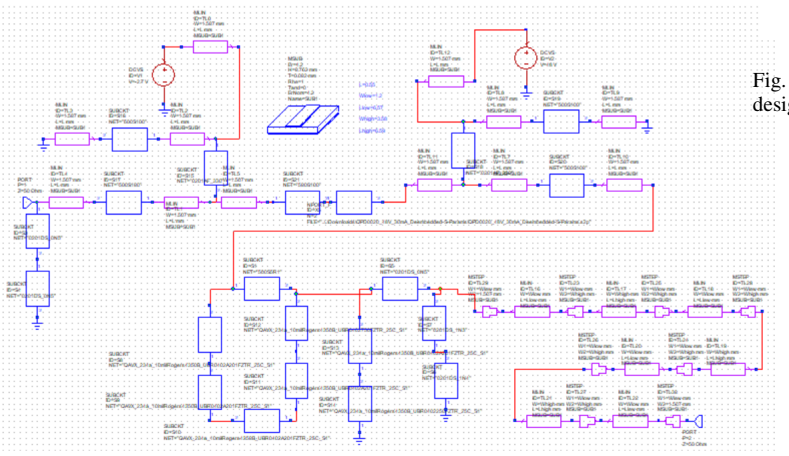

Fig. 20. Schematic of final design. The bias-tee microstrip interconnects each have 50 Ω impedance (1.507 mm width) and 0.55 mm length. The stop band filter has microstrip sections of length 6.6 mm and width alternating between 1.2 mm and 2.6 mm.

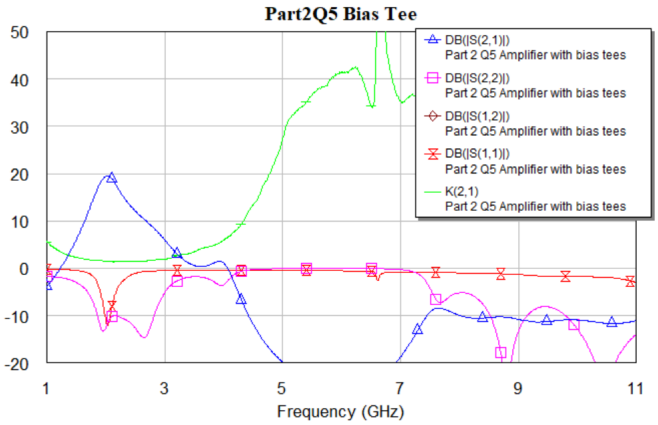

Fig. 21. Performance of final design with 0 source inductance.

Our gain at 2 GHz was 19.49 dB, and our 3 dB bandwidth was 0.38 GHz. We found that if we neglected the source inductance, our design performed well at our operating frequency and was unconditionally stable throughout the FET frequency range provided by Qorvo. However, once a small amount of source inductance is added, this design is no longer unconditionally stable over the entire frequency range, and the actual source inductance would need to be compensated for.

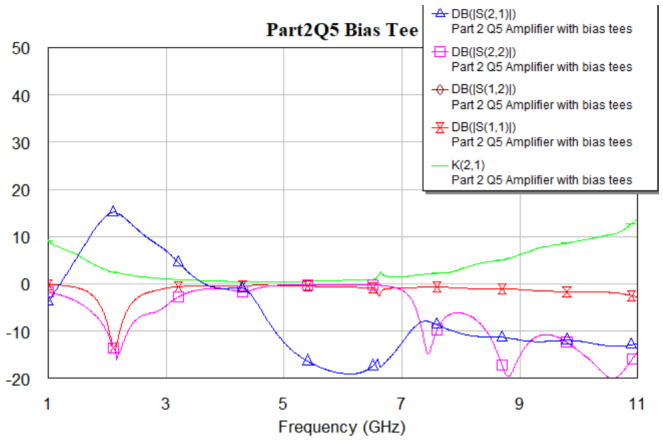

Fig. 22. Performance of final design with 0.1 nH source inductance. The design is now potentially unstable from 3.04 GHz to 6.53 GHz.

Manufacturer	Part Number	Value
Coilcraft	0201DS-0N5	0.5 nH
Coilcraft	0201DS-1N3	1.3 nH
Coilcraft	0201DS-1N4	1.4 nH
Coilcraft	0201AF-330	33 nH
ATC	500S100	10 pF
ATC	500S5R1	5.1 pF
AVX	UBR0402A201FZTR	200 Ω
AVX	UBR0402A750FZTR	75 Ω
AVX	UBR0402A250FZTR	25 Ω

TABLE III
LUMPED ELEMENTS USED IN AMPLIFIER DESIGN