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ECEN 5634
Lab 8 Report

Part II

Q1: In this part of the lab, we characterized the bias Tee network, which consisted of a radial stub and a capacitor. Other possible designs for the bias Tee are shown in Figure 1. In each case, a high pass filter blocks the DC voltage from the RF input, and a low pass filter blocks the RF signal from the DC input. One design we could use would utilize surface mounted lumped elements (a capacitor and an inductor). Another method could use a short stub for the high pass filter and a stepped impedance low pass filter on the DC line.

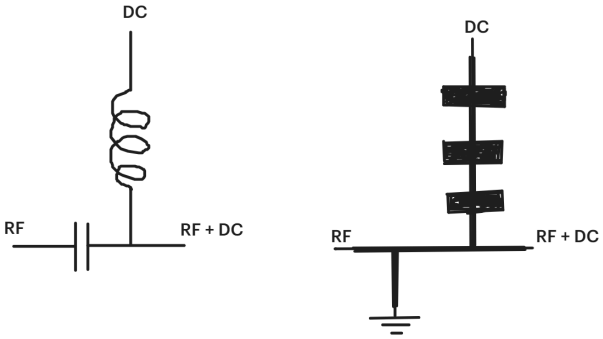

Figure 1: Other possible bias Tee networks.

Q2: We connected the bias Tee to the PNA and measured its S-parameters, with the RF input connected to port 1, the RF (and DC) output connected to port 2, and the DC input unconnected. Our results are shown in Figure 2, and as we expect, it looks like a high pass filter. We discovered that there was a dip in S_{21} at 1.398 GHz, however, that would make it not function at this frequency (because it would block the RF signal).

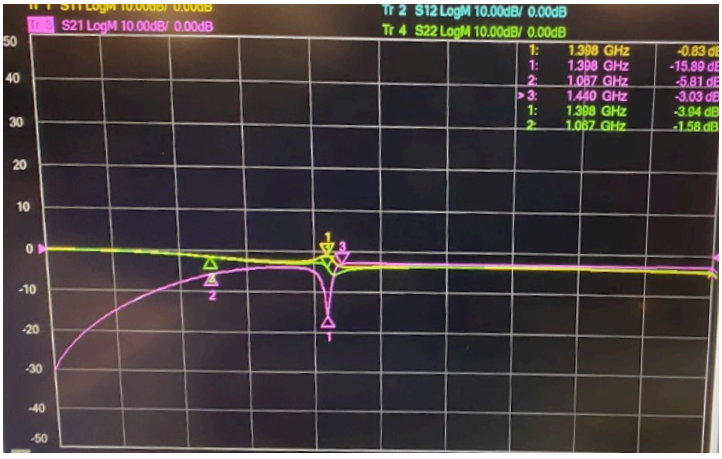

Figure 2: Bias Tee S-parameters with DC bias line unconnected.

Q3: We defined the band to be where $|S_{21}|$ was greater than -3 dB, which was from 1.44 GHz to 2.5 GHz (the maximum of the range measured). This means that our bandwidth was 1.06 GHz. The optimum operating frequency was 1.5 GHz, where S_{21} had its maximum value. To make a more broadband biasing circuit, we could increase the value of the DC blocking capacitor. This would decrease the impedance of the capacitor at all frequencies and make $|S_{21}|$ higher, extending the range to lower frequencies. We could also determine the cause of the dip in S_{21} and create a design that eliminates it.

Part III

Q5: We measured the S-parameters of the amplifier first with its drain voltage set to 5 V and current set to 0.5 A, which required 1.67 V gate voltage. We verified that the amplifier was working because after adjusting for the 30 dB attenuator, we found that it had a maximum gain (S_{21}) of 26.55 dB, which means that it takes a small signal input and outputs a much larger signal. We did not observe any oscillations, since the gain kept increasing as we increased the gate voltage, and oscillations would cause it to drop. If there were oscillations, we could suppress them by adding resistance or adding band stop filters at the oscillating frequencies. The best operating frequency is 1.968 GHz, where we observed the maximum gain of 26.55 dB. We measured 517 mA of current being drawn from the drain power supply.

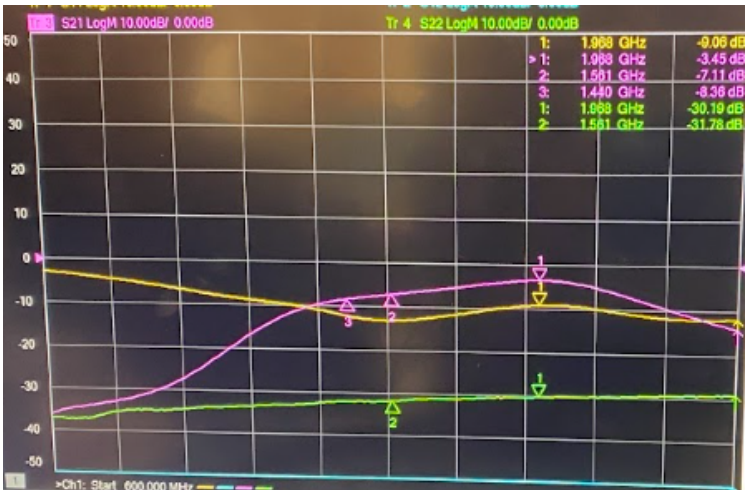

Figure 3: Amplifier S-parameters measured by PNA for gate voltage of 1.67 V and drain voltage of 5 V.

Q6: We then varied the drain voltage and observed the changes in gain and current drawn. We found that as we decreased the drain voltage, the current drawn from the power supply and $|S_{21}|$ both decreased. This makes sense because we are providing less DC power, and because the DC voltage is less, the RF signal cannot swing as far from the DC voltage.

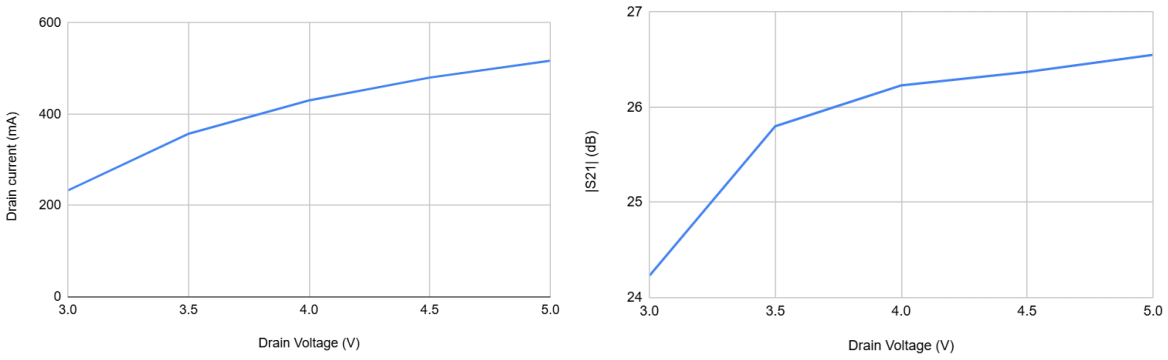

Figure 4: Change in drain current (left) and magnitude of S_{21} (right) as we varied the drain voltage while keeping the gate voltage constant at 1.67 V.

Q7: We then kept the drain voltage constant and experimented with varying the gate voltage. We found that as gate voltage increases, so does drain current and gain of the amplifier. This is what we expect since gate voltage is what opens the channel for current to flow. At 1.2 V gate voltage, the amplifier was still off. The gain then increased but leveled off as it neared its maximum value around 1.45 V gate voltage.

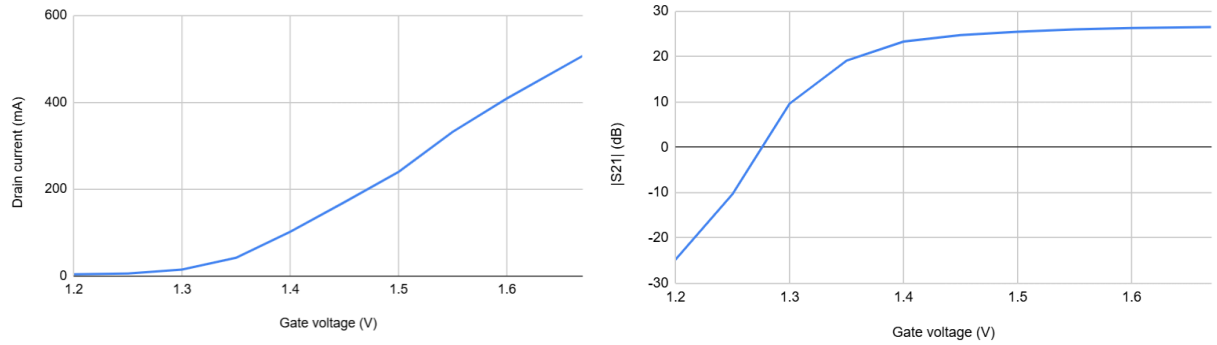

Figure 5: Change in drain current (left) and magnitude of S_{21} (right) as we varied the gate voltage while keeping the drain voltage constant at 5 V.

Part IV

Q8: In this part, we set the drain voltage and gate voltage of the amplifier to 5 V and 1.67 V respectively, and measured the output RF power and we varied the input RF power. We found that output power varied linearly with input power, which implied that the gain was constant, as is displayed in Figure 6. We observed that the gain compressed a small amount near the end, but we did not increase the input power enough to reach the 1 dB compression point. At -1 dB input power, it had compressed 0.25 dB. We estimate that the 1 dB compression point is likely around 0 dB input RF power.

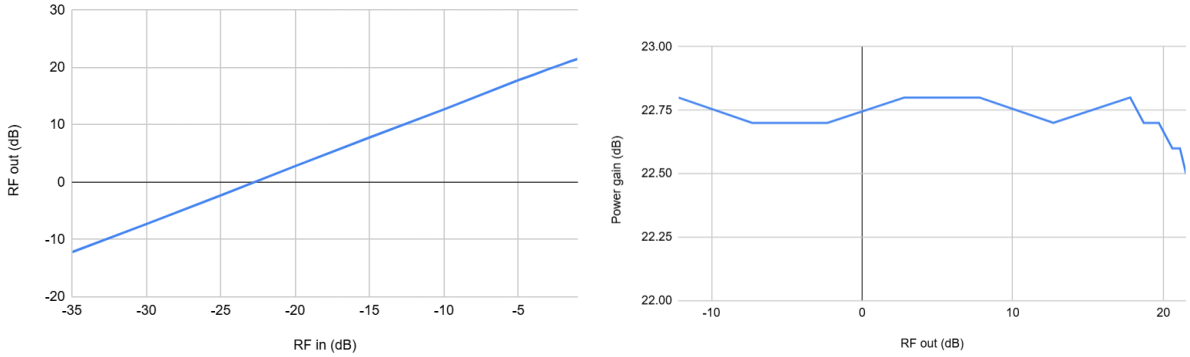

Figure 6: Change in drain current (left) and magnitude of S_{21} (right) as we varied the gate voltage while keeping the drain voltage constant at 5 V.

Q9: We then calculated the drain efficiency, the PAE, and the total efficiency for each power level. We found that the three different efficiencies were nearly the same at each power level, due to the high gain of the amplifier. Additionally, we found that the amplifier is very inefficient, but that its efficiency increases as RF input power increases. Still, it takes a lot of DC power to amplify the RF signal. The maximum efficiency that we measured was 5.4%, when it took 2615 mW of DC power to generate 141 mW of RF output power.

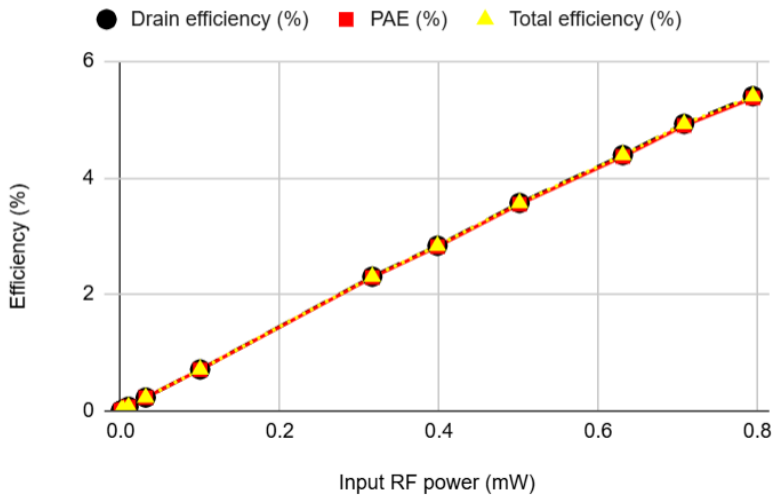

Figure 7: Efficiency of amplifier as a function of input RF power, keeping gate voltage and drain voltage constant at 1.67 V and 5 V.

We did not experiment with changing the bias voltage in this part of the lab. However, we used our data from earlier in the lab when we measured the gain versus drain voltage, to construct Figure 8. Note that this was the maximum gain across all frequencies, so it was higher (by about 4 dB) than what we observed in this part of the lab with the RF signal generator. We also assumed 1 mW RF input power for these calculations. These factors combined to give us a much higher efficiency than displayed in Figure 7, but we still see that the trend as drain voltage increases is for efficiency to decrease.

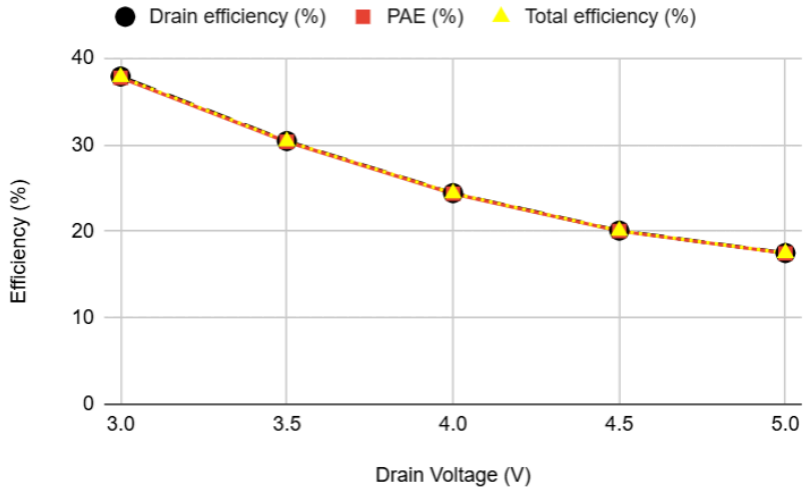

Figure 8: Efficiency of amplifier at "best" operating frequency as drain voltage varies, keeping gate voltage constant at 1.67 V and assuming 1 mW input power. This uses our PNA measurements from **Q6**.

Part V

Q10: We then combined two input signals separated by 10 MHz, and observed the output on the spectrum analyzer as we varied the input power levels. We observed that the power of the fundamental tones on the output increased as we increased the input power, and that IMD3 tones appeared and grew as well. We first observed the IMD3 tones at -6 dB input power.

Figure 9: Spectrum analyzer display for two-tone input at -10 dB input power (left) and -2 dB input power (right). Note that in this setup we again used a 30 dB attenuator to protect the lab equipment.

Q11: We then varied the power levels of the input tones and measured the output power of the fundamental frequencies as well as the intermodulation frequencies. Our results are shown in Figure 10. We extrapolated the two lines and found that they intersect at the point (14 dB, 33 dB). Assuming that 0 dB input power is the 1 dB compression point, this is 14 dB above that point.

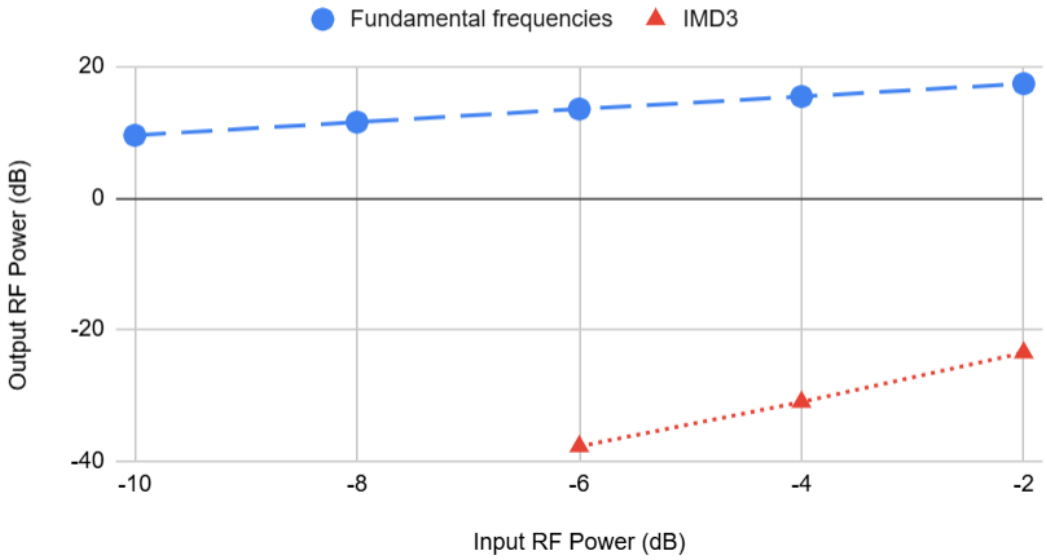

Figure 10: Output power in two tones and intermodulation frequencies as a function of input power level.

Part VI

We next performed a two-tone power sweep using the PNA. We found that the IMD3 curve is approximately a straight line with 3x the slope of the main power curve. It is not perfect because the approximation neglects the higher order terms and their possible contributions to the fundamental frequencies and to the 3rd-order intermodulation frequencies. We also found that the curve was noisy at lower power levels.

We found that as we increased the gate voltage, the IMD3 curve dropped significantly below the main power curve, and the point at which their linear extrapolations would intersect moved to a higher power level (to the right). We also found that the IMD3 curve's slope slightly increased.

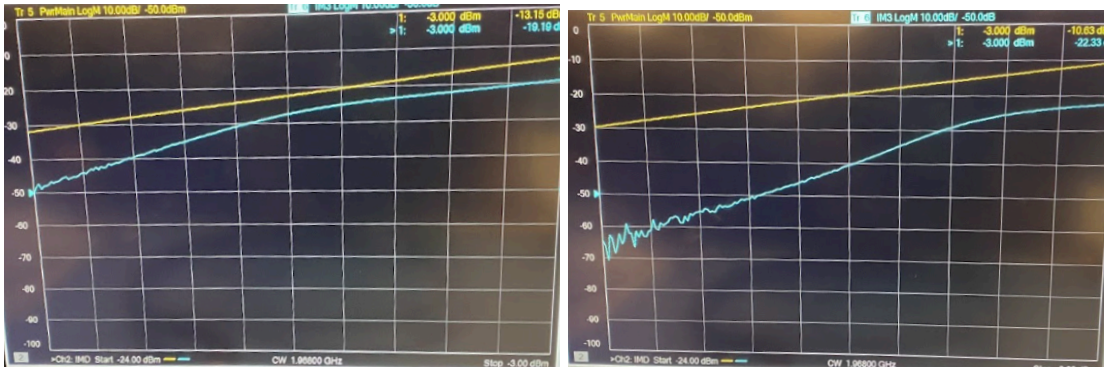

Figure 11: PNA two-tone power sweep with gate voltage of 1.4 V (left) and 1.5 V (right).

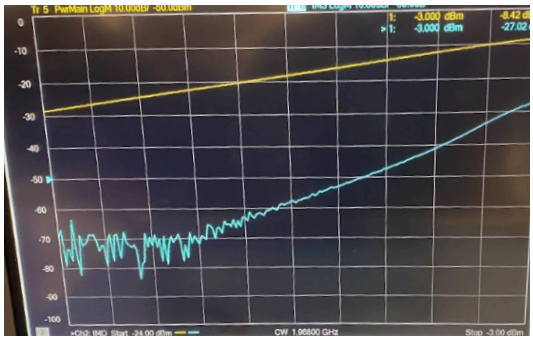

Figure 11: PNA two-tone power sweep with gate voltage of 1.67 V.