MAKEFILES

How to Automagically Build and Compile Your Programs

MOTIVATION

The why, what and how of makefiles for you and me.

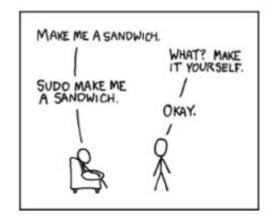


Figure: xkcd

(comic is for sudo, but who cares, it has 'make")

WHY MAKEFILES?

- → Lots of source files: foo.h, foo2.h, foobar1.c, foobar2.c
- → How to manage them all?
- → Compiling is complicated!!!
- → Solution: make

WHAT ARE MAKEFILES?

- → make automagically build and manage your programs
- → Compile quickly with a single command
- → Recompile is even quicker

HOW DOES IT WORK?

- → Give targets (usually a file to be created)
- → Specify dependencies for each target
- → Give command to create target from dependencies
- → make recursively builds the targets from the set of dependencies
- → Recompilation timestamp of modification

.HAND.CPP

- → .h files contain
 - Declarations
 - Functions that the class promises
- → .c files contain
 - Definitions
 - Implementations of the promised methods
 - Other functions that are not a part of any class

BIGINT EXAMPLE

- → The BigInt data type in RSA
 - BigInt.h ~ with proposed methods: +, -, *, /, !
 - BigInt.c ~ with implementation of methods
 - Rsa.c ~ ONLY needs #include "BigInt.h" (doesn't need BigInt.c)

CREATING OBJECT FILE

- → Object file or (.o file)
 - For creating rsa.o, no need to include BigInt.c!
 - Eventually need BigInt.c for running
 - Link later
 - You also don't need main()
- → Command:

```
gcc -Wall -c rsa.c
```

- -Wall: all warnings turned on
- -c: Compiles but doesn't link

MAKEFILES

A makefile describes the dependencies between files

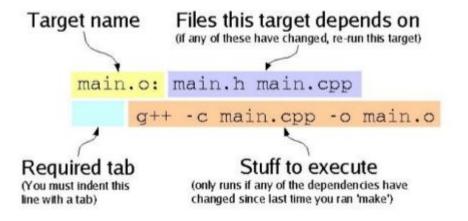


Figure: Content of a Makefile

TARGET, DEPENDENCIES, COMMANDS

- → Target is usually a file. Remember ";"
- → Dependencies: .c, corresponding .h and other .h files
- → Determining dependencies
- → The all important [tab]
- → Commands: can be multiple

MACROS

Use them!

```
Like #define
OBJS = rsa.o main.o
CPP = g++
DEBUG = -g
CPPFLAGS = -Wall -c $(DEBUG)
LDFLAGS = -1m
Usage: $(variable)
rsa : $(OBJS)
        $(CPP) $(LDFLAGS) $(OBJS) -o rsa
 ► Automatic variables : $0 , $<, $^ ...
```

NAMING THE FILE

- → Naming and running the make file
 - makefile ~ run with make
 - Makefile ~ run with make
 - Give any filename ~ run as make -f <filename>
- → make picks the first target in the file and executes the commands if the dependencies are more recent than the target

PHONY TARGETS

- → Dummy targets to run commands. They don't actually create files.
 - make all
 - make clean
 - make tar
- → Use .PHONY or directly name

EXAMPLE MAKEFILE

Makefile

clean :

\$(CPP) \$(CPPFLAGS) rsa.cpp -o \$@

\$(CPP) \$(CPPFLAGS) BigInt.cpp -o \$@

BigInt.o: BigInt.cpp BigInt.h

rm -f *.o *~ rsa

AUTOMATIC VARIABLES

- → \$0, \$<, \$^</p>
 - \$@: used for the target variable

 - \$^: is like *all the above* ~ all the prerequisites

DEFAULT AUTOMATIC RULES TO COMPILE

'MAKE' FROM WITHIN THE EDITOR

- → Some editors like Vim allow you to call 'make' while still editing the makefile (:
 - :make ~ to run the Makefile
- → To navigate through the errors and fix compilation issues fast, try
 - :copen ~ Opens the quickfix window, to show the results of the compilation
 - :cnext or :cn ~ jump to the next error in source code
 - cprev or :cp ~ jump to the previous error in source code

REMARKS

- → Don't forget to put the TAB before entering command
- → Look at example Makefiles
- → Lots of tutorials available online:
 - This is a good one!!
 - http://www.gnu.org/software/make/manual/make.html

QUESTIONS?

Just make it!