CSE331 Computer Architecture
Spring 2021
Homework 1 (100 pts)
Julian Garcia
ID: 900334702

1. (**15 pts, 5/5/5**) Of the three factors in processor performance equation (*EXCPU = Number of instructions × CPI × cycle time*), which is most influenced by:
   (a) The technology
   The cycle time is most influenced by this
   (b) The compiler
   The number of instructions is most influenced by this
   (c) The computer architect
   The CPI is most influenced by this

2. (**15 pts**) When running an integer benchmark on a RISC machine, the average instruction mix was as follows:

Instructions	*Average Frequency*
Load	26%
Store	9%
Arithmetic	14%
Compare	13%
Cond. branch	16%
Uncond. branch	1%
Call/returns	2%
Shift	4%
Logical	9%
Misc.	6%

The following measurements of average CPI for individual instruction categories were made:

Instruction type	*Average CPI (clock cycles)*
All ALU instructions	1
Load–store	1.4
Conditional branches:	
Taken	2.0
Not taken	1.5
Jumps	1.2

Assume that 60% of the conditional branches are taken and that all instructions in the Misc. category are ALU instructions. What is the CPI of the benchmark on this RISC machine?

$Freq_{Jump} = 2\% + 1\% = 3\%$

$Freq_{ALU} = 6\% + 14\% + 9\% + 4\% + 13\% = 46\%$

$Freq_{ConditionalTaken} = 0.6 * 0.16 = 0.096 = 9.6\%$

$Freq_{ConditionalNotTaken} = 0.4 * 0.16 = 0.064 = 6.4\%$

Op	Freq	CPI_i	Freq x CPI_i
ALU	46%	1	0.46
LOAD	26%	1.4	0.364
STORE	9%	1.4	0.126
BRANCH TAKEN	9.6%	2.0	0.192
BRANCH NOT	6.4%	1.5	0.096
JUMPS	3%	1.2	0.036
TOTAL	-	-	1.274

CPI = 1.274

3. (**30 pts, 10/10/10**) Consider two implementations M1 and M2 of the same ISA. We are interested in the performances of two programs P1 and P2, which have the following instruction mixes:

Operations	*P1*	*P2*
Load/store	40%	50%
ALU	50%	20%
Branches	10%	30%

The *CPI*s for each machine are:

Operations	*M1*	*M2*
Load–store	2	2
ALU	1	2
Branches	3	2

(a) Assume that the clock rate of M1 is 1 GHz. What should be the clock rate of M2 so that both machines have the same execution time for P1?

$CPI_{M1P1} = 2 * 0.4 + 1*0.5 + 3*0.1 = 1.6$
$CPI_{M2P1} = 2 * 0.4 + 2*0.5 + 2*0.1 = 2$

CPI Ratio = 2/1.6 = 1.25
Ideal Clock Rate of M2 = 1.25 * 1GHz = 1.25GHz

The clock rate of M2 should be 1.25GHz so that both machines have the same execution time for P1

(b) Assume now that both machines have the same clock rate and that P1 and P2 execute the same number of instructions. Which machine is faster for a workload consisting of equal runs of P1 and P2?

$CPI_{M1P2} = 2 * 0.5 + 1*0.2 + 3*0.3 = 2.1$
$CPI_{M2P2} = 2 * 0.5 + 2*0.2 + 2*0.3 = 2$

$CPI_{M1P1} = 1.6$
$CPI_{M2P1} = 2$

$CPI_{M1P1P2} = 3.7$
$CPI_{M2P1P2} = 4$

$CPI_{M1P1P2} < CPI_{M2P1P2}$

Machine 1 is faster for a workload consisting of equal runs P1 and P2

(c) Find a workload (using only P1 and P2) that makes M1 and M2 have the same performance when they have the same clock rate.

No matter the process, M2 always takes 2 * I clock cycles independent of frequencies.
So we need to find a workload using P1 and P2 equal to 2
So for M1
Let x be the % of P1
$x * 1.6 + (1-x) * 2.1 = 2$
$0.1 = 0.5 * x$
$x = 0.2$
So 20 % of all runs are from P1 and 80% are from P2 to give M1 and M2 the same performance.

4. (**20 pts, 10/5/5**) Assume the sequential execution occurs in 15% of the program, i.e. other 85% of the program can be parallelized with N processor with a speedup of N :

(a) What is the maximum overall speedup with an infinite number of processors?

Max Speedup = $\frac{1}{(1-0.8) + (0.8/N)}$
N = Infinity
Max Speedup = $\frac{1}{(1-0.8) + 0}$
Max Speedup = 5

(b) How many processors are required to be within 20% of the maximum speedup?

$5 * 0.8 = 4$
$4 = \frac{1}{(1-0.8) + (0.8/N)}$
$4 = \frac{1}{(0.2 + (0.8/N))}$
$(0.2 + 0.8/N)*4 = 1$
$0.2 + 0.8/N = 0.25$
$0.8/N = 0.05$

0.05*N = 0.8
N = 16
16 Processors are needed to be within 20% of the maximum speedup

(c) How many processors are required to be within 2% of the maximum speedup?

5 * 0.98 = 4.9

$4.9 = \frac{1}{(1-0.8) + (0.8/N)}$

$4.9 = \frac{1}{(0.2 + (0.8/N))}$

(0.2 + 0.8/N)*4.9 = 1
0.2 + 0.8/N = 0.20408
0.8/N = 0.00408
0.00408*N = 0.8
N = 196
196 Processors are needed to be within 20% of the maximum speedup

5. (**20 pts, 5/5/10**) Availability is the most important consideration for designing servers, followed closely by scalability and throughput.

(a) We have a single processor with a failure in time (FIT) of 100. What is the mean time to failure (MTTF) for this system?

FIT = 100
MTTF = 1,000,000,000/FIT
MTTF = 1,000,000,000/100
MTTF = 10,000,000 hours

(b) If it takes one day to get the system running again, what is the availability of the system?

MTTR = 24hours
Module availability = MTTF/(MTTF + MTTR)
Module availability = 10,000,000 / (10,000,000 + 24)
Module availability = 0.9999976

(c) Imagine that the government, to cut costs, is going to build a supercomputer out of inexpensive computers rather than expensive, reliable computers. What is the MTTF for a system with 1000 processors mentioned in (a)? Assume the processor has the exponentially distributed lifetime and if one processor fails, the system fails.

Failure Rate = 1000*(1/10,000,000)
= 1000/10,000,000
= 10,000/100,000,000
= 100,000/1,000,000,000
= 100,000FIT