Part (a):

Describe how to break down the virtual address into:

Virtual page offset:

The page size is 1KB, so 1KB = 2^10, so 10 bits are needed to indicate the page offset. The last 10 bits of the virtual address correspond to the page offset.

Virtual Page number:

Since the last 10 bits are for the page offset, we have 16-10 = 6 bits for the virtual page number.

TLB Index:

TLB has 16 entries and is 2-way set associative. Therefore, we need 16/2 = 2^3 sets. So we need 3 bits to indicate TLB index.

TLB tag:

6 - 3 = 3 bits are left for the TLB tag, which are the first 3 bits of the virtual address.

Part (b):

Describe how to break down the physical address:

Physical Page offset:

Same as virtual page offset, so 10bits, the last 10bits of the physical address correspond to this

Physical Page Number:

Remaining bits in physical address are 16-10 = 6. So the first 6 bits are the physical page number

Cache block offset:

The block size is 16B, and $16=2^4$. 4 Bits are used for this field, so the last 4 bits of the physical address are used for this.

Cache set index: The cache is two way set associative and the cache size is 512B, so we have $512B/(2^{16})$ =

Cache tag:

Part (c):

	Memory Access	Hit (Y/N)	Bus Activity	No. of Bytes Exchanged
1	W 10-5-4	N	Write	16
2	R 10-10-10	N	Read	16
3	R 10-10-10	Y	None	1
4	W 5-4-0	N	Write	16
5	R 5-4-0	Y	None	1
6	R 10-10-5	Y	None	1
7	R 10-4-15	N	Both	16+16
8	W 10-10-5	Y	Write	16
9	W 10-10-6	Y	Write	16
10	R 5-10-10	N	Read	16