PE 0	PE 1 Out: 6 80:LOAD:3	PE 2 Out: 6 80:LOAD:3	PE 3	PE 4	PE 5 Out: 6 80:LOAD:3	PE 6	PE 7	PE 8	PE 9	PE 10	PE 11	PE 12	PE 13	PE 14	PE 15	C-Box		
	In0 : PE1.5 71:LOAD:0(ref In1 : PE1.266 72:CONST:10  72:DMA-LOAD  72:DMA-LOAD→ 0				In0 : PE5.258 86:CONST:2 In1 : PE1.6 80:LOAD:3  88:IMUL  88:IMUL→ 0	In0: PE6.19 69:LOAD:9 In1: PE2.6 80:LOAD:3  81:IADD→ 0			In0 : PE9.259 94:CONST:3 In1 : PE5.6 80:LOAD:3  96:IMUL  96:IMUL→ 0									
	Out: 0 72:DMA-LOAD	C72:DMA-LOAD→ 0  Out: 0 72:DMA-LOAD			Out: 0 88:IMUL→ 0  C96:IMUL→ 0	In0 : PE6.19 69:LOAD:9 In1 : PE5.0 88:IMUL  89:IADD→ 1			Out: 0 96:IMUL									
	In0: PE1.5 71:LOAD:0(ref In1: PE1.266 72:CONST:10				Out: 0 96:IMUL→ 17 In0: PE5.256 100:CONST:0	$\longrightarrow$				In0 : PE6.0 81:IADD						In1 : PE6 75:IF → 0  0: 75:IFGE(0)		
	3024:DMA-LOAD 0	In0 : PE6.1 89:IADD  90:STORE:11→ 12 0			101:STORE:13→ 17 0	97:IADD→ 20 0 Out: 1 89:IADD				82:STORE: $10 \rightarrow 30$ 0						0: 75:IFGE(0)		
	Out: 6 80:LOAD:3→ 1  In0: PE5.17 101:STORE:13 In1: PE2.12 90:STORE:11  165:IADD→ 1  Out: 1 165:IADD	Out : 12 90:STORE:11→ (		In0 : PE5.17 101:STORE:13  261:I2F→ 0	In0 : PE5.17 101:STORE:13 In1 : PE1.6 80:LOAD:3 106:IFGE	Out: 19 69:LOAD:9→ 0  In0: PE5.17 101:STORE:13 In1: PE10.30 82:STORE:10  141:IADD→ 0  Out: 20 98:STORE:12→ 1				Out: 30 82:STORE:10						0: 75:IFGE(0)  In1 : PE5 106:I → 1		
In0 : PE0.0 257:LOAD:6 In1 : PE4.0 261:I2F 262:FMUL	In0 : PE1.5 71:LOAD:0(ref In1 : PE1.261 94:CONST:5 122:DMA-LOAD(re	C165:IADD→ 1  Out: 0 69:LOAD:9			C98:STORE:12→ 0  Out: 0 98:STORE:12	C101:STORE:13→ 1  Out: 1 101:STORE:13→ 2  In0: PE6.1 101:STORE:13	In0 : PE7.5 71:LOAD:0(ref In1 : PE7.260 94:CONST:4 110:DMA-LOAD(re 0			In0 : PE6.1 101:STORE:13 In1 : PE10.257 585:CONST:						0: 106:IFGE(1)  0: 106:IFGE(1)		
262:FMUL	122:DMA-LOAD(re→ 2 0 Out : 2 122:DMA-LOAD(ref	Out: 1 165:IADD→ 0  C122:DMA-LOAD(r→ 0	C165:IADD→ 0			In1: PE2.0 69:LOAD:9 $117:IADD \rightarrow 2$ Out: 2 117:IADD $\rightarrow$ 3 $C110:DMA-LOAD(r \rightarrow 3)$	110:DMA-LOAD(re→ 0 0 Out: 0 110:DMA-LOAD(re	ef)	C98:STORE:12→ 0  In0: PE5.17 101:STORE:13 In1: PE9.0 98:STORE:12  189:IADD→ 1	In1 : PE10.257 585:CONST:  585:IADD→ 0								
262:FMUL			C122:DMA-LOAD(r→ 1 Out: 1 122:DMA-LOAD(re	C117:IADD→ 1	Out: $1\ 117:IADD \rightarrow 1$ C $C110:DMA-LOAD(r \rightarrow 1)$ ut: $1\ 110:DMA-LOAD(ref)$		→ 3  Dut: 0 110:DMA-LOAD(ref)			Out: 0 585:IADD								
262:FMUL→ 5  Out: 5 262:FMUL→ 5			In0 : PE3.1 122:DMA-LOAD( In1 : PE7.0 110:DMA-LOAD( 103:HANDLE-CMP 0		C141:IADD→ 1  Out: 1 141:IADD→ 1	Out : 2 117:IADD	C122:DMA-LOAD(r→ 0		Out : 1 189:IADD							0: 106:IFGE(1)  0: 106:IFGE(1)		
C261:I2F $\rightarrow$ 5  Out: 5 261:I2F $\rightarrow$ 5  C165:IADD $\rightarrow$ 5	C262:FMUL $\rightarrow$ 2  Out: 1 165:IADD $\rightarrow$ 1  C261:I2F $\rightarrow$ 1			C141:IADD→ 0  Out: 2 110:DMA-LOAD(ref)  In0: PE4.15 429:LOAD:8 In1: PE0.5 261:I2F  434:FMUL	C189:IADD→ 1  Out: 1 189:IADD	C189:IADD→ 4	130:DMA-LOAD(F) 0	C110:DMA-LOAD(r→ 0								0: 106:IFGE(1)		
	Out : 1 261:I2F  Out : 2 262:FMUL	In0 : PE2.11 343:LOAD:7 In1 : PE1.1 261:I2F 348:FMUL		Out : 1 117:IADD  434:FMUL		Out: 0 141:IADD→ 5  C130:DMA-LOAD(F→ 5	In0 : PE7.0 122:DMA-LOAD( In1 : PE6.0 141:IADD	In0: PE8.0 110:DMA-LOAD( In1: PE4.1 117:IADD  118:DMA-LOAD(F) 0			In0 : PE7.1 130:DMA-LOAD( 131:STORE:23→ 33 0					0: 106:IFGE(1)		
		348:FMUL	Out: 0 165:IADD	434:FMUL Out: 0 141:IADD	In0 : PE1.2 262:FMUL  274:FSIN		<b>→</b>	118:DMA-LOAD(F)→ 1 0 F) Out: 1 118:DMA-LOAD(F In0: PE8.0 110:DMA-LOAD(In1: PE4.0 141:IADD								0: 106:IFGE(1)  0: 106:IFGE(1)		
		348:FMUL		434:FMUL → 2	274:FSIN 274:FSIN	Out : 5 130:DMA-LOAD(F)		$142:DMA-LOAD(F)$ $0$ $142:DMA-LOAD(F) \rightarrow 2$ $0$	C118:DMA-LOAD(F→ 2	In0 : PE6.5 130:DMA-LOAD(	Out: 0 154:DMA-LOAD(F→ 0  Out: 0 154:DMA-LOAD(F  In0: PE7.1 130:DMA-LOAD( In1: PE11.0 154:DMA-LOAD  248:FSUB					0: 106:IFGE(1)		
Out: 5 165:IADD→ 3  In0: PE4.2 434:FMUL  435:STORE:38→ 3	0 Out: 2 262:FMUL→ 9		C178:DMA-LOAD(F→ 1	Out: 2 434:FMUL→ 3  C165:IADD→ 3  Out: 3 165:IADD→ 4	274:FSIN		Unt: 1 178:DMA-LOAD(F)  In0: PE7.0 122:DMA-LOAD(In1: PE6.4 189:IADD  202:DMA-LOAD(F)  0	0	C142:DMA-LOAD(F→ 3  Out: 3 142:DMA-LOAD(F	222:FADD	248:FSUB					0: 106:IFGE(1)  0: 106:IFGE(1)		
	In0 : PE2.0 348:FMUL  349:STORE:34→ 9 0	C262:FMUL→ 1  Out: 1 262:FMUL→ 1	Out: 1 178:DMA-LOAD(F	C118:DMA-LOAD(F→ 4  Dut: 4 118:DMA-LOAD(F)→	274:FSIN	<b>———</b>	202:DMA-LOAD(F)→ 1 0	0 Out : 2 142:DMA-LOAD(F)-	→ 2	222:FADD	248:FSUB		C142:DMA-LOAD(F→ 0			0: 106:IFGE(1)		
C118:DMA-LOAD(F→ 5  Dut: 5 118:DMA-LOAD(F)  In0: PE4.4 142:DMA-LOAD  143:STORE:24→ 1	) → 1	C178:DMA-LOAD(F→ 1		C142:DMA-LOAD( $F \rightarrow 4$ Dut: 4 142:DMA-LOAD( $F$ )  C166:DMA-LOAD( $F \rightarrow 4$	274:FSIN 274:FSIN→ 1	267:FCOS 267:FCOS	203:STORE:29→ 22 0	166:DMA-LOAD(F)→ 2 0 Out: 2 166:DMA-LOAD(F) In0: PE8.0 110:DMA-LOAD(In1: PE9.1 189:IADD 190:DMA-LOAD(F)		222:FADD	248:FSUB					0: 106:IFGE(1)		
	Out: 2 262:FMUL $\rightarrow$ 7  In0: PE2.1 178:DMA-LOAD(  179:STORE:27 $\rightarrow$ 7  Out: 1 118:DMA-LOAD(F) $\rightarrow$			Dut : 4 166:DMA-LOAD(F)→	C262:FMUL→ 2  Solut: 2 262:FMUL→ 2	267:FCOS	Out : 1 202:DMA-LOAD(F	190:DMA-LOAD(F)→ 3 0 R)ut: 3 190:DMA-LOAD(F)—	28	222:FADD→ 0	248:FSUB→ 1 Out: 0 154:DMA-LOAD(F)-	→ <b>(</b>				0: 106:IFGE(1)  0: 106:IFGE(1)		
	C348:FMUL→ 1  Out: 1 348:FMUL→ 1		In0 : PE2.0 118:DMA-LOAD( In1 : PE7.2 154:DMA-LOAD(		C166:DMA-LOAD( $F \rightarrow 2$ Out: 1 274:FSIN $\rightarrow$ 1	267:FCOS	Out: 2 154:DMA-LOAD(F)-	In0 : PE8.3 190:DMA-LOAD(  191:STORE:28→ 23  0	In0 : PE5.2 262:FMUL  263:STORE:30→ 29 0  Out : 3 142:DMA-LOAD(F)-	C154:DMA-LOAD(F→ 1 Put: 1 154:DMA-LOAD(F)-	, , , , , , , , , , , , , , , , , , ,							
C348:FMUL→ 5  Out: 5 348:FMUL	C178:DMA-LOAD(F→ 2	In0: PE1.1 274:FSIN	321:FADD		C348:FMUL $\rightarrow$ 1  Out: 2 166:DMA-LOAD(F)-  C434:FMUL $\rightarrow$ 3	267:FCOS  267:FCOS	C248:FSUB→ 2	C154:DMA-LOAD(F→ 4	In0 : PE5.2 166:DMA-LOAD( In1 : PE8.3 190:DMA-LOAD( 209:FADD	) Φut : 1 142:DMA-LOAD(F)	C142:DMA-LOAD(F→ 0	→ (	In0 : PE9.1 154:DMA-LOAD( 155:STORE:25→ 34		C202:DMA-LOAD(F→ 0	0: 106:IFGE(1)		
C178:DMA-LOAD(F→ 5		Out: 0 118:DMA-LOAD(F)->	321:FADD	360:FSIN	Out: 3 434:FMUL	267:FCOS→ 4  Out: 4 267:FCOS→ 4		<pre>put : 4 154:DMA-LOAD(F</pre> put : 1 118:DMA-LOAD(F	209:FADD		Out: 0 142:DMA-LOAD(F	C154:DMA-LOAD(F→ 0	In0 : PE9.2 118:DMA-LOAD(In1 : PE13.0 142:DMA-LOAD) 212:FADD		Out: 0 202:DMA-LOAD(F)-			
		C274:FSIN→ 0	321:FADD		C267:FCOS→ 4  Out: 2 166:DMA-LOAD(F)		→ 4		209:FADD			In0 : PE8.1 118:DMA-LOAD( In1 : PE12.0 154:DMA-LOAD 407:FSUB	212:FADD					
			321:FADD 321:FADD→ 2	360:FSIN		C248:FSUB→ 5	In0 : PE6.4 166:DMA-LOAD( 167:STORE:26→ 21		209:FADD  209:FADD	C118:DMA-LOAD(F→ 1  Out: 1 118:DMA-LOAD(F)	C118:DMA-LOAD(F→ 0	407:FSUB 407:FSUB	212:FADD  212:FADD	In0 : PE10.1 118:DMA-LOAD  119:STORE:22→ 35 0		0: 106:IFGE(1)		
	φut : 2 178:DMA-LOAD(F)	Out : 1 178:DMA-LOAD(F)->	Out : 2 321:FADD	360:FSIN	In0: PE6.5 248:FSUB In1: PE1.2 178:DMA-LOAD(  251:FADD  Out: 1 348:FMUL	Out : 5 248:FSUB→ 6  C222:FADD→ 6  Out : 6 222:FADD→ 6	C321:FADD→ 2		209:FADD→ 1	Out: 0 222:FADD	Out: 0 118:DMA-LOAD(F	407:FSUB	212:FADD		In0 : PE11.0 118:DMA-LOAD In1 : PE15.1 142:DMA-LOAD 235:FSUB			
	Out : 3 434:FMUL→ 1		In0 : PE2.1 222:FADD In1 : PE3.1 178:DMA-LOAD(	360:FSIN→ 2	251:FADD Out: 4 267:FCOS	C178:DMA-LOAD( $F \rightarrow 6$	J [	F)	In0 : PE5.1 348:FMUL  353:FCOS  Out : 1 209:FADD			407:FSUB	212:FADD→ 0  In0 : PE13.0 212:FADD In1 : PE9.1 209:FADD		235:FSUB			
In0 : PE1.1 222:FADD In1 : PE0.5 178:DMA-LOAD	C222:FADD→ 1  Out: 1 222:FADD	439:FCOS	423:FSUB	C267:FCOS→ 6  Out: 6 267:FCOS	251:FADD	Out: 5 248:FSUB  Out: 5 248:FSUB  In0: PE5.3 434:FMUL  446:FSIN		In0 : PE4.6 267:FCOS  270:STORE:31→ 24 0	353:FCOS 353:FCOS	C178:DMA-LOAD(F→ 0  In0: PE6.5 248:FSUB In1: PE10.0 178:DMA-LOAD  337:FSUB		407:FSUB→ 0	215:FADD  215:FADD		235:FSUB 235:FSUB	0: 106:IFGE(1)		
225:FADD		439:FCOS	423:FSUB	Out : 6 267:FCOS	251:FADD	Out : 4 166:DMA-LOAD(F)	C166:DMA-LOAD(F→ 1  Out: 1 166:DMA-LOAD(F	C407:FSUB $\rightarrow$ 1  F) Out: 1 407:FSUB $\rightarrow$ 1	353:FCOS	337:FSUB		Out: 0 407:FSUB	215:FADD		235:FSUB			
225:FADD		439:FCOS	423:FSUB	In0 : PE8.1 407:FSUB In1 : PE4.4 166:DMA-LOAD( 410:FSUB Out : 2 360:FSIN	251:FADD→ 1	446:FSIN	Out : 2 321:FADD	C267:FCOS→ 1	353:FCOS	337:FSUB	C166:DMA-LOAD(F→ 0  In0 : PE7.2 321:FADD In1 : PE11.0 166:DMA-LOAD		215:FADD		235:FSUB→ 1  Out: 1 235:FSUB			
225:FADD  225:FADD		439:FCOS	423:FSUB 423:FSUB→ 1		C360:FSIN→ 2  In0 : PE6.3 585:IADD  585:STORE:13→ 17 0	446:FSIN  Out: 3 585:IADD  446:FSIN  Out: 6 202:DMA-LOAD(F)			353:FCOS  353:FCOS→ 1  Out: 1 353:FCOS→ 2	337:FSUB	324:FSUB		$215:FADD$ $215:FADD \to 0$ $Out: \ 0 \ 215:FADD \to 0$	C235:FSUB→ 1		0: 106:IFGE(1)		
225:FADD→ 5  Out: 5 225:FADD		439:FCOS→ 1	Out : 1 423:FSUB	410:FSUB Out: 1 117:IADD	C202:DMA-LOAD(F→ 3	446:FSIN		In0 : PE9.1 353:FCOS  356:STORE:35→ 25 0  Out : 2 166:DMA-LOAD(F	C215:FADD→ 2  Out: 2 215:FADD	337:FSUB→ 0	324:FSUB		C235:FSUB→ 0  Out: 0 235:FSUB	Out : 1 233.1 30B		0: 106:IFGE(1)  0: 106:IFGE(1)		
	C225:FADD→ 1  Out: 1 225:FADD→ 1	C423:FSUB→ 2  Out : 2 423:FSUB			C215:FADD→ 5  Out: 2 360:FSIN→ 2	446:FSIN→ 3		In0: PE8.0 110:DMA-LOAD( In1: PE4.1 117:IADD In2: PE9.2 215:FADD  500:DMA-STORE(F  0  Out: 3 190:DMA-LOAD(F	In0: PE10.0 337:FSUB In1: PE8.3 190:DMA-LOAD(			In0 : PE13.0 235:FSUB In1 : PE8.2 166:DMA-LOAD( 238:FADD						
	C423:FSUB $\rightarrow$ 1  Out: 1 423:FSUB $\rightarrow$ 1  C439:FCOS $\rightarrow$ 1  Out: 1 439:FCOS $\rightarrow$ 2			410:FSUB→ 1  Out: 5 190:DMA-LOAD(F)	In0 : PE1.1 423:FSUB In1 : PE4.5 190:DMA-LOAD( 426:FSUB	C360:FSIN→ 4  Out: 4 360:FSIN→ 4  C251:FADD→ 4  Out: 4 251:FADD→ 4			340:FADD  340:FADD	C353:FCOS $\rightarrow$ 0  C360:FSIN $\rightarrow$ 1  Out: 1 360:FSIN	324:FSUB 324:FSUB→ 0	238:FADD  238:FADD						
In0 : PE1.1 439:FCOS  442:STORE:39→ 4					426:FSUB	C274:FSIN→ 4	C251:FADD $\rightarrow$ 1  Out: 1 251:FADD $\rightarrow$ 1		340:FADD		C360:FSIN→ 1  Out: 0 324:FSUB→ 0	238:FADD		In0 : PE10.1 360:FSIN  363:STORE:36→ 37 0		0: 106:IFGE(1)		
		C215:FADD→ 1  Out: 1 215:FADD	In0 : PE2.1 215:FADD  216:STORE:14→ 14		426:FSUB	In0 : PE7.1 324:FSUB In1 : PE6.6 202:DMA-LOAD(	C324:FSUB → 1  Out : 1 324:FSUB		340:FADD		C251:FADD→ 0  Out: 0 251:FADD	238:FADD  238:FADD→ 0			In0 : PE11.0 251:FADD In1 : PE15.0 202:DMA-LOAD	0: 106:IFGE(1)		
					426:FSUB  Out: 2 225:FADD→ 1	327:FSUB		<pre>put : 3 190:DMA-LOAD(F</pre>	340:FADD→ 1  Out: 1 340:FADD→ 2			In0 : PE12.0 238:FADD In1 : PE8.3 190:DMA-LOAD( 241:FSUB			254:FSUB			
					426:FSUB→ 1  Out: 1 426:FSUB→ 2	327:FSUB Out: 3 446:FSIN			C225:FADD→ 2  Out: 2 225:FADD	In0 : PE9.1 340:FADD In1 : PE10.0 353:FCOS 390:FMUL		241:FSUB	In0 : PE9.2 225:FADD In1 : PE14.0 202:DMA-LOAD	Out: 0 202:DMA-LOAD(F)	254:FSUB			
	C426:FSUB→ 2  Out: 2 426:FSUB	In0 : PE6.3 446:FSIN In1 : PE1.2 426:FSUB 468:FMUL		C446:FSIN→ 4	C446:FSIN $\rightarrow$ 2  Out: 2 446:FSIN $\rightarrow$ 2  C340:FADD $\rightarrow$ 2	327:FSUB  Out: 3 446:FSIN  327:FSUB			Out : 1 340:FADD	390:FMUL 390:FMUL		241:FSUB 241:FSUB	228:FADD  228:FADD		254:FSUB			
	Out : 1 439:FCOS	468:FMUL		In0 : PE4.1 410:FSUB In1 : PE5.3 202:DMA-LOAD( 413:FADD	Out: 3 202:DMA-LOAD(F)-	327:FSUB→ 5  Out: 5 327:FSUB		In0 : PE4.4 446:FSIN  449:STORE:40→ 28 0		390:FMUL		241:FSUB	228:FADD		254:FSUB→ 0 Out: 0 254:FSUB	0: 106:IFGE(1)		
In0: PE4.2 360:FSIN In1: PE1.1 340:FADD	C340:FADD→ 1  Out: 1 340:FADD	468:FMUL		413:FADD Out: 2 360:FSIN	C327:FSUB→ 2  Out: 3 439:FCOS		C327:FSUB→ 1  Out: 1 327:FSUB→ 1	Out: 1 267:FCOS→ 1		390:FMUL→ 1	C254:FSUB→ 0  Out: 0 254:FSUB→ 0	241:FSUB → 0  Out: 0 241:FSUB  In0: PE12.0 241:FSUB In1: PE8.1 267:FCOS	228:FADD					
382:FMUL  382:FMUL		468:FMUL→ 0	In0 : PE2.0 274:FSIN In1 : PE7.1 254:FSUB 296:FMUL	413:FADD  413:FADD	Out: 1 426:FSUB	C254:FSUB→ 5	C254:FSUB→ 1  Out: 1 254:FSUB	C241:FSUB→ 1	C439:FCOS→ 1  In0 : PE5.1 426:FSUB In1 : PE9.1 439:FCOS  476:FMUL	Out: 0 353:FCOS	C327:FSUB→ 0  Out: 0 327:FSUB  In0: PE11.0 327:FSUB In1: PE10.0 353:FCOS  373:FMUL	287:FMUL 287:FMUL	228:FADD  228:FADD→ 0		C327:FSUB→ 0			
382:FMUL	C468:FMUL→ 1	Out: 0 468:FMUL	296:FMUL	413:FADD	In0 : PE6.5 254:FSUB In1 : PE5.4 267:FCOS 304:FMUL	Out: 5 254:FSUB			Out : 1 439:FCOS  476:FMUL		Out : 1 360:FSIN  373:FMUL	287:FMUL	Out: 0 228:FADD→ 1  C439:FCOS→ 1	In0 : PE13.0 228:FADD  229:STORE:15→ 36 0	In0 : PE11.1 360:FSIN In1 : PE15.0 327:FSUB 399:FMUL	0: 106:IFGE(1)		
382:FMUL			296:FMUL	413:FADD→ 1	304:FMUL Out: 2 327:FSUB				476:FMUL		373:FMUL	287:FMUL			399:FMUL			
382:FMUL→ 5  Out: 5 382:FMUL	C382:FMUL→ 2		296:FMUL→ 1 Out: 1 296:FMUL	C327:FSUB→ 2  Out: 2 327:FSUB  Out: 1 413:FADD	304:FMUL			In0: PE4.2 327:FSUB $367:STORE:37 \rightarrow 26$ $0$ Out: 1 241:FSUB $\rightarrow$ 1	476:FMUL 476:FMUL→ 1		373:FMUL→ 0	287:FMUL→ 0  Out: 0 287:FMUL			399:FMUL 399:FMUL	0: 106:IFGE(1)		
	Out : 2 382:FMUL→ 2	C296:FMUL→ 0	Out: 1 296:FMUL	Out : 1 413:FADD	304:FMUL→ 1	Out : 4 274:FSIN		Out : 1 241:FSUB→ 1  C287:FMUL→ 1	C241:FSUB→ 2  Out: 2 241:FSUB→ 2			Out: 0 287:FMUL	Out: 0 228:FADD		399:FMUL→ 0 Out: 0 399:FMUL			
		In0 : PE6.3 446:FSIN In1 : PE1.2 413:FADD			C228:EADD + 2	Out : 3 446:FSIN			C228:FADD→ 2  Out: 2 228:FADD→ 2					C399:FMUL→ 0  Out: 0 399:FMUL		0: 106:IFGE(1)		
	$281:STORE:33 \rightarrow 8$ $0$ Out: 2 413:FADD \rightarrow 2 $C296:FMUL \rightarrow 2$ Out: 2 296:FMUL	485:FMUL  Out: 0 296:FMUL  485:FMUL	C382:FMUL→ 1  Out: 1 382:FMUL		C228:FADD $\rightarrow$ 2  Out: 2 228:FADD $\rightarrow$ 2  C413:FADD $\rightarrow$ 2  Out: 2 413:FADD	C228:FADD→ 3  Out: 3 228:FADD	C382:FMUL $\rightarrow$ 1  Out: 1 382:FMUL $\rightarrow$ 1	C390:FMUL→ 2  Out: 2 390:FMUL	C390:FMUL→ 2  Out: 2 390:FMUL	313:FMUL			C399:FMUL→ 0  Out: 0 399:FMUL					
	Out : 1 468:FMUL	485:FMUL				Out : 2 117:IADD	C228:FADD→ 1	Out : 1 287:FMUL	C413:FADD→ 2  Out: 2 413:FADD	313:FMUL	In0 : PE11.0 373:FMUL In1 : PE7.1 382:FMUL  383:FSUB	In0 : PE8.2 390:FMUL In1 : PE13.0 399:FMUL 400:FADD				0: 106:IFGE(1)		
		485:FMUL 485:FMUI → 0		In0 : PE8.1 287:FMUL In1 : PE0.5 296:FMUL  297:FSUB	C468:FMUL→ 2  Out: 1 304:FMUL	In0 : PE5.1 304:FMUL In1 : PE10.0 313:FMUL	In0 : PE7.0 122:DMA-LOAD( In1 : PE6.2 117:IADD In2 : PE7.1 228:FADD  512:DMA-STORE(F  0		Out : 2 413:FADD	$313:FMUL \rightarrow 0$ Out: $0.313:FMUL \rightarrow 0$ $C413:FADD \rightarrow 0$		400:FADD	In0 : PE9.2 413:FADD In1 : PE13.1 439:FCOS 459:FMUL					
	C485:FMUL→ 1  Out: 1 485:FMUL	485:FMUL→ 0  Out: 0 485:FMUL		297:FSUB		314:FADD			Out : 1 476:FMUL	C413:FADD → 0  Out: 0 413:FADD	383:FSUB 383:FSUB	400:FADD	459:FMUL	In0 : PE10.0 413:FADD  453:STORE:41→ 38 0		0: 106:IFGE(1)		
	1 485:FMUL			297:FSUB	In0 : PE9.1 476:FMUL In1 : PE1.1 485:FMUL 486:FADD	314:FADD			1 4/6:FMUL		383:FSUB	400:FADD	459:FMUL					
				297:FSUB	486:FADD Out: 2 468:FMUL	314:FADD		In0 : PE12.0 400:FADD  401:STORE:19 > 27		In0: PE11.0 383:FSUB	383:FSUB→ 0  Out: 0 383:FSUB	400:FADD→ 0  Out: 0 400:FADD	459:FMUL→ 0  Out: 0 459:FMUL			0: 106:IFGE(1)		
				297:FSUB→ 1  Out: 1 297:FSUB  Out: 0 141:IADD	486:FADD	314:FADD → 2  Out: 2 314:FADD		401:STORE:19 $\rightarrow$ 27 0	469:FSUB 469:FSUB	384:STORE:18 $\rightarrow$ 32 0 C383:FSUB $\rightarrow$ 0	Out: 0 383:FSUB					0: 106:IFGE(1)		
In0 : PE4.1 297:FSUB  298:STORE:16→ 2				Out : 0 141:IADD	486:FADD	Out: 0 141:IADD	C314:FADD→ 1	In0 : PE8.0 110:DMA-LOAD( In1 : PE4.0 141:IADD In2 : PE8.1 297:FSUB 524:DMA-STORE(F	469:FSUB	In0 : PE6.2 314:FADD  315:STORE:17→ 31 0		Out: 0 400:FADD				0: 106:IFGE(1)  0: 106:IFGE(1)		
					486:FADD→ 1  Out: 1 486:FADD		In0: PE7.0 122:DMA-LOAD( In1: PE6.0 141:IADD In2: PE7.1 314:FADD  536:DMA-STORE(F  0	C400:FADD→ 1  Out: 1 400:FADD	469:FSUB							0: 100:IFGE(1)		
298:STORE:16→ 2	In0 : PE5.1 486:FADD					C486:FADD→ 0			469:FSUB									
298:STORE:16→ 2	In0 : PE5.1 486:FADD  487:STORE:21→ 10 0			C400:FADD → 0  Out: 0 400:FADD	C400:FADD→ 18			]	469:FSUB→ 1 Out : 1 469:FSUB→ 2				]	]			] [	
298:STORE:16→ 2			Out: 0 165:IADD	Out: 0 400:FADD	C400:FADD $\rightarrow$ 1  Out: 1 400:FADD $\rightarrow$ 18  In0: PE9.1 469:FSUB  470:STORE:20 $\rightarrow$ 18 0	C400:FADD→ 2  Out: 2 400:FADD			469:FSUB→ 1  Out: 1 469:FSUB→ 2  C383:FSUB→ 2  Out: 2 383:FSUB	Out: 0 383:FSUB						0: 106:IFGE(1)  0: 106:IFGE(1)		
298:STORE:16→ 2			Out: 0 165:IADD	Out : 0 400:FADD  Out : 3 165:IADD  Out : 3 165:IADD	Out: $1 \ 400:FADD \rightarrow 18$ In0: PE9.1 $469:FSUB$ $470:STORE:20 \rightarrow 18$ $0$	Out : 2 400:FADD  Out : 0 486:FADD	In1: PE3.0 165:IADD In2: PE6.2 400:FADD  560:DMA-STORE(F  0  In0: PE7.0 122:DMA-LOAD(In1: PE3.0 165:IADD	In1: PE4.3 165:IADD	Out: 1 469:FSUB → 2  C383:FSUB → 2  Out: 2 383:FSUB  Out: 1 469:FSUB	Out: 0 383:FSUB								
298:STORE:16→ 2 (1)				Out : 0 400:FADD  Out : 3 165:IADD  Out : 3 165:IADD	Out: $1 \ 400:FADD \rightarrow 18$ In0: PE9.1 $469:FSUB$ $470:STORE:20 \rightarrow 18$ $0$	Out : 2 400:FADD  Out : 0 486:FADD	In1: PE3.0 165:IADD In2: PE6.2 400:FADD  560:DMA-STORE(F  0  In0: PE7.0 122:DMA-LOAD(	In1: PE4.3 165:IADD In2: PE9.2 383:FSUB 548:DMA-STORE(F 0 In0: PE8.0 110:DMA-LOAD(	Out: 1 469:FSUB → 2  C383:FSUB → 2  Out: 2 383:FSUB  Out: 1 469:FSUB	Out: 0 383:FSUB						0: 106:IFGE(1)		