Placement with Irregularities

Mini Task Report

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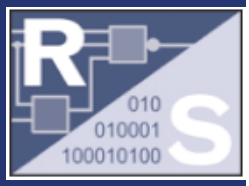

1 Introduction

1.1 stuff

2 Task Description

2.1 Is that even necessary?

3 Approaches to the Problem

3.1 Isoelectric Plane Search

here we tell about the potential stuff

3.2 Hand Routing

handrouting tells us that bullshit is happening

4 Insights

In the process of the task, we found out that... X Y Z doesn't work as expected

4.1 Possible Solutions

For the encountered problems, we propose the following approaches

5 Conclusion

the task was to - examine re-placed designs' net lists

- find out if something does not work

- expected: only one or two PIPs are missing due to irreguar structure of FPGA

- if problem is encountered, find rule/mask based method to fix these missing pips

what we did was:

- handle net by net

- for each Pin, determine all elements of the isoelectric it is connected to (class potential)

- checking method: if (potential(source)!=potential(sink) -> broken

- for broken nets:

- search isoelectric of source, sink for adjacent, non-set PIPs (interesction of sets). if !=empty set, activate this pip

- why it did not work:

- even for correct (in terms of make file) nets, the method fails

- hand routing (function of RapidSmith framework) neither does

- we suspect missing information in fabric;

- according to the hand router, the method of "isoelectric search"

results in correct sub nets; might be useful for later work