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ECEC 414
Simulation Project
Introduction to gem5

Cache Experiment

Experiment Chosen: Keep number of processors fixed at 4, block size fixed at 64B and vary L1 cache capacity : 16KB, 32KB, 64KB

Benchmarks Used: FFT, WaterSpatial

Results:

	FFT				WaterSpatial			
L1 Cache Size (KB)	L1 Cache Avg Miss Rate	L2 Bus Traffic (Trans/Proc)	Execution Cycles	Harmonic Mean IPC	L1 Cache Avg Miss Rate	L2 Bus Traffic (Trans/Proc)	Execution Cycles	Harmonic Mean IPC
16	0.04713	63754.25	28594813	2.0314	0.00813	250241.5	225482432	2.6020
32	0.04598	61257.5	28501404	2.0406	0.00506	162422.5	223032033	2.6296
64	0.04569	60286.5	28446048	2.0465	0.00323	89644.75	220334496	2.6599

The following parameters have the specified behavior as L1 cache size is increased:

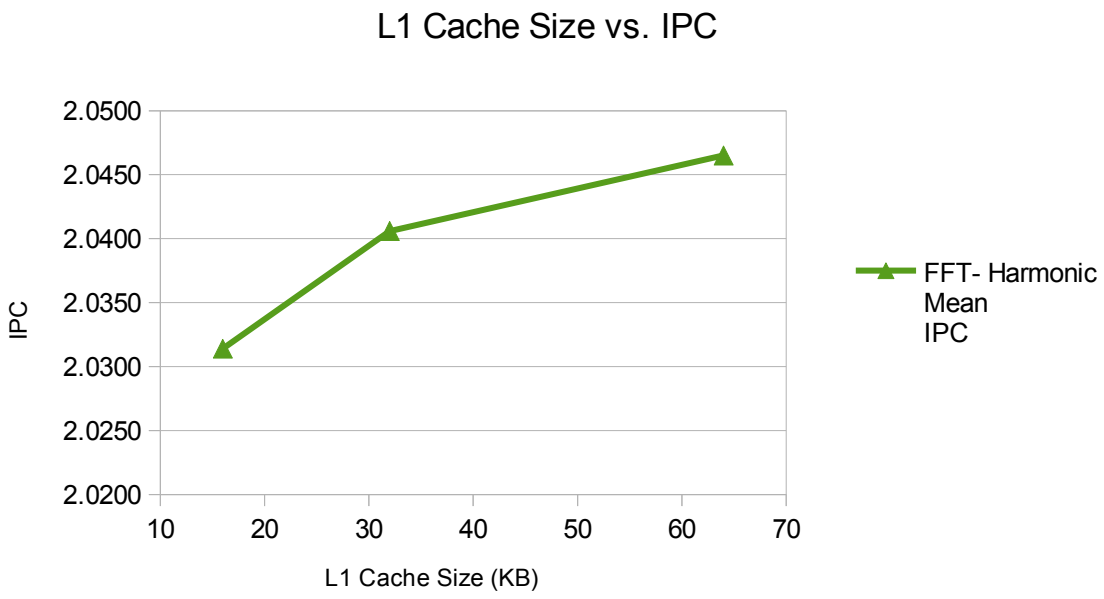
- Miss rate: decreases
- L2 bus traffic: decreases
- Execution cycles: decreases
- IPC: increases

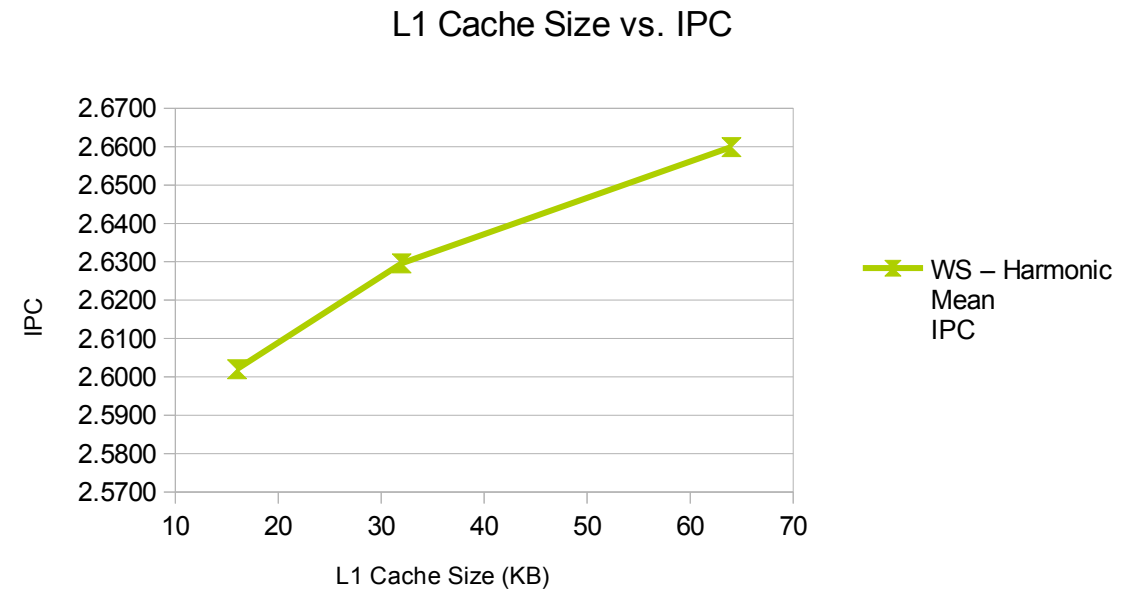
Result Explanations:

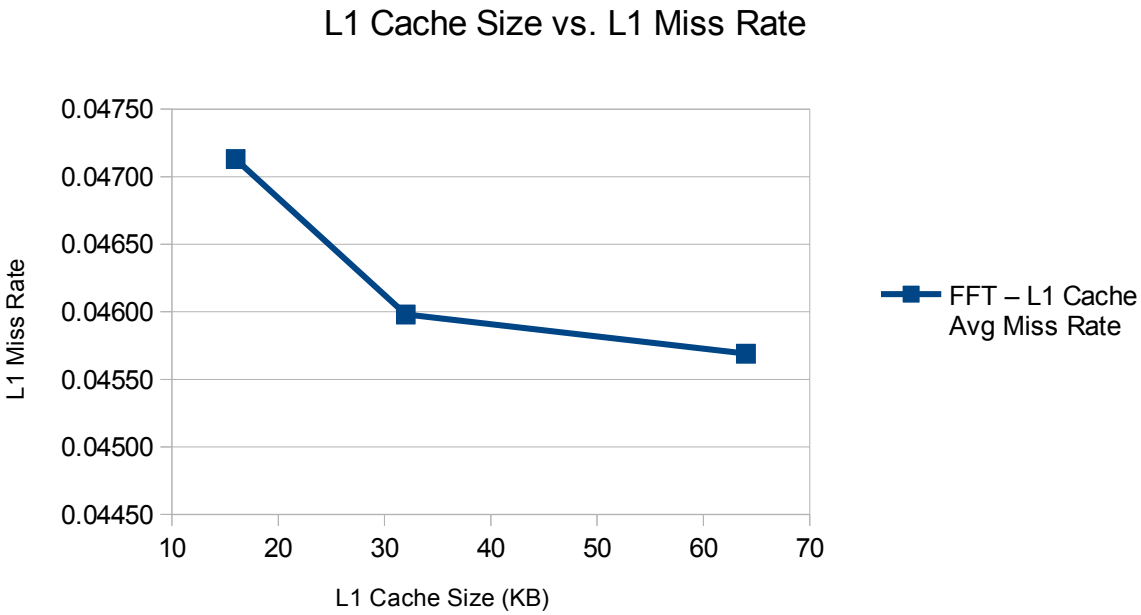
- Miss rate: decreases
  - Since more data can be stored in the L1 cache, it is more likely that the data requested will already be present in the cache → decreasing L1 miss rate.
- L2 bus traffic: decreases
  - Since more data is being found in the L1 cache, less requests to the L2 cache are made → L2 bus traffic decreases.
- Execution cycles: decreases
  - Since extra cycles do not need to be 'spent' accessing L2 or main memory (due to larger L1) the number of total execution cycles decreases.
- IPC: increases
  - When more memory operations can be completed through L1 cache, on average it takes less cycles to complete a single instruction → larger IPC.

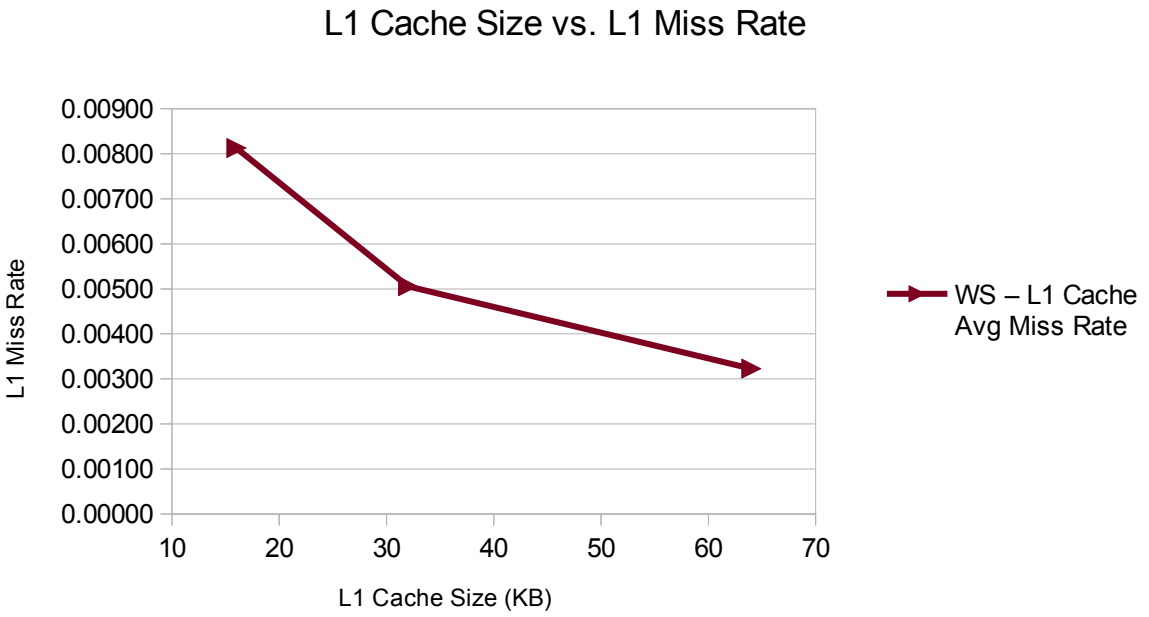
Workload Analysis:

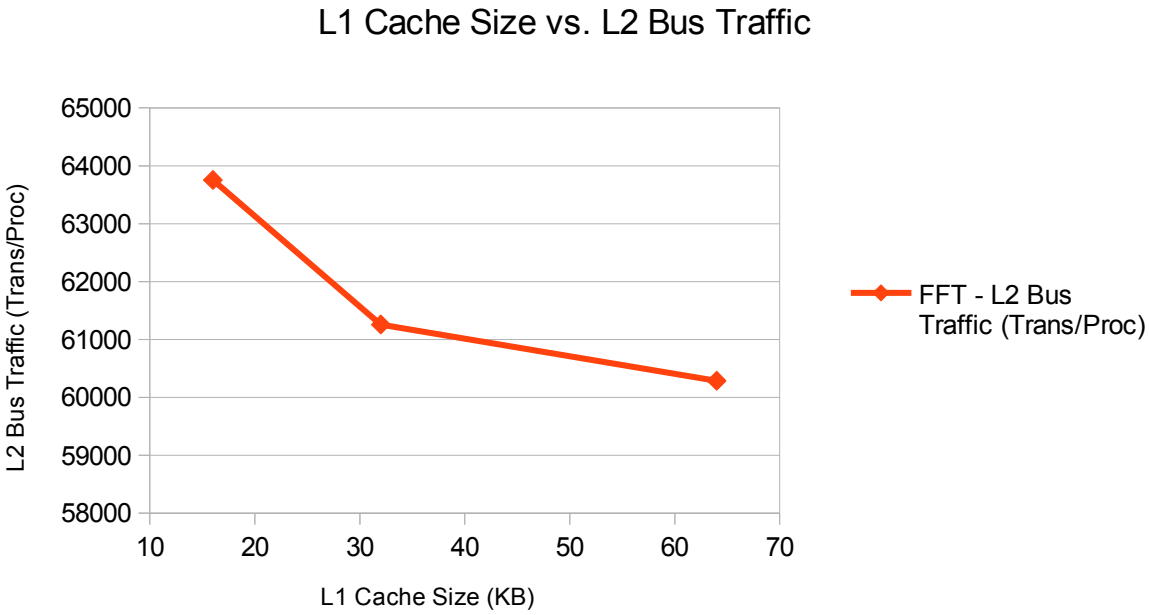
- Miss rate: decreases
  - WaterSpatial shows a sharper decrease in miss rate as the L1 becomes larger. This would indicate that the cache configuration for L1 is such that WaterSpatial benefits more than FFT (i.e. WaterSpatial likely has higher temporal and spacial data locality throughout the code)
- L2 bus traffic: decreases
  - Again, WaterSpatial shows a sharper decrease in L2 bus traffic. This can be directly correlated to the decrease in L1 misses as described above.
- Execution cycles: decreases
  - Both FFT and WaterSpatial have approximately equal decreases in execution cycles (as a percentage of the original number of cycles). This would indicate that both benchmarks have an approximately equal percentage of instructions that benefit from larger L1 cache sizes.
- IPC: increases
  - WaterSpatial shows a larger increase in IPC, this can be directly correlated to the lower miss rate in the L1 cache as described above.

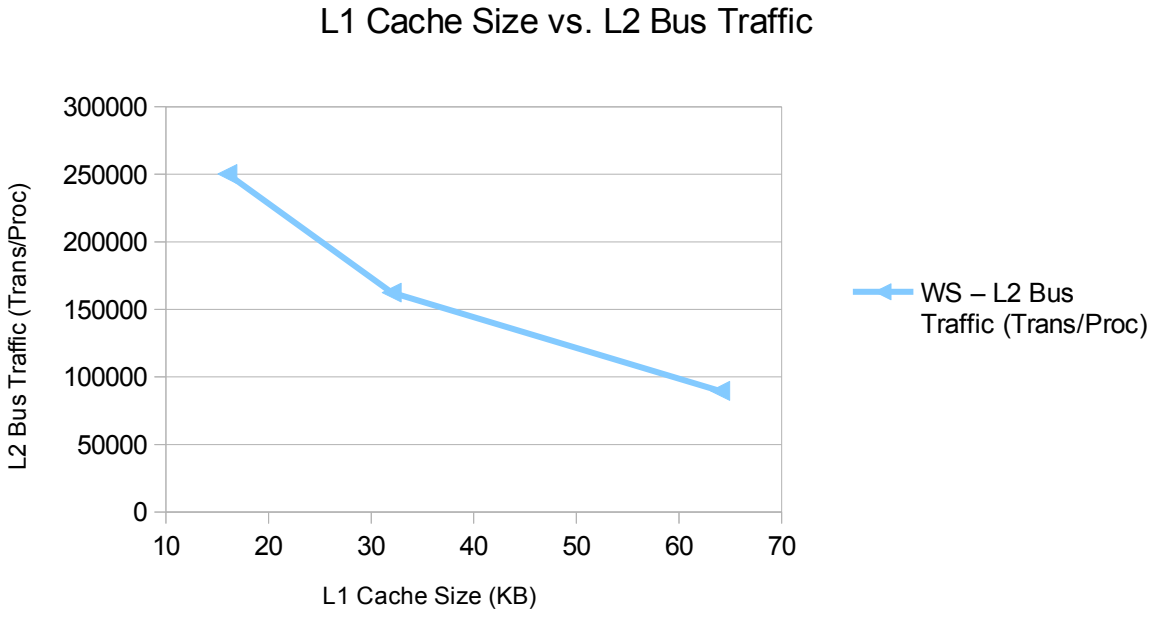


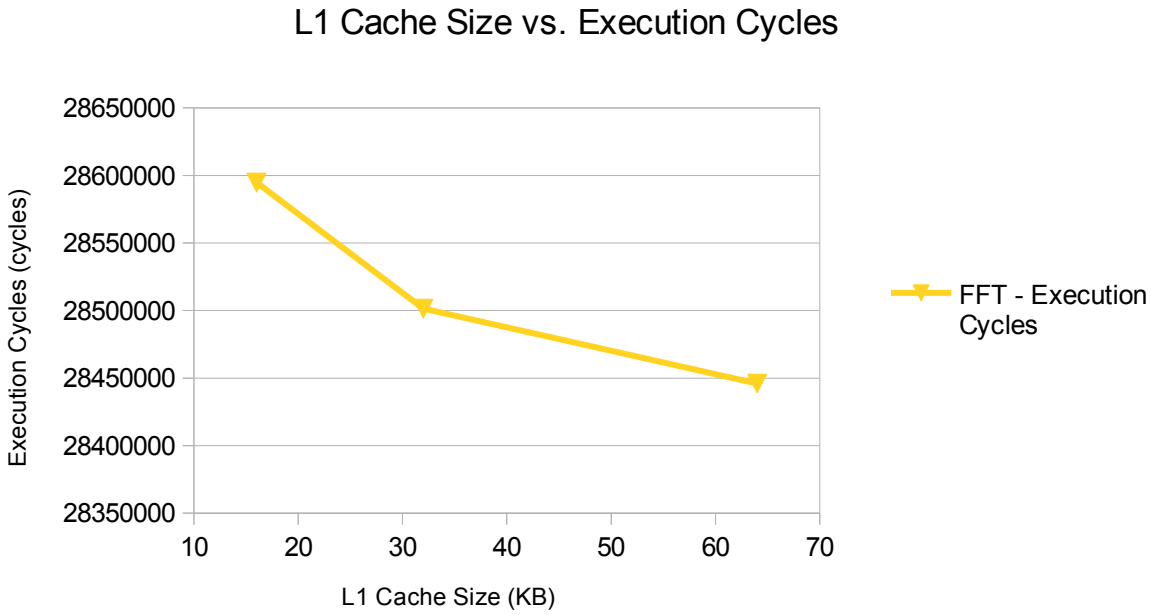

L1 Cache Size vs. IPC
IPC
2.6700
2.6600
2.6500
2.6400
2.6300
2.6200
2.6100
2.6000
2.5900
2.5800
2.5700
10
20
30
40
50
60
70
L1 Cache Size (KB)
WS – Harmonic Mean IPC

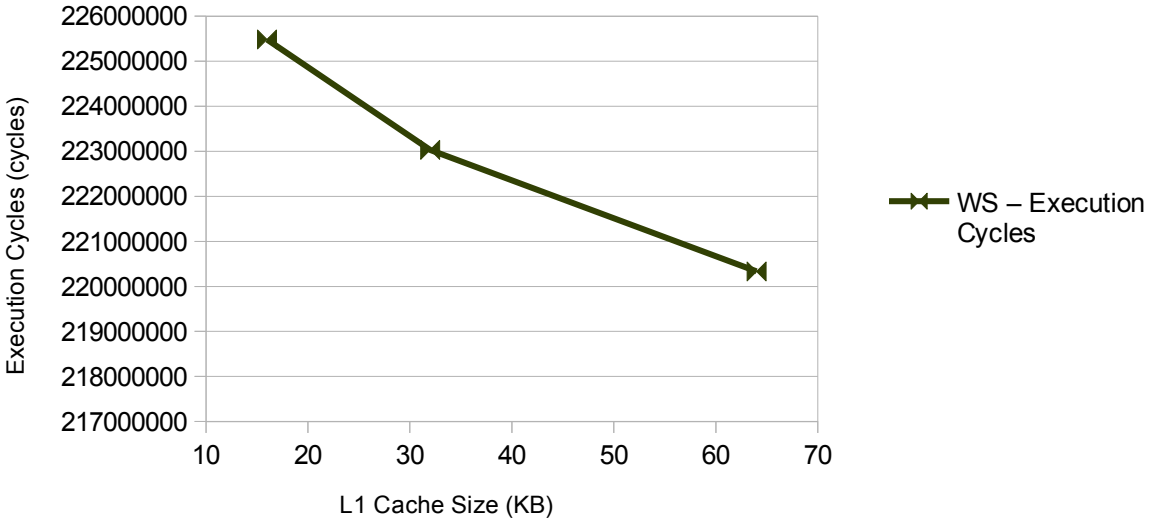

L1 Cache Size vs. L1 Miss Rate
L1 Miss Rate
0.04750
0.04700
0.04650
0.04600
0.04550
0.04500
0.04450
10
20
30
40
50
60
70
L1 Cache Size (KB)
FFT – L1 Cache Avg Miss Rate


L1 Cache Size vs. L1 Miss Rate
0.00900
0.00800
0.00700
0.00600
0.00500
0.00400
0.00300
0.00200
0.00100
0.00000
L1 Miss Rate
10
20
30
40
50
60
70
L1 Cache Size (KB)
WS – L1 Cache Avg Miss Rate


L1 Cache Size vs. L2 Bus Traffic
65000
64000
63000
62000
61000
60000
59000
58000
L2 Bus Traffic (Trans/Proc)
10
20
30
40
50
60
70
L1 Cache Size (KB)
FFT - L2 Bus Traffic (Trans/Proc)


L1 Cache Size vs. L2 Bus Traffic
L2 Bus Traffic (Trans/Proc)
300000
250000
200000
150000
100000
50000
0
10
20
30
40
50
60
70
L1 Cache Size (KB)
WS – L2 Bus Traffic (Trans/Proc)


L1 Cache Size vs. Execution Cycles
Execution Cycles (cycles)
28650000
28600000
28550000
28500000
28450000
28400000
28350000
10
20
30
40
50
60
70
L1 Cache Size (KB)
FFT - Execution Cycles


L1 Cache Size vs. Execution Cycles
Execution Cycles (cycles)
226000000
225000000
224000000
223000000
222000000
221000000
220000000
219000000
218000000
217000000
10
20
30
40
50
60
70
L1 Cache Size (KB)
WS – Execution Cycles