



Drexel University
Electrical and Computer Engineering Department

ECEC 471
Introduction to VLSI Design

Lab Assignment 7
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The diagram illustrates a digital logic circuit. At its core is a 74VHC04 hex inverter, which provides inverted versions of its inputs. These inverted signals are used as clock inputs for two 74VHC15 monostable multivibrators. One 74VHC15 is configured with a timing network consisting of a resistor and a capacitor, and its output is connected to a comparator. The other 74VHC15 is similarly configured but its output is connected to a different part of the circuit. The circuit also includes a 74VHC15 configured as a buffer or delay element. Various logic gates, including AND and OR gates, are used to combine signals from the inverters, monostables, and buffers to produce the final outputs 'q' and 'zbar'. The circuit is powered by a 5V supply and has ground connections.

Fig. 1. Schematic view of DFF.

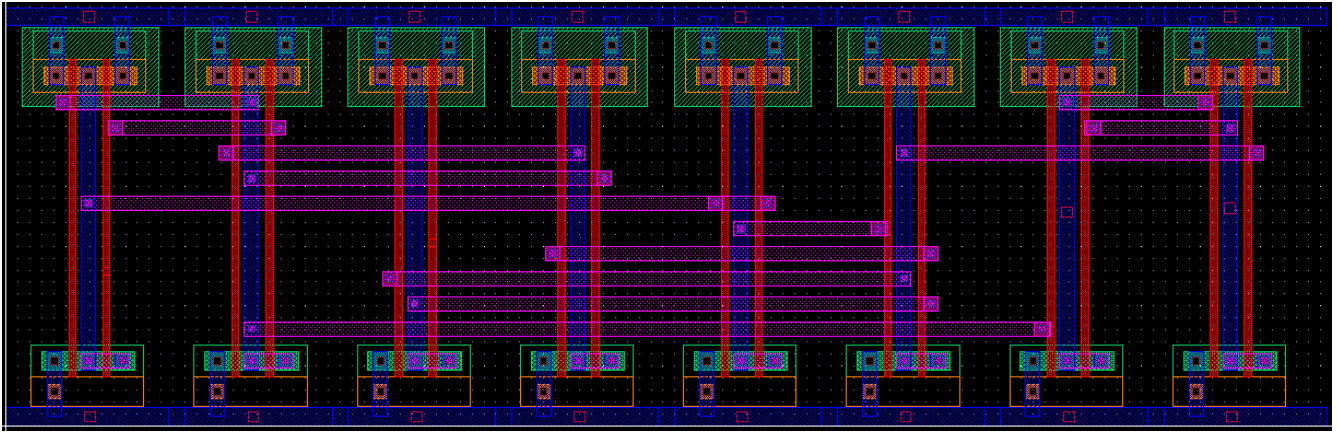


Fig. 2. Layout view of DFF.

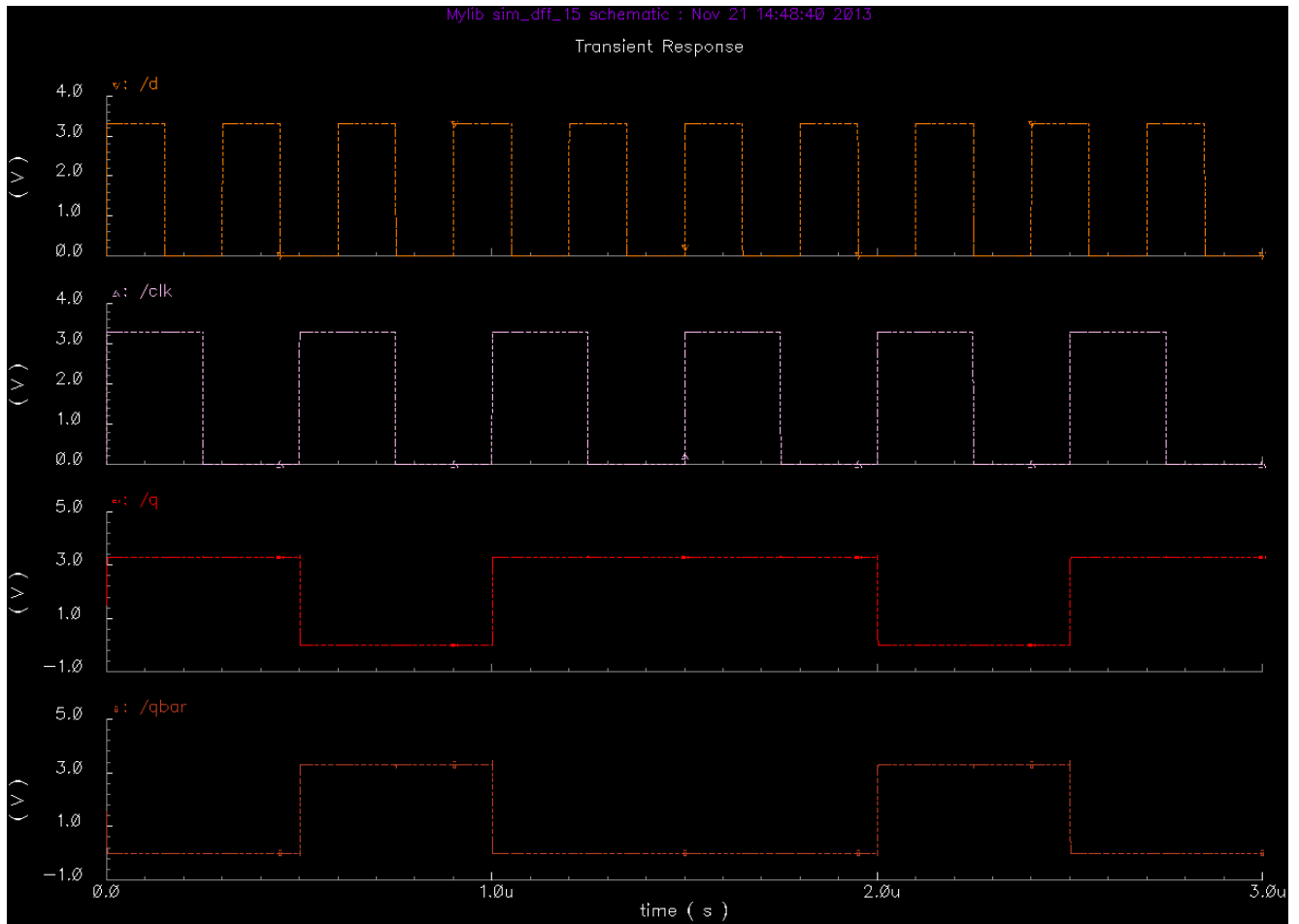


Fig. 3. Simulation results verifying the functionality of the flip-flop schematic view.

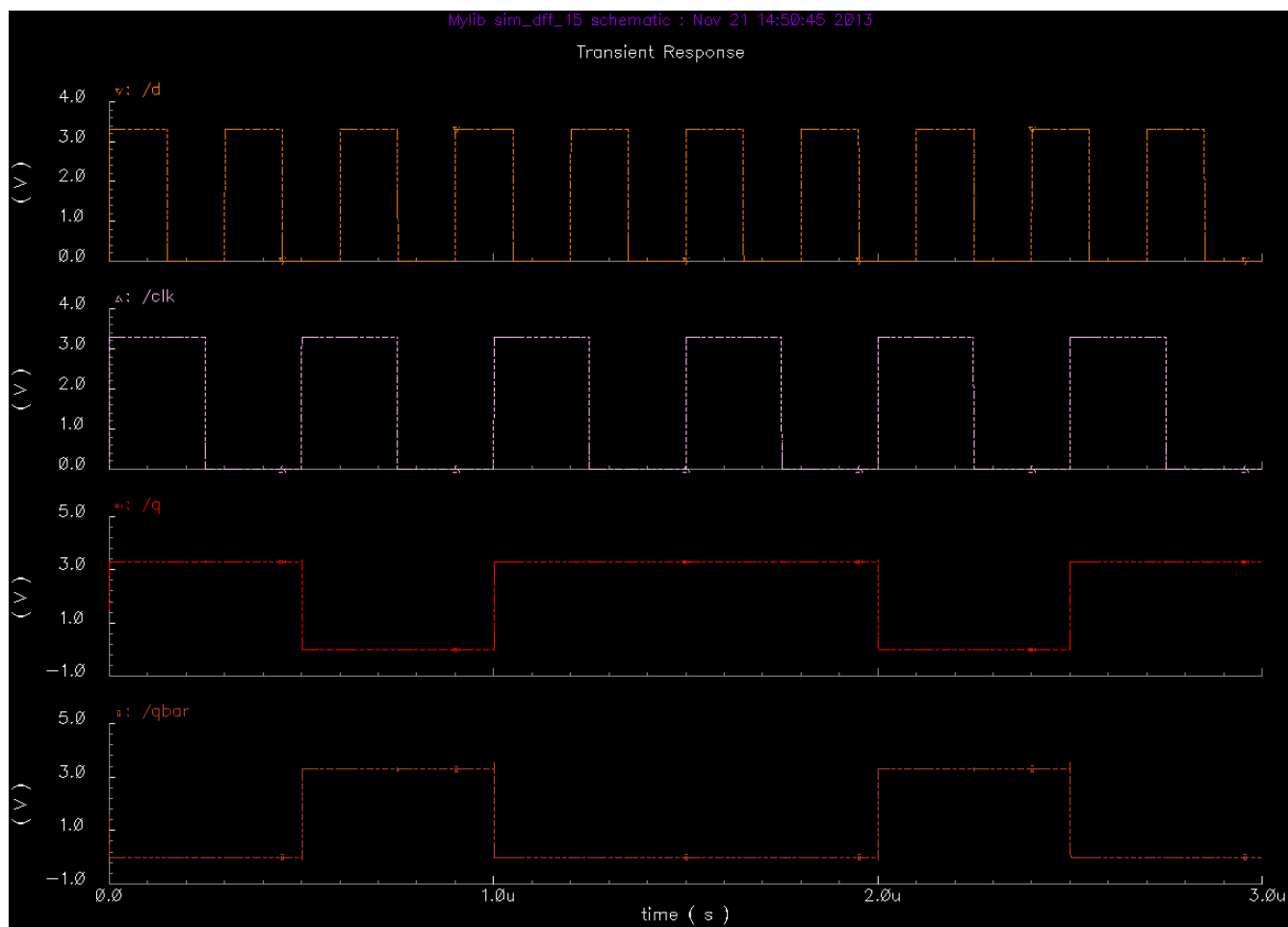


Fig. 4. Simulation results verifying the functionality of the flip-flop layout view.

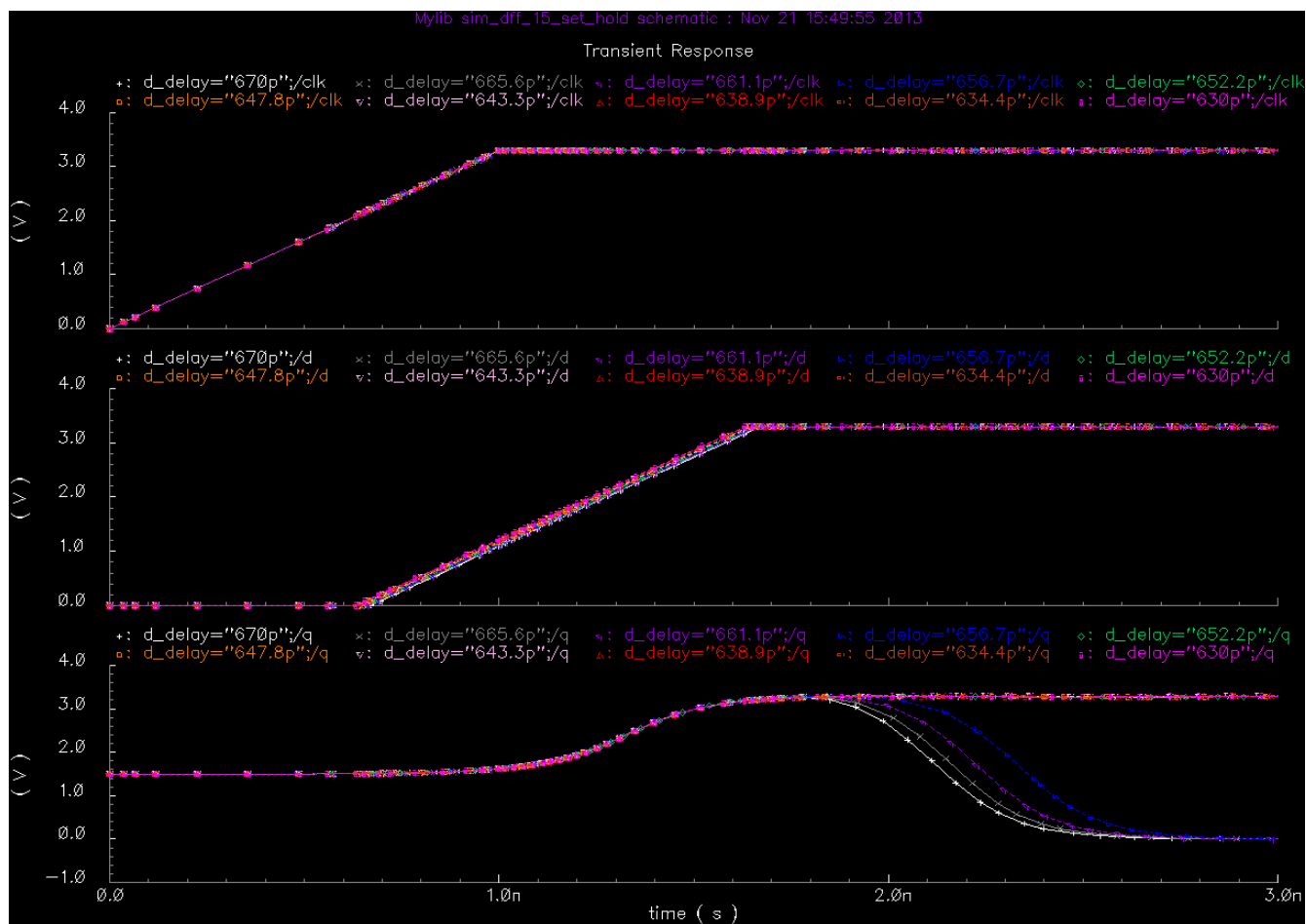


Fig. 5. Setup time simulation results for schematic view.

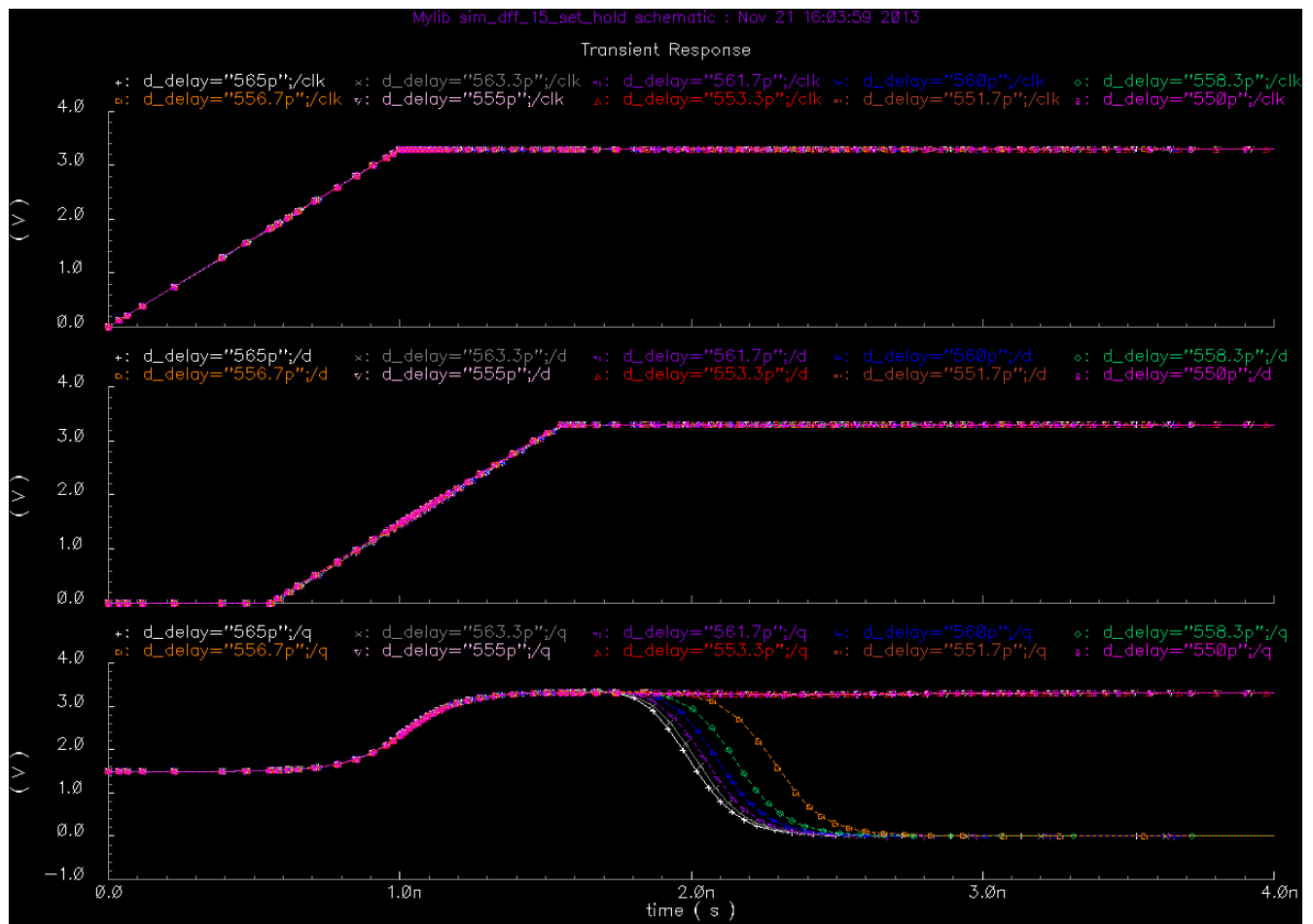


Fig. 6. Setup time simulation results for layout view.

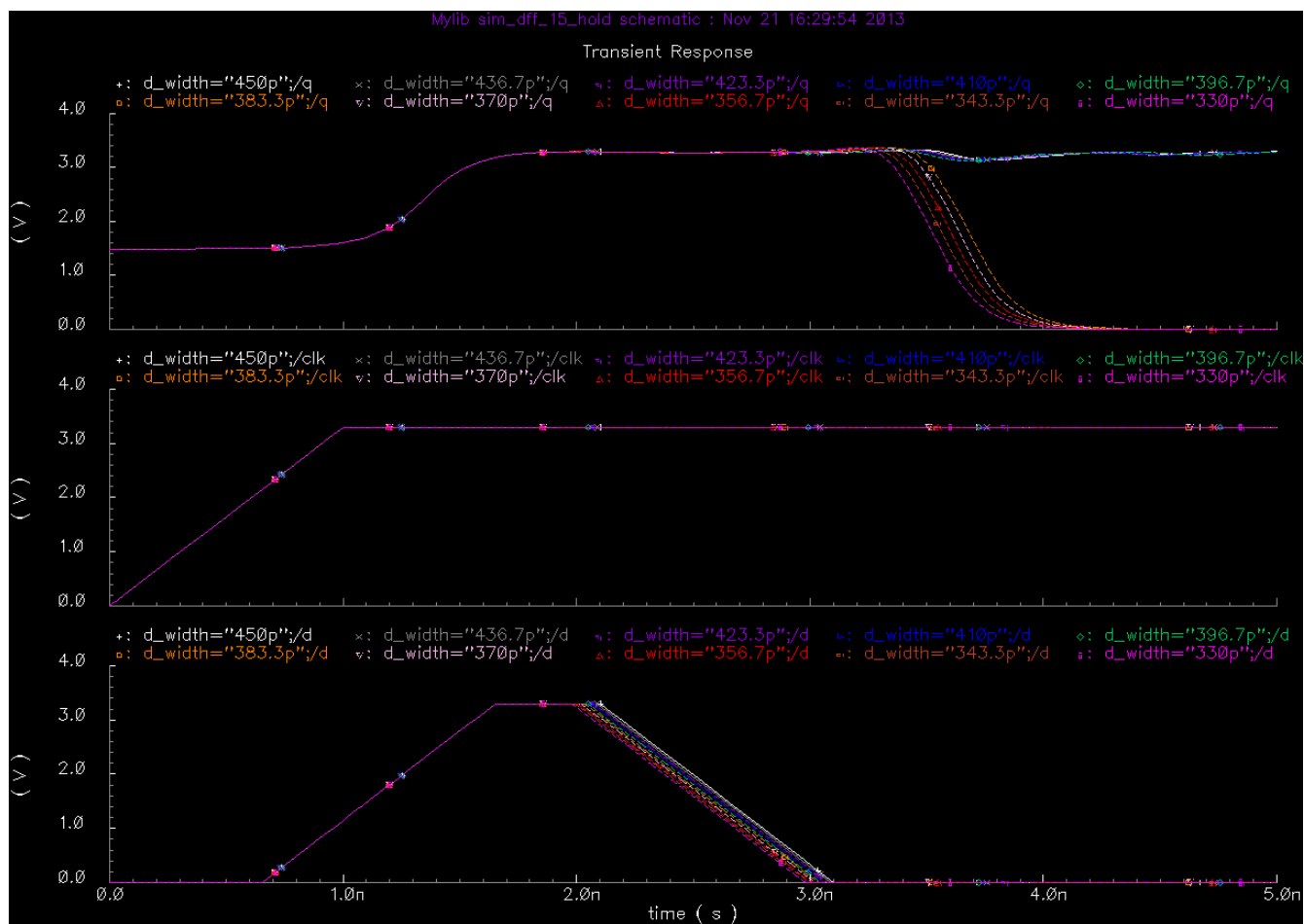


Fig. 7. Hold time simulation results for schematic view.

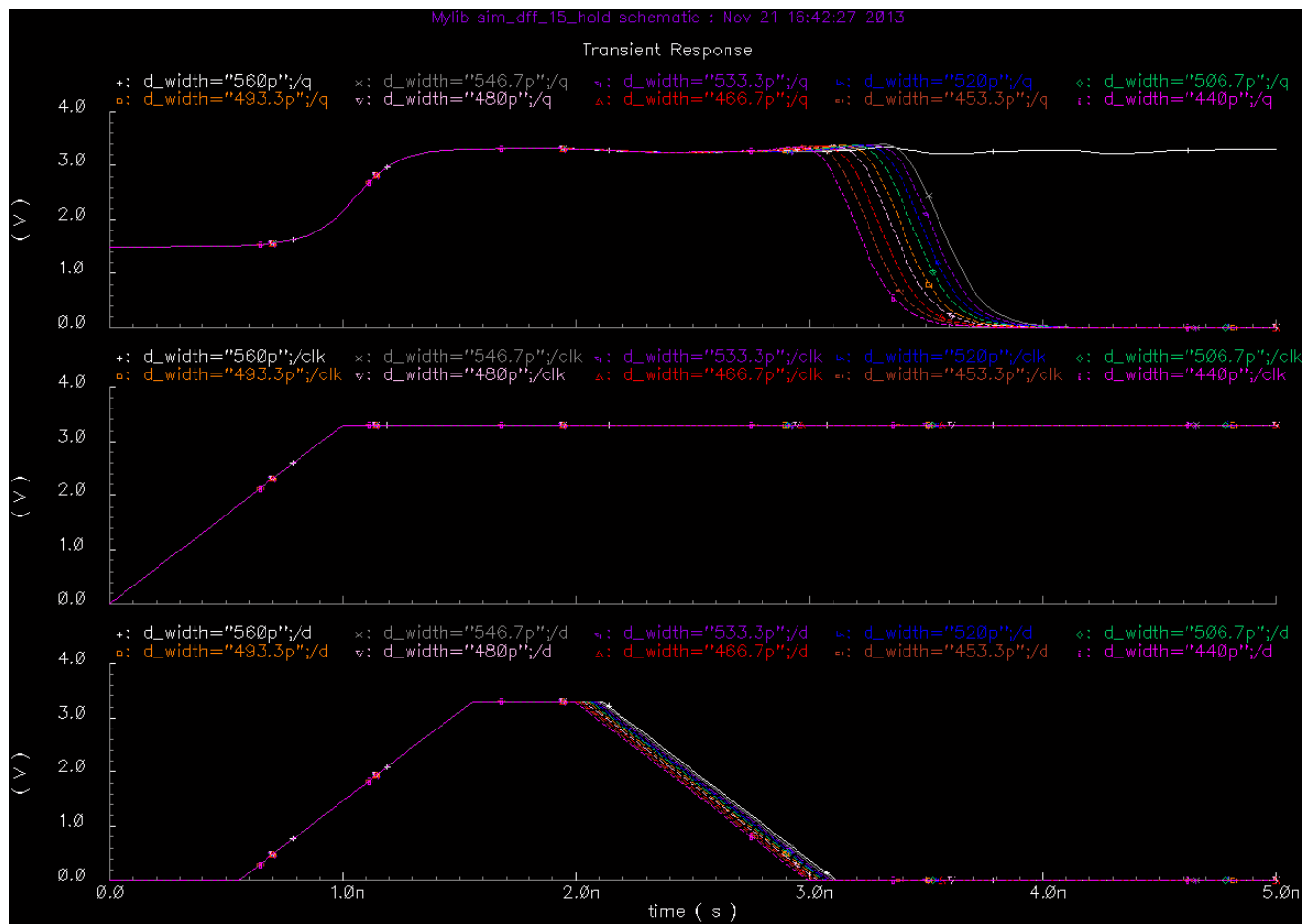


Fig. 8. Hold time simulation results for layout view.

Table 1. Summary of timing information of DFF.

	Setup Time (ps)			Hold Time (ps)			Clocking in '0'		Clocking in '1'	
	Low Bound	High Bound	Average	Low Bound	High Bound	Average	Propagation Delay (ns)	Transition Time (ps)	Propagation Delay (ns)	Transition Time (ps)
Schematic	652.2	656.7	654.45	383.3	396.7	390	1.46	391.76	0.81	542.49
Layout	555	556.7	555.85	546.7	560	553.35	1.25	330.35	0.71	449.06