Drexel University
Electrical and Computer Engineering Department

ECEC 471
Introduction to VLSI Design

Lab Assignment 5
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Lab 5 completes schematic and layout based simulations to characterize both NAND and AND gate functionality. The NAND and AND gates have their PMOS transistors sized in an attempt to be as symmetrical as possible.

(This report is done in roughly the same order as the deliverable bullet points with in the Lab 5 PDF.)

Before-Sizing

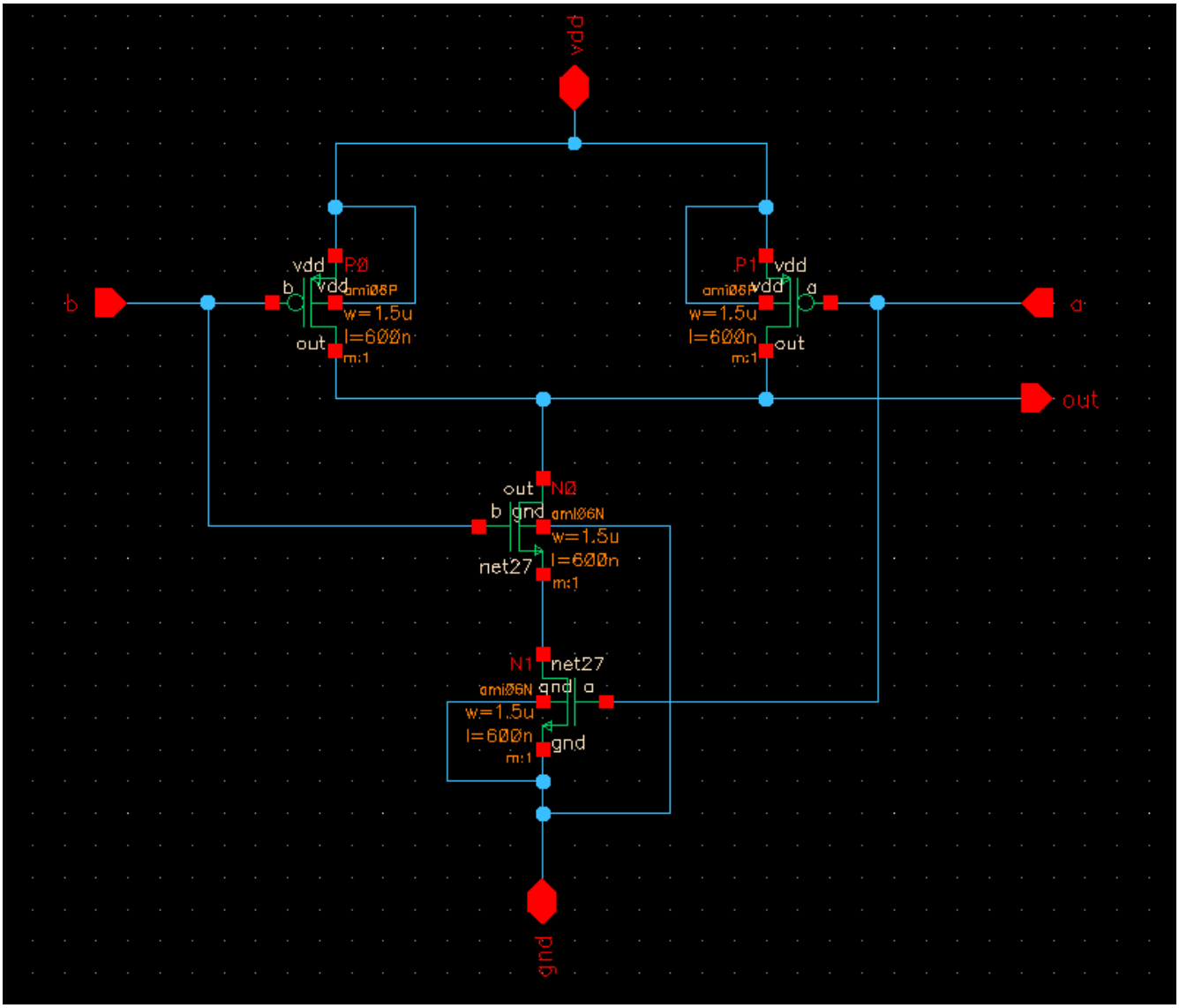

Figure 1. Schematic view of the NAND gate (transistors show after sizing values).

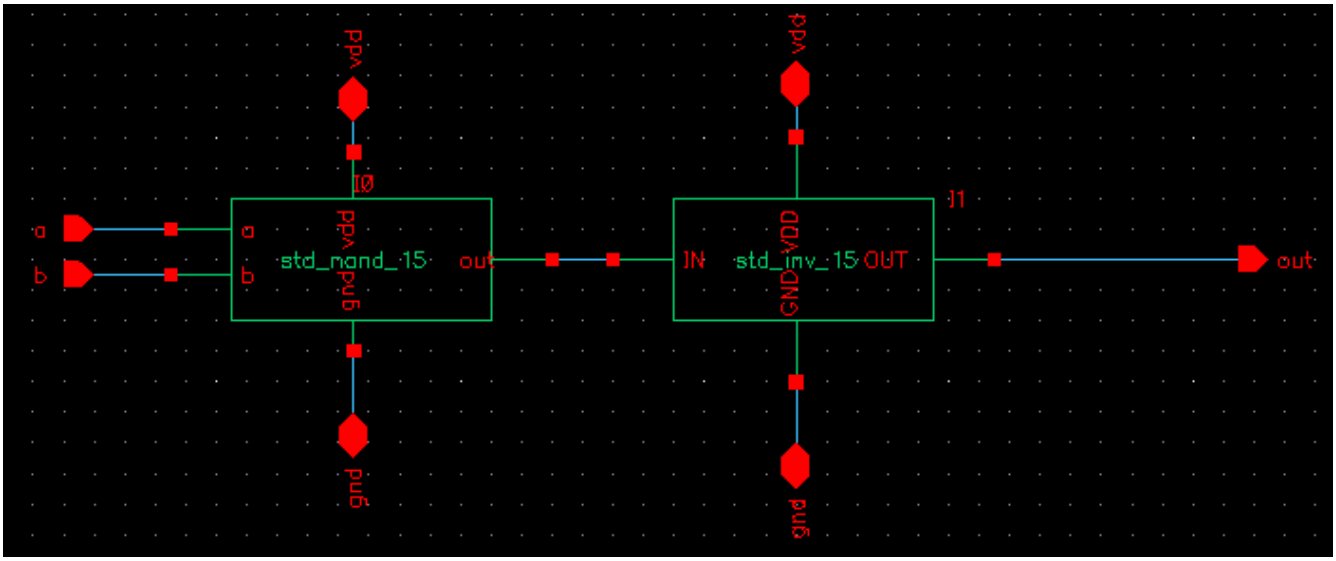

Figure 2. Schematic view of the AND gate.

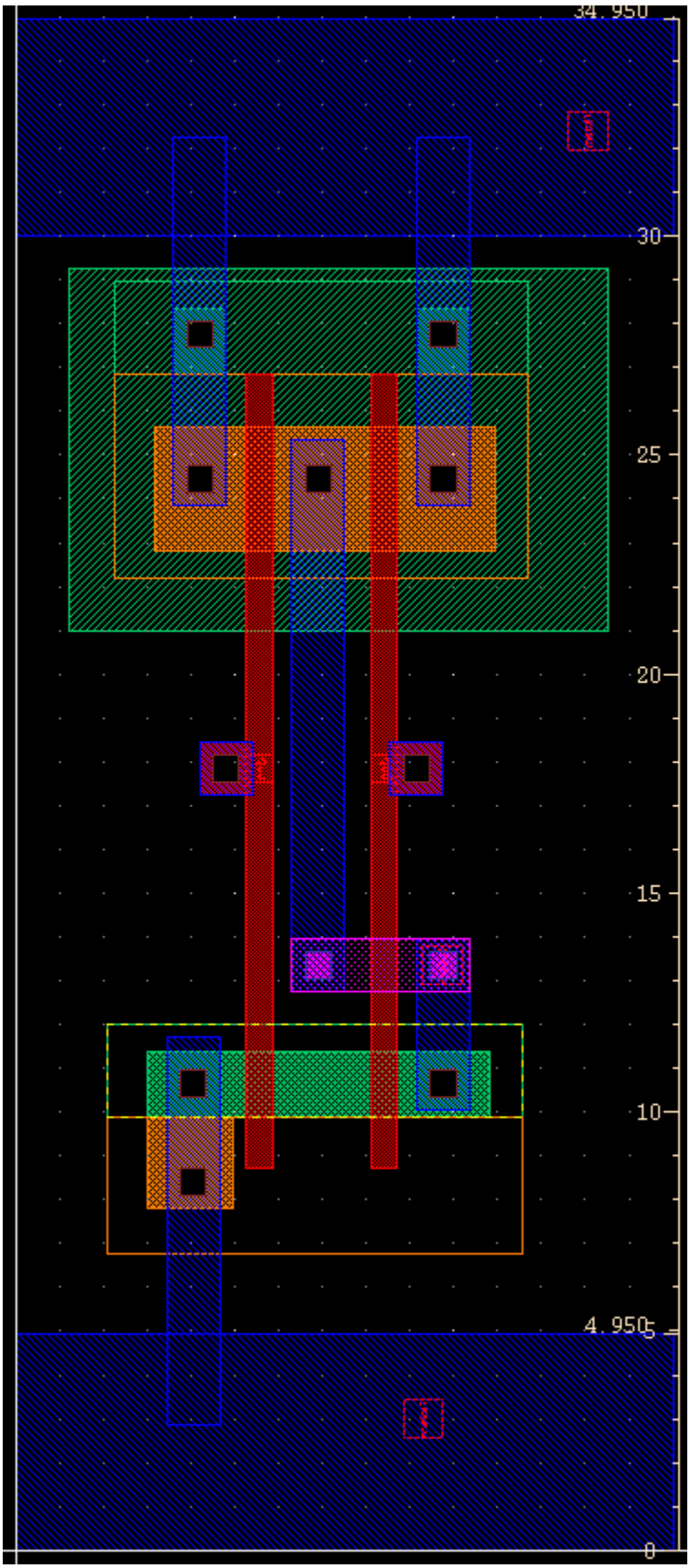

Figure 3. Layout view of the NAND gate (before sizing).

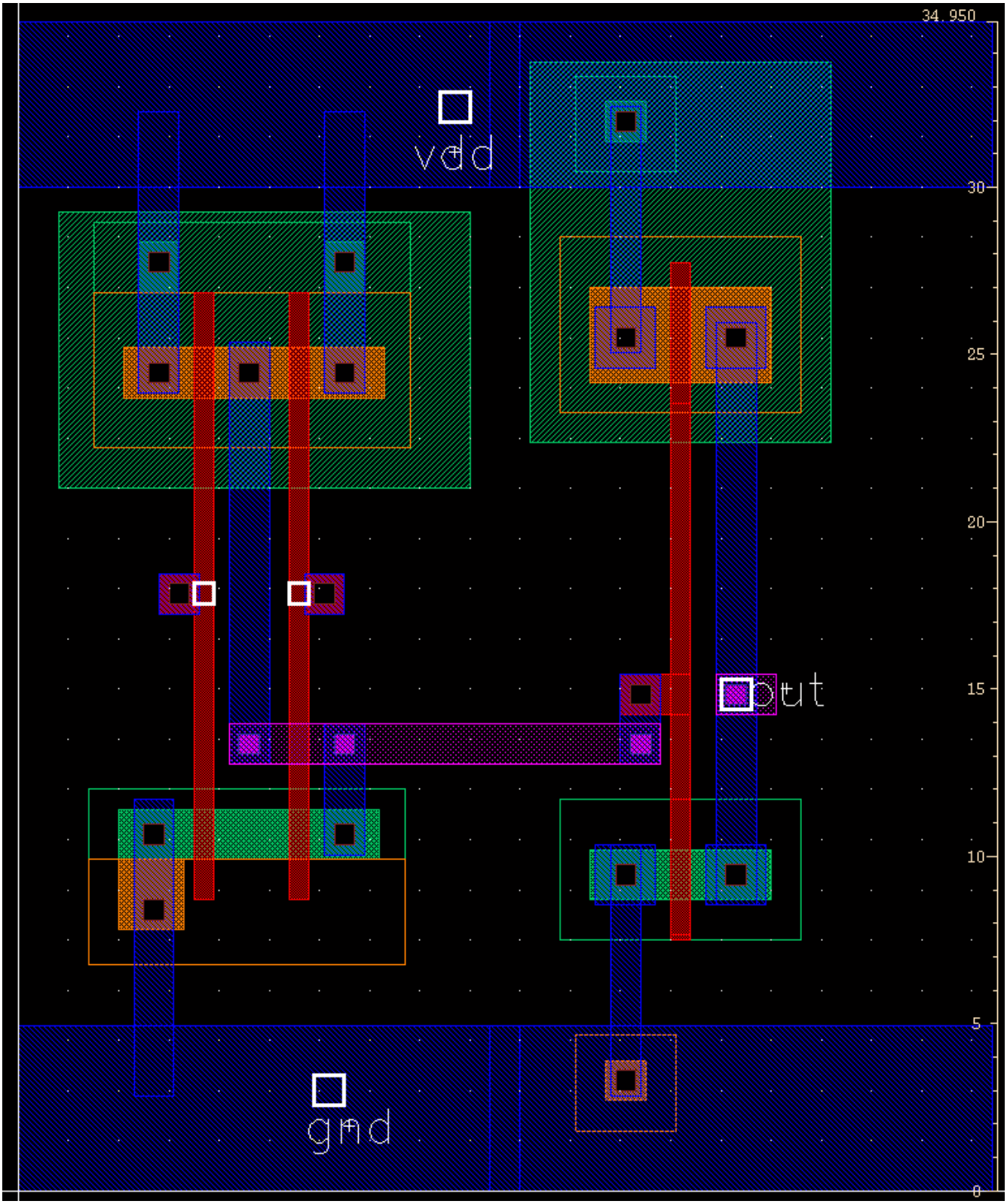

Figure 4. Layout view of the AND gate (before sizing).

```
DRC started.......Thu Oct 31 12:05:06 2013
    completed ....Thu Oct 31 12:05:06 2013
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "std_nand_15 layout"   *********
   Total errors found: 0
```

Figure 5. DRC results for NAND gate (before sizing).

```
DRC started.......Thu Oct 31 16:56:35 2013
    completed ....Thu Oct 31 16:56:36 2013
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "std_and_15 layout"   *********
   Total errors found: 0
```

Figure 6. DRC results for AND gate (before sizing).

```
LVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/DREXEL/jvk27/ECEC471/LVS
```

Figure 7. LVS results for NAND gate (before sizing).

```
LVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/DREXEL/jvk27/ECEC471/LZVS
```

Figure 8. LVS results for AND gate (before sizing).

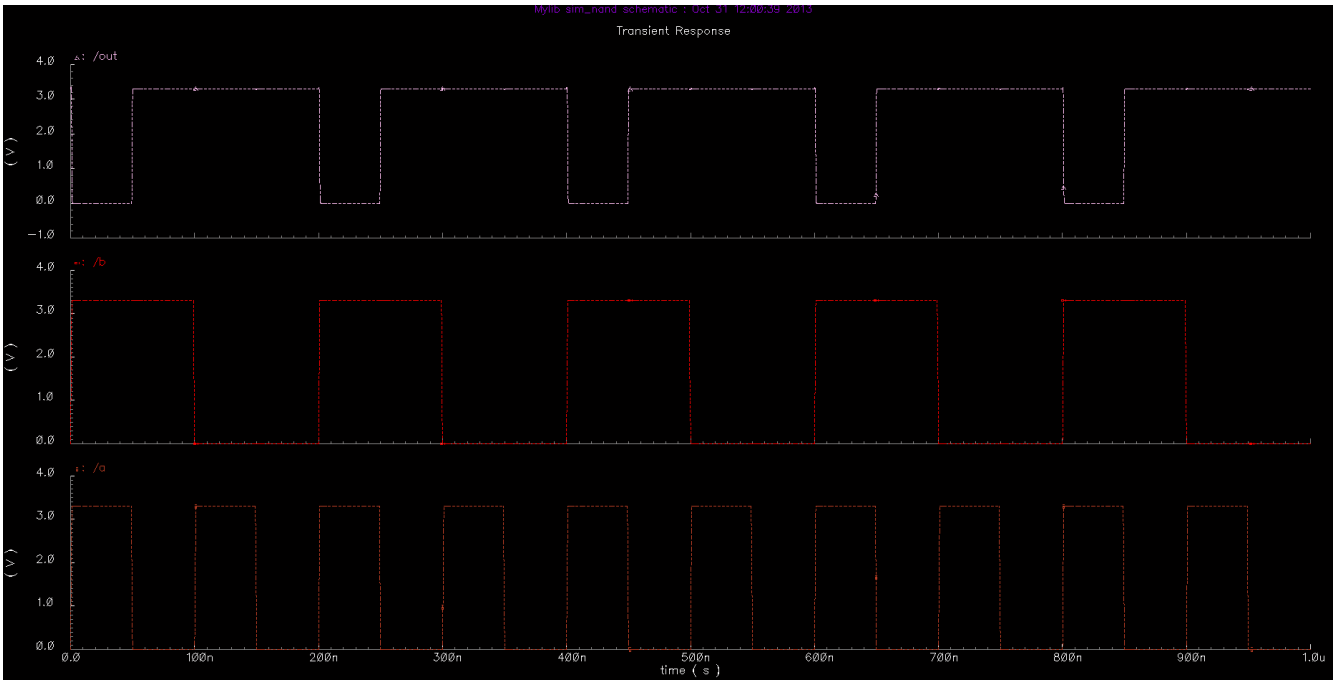

Figure 9. Transient simulation for NAND gate schematic only (before sizing).

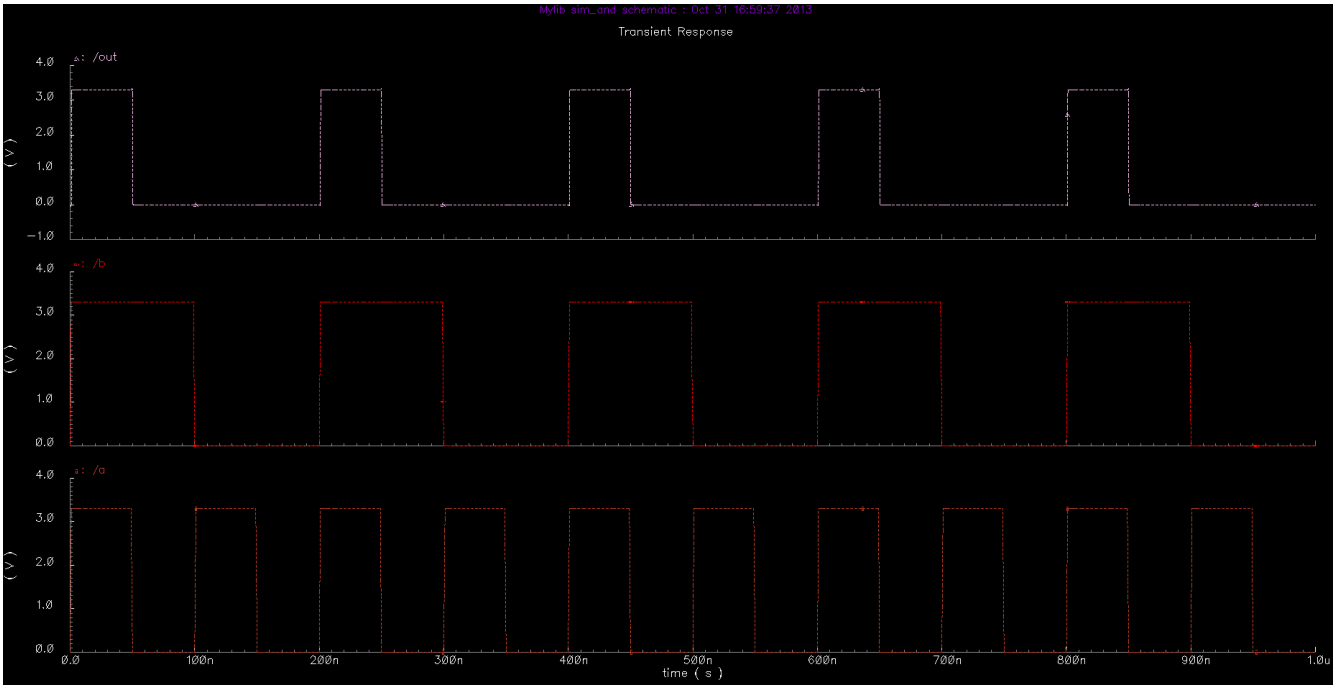

Figure 10. Transient simulation for AND gate schematic only (before sizing).

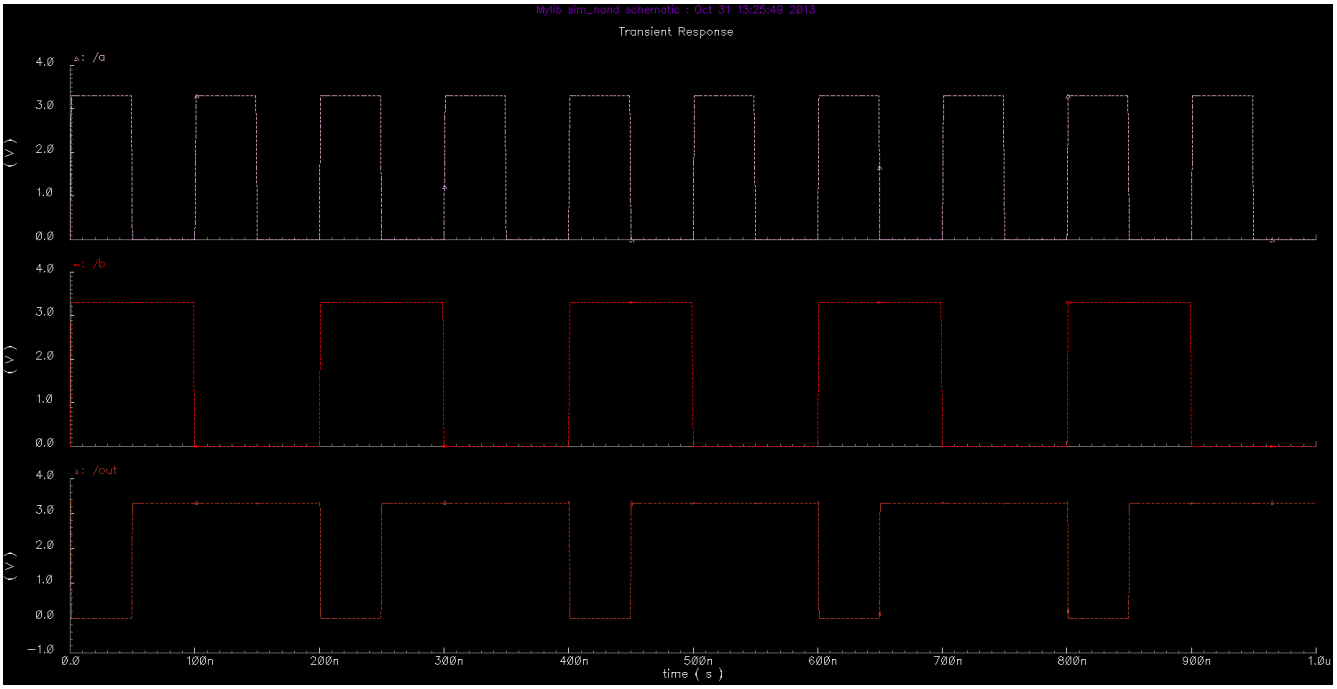

Figure 11. Transient simulation for NAND gate using layout/extraction (after sizing).
(Note: No layout based simulation for NAND gate was collected before sizing, this figure will be referenced later during the sizing section.)

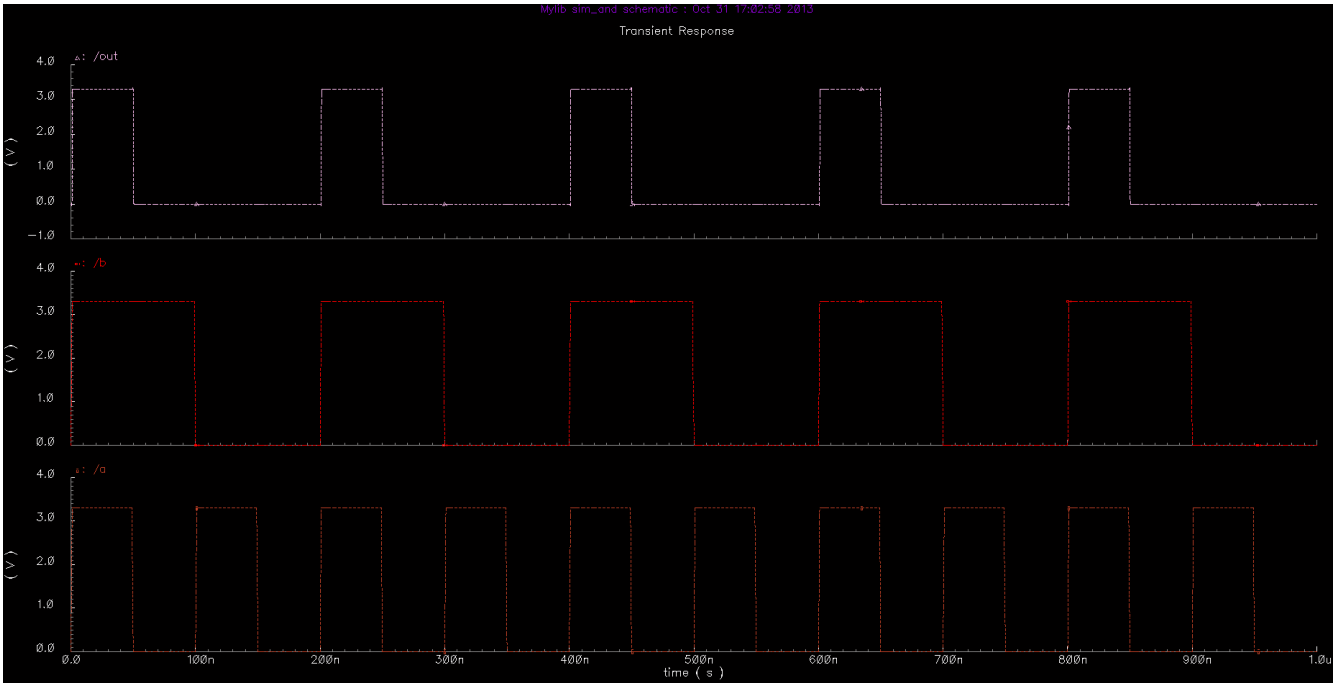

Figure 12. Transient simulation for AND gate using layout/extraction (before sizing).

Sizing

Timing measurements were made after the symmetric sizing changes. The sizing information will be shown before the timing information.

A parametric sweep of PMOS widths from 1.5um to 3.0um was completed for both the NAND and AND gate. In both cases, all PMOS transistors are sized to the same sweep value – that is, during the AND testing, both NAND and INV PMOS transistors were sized simultaneously.

The analysis for this parametric sweep was a DC sweep from 0V to 3.3V. Since both the NAND and AND gate have two inputs and threshold analysis requires a a Vin vs. Vout curve, the two inputs were tied together as seen below.

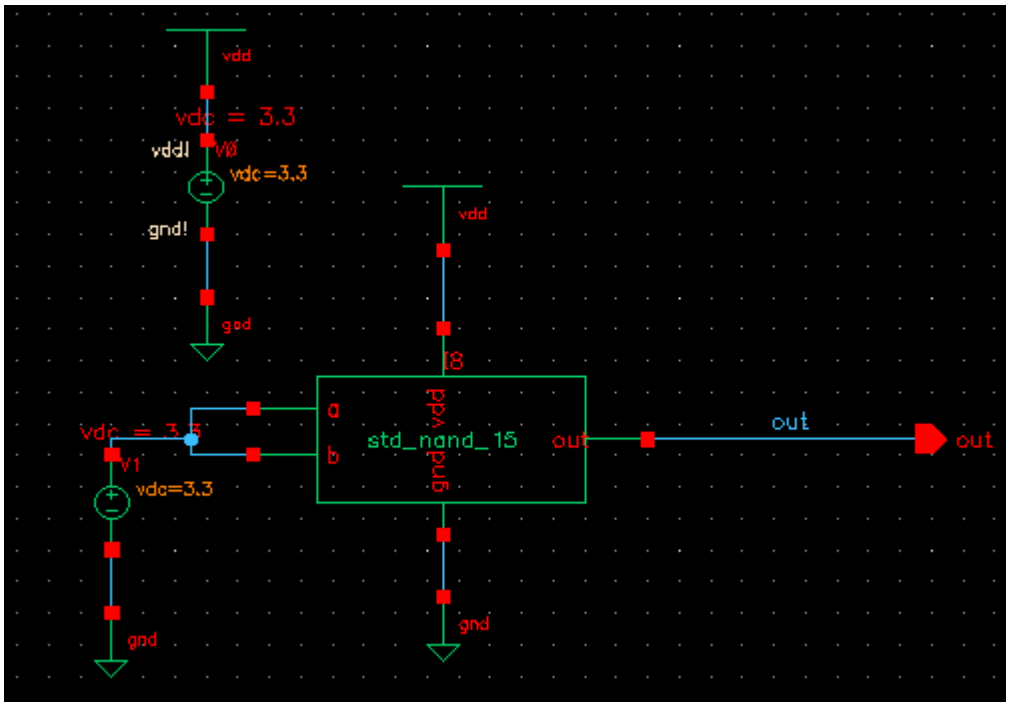

Figure 13. Schematic used for determining the symmetric sizing of the NAND gate.

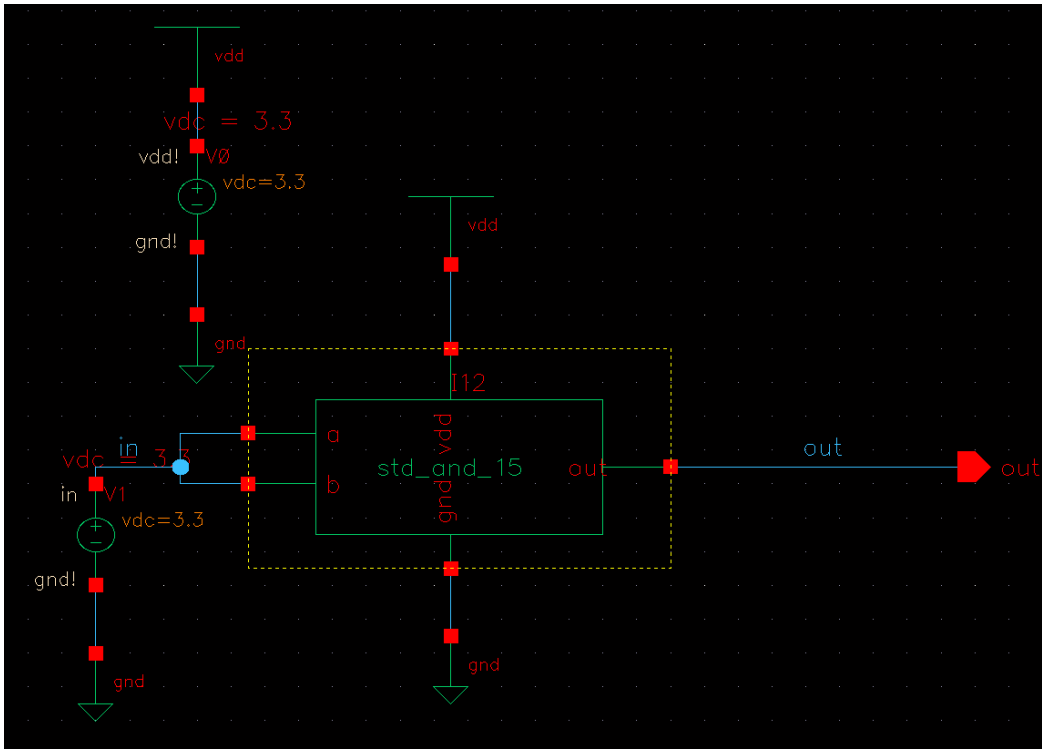

Figure 14. Schematic used for determining the symmetric sizing of the AND gate.

The results from the sizing experiment show that *no PMOS sizing* between 1.5um and 3.0um provides perfectly symmetrical operation for either the NAND or AND gates. However, the closest-to-symmetric value for the **PMOS sizing is 1.5um in both cases**.

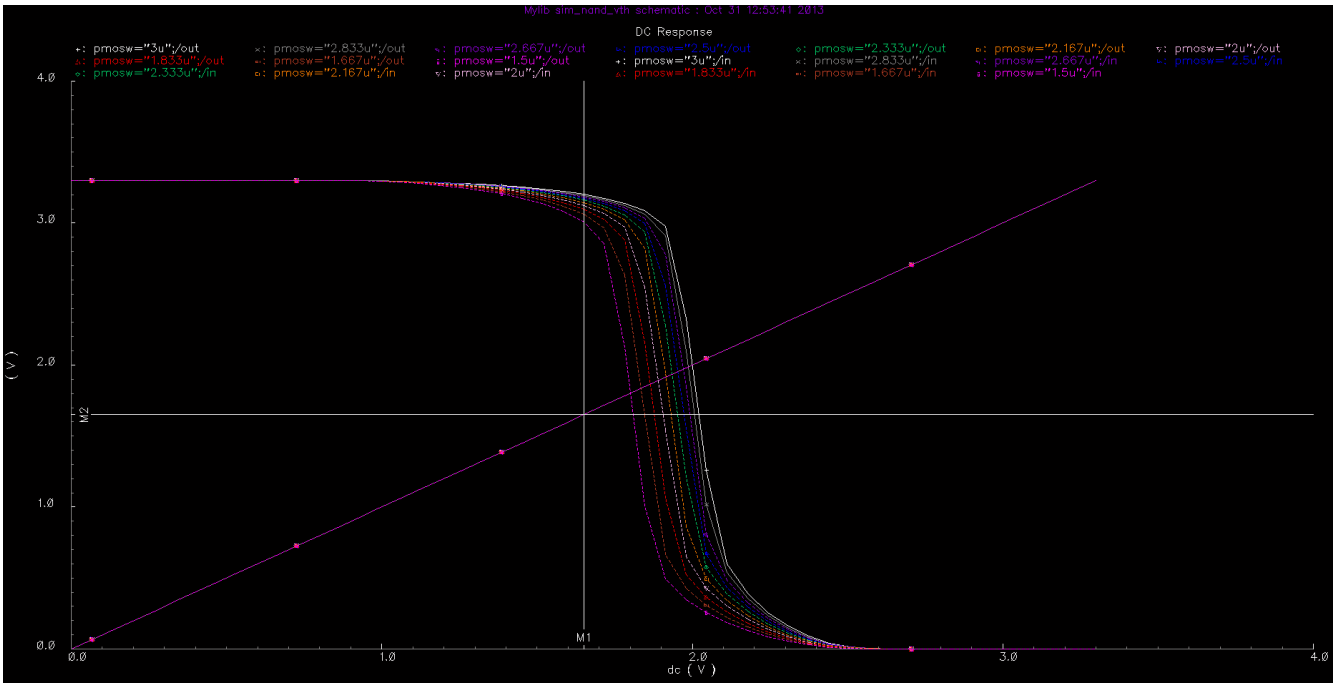

Figure 15. Results from PMOS sizing parametric analysis for NAND gate.

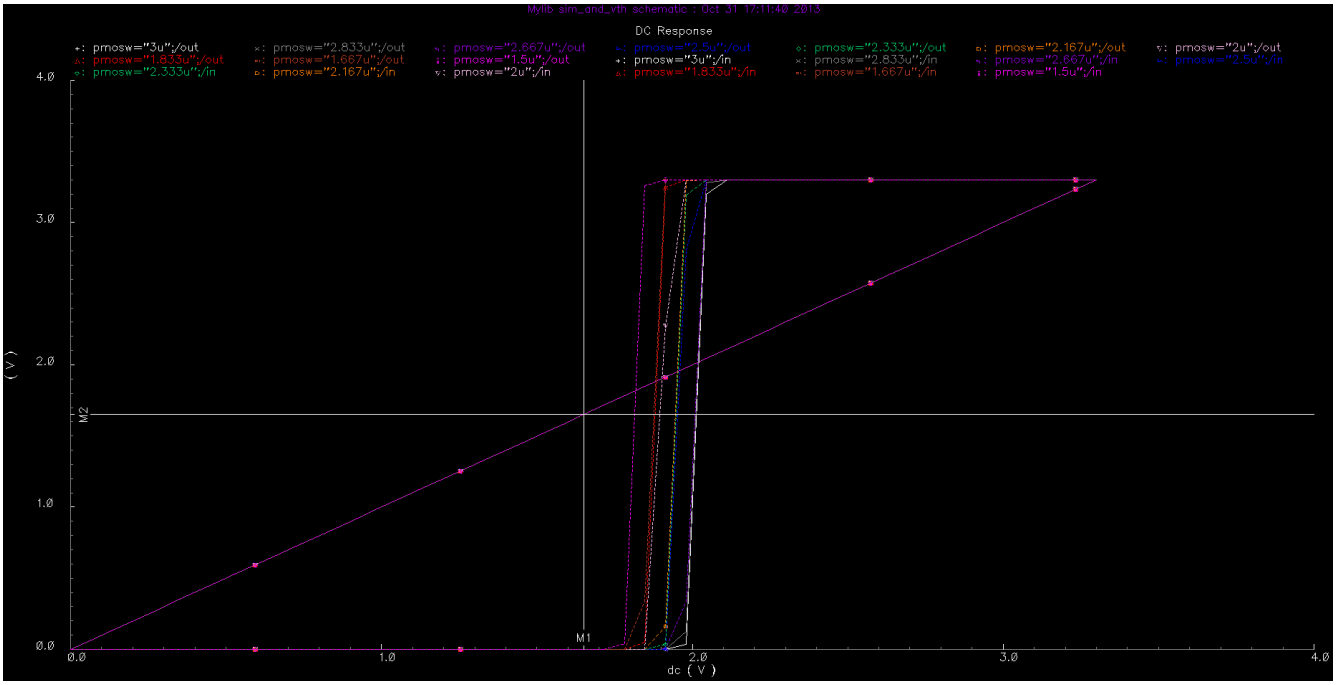

Figure 16. Results from PMOS sizing parametric analysis for AND gate.

Fig. 1 shows the schematic of the NAND gate with sized transistor values. The schematic for the AND gate does not show transistor sizes so it is not shown as 'sized' here.

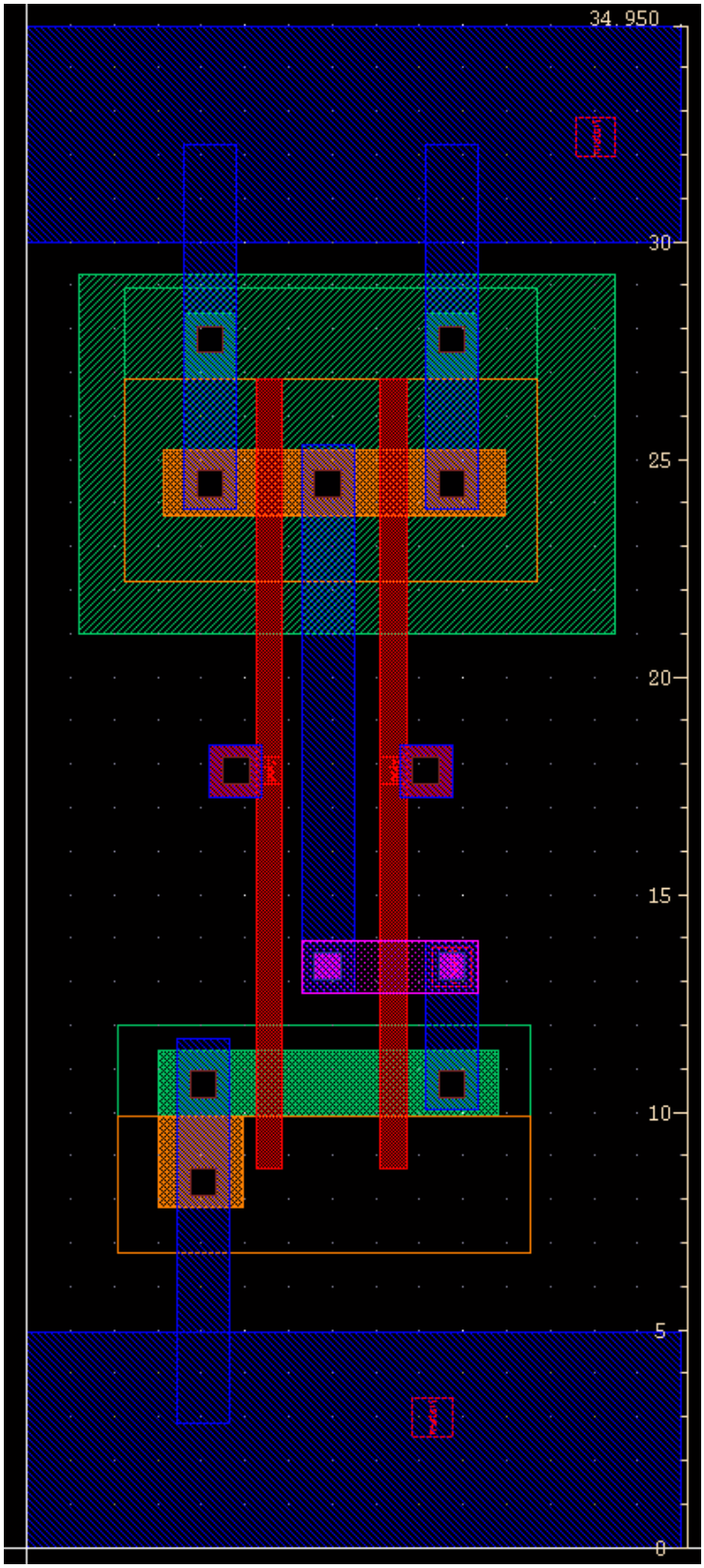

Figure 17. Layout view of the NAND gate (after sizing).

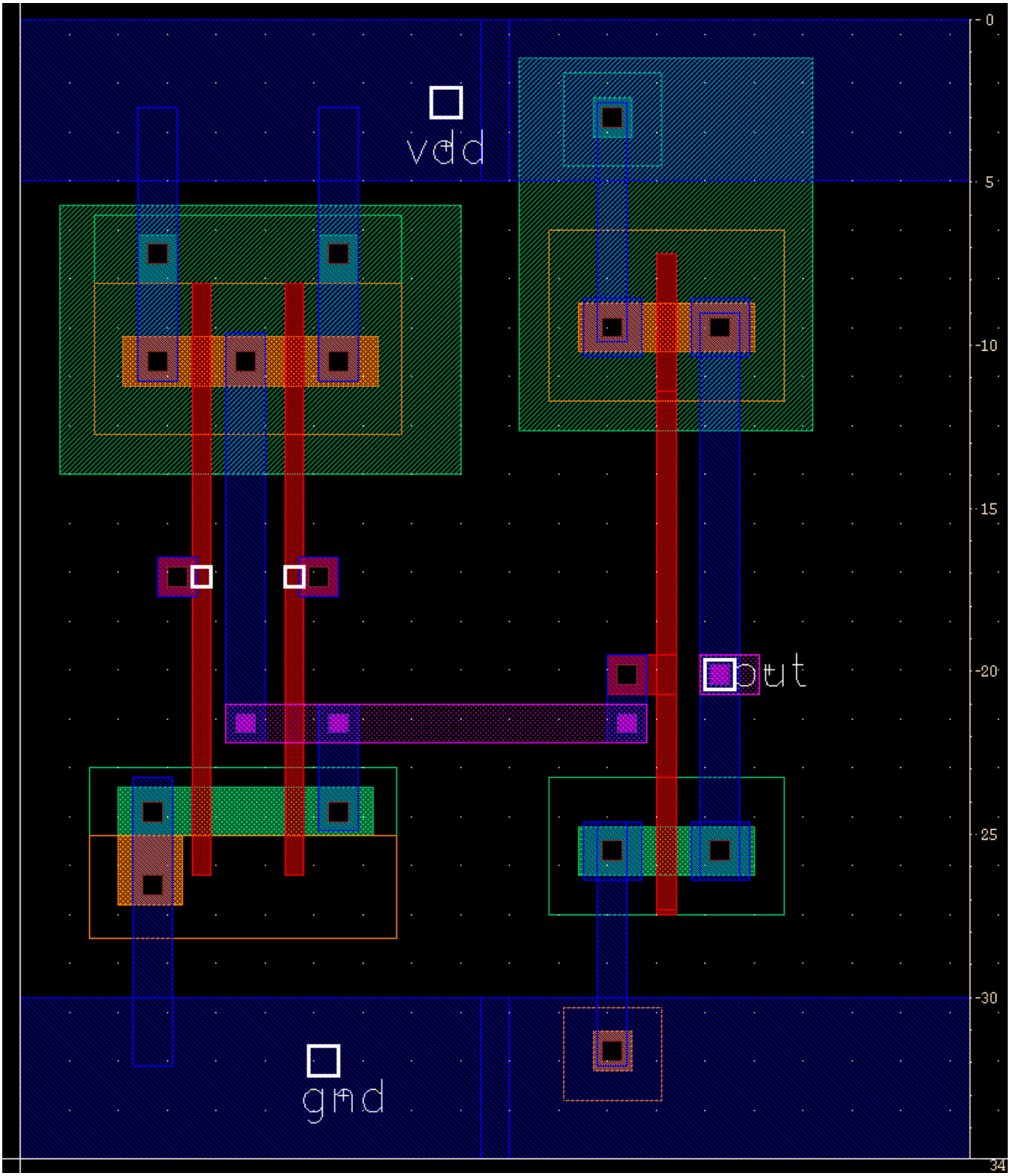

Figure 18. Layout view of the AND gate (after sizing).

```
DRC started.......Thu Oct 31 13:15:40 2013
    completed ....Thu Oct 31 13:15:41 2013
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "std_nand_15 layout"   *********
   Total errors found: 0
```

Figure 19. DRC results for NAND gate (after sizing).

```
DRC started.......Thu Oct 31 17:22:20 2013
    completed ....Thu Oct 31 17:22:20 2013
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "std_and_15 layout"   *********
   Total errors found: 0
```

Figure 20. DRC results for AND gate (after sizing).

```
   Total errors found: 0
LVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/DREXEL/jvk27/ECEC471/LVS
```

Figure 21. LVS results for NAND gate (after sizing).

```
LVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/DREXEL/jvk27/ECEC471/LVS
```

Figure 22. LVS results for AND gate (after sizing).

After-Sizing Timing

Now that the transistors have been sized as to provide as close to symmetric operation as possible, simulations using the sized layout and extracted capacitances are shown below. From this, information on timing parameters such as rise/fall time and propagation delay can be collected.

Fig. 11 shows the transient simulation for NAND gate using layout/extraction (after sizing).

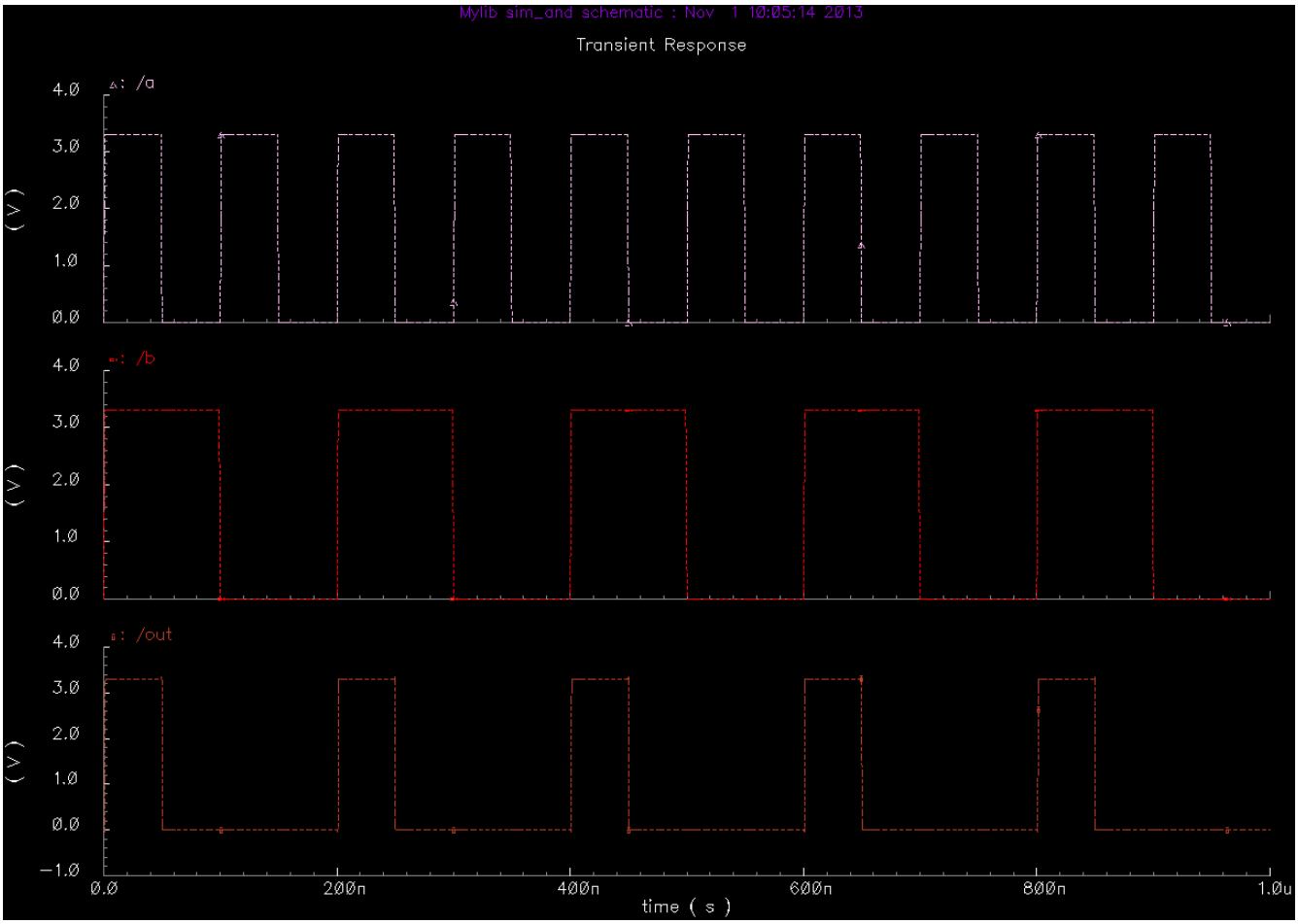

Figure 23. Transient simulation for AND gate using layout/extraction (after sizing).

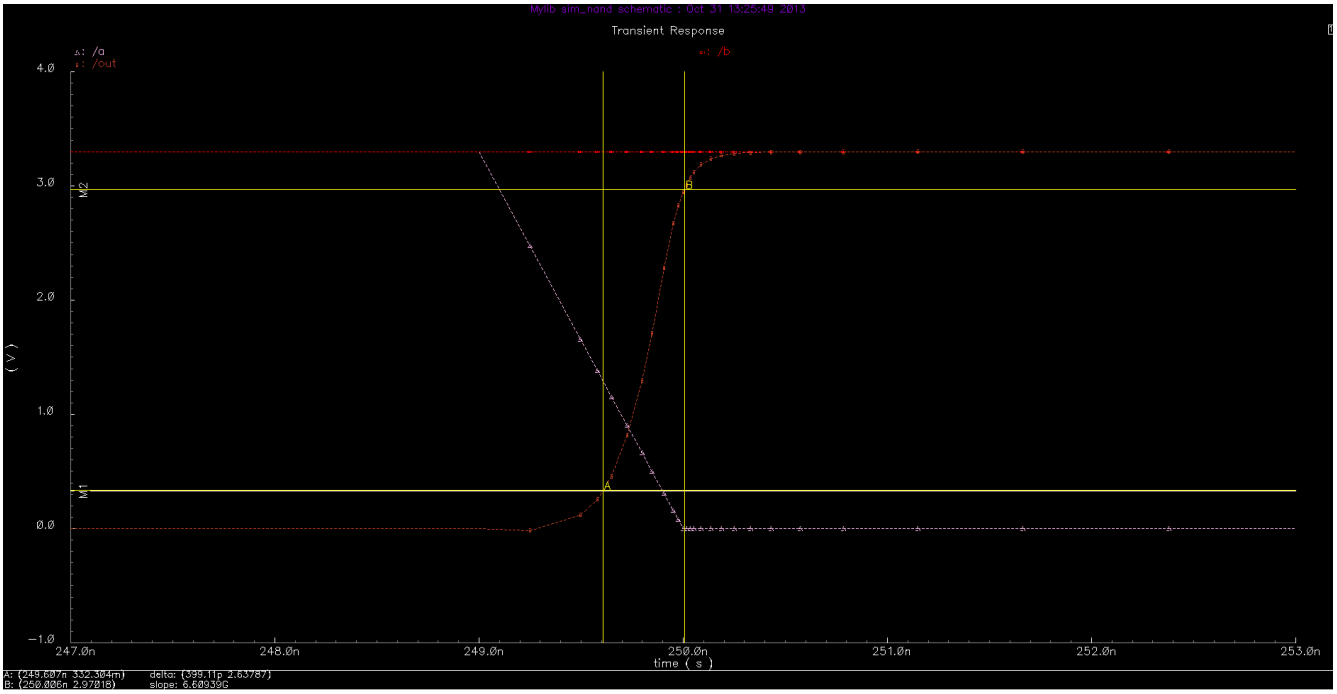

Figure 24. NAND gate output signal rise time measurement (after sizing).

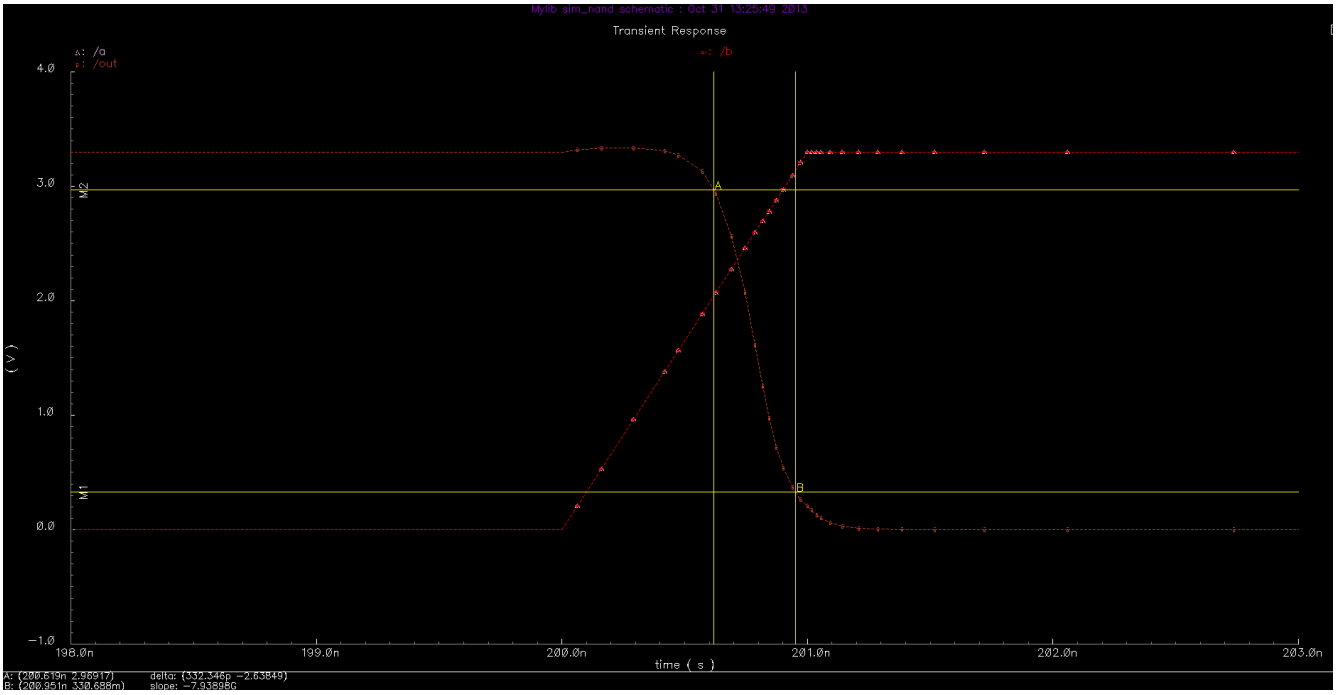

Figure 25. NAND gate output signal fall time measurement (after sizing).

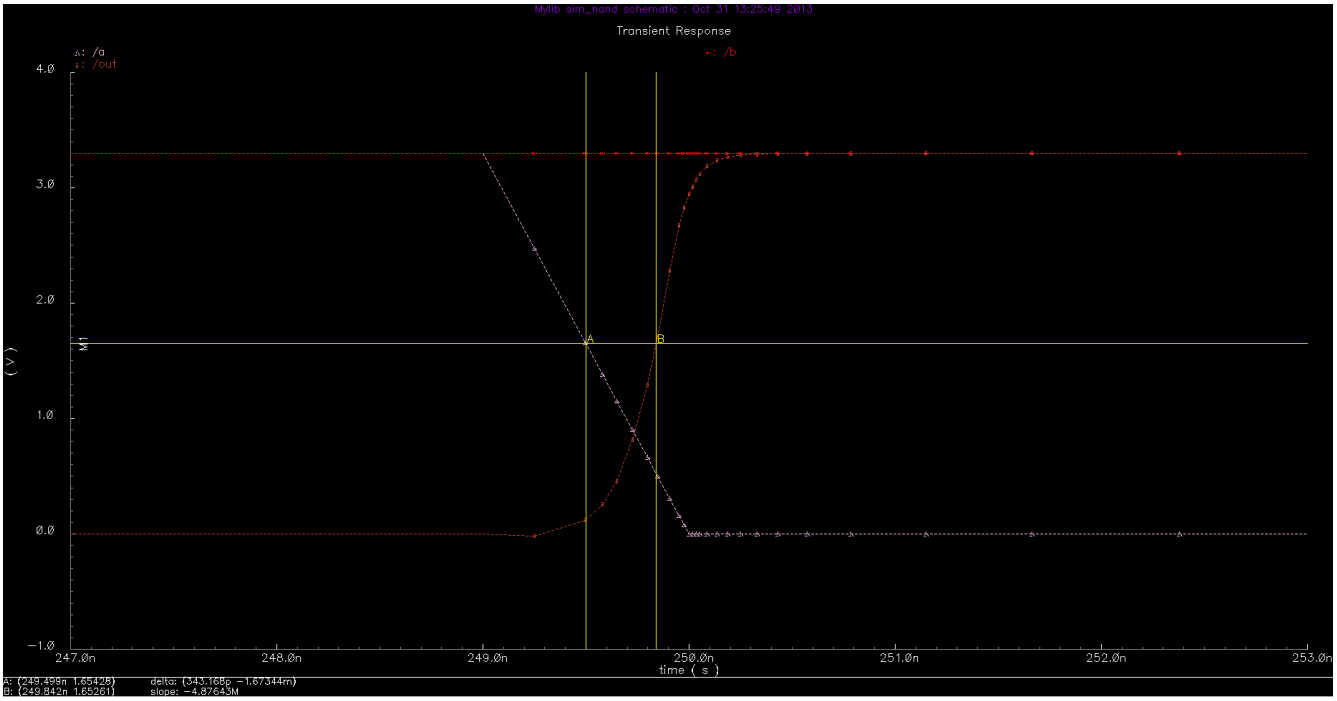

Figure 26. NAND gate output signal rising propagation delay measurement (after sizing).

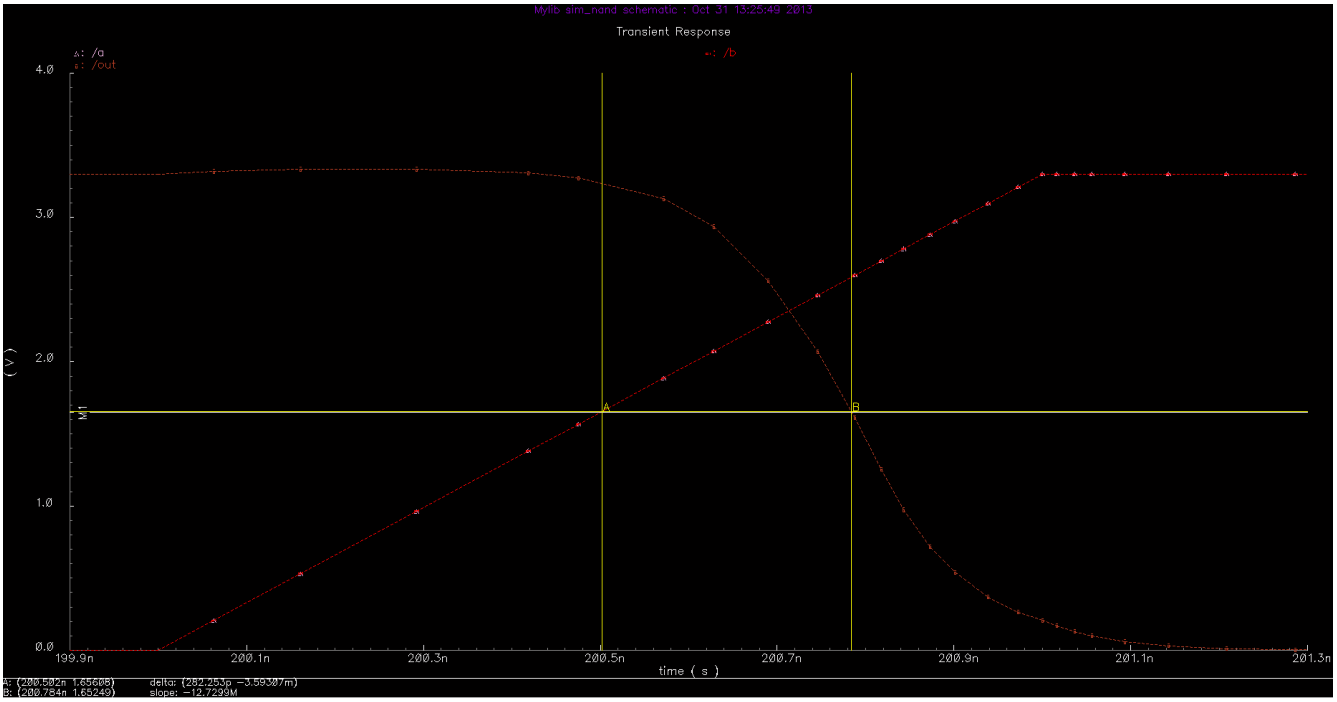

Figure 27. NAND gate output signal falling propagation delay measurement (after sizing).

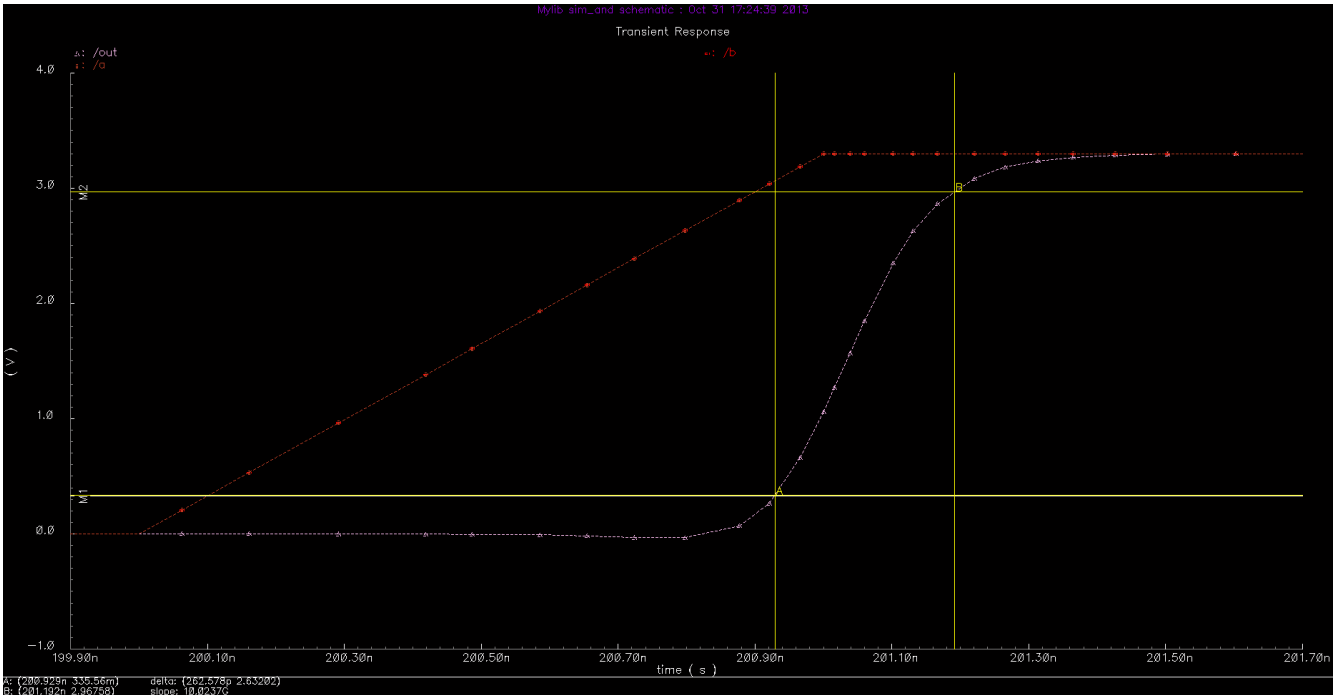

Figure 28. AND gate output signal rise time measurement (after sizing).

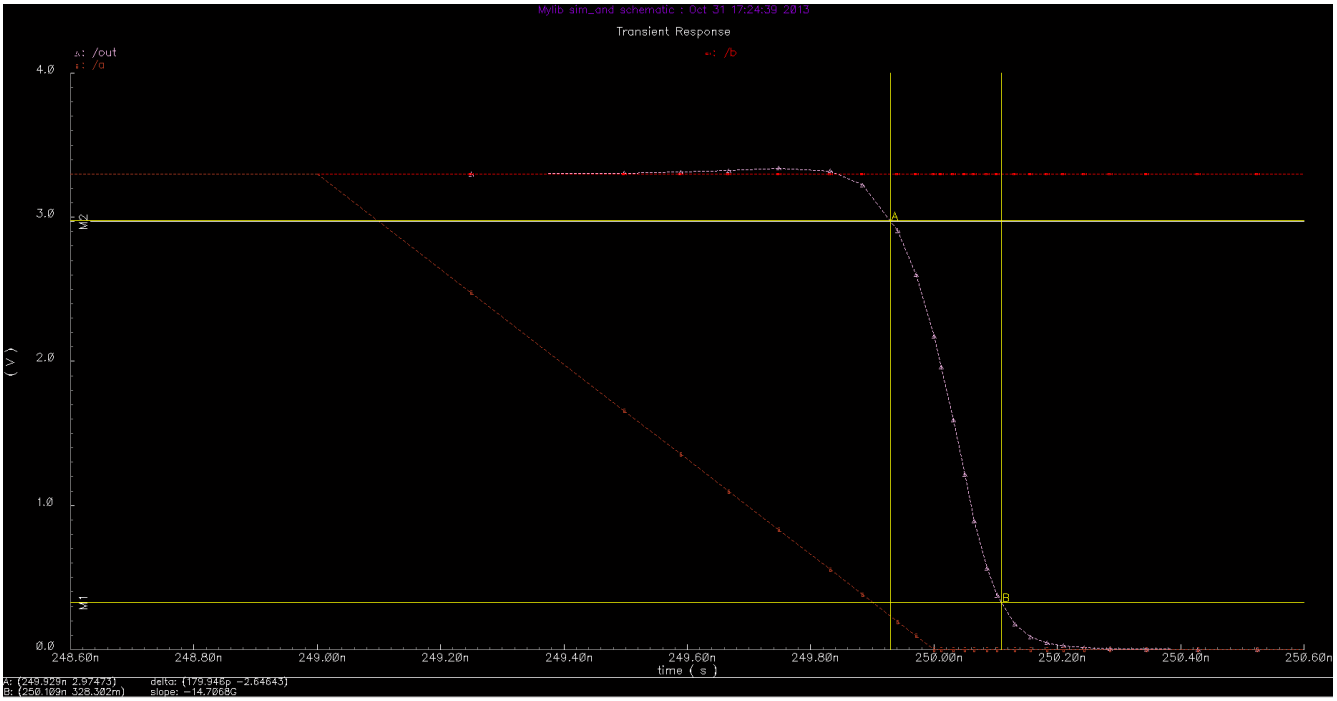

Figure 29. AND gate output signal fall time measurement (after sizing).

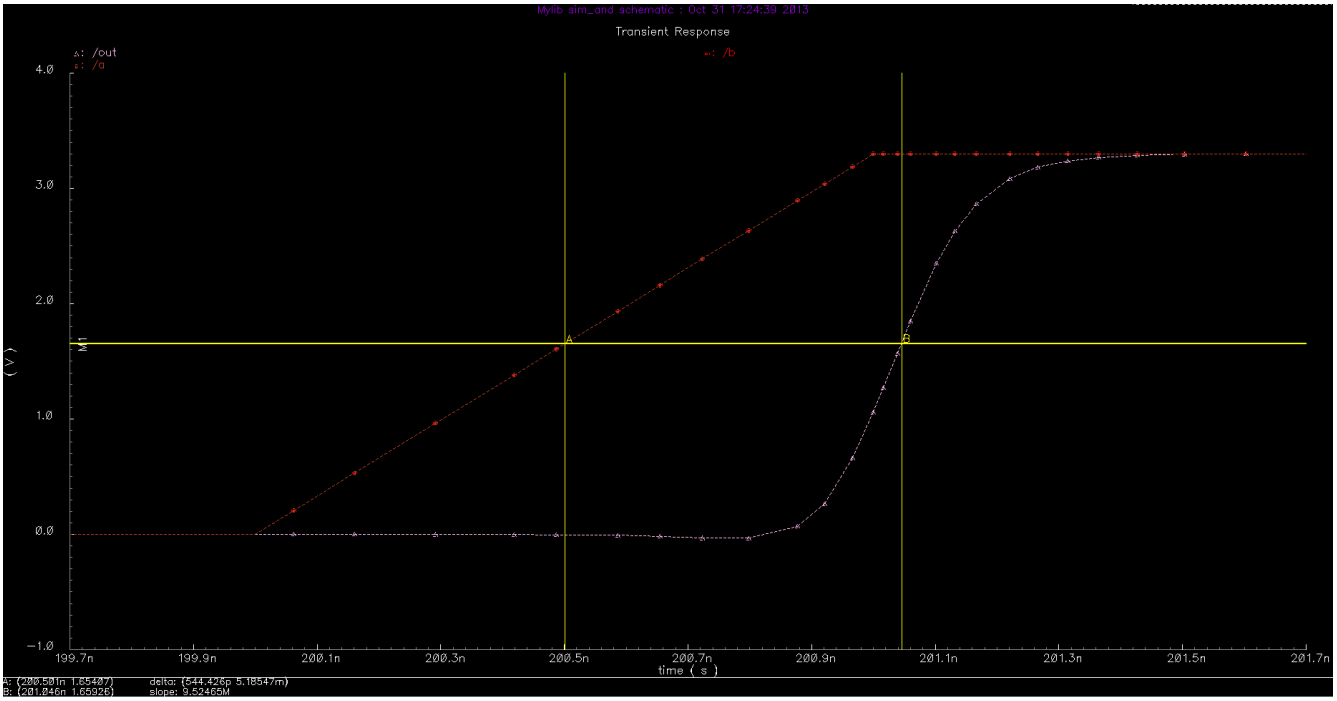

Figure 30. AND gate output signal rising propagation delay measurement (after sizing).

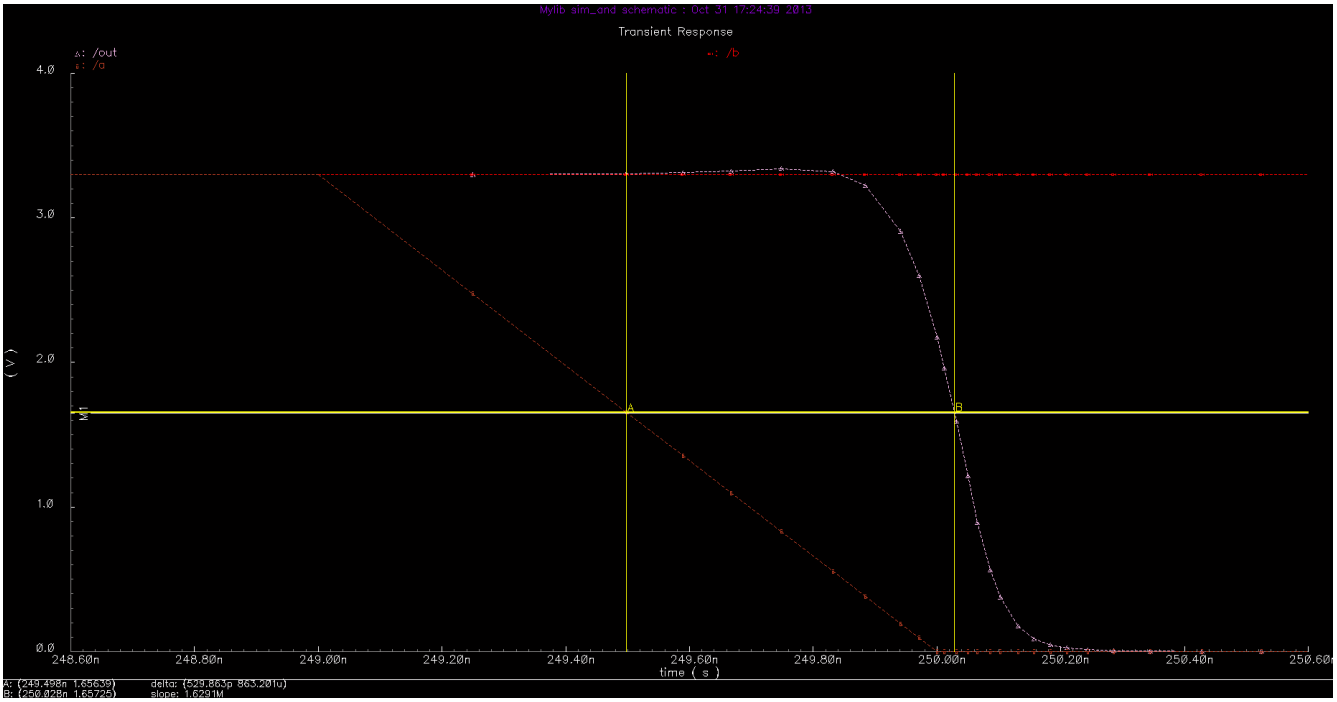

Figure 31. AND gate output signal falling propagation delay measurement (after sizing).

Table. 1. Summary of Timing Data for NAND and AND Gates

Time Unit: ps	**NAND**	**AND**
Output Rise Time	399.11	262.578
Output Fall Time	332.346	179.946
Output Rising Propagation Delay	343.168	554.426
Output Falling Propagation Delay	282.253	529.863