Fall 2013 **Introduction to VLSI Design**

Lab Assignment #7

Instructor: Dr. Ioannis Savidis
TA: Ying Teng E-Mail:yt74@drexel.edu

Drexel University
Electrical and Computer Engineering
Nov. 13th, 2013 (Wednesday)

---

1 Objectives

The goals of this assignment are to:

- Design an `edge-triggered flip-flop` using CMOS gates.
- Understand the functionality and characteristics of an `edge-triggered flip-flop`.

2 Assignments

The lab assignment is to design an `edge-triggered flip-flop`.

- Port `D` and port `CLK` are, respectively, the data input and the clock input. The port Q is the data output. The logic function of the `Flip-flop` is represented by the following equation:

$$Q = \begin{cases} D & \texttt{if } \textit{rising edge of } CLK \\ Q_{prev} & \texttt{if } \textbf{no } \textit{rising edge} \end{cases} \quad (1)$$

- Design a `flip-flop` using previously designed standard cells (Inverters, NAND gate, etc.).

3 Deliverables

The lab assignment is due next Friday, November 23^{rd}. The report should include:

1. The schematic and the layout view of the `flip-flop`.
2. Simulation results verifying the functionality of the `flip-flop` for both the schematic and the layout. The simulation results should clearly present the edge trigger characteristic of the `flip-flop`.
3. Marks of the setup time and hold time on the simulation results. The report should also include timing information of the `flip-flop` such as the propagation delay and rise/fall time.

`NOTE:` Pay attention when using standard cells for your designs. In addition to the correctness and functionality of the design, good, compact wiring will be an important aspect of your evaluation.

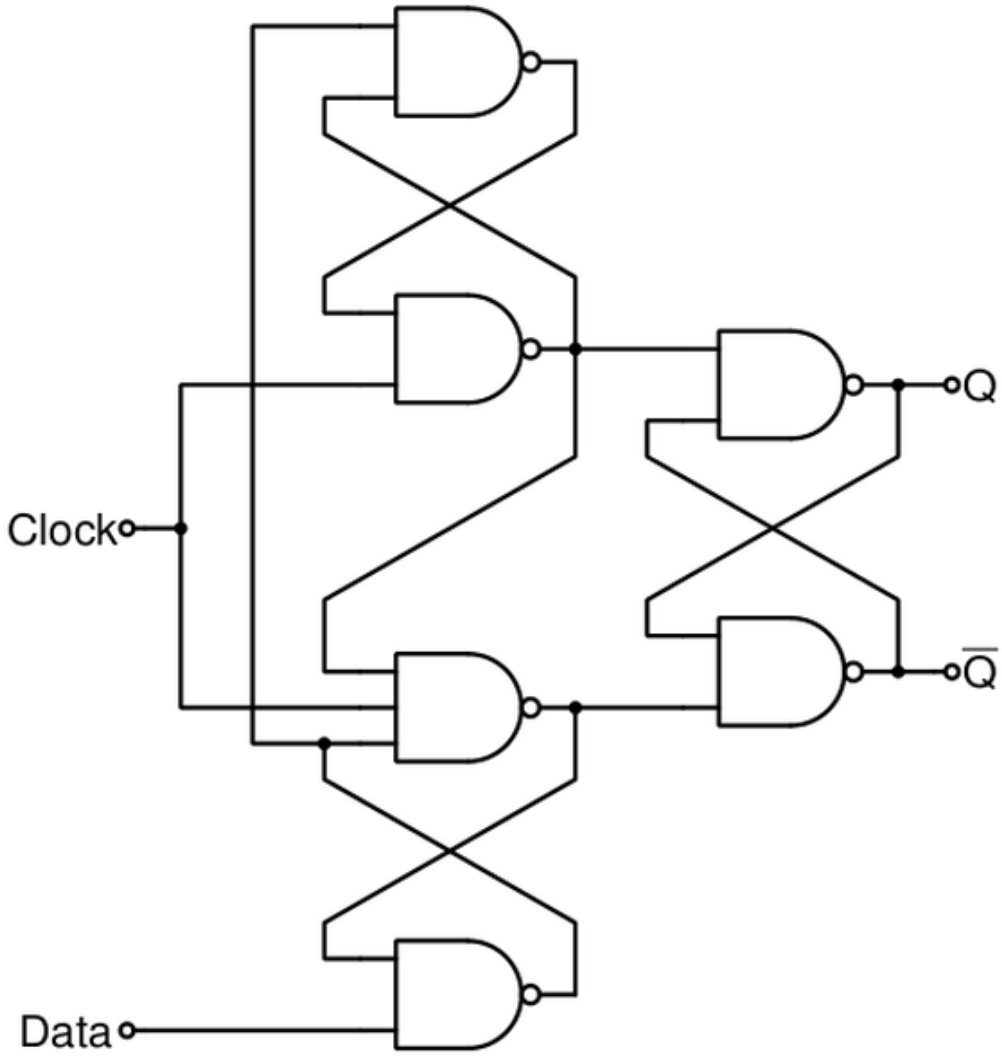

Figure 1: A schematic illustration of the *DFF*.