Drexel University
Electrical and Computer Engineering Department

ECEC 471
Introduction to VLSI Design

Lab Assignment 6A
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Lab 6A completes schematic and layout based simulations to characterize 2-to-1 MUX functionality. Special attention is paid to timing characteristics such as worst case propagation delay, and rise/fall time.

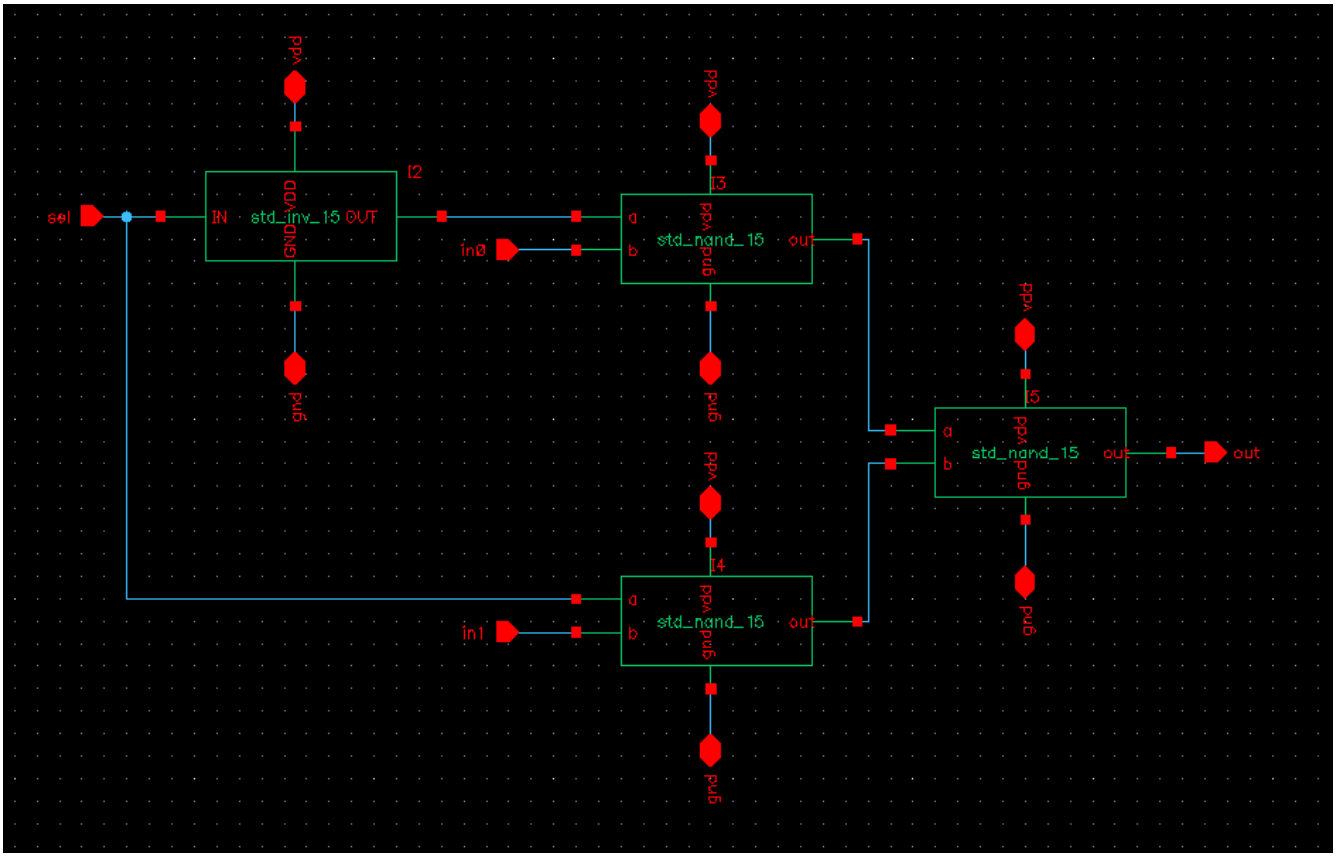

Fig. 1. Schematic view of 2-to-1 MUX.

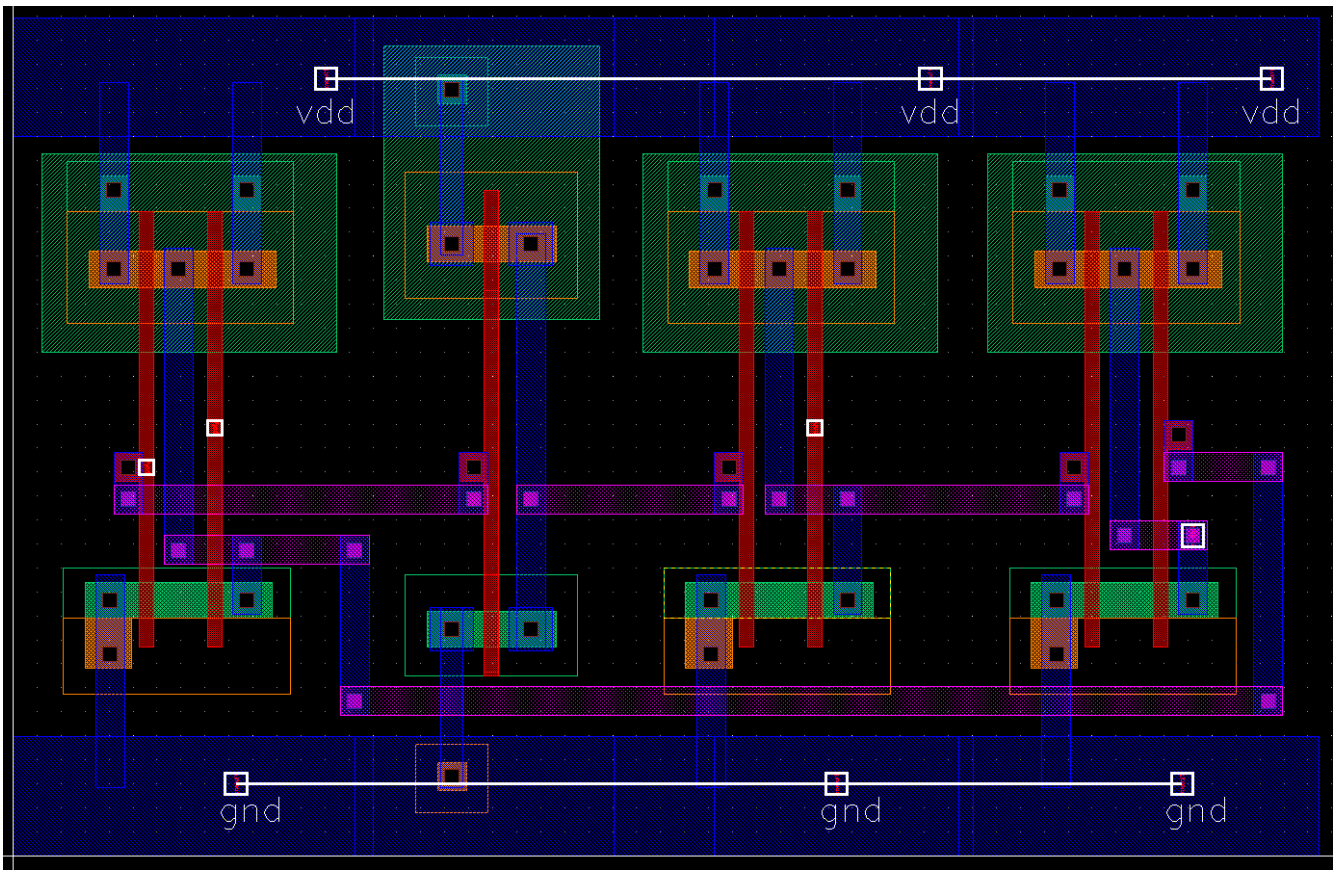

Fig. 2. Layout view of 2-to-1 MUX.

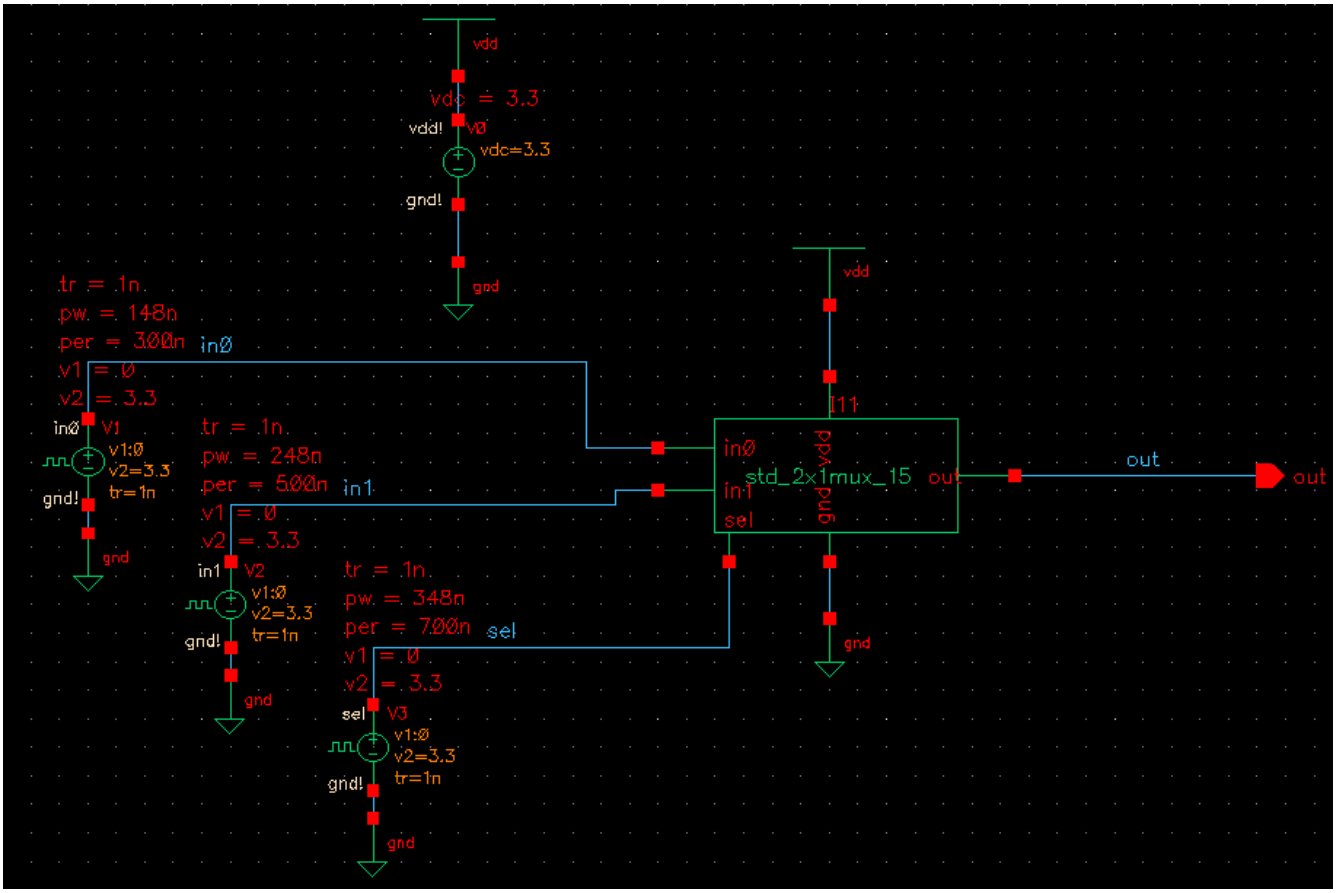

Fig. 3. Schematic view for simulation.

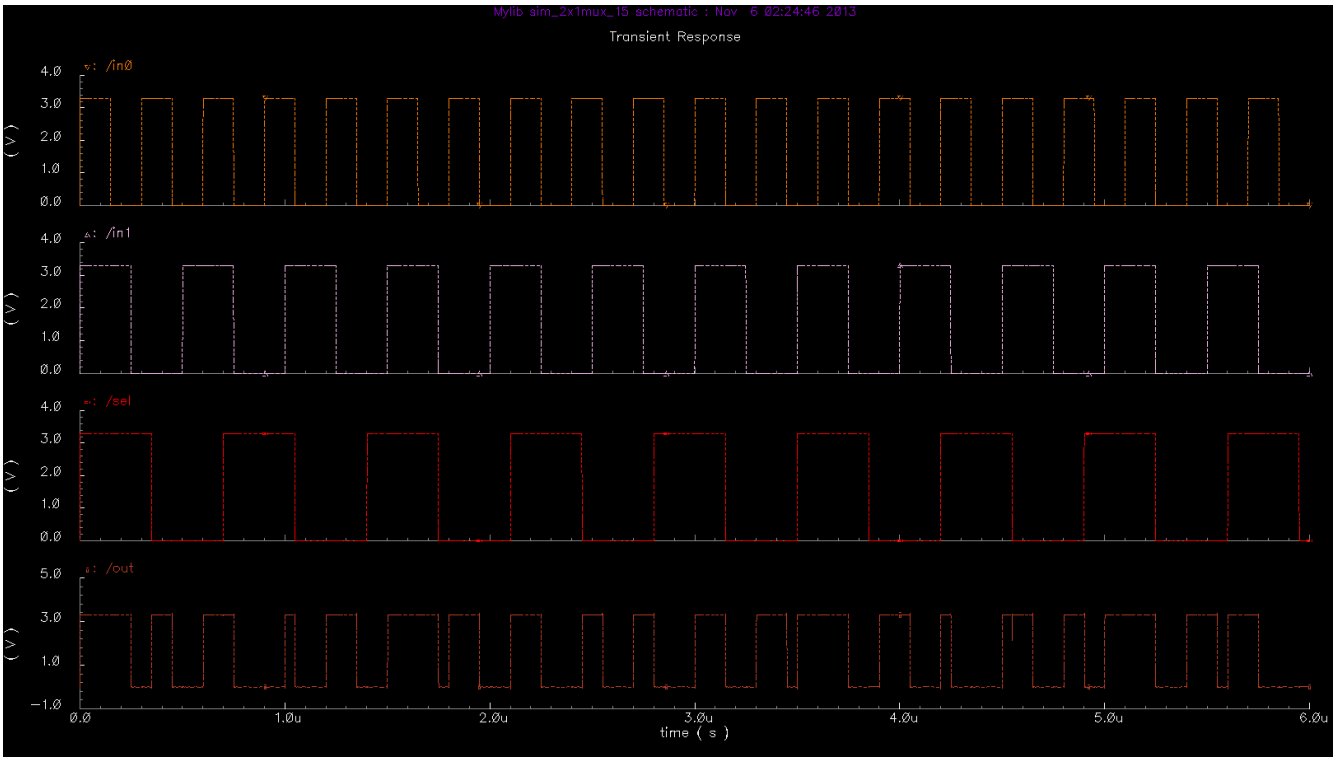

Fig. 4. Schematic based simulation verifying the functionality of the multiplexer .

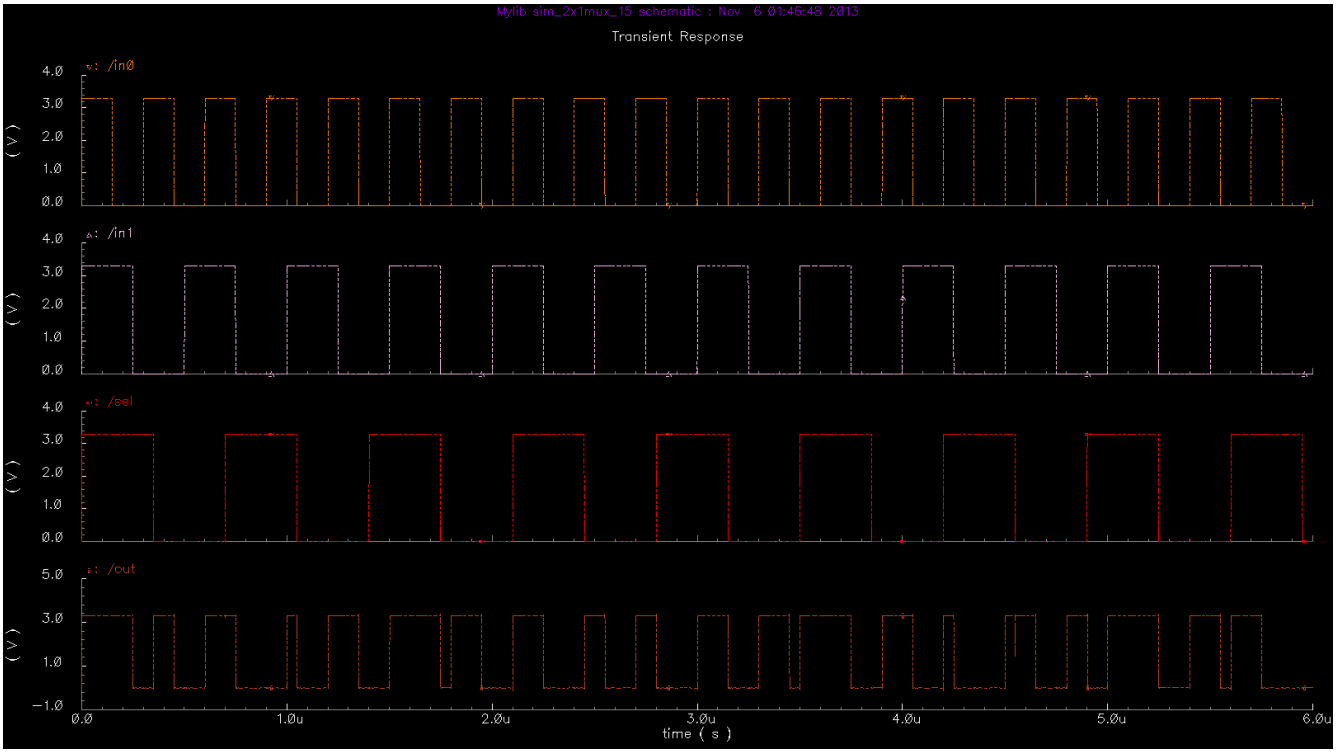

Fig. 5. Layout based simulation verifying the functionality of the multiplexer .

Per Prof. Savidis, a subset of possible input patterns were examined. The table below contains the input patterns characterized and timing information. 'R' indicates a rising signal, 'H' a high signal, 'F' a falling signal, and 'L' a low signal. Zeros in the propagation delay columns indicate that the input signal specified was not switching at the time or was not critical to the propagation delay (i.e. output transition occurred before input transition).

Table. 1. Worst case schematic based timing information.

Schematic Only Based							
				Propagation Delay from Input (ps)			
In0	**In1**	**Sel**	**Output**	**In0**	**In1**	**Sel**	**Transition Time (ps)**
R	R	R	R	646.265	646.265	646.265	319.243
R	F	H	F	0	574.316	0	317.273
R	R	F	R	635.897	635.897	1643	414.981
F	H	L	F	611.393	0	0	290.784
R	H	L	R	638.849	0	0	425.599
R	F	L	R	647.852	1642	0	417.88
F	L	L	F	603.198	0	0	296.501
R	L	L	R	638.296	0	0	420.444

Table. 2. Worst case layout/extracted based timing information.

Extracted Layout Based							
				Propagation Delay from Input (ps)			
In0	**In1**	**Sel**	**Output**	**In0**	**In1**	**Sel**	**Transition Time (ps)**
R	R	R	R	546.851	546.851	546.851	248.296
R	F	H	F	0	495.647	0	254.128
R	R	F	R	535.572	535.572	1533	318.395
F	H	L	F	512.975	0	0	236.2
R	H	L	R	534.189	0	0	325.109
R	F	L	R	532.533	1537	0	319.507
F	L	L	F	509.865	0	0	233.386
R	L	L	R	531.135	0	0	319.724

Table. 3. Worst case timing information summary.

			Input Pattern				
		Value (ps)	**In0**	**In1**	**Sel**	**Output**	**Signal**
Schematic	**Max Propagation Delay**	1643	R	R	F	R	Sel
	Max Transition Time	425.599	R	H	L	R	
Extracted	**Max Propagation Delay**	1537	R	F	L	R	In1
	Max Transition Time	325.109	R	H	L	R	