Fall 2013 **ECE-C471 Introduction to VLSI Design**

Lab Assignment #2

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1 Objective

The main objectives of this lab is to learn the Cadence custom design tools (**Virtuoso**) and the how to perform custom layout design in VLSI. The tasks of this lab are the following:

- Build an *Inverter* using transistors in the *Schematic View* of *Virtuoso*,
- Simulate the schematic inverters using *Virtuoso*,
- Build the *Inverter* in *Layout View* of *Virtuoso* without any DRC (Design Rule Check) errors,
- Match the *Schematic View* with the *Layout View* of the *Inverter* using LVS (Layout Versus Schematic);
- Extract the parasitic parameters of the *Inverter* layout.

2 Running *Virtuoso*

Cadence is one of the most widely used IC design software throughout the world. Cadence contains many sub-programs, each of which is responsible for one step in the IC design flow. In the content of this course, you will learn *Virtuoso*, the custom design tool designed by Cadence.

2.1 Prepare your PC for Cadence

First, you should the open Xwin-32 software and login to your account on **xunil.coe.drexel.edu**. When you login to the Linux host, check if your **.bashrc** file contains the following lines:

```
export IC51=/usr/lical/cadence/ic51
export CDS_INST_DIR = /usr/local/cadence/ic51
export CDS_INSTALL_DIR = $CDS_INST_DIR/tools.lnx86/dfII
export CDS_ROOT = $CDS_INST_DIR
export CDSDIR = CDS_INST_DIR/tools.lnx86
export CDK_DIR = /usr/local/cadence/ncsu-cdk-1.5.1
export PATH = $PATH:$CDSDIR/dfII/bin:$CDSDIR/bin:$CDSDIR/SKILL06.20/context:
$CDSDIR/SKILL06.30/context:$CDSDIR/dracula/bin
```

export LM_LICENSE_FILE = 5280@license1.ece.drexel.edu
export CDS_Netlisting Mode = "Analog"
export SYSTEM_CDS_LIB_DIR=$CDS_INST_DIR/share/cdssetup/dfII

Second, check if you have the **cds.lib** file in your account root directory. If so, check if the **cds.lib** file contains the following lines:

SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
DEFINE basic $CDK_DIR/lib/basic
DEFINE NCSU_Analog_Parts $CDK_DIR/lib/NCSU_Analog_Parts
DEFINE NCSU_Digital_Parts $CDK_DIR/lib/NCSU_Digital_Parts
DEFINE MOSIS_Layout_Test $CDK_DIR/lib/MOSIS_Layout_Test
DEFINE NCSU_TechLib_ami06 $CDK_DIR/lib/NCSU_TechLib_ami06
DEFINE NCSU_TechLib_ami16 $CDK_DIR/lib/NCSU_TechLib_ami16
DEFINE NCSU_TechLib_hp06 $CDK_DIR/lib/NCSU_TechLib_hp06
DEFINE NCSU_TechLib_tsmc02 $CDK_DIR/lib/NCSU_TechLib_tsmc02
DEFINE NCSU_TechLib_tsmc02d $CDK_DIR/lib/NCSU_TechLib_tsmc02d
DEFINE NCSU_TechLib_tsmc03 $CDK_DIR/lib/NCSU_TechLib_tsmc03
DEFINE NCSU_TechLib_tsmc03d $CDK_DIR/lib/NCSU_TechLib_tsmc03d
DEFINE NCSU_TechLib_tsmc04_4M2P $CDK_DIR/lib/NCSU_TechLib_tsmc04_4M2P

After including the **.bashrc** file and **cds.lib** files, type **icfb** to run the Cadence Virtuoso software.

3 Design Requirements

Different technology libraries contain different feature sizes and design rules. The **AMI06** ($0.6\mu m$) technology library will be used throughout this quarter unless noted otherwise. All standard cells designed in this class should have the same height of 35μm. It is recommended that you reduce the maximum cell height below 35μm to reduce area, but make sure that **all the cells you design this quarter have the same height**. This is especially helpful in the following labs when you required to build a new gate using the previously designed gates.

4 Lab reports

Lab reports are due on the following Wednesday before class. Unless explicitly stated, lab reports are typically due one week after the laboratory session. **Electronic submission in pdf or doc format through email** is accepted.

The lab report of the Inverter lab should include the following:

1. A screen shot of the *Schematic view* of the Inverter, similar to what is shown in Figure 1;
2. The screen shot of the *Layout view* of the Inverter similar to what is shown in Figure 2;
3. The screen shot of the *Extracted view* of the Inverter;
4. The layout DRC and LVS verification results;
5. The functionality of both the **Schematic-based** and **Layout-based** simulations:

(a) Mark the timing information on the plot including the rise time tr, fall time tf and propagation delay $tprop$;

(b) Report all the measurement results in a **table**, such as:

Sim type	tr	tf	$tprep$
Front end sim			
Back end sim			