Drexel University
Electrical and Computer Engineering Department

ECEC 471
Introduction to VLSI Design

Lab Assignments 2,3,4
October 23rd, 2013

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Lab 2 + 3

Labs 2 and 3 complete schematic and layout based simulations to characterize inverter function. Lab 3 specifically sizes the PMOS transistor channel width such that the switching threshold is half of Vdd.

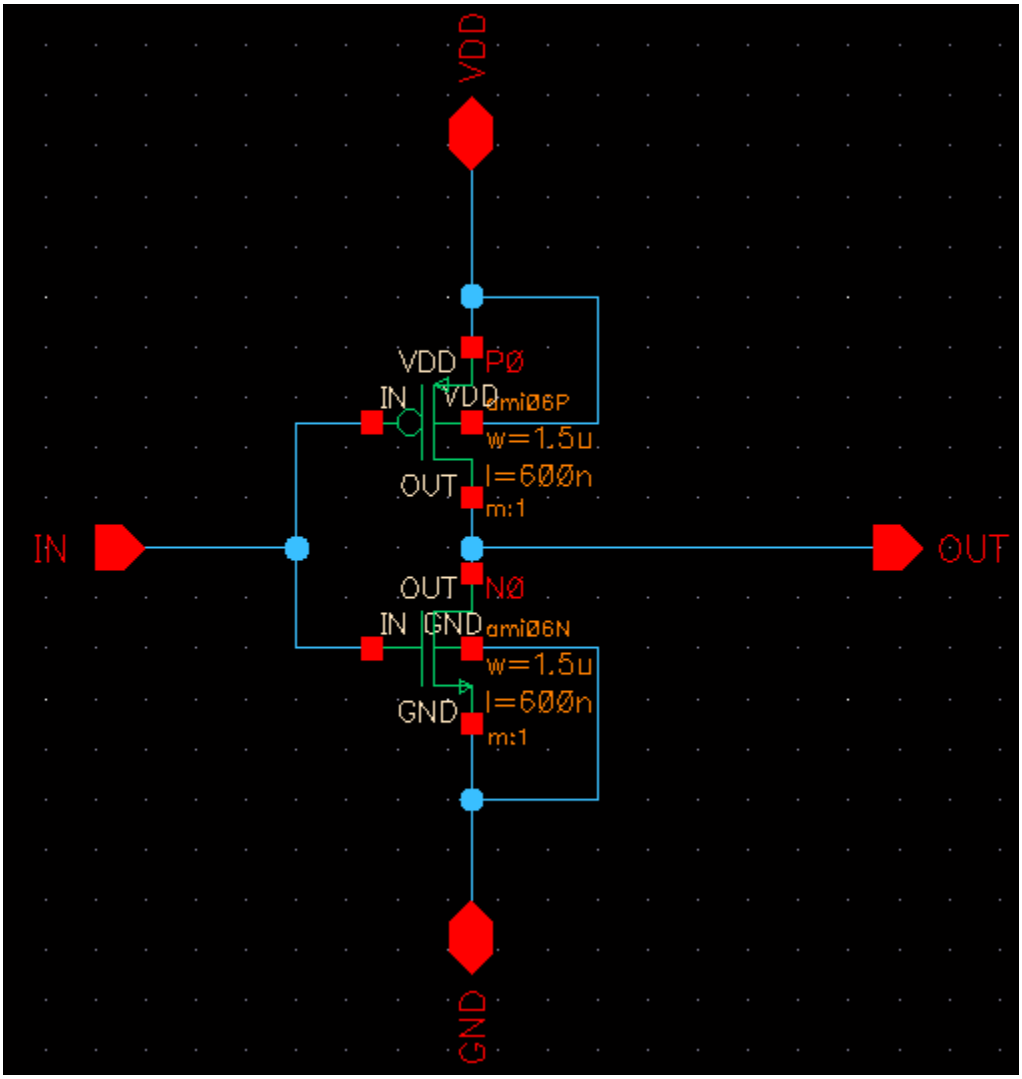

Figure 1. Schematic view of the inverter

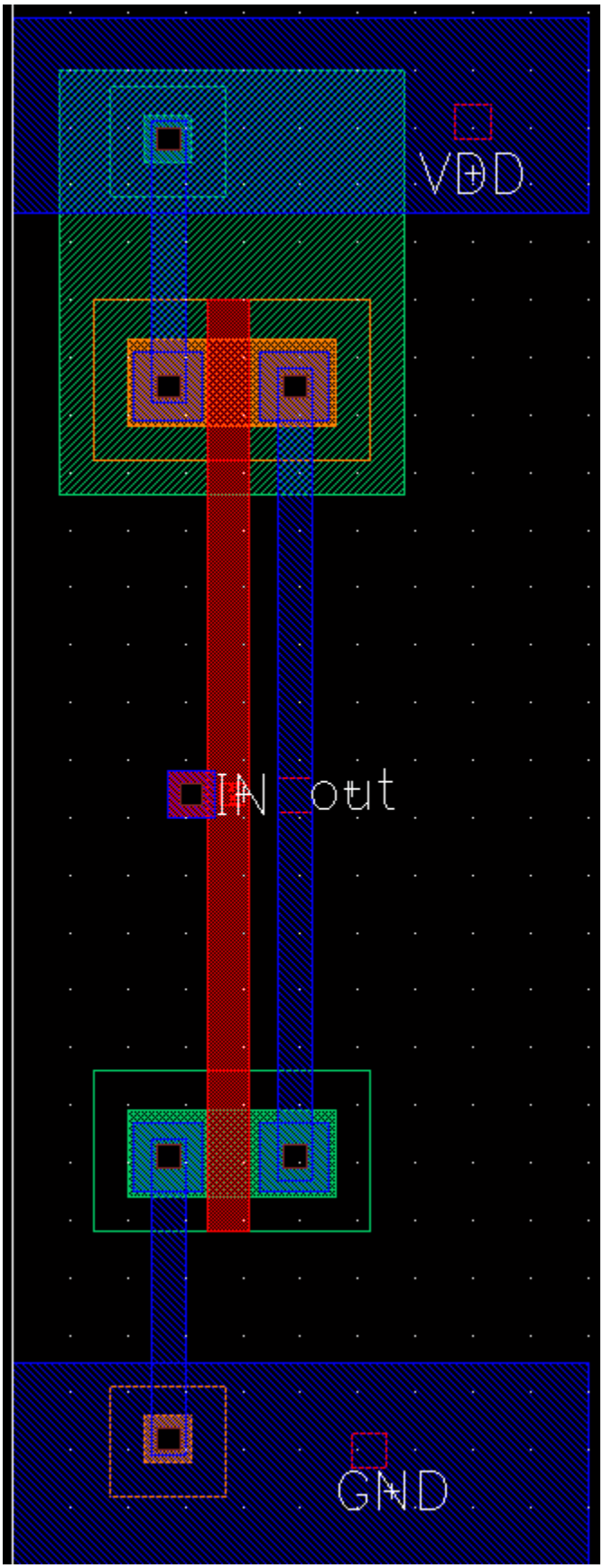

Figure 2. Layout view of the inverter

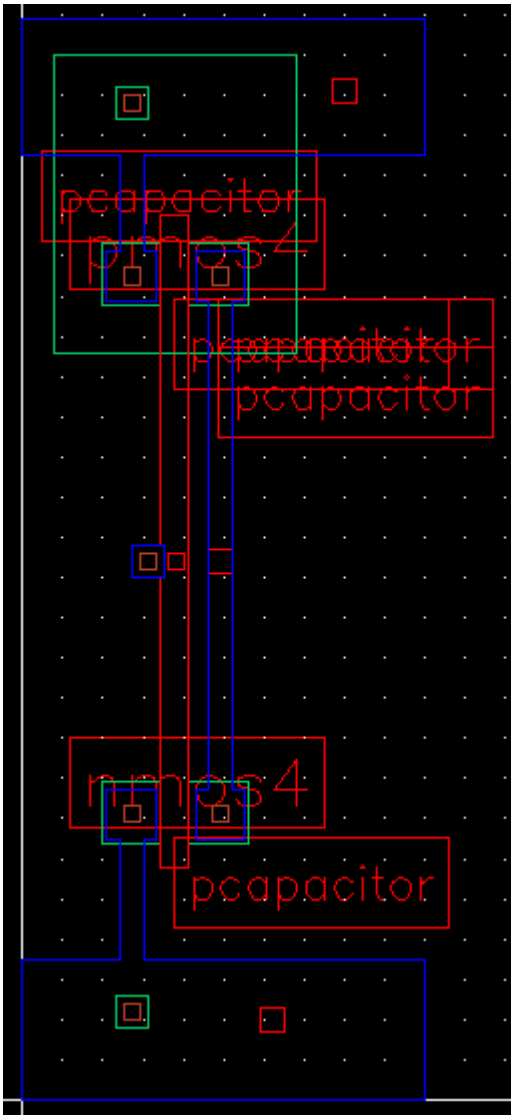

Figure 3. Extracted view of the inverter

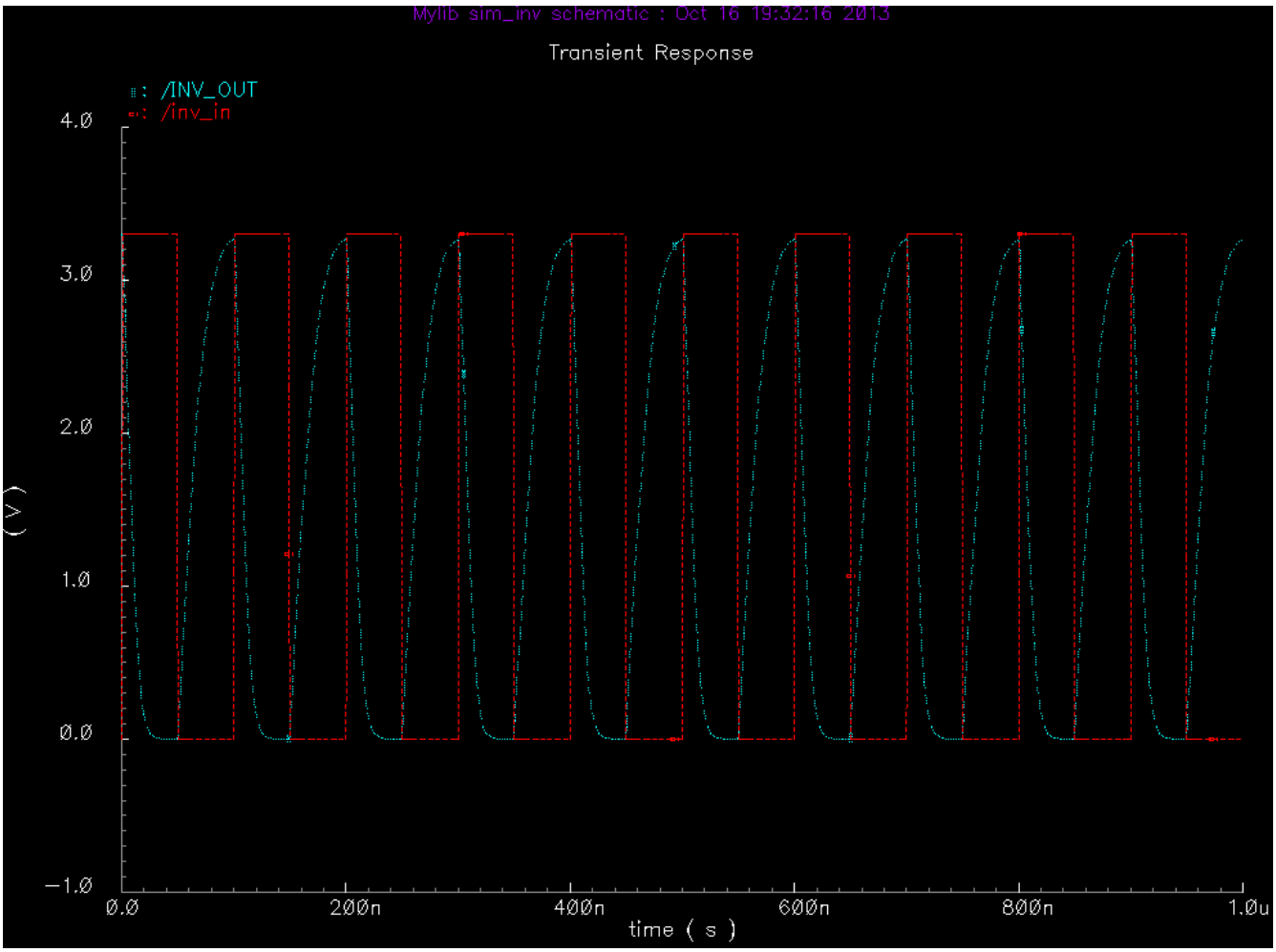

Figure 4. Schematic-based transient simulation

Note: Propagation delay, DRC, LVS, and layout based simulations were only collected during Lab 3 (after the switching threshold PMOS sizing,
i.e. No layout based data was collected during Lab 2, only during Lab 3)

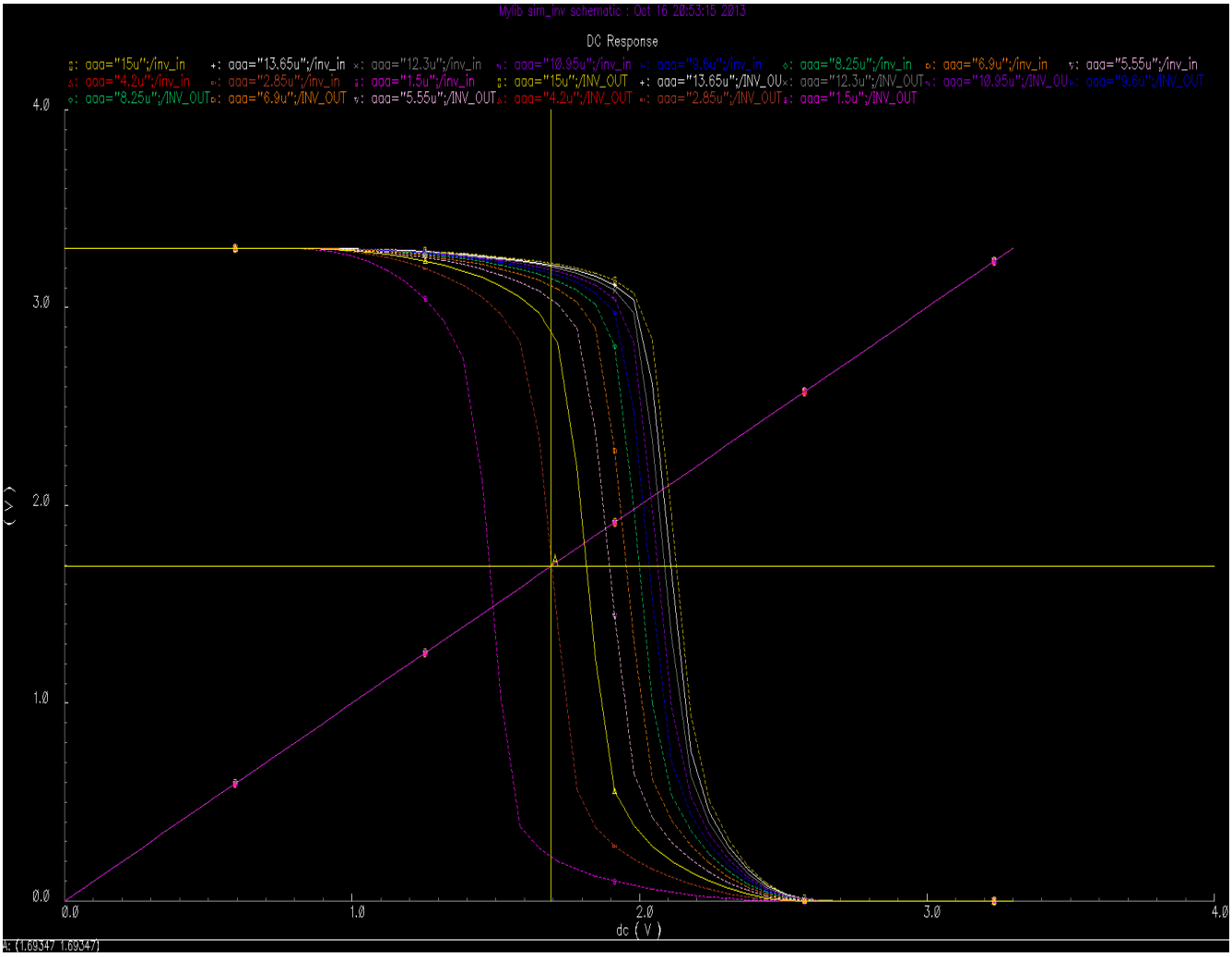

Figure 5. DC sweep simulation plot used to choose the channel width

PMOS Width: 2.85 um
NMOS Width: 1.5 um

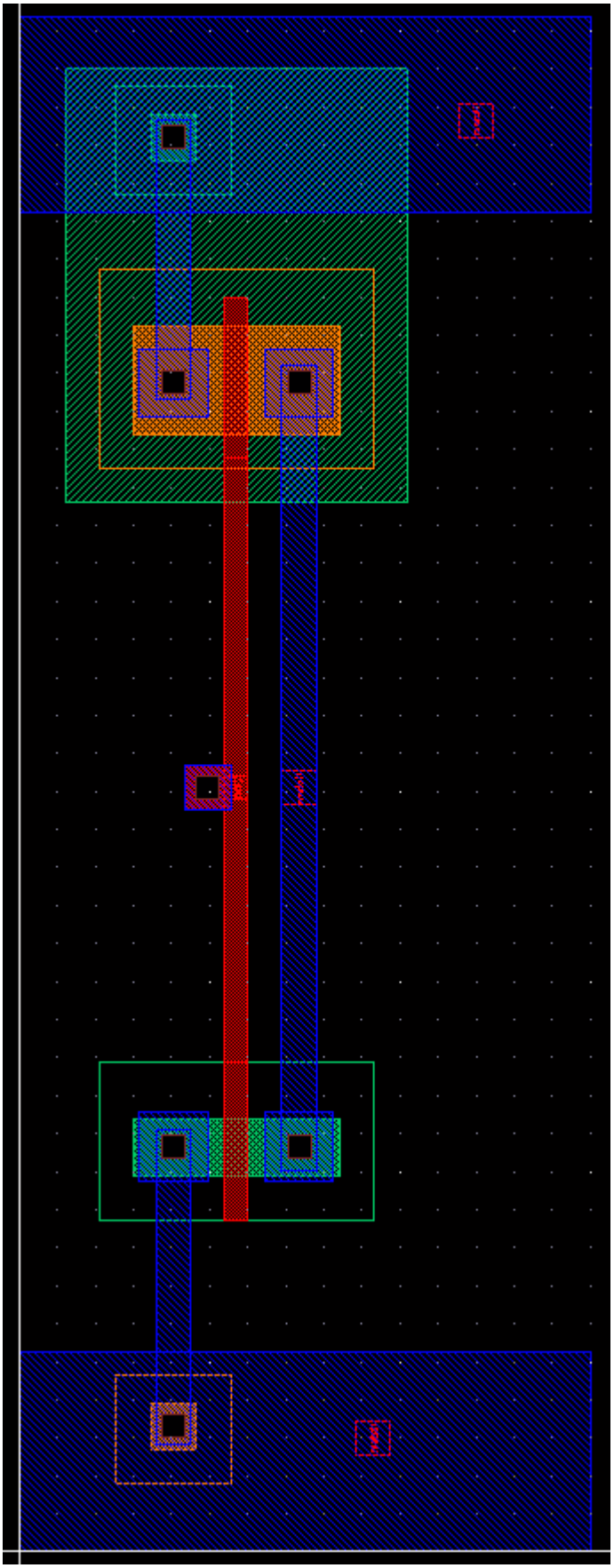

Figure 6. Layout view of the symmetrical inverter

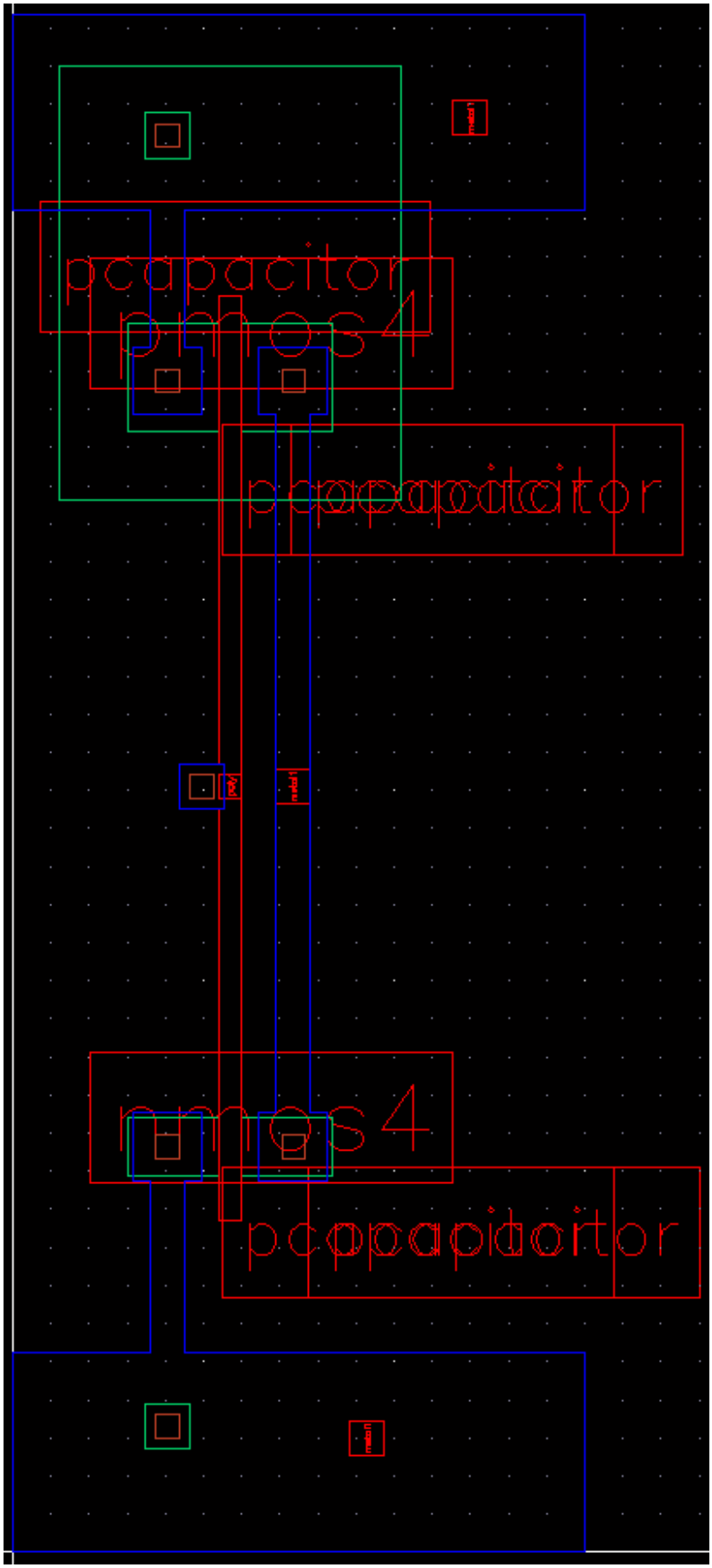

Figure 7. Extracted view of the symmetrical inverter

```
DRC started.......Wed Oct 16 23:39:31 2013
    completed ....Wed Oct 16 23:39:31 2013
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "std_inv_15 layout"   *********
   Total errors found: 0
```

Figure 8. DRC verification results for symmetrical inverter

```
LVS job is now started...
The LVS job has completed. The net-lists match.
Run Directory: /home/DREXEL/jvk27/ECEC471/LVS
```

Figure 9. LVS verification results symmetrical inverter

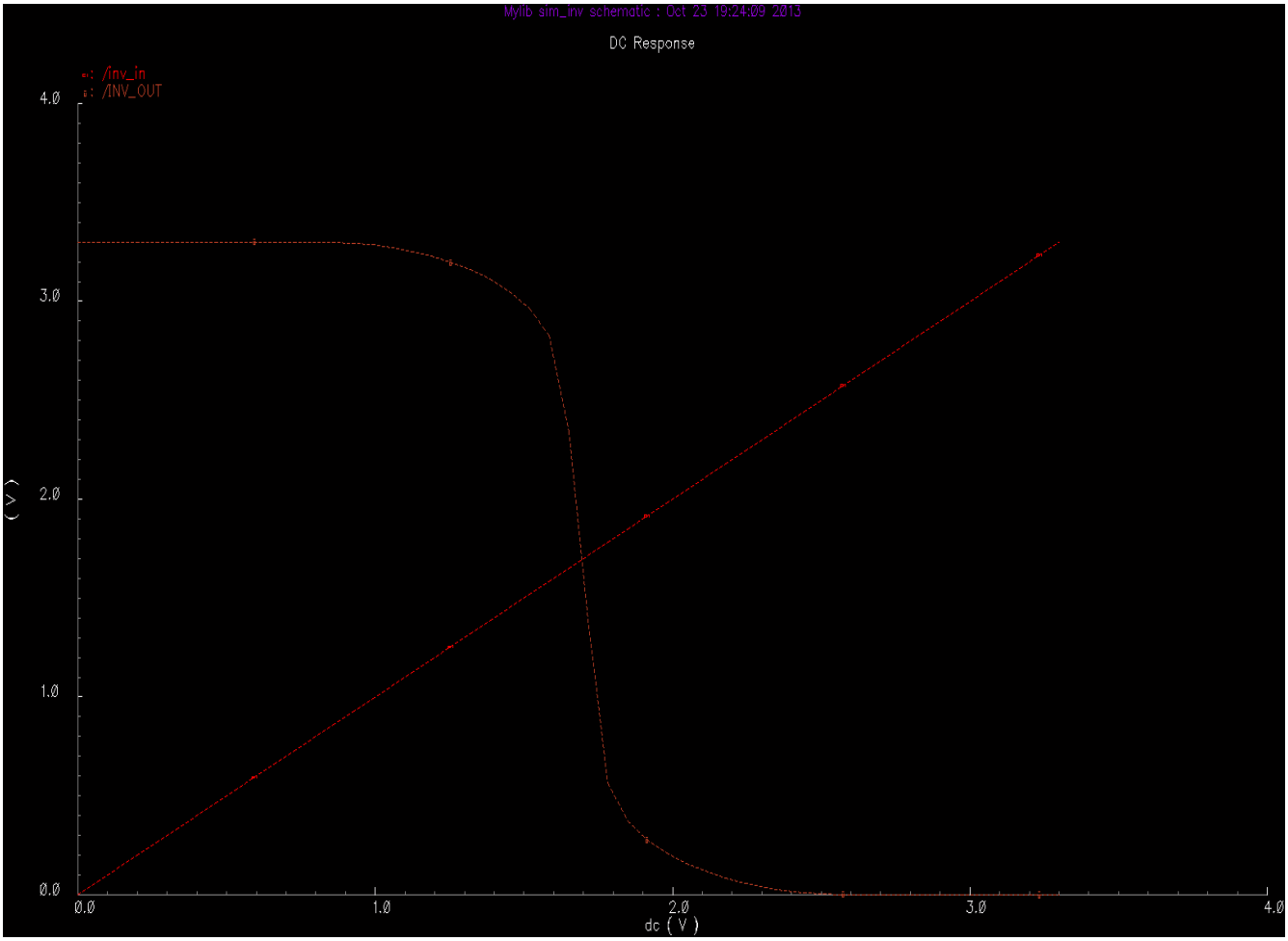

Figure 10. DC simulation results for schematic view (no extracted caps)

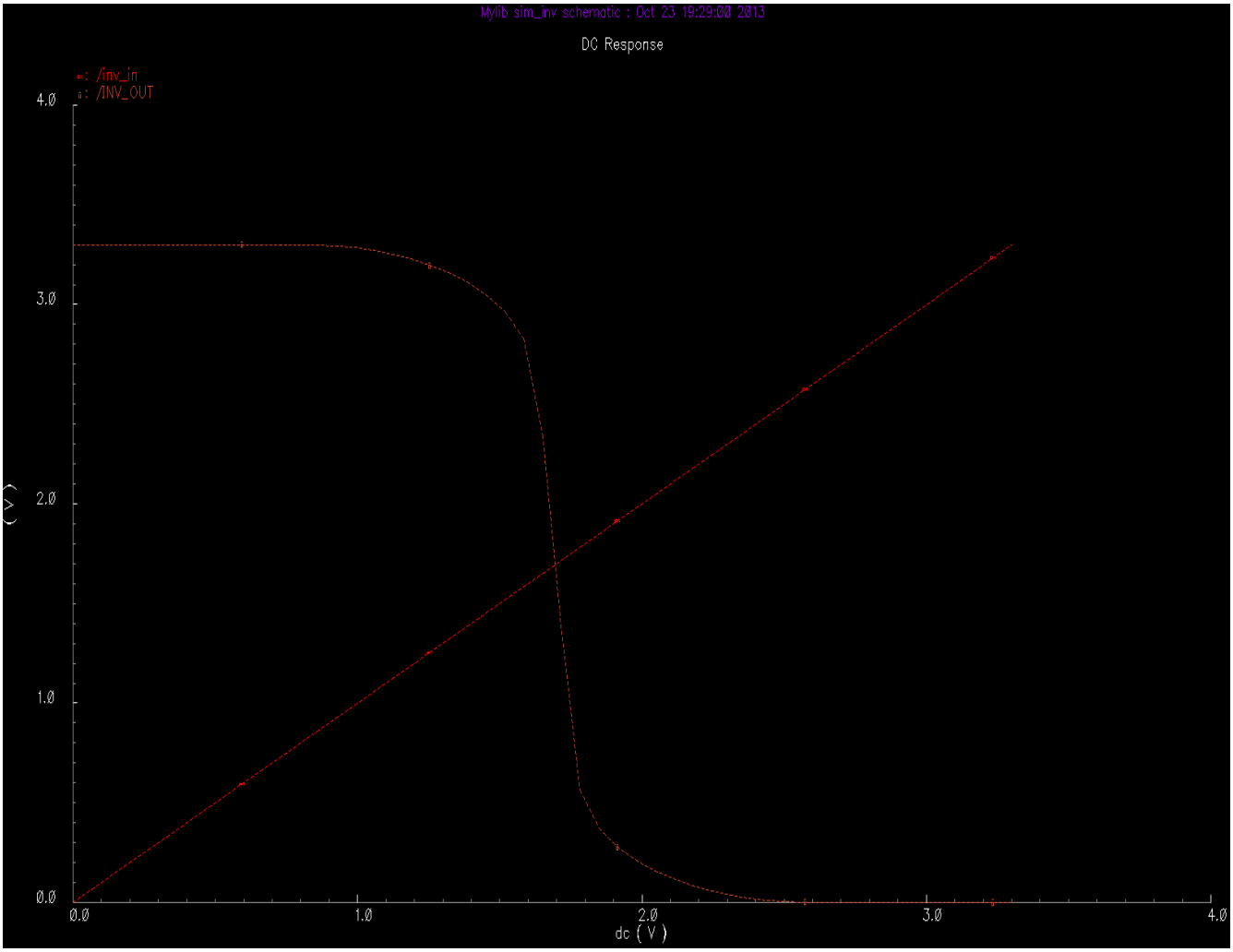

Figure 11. DC simulation results for layout view (included extracted caps)

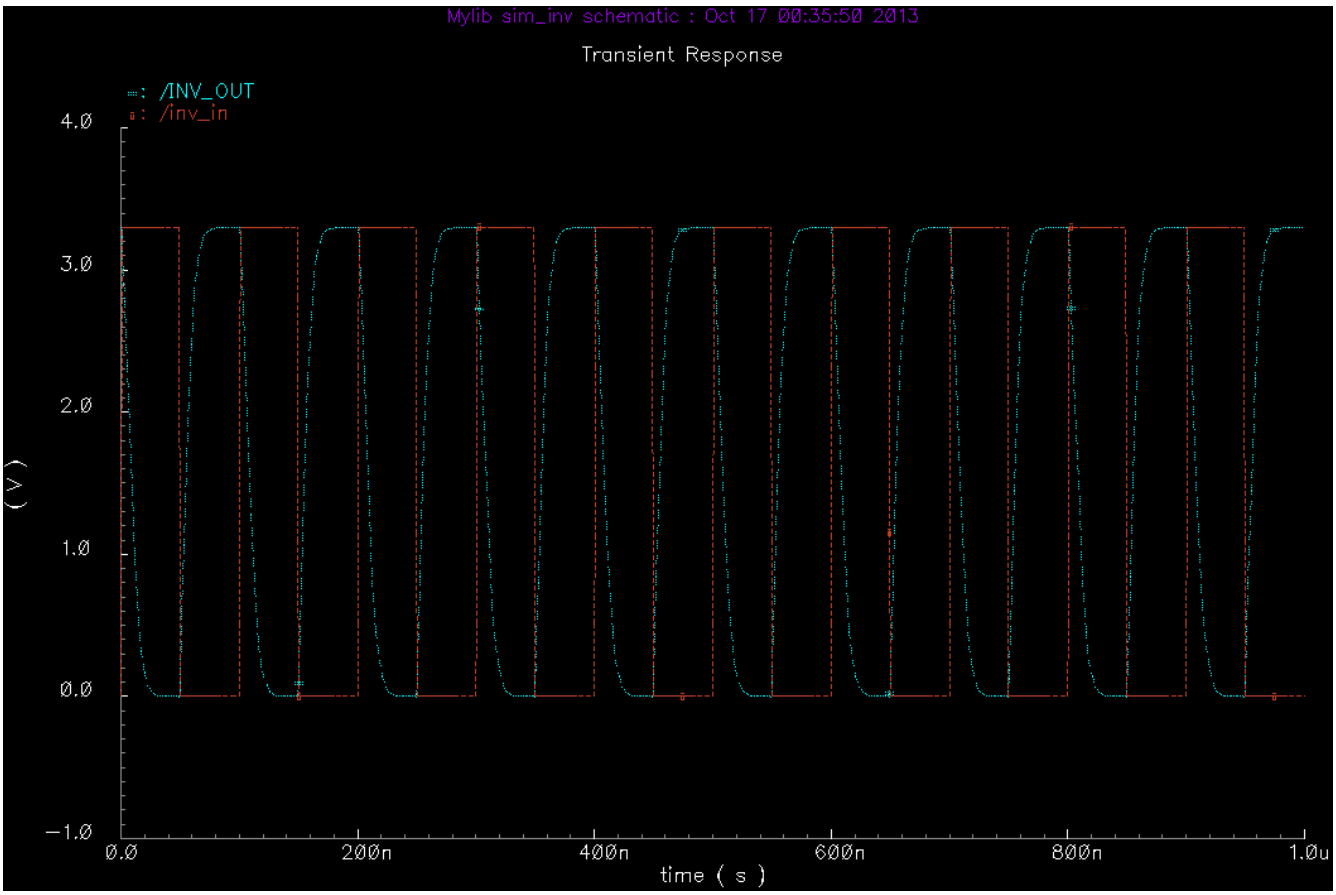

Figure 12. Transient simulation result for the newly designed symmetrical inverter

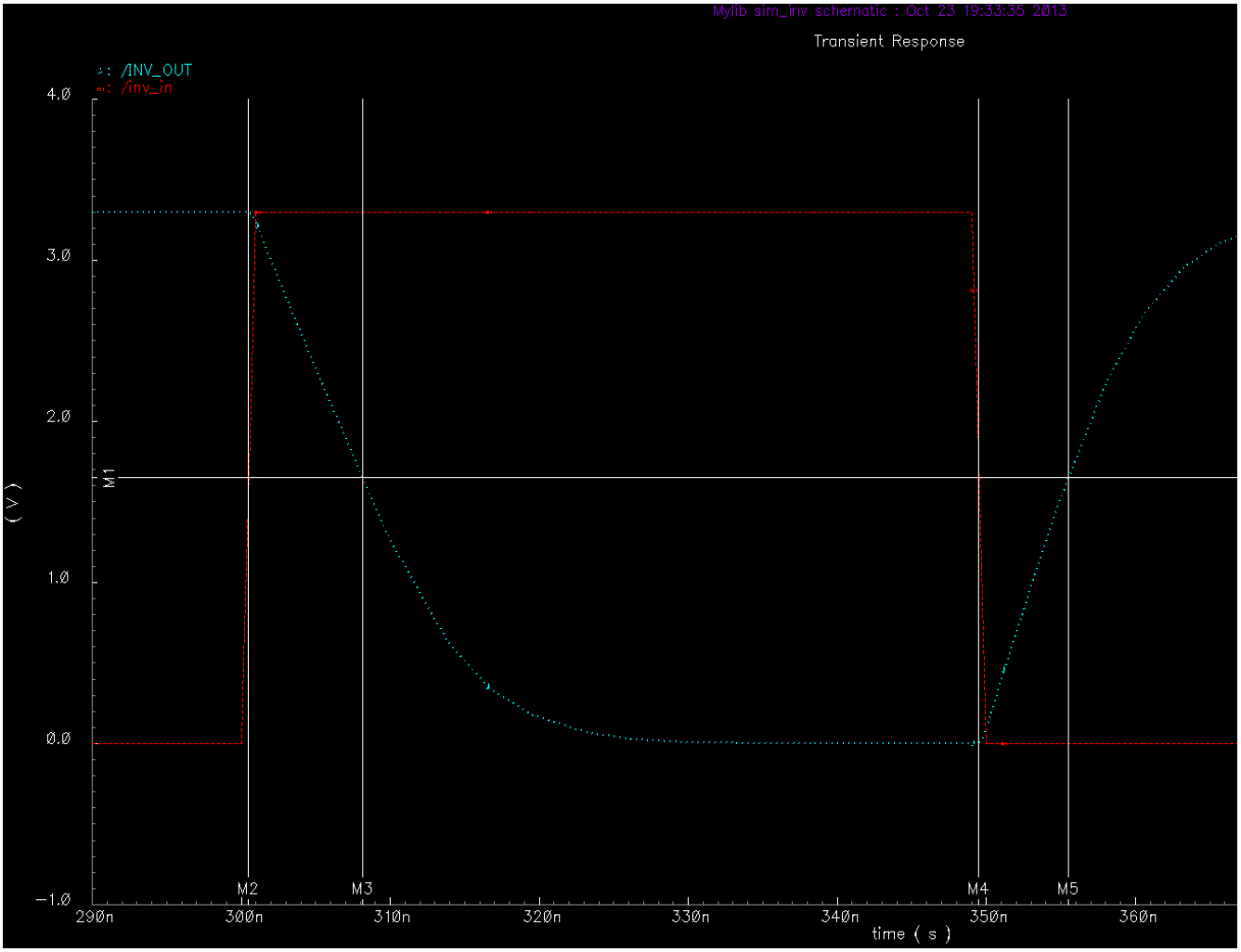

Figure 13. Transient simulation result for the newly designed symmetrical inverter with critical points marked (see below).

Table 1. Marker values and units

Marker	**Value**	**Unit**
M1	1.65	V
M2	300.499	ns
M3	308.174	ns
M4	349.497	ns
M5	355.536	ns

The critical points (M2 through 5) marked above are the ½ Vdd (M1) time points for rising and falling propagation. Thus the rise and fall propogation times can be calculated as:

Rising input propagation = M3 – M2 = 7.675 ns
Falling input propagation = M5 – M4 = 6.039 ns

Lab 4

This lab evaluates the sizing of inverters in a chain and examines the operating frequency of a 21-inverter ring oscillator. The chain of inverters is first optimized to minimize the propagation delay from input to output when driving a load capacitance. Next, all inverters in the chain are made equal-sized and the propagation delay is examined once more as the inverter sizes are swept over a range.

The optimal number of inverters in a chain is given in the equation below (1).

$$f = \sqrt[n]{C_l / C_{gin}} \tag{1}$$

Where f is the sizing factor, n is the number of stages, C_l is the load capacitance, and C_{gin} is the first gate input capacitance. (1) can be solved for n.

$$n = \ln \frac{C_l}{C_{gin}} \tag{2}$$

$$\begin{gathered} C_l = 1\text{pF} \\ C_{gin} = 10\text{fF} \\ f = e \\ n = 4.6 \approx 4 \end{gathered} \tag{3}$$

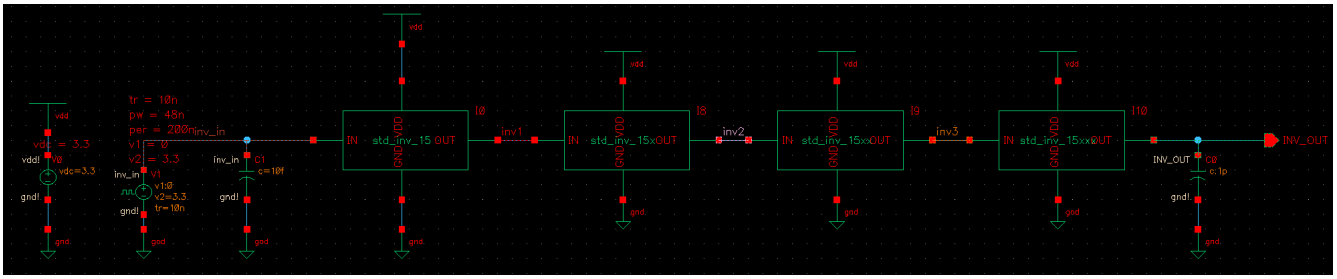

Figure 14. Schematic view of the inverter chain

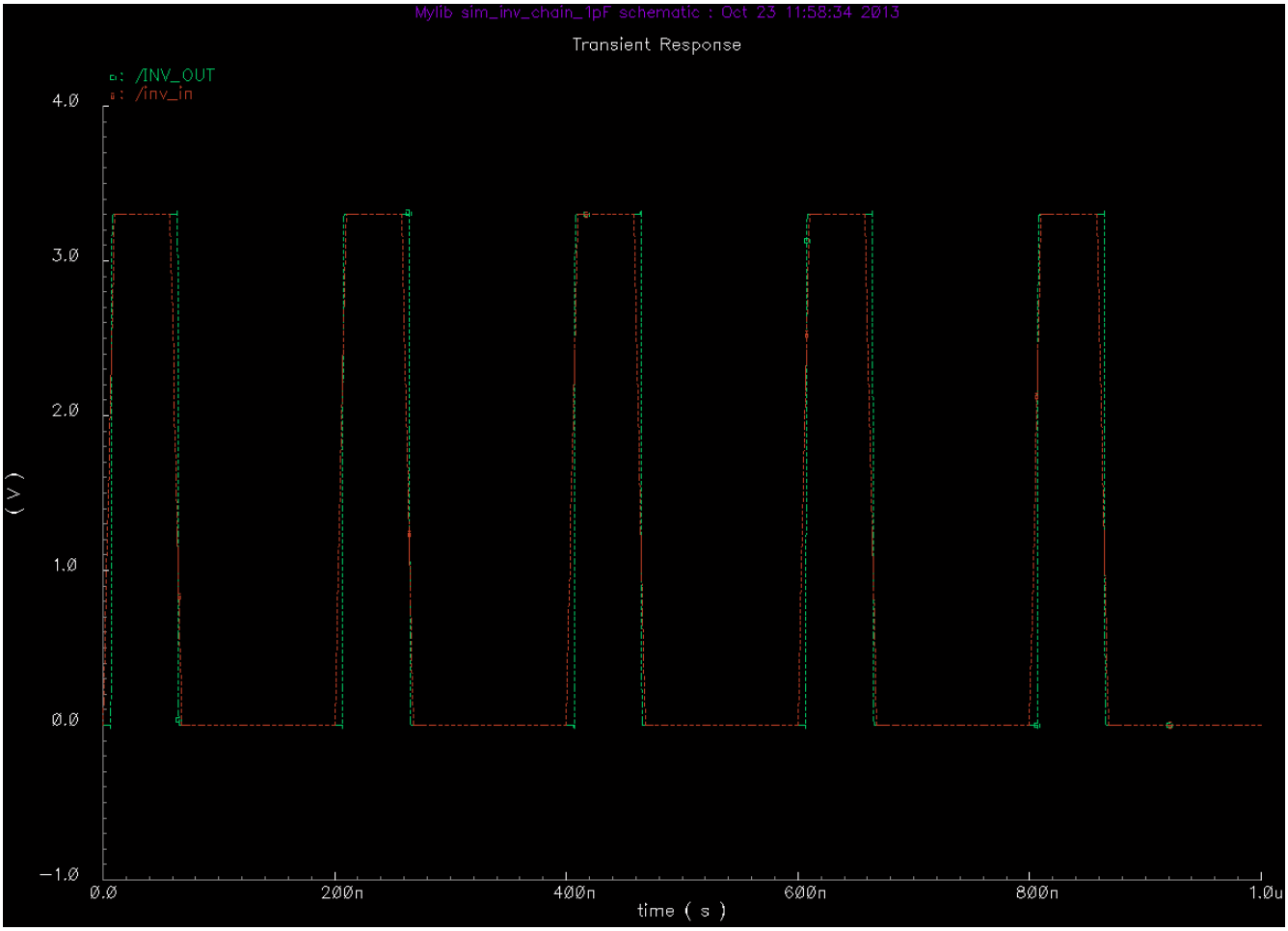

Figure 15. Simulation waveform

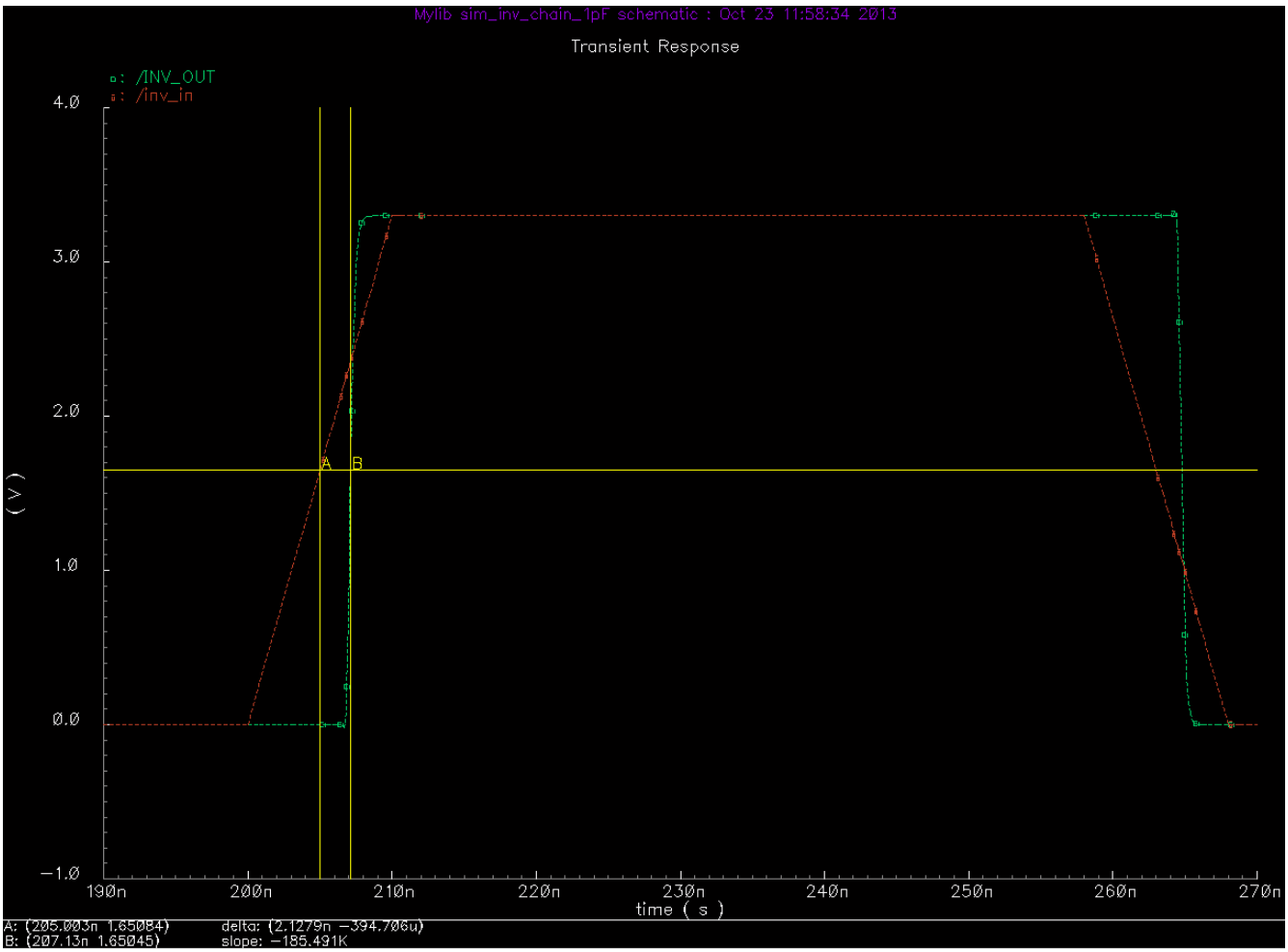

Figure 16. Simulation waveform (zoomed) with markers delineating the rising propagation delay of 2.1 ns

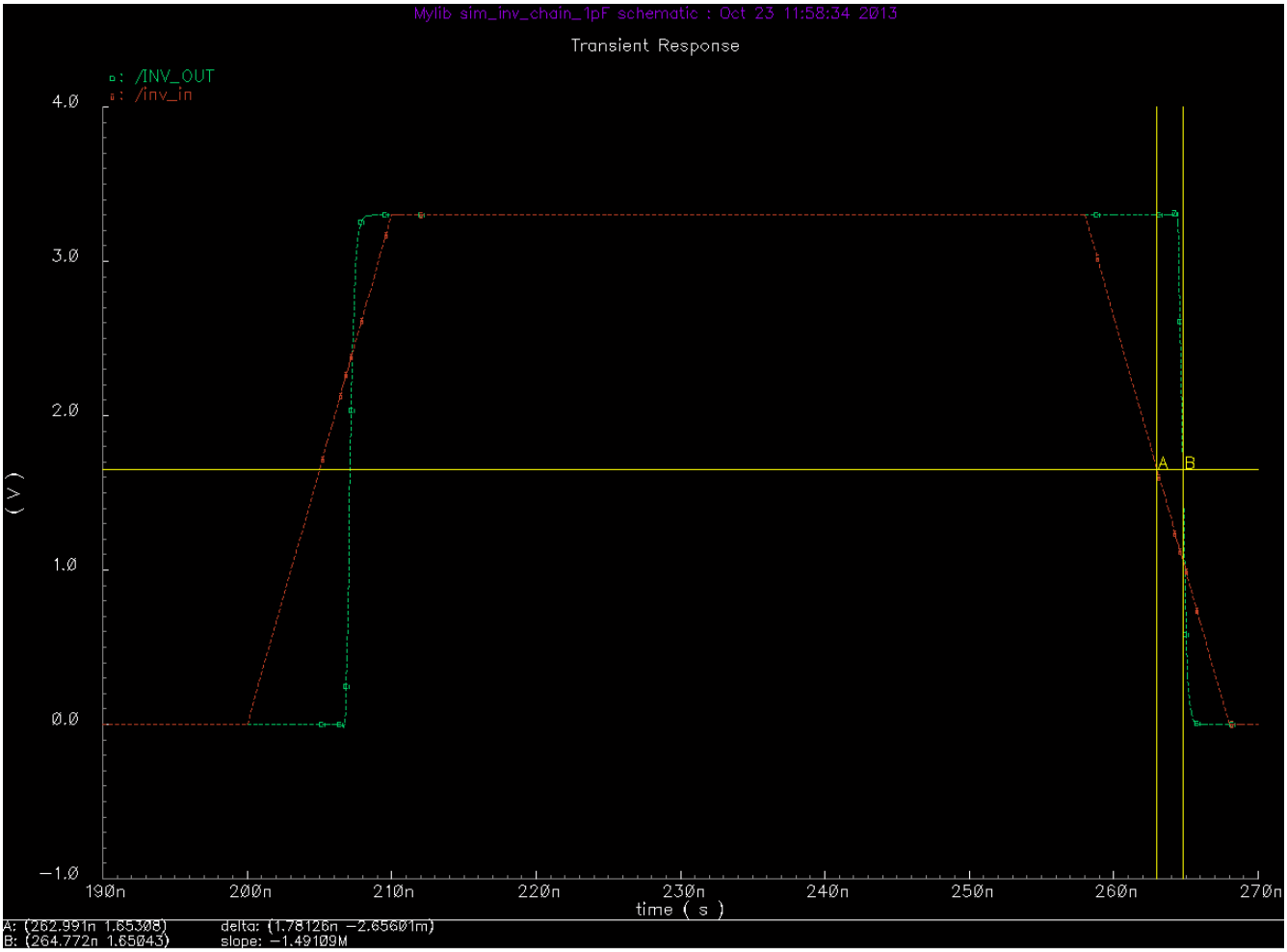

Figure 17. Simulation waveform (zoomed) with markers delineating the falling propagation delay of 1.8 ns

Using simulations results, the rise/fall (labeled as *transitions* below) propagation for each inverter was measured.

Table 2. Transition times for each inverter in the chain

Inverter	Transition 1 Time (ns)	Transition 2 Time (ns)	Average Transition Time (ns)
INV1	1.1392	0.8398	0.9895
INV2	0.4148	0.3384	0.3766
INV3	0.2096	0.2519	0.23075
INV4	0.3681	0.344	0.35605

The total propagation delay (as measured from the input to the first inverter to the output of the last) is shown below.

Table 3. Propagation delay through the entire chain

Transition 1 Time (ns)	Transition 2 Time (ns)	Average Transition Time (ns)
2.1279	1.7812	1.95455

Note: The sum of the average transition times for each inverter (Table 2) equals the value shown for the average total propagation delay through the entire chain (Table 3).

Compared to the same capacitive load being driven by a single inverter (Table 1, avg=6.857 ns) the chain is able to drive the load roughly ~3.5 times faster.

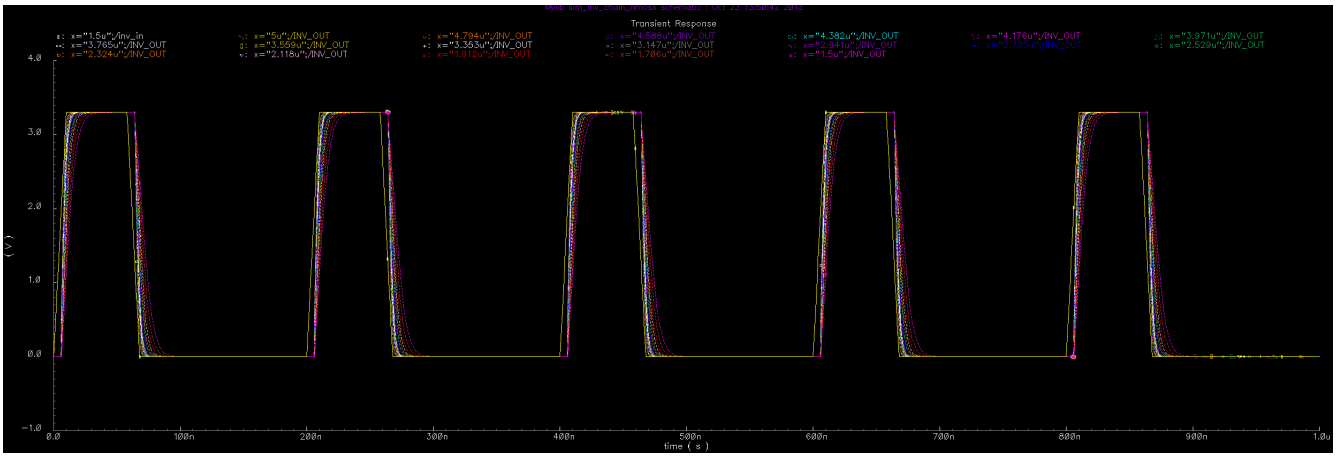

Figure 18. Sweep of inverter size from NMOS width=1.5 um 5.0 um and resulting transient waveforms
Note: The ratio of PMOS to NMOS as computed in Lab 3 was 1.9. Thus, to maintain this ratio, the PMOS width was swept from 2.85 um to 9.5 um during this process.

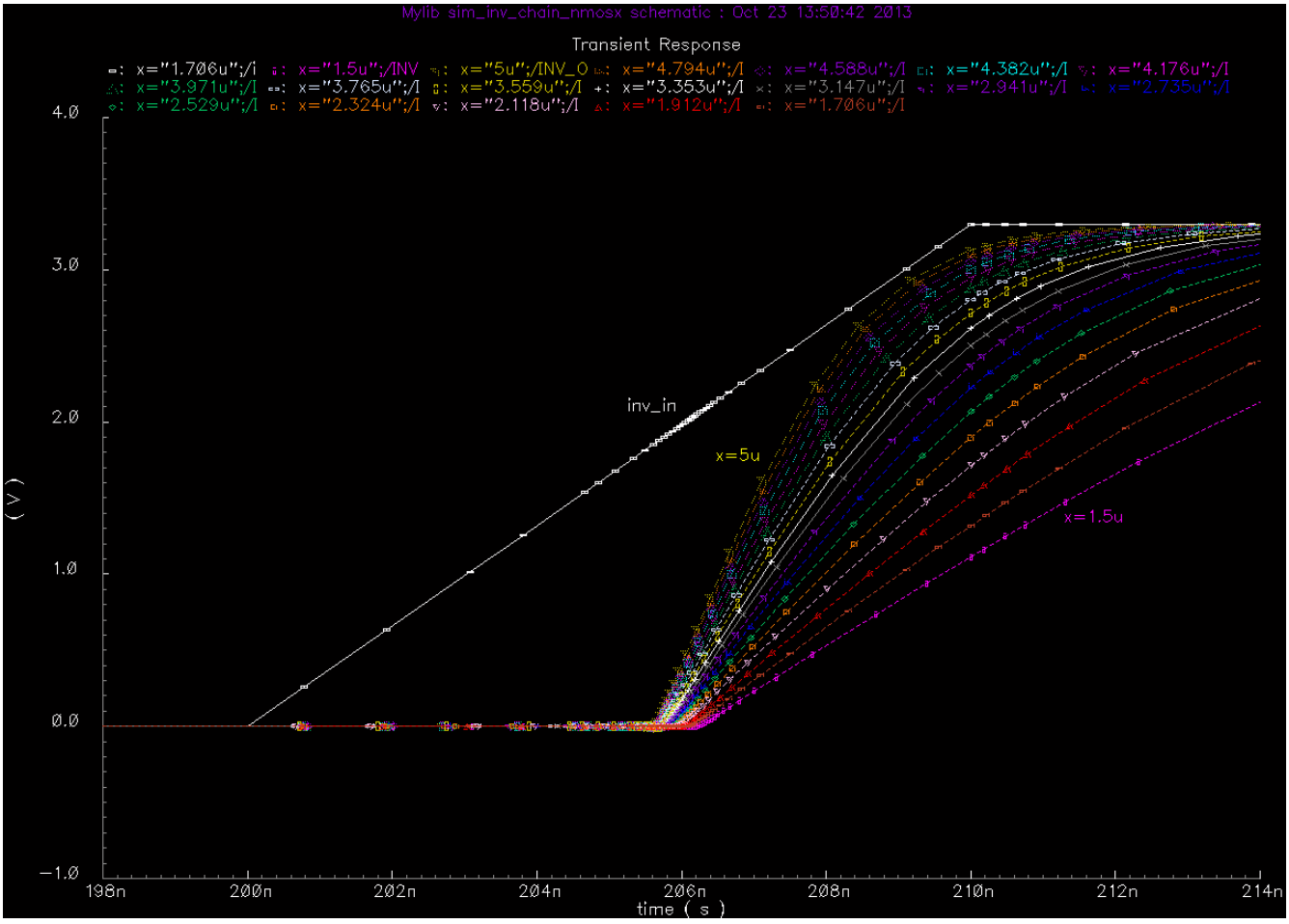

Figure 19. Rising portion of the resulting transient waveforms for sweep of inverter size

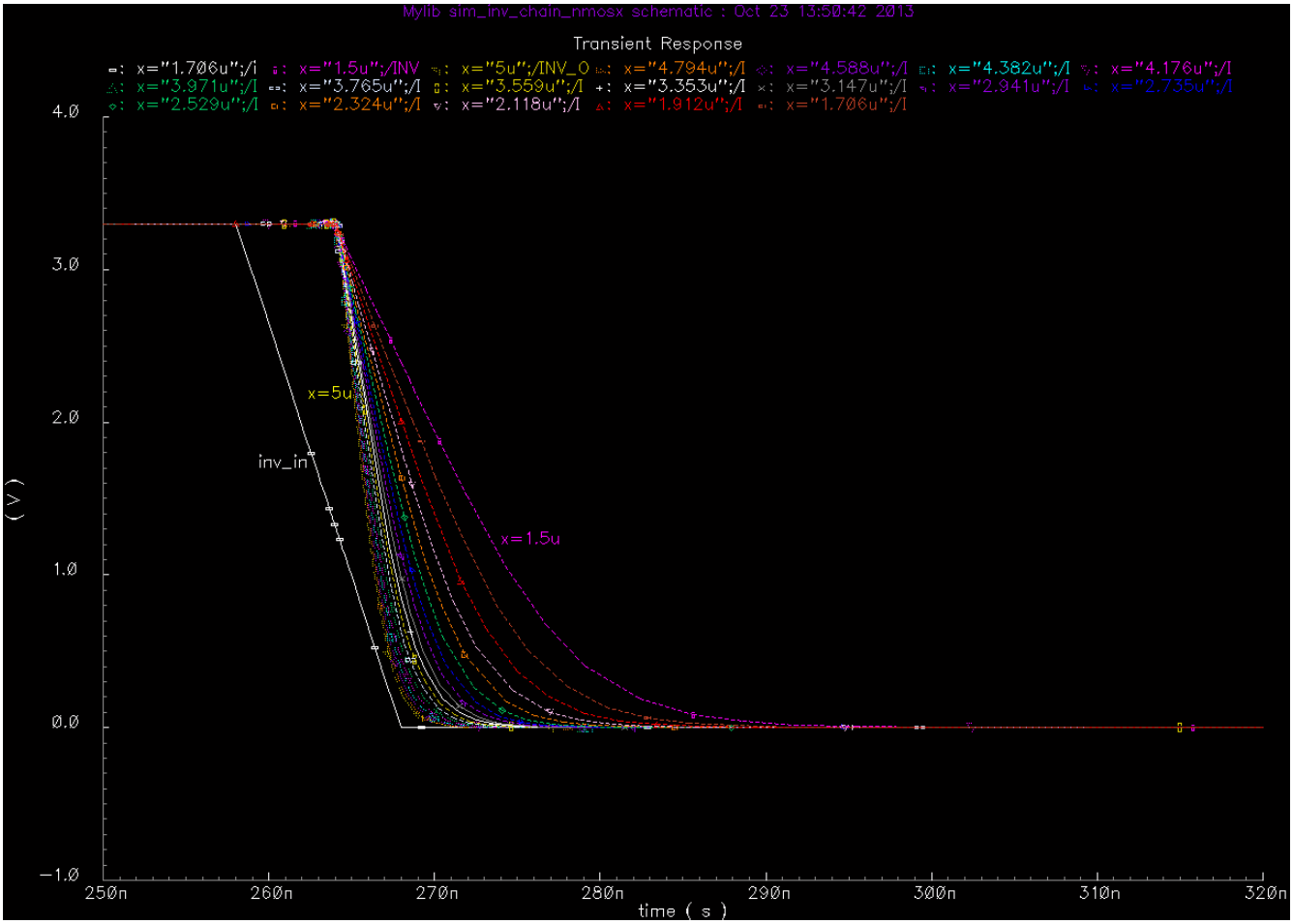

Figure 20. Falling portion of the resulting transient waveforms for sweep of inverter size

Table 3. Rise and fall times as a function of transistor width

NMOS Width (um)	Rise Time (ns)	Fall Time (ns)
5	2.16	2.65
4.794	2.25	2.73
4.588	2.34	2.81
4.382	2.44	2.9
4.176	2.54	2.99
3.971	2.67	3.1
3.765	2.79	3.25
3.559	2.93	3.39
3.353	3.08	3.54
3.147	3.28	3.73
2.941	3.51	3.97
2.735	3.74	4.23
2.529	4.05	4.56
2.324	4.4	4.96
2.118	4.84	5.48
1.912	5.37	6.15
1.706	6.05	7.06
1.5	6.95	8.34

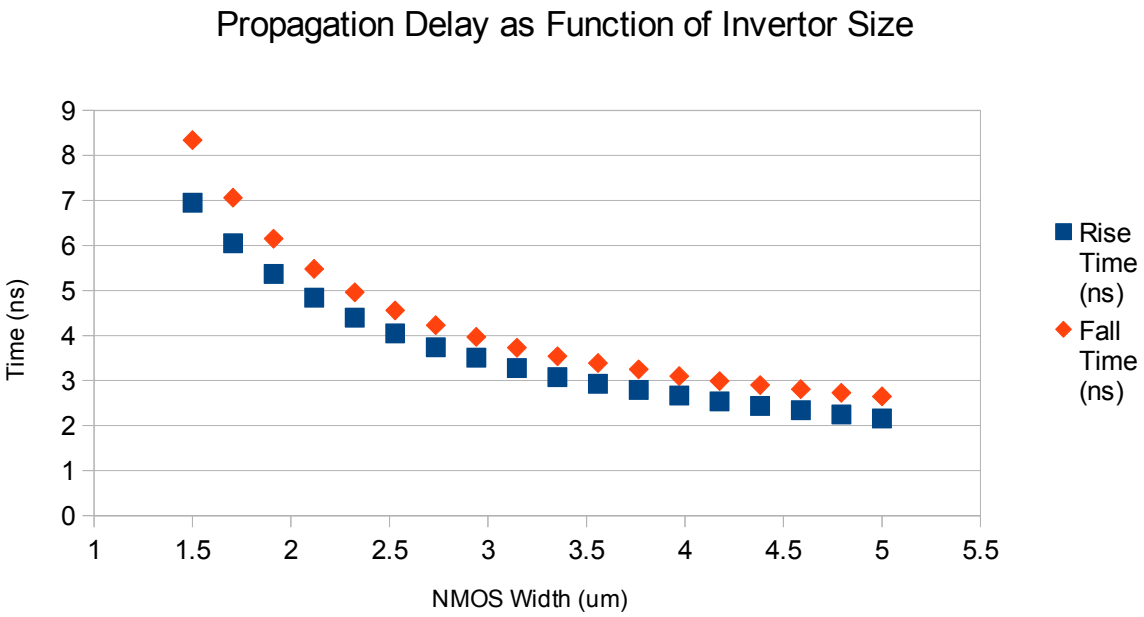

Figure 21. Change in propagation delay as a function of the size of the inverters

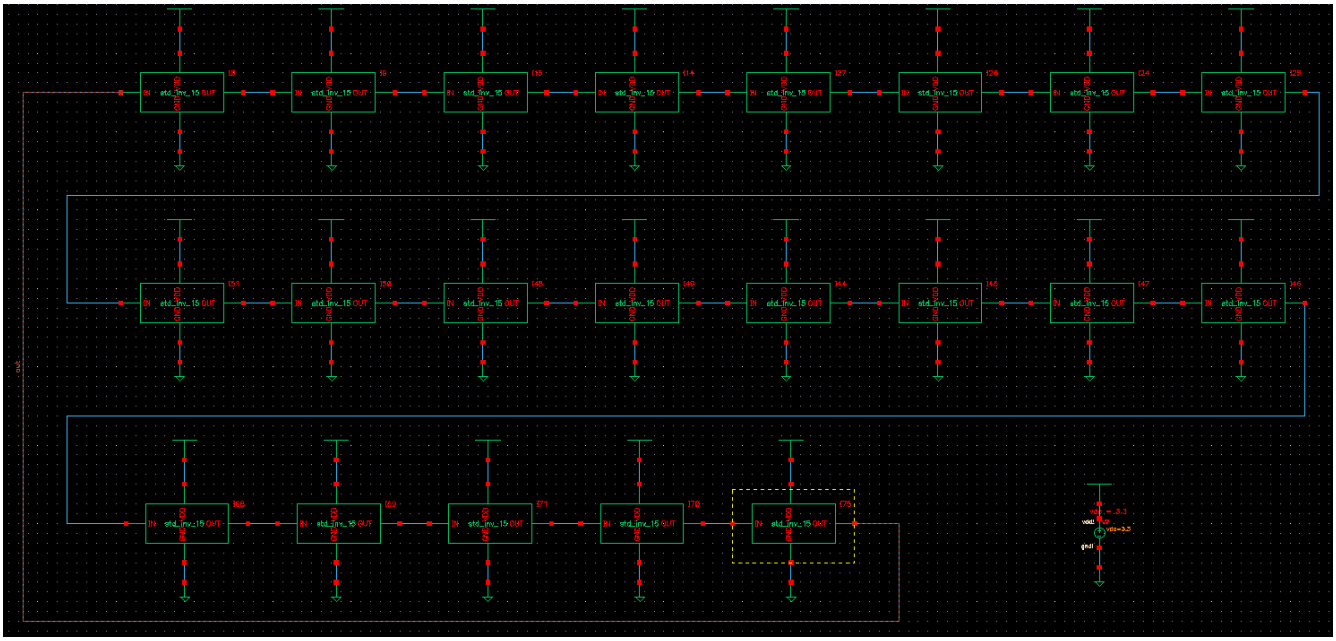

Figure 22. Schematic view of ring oscillator

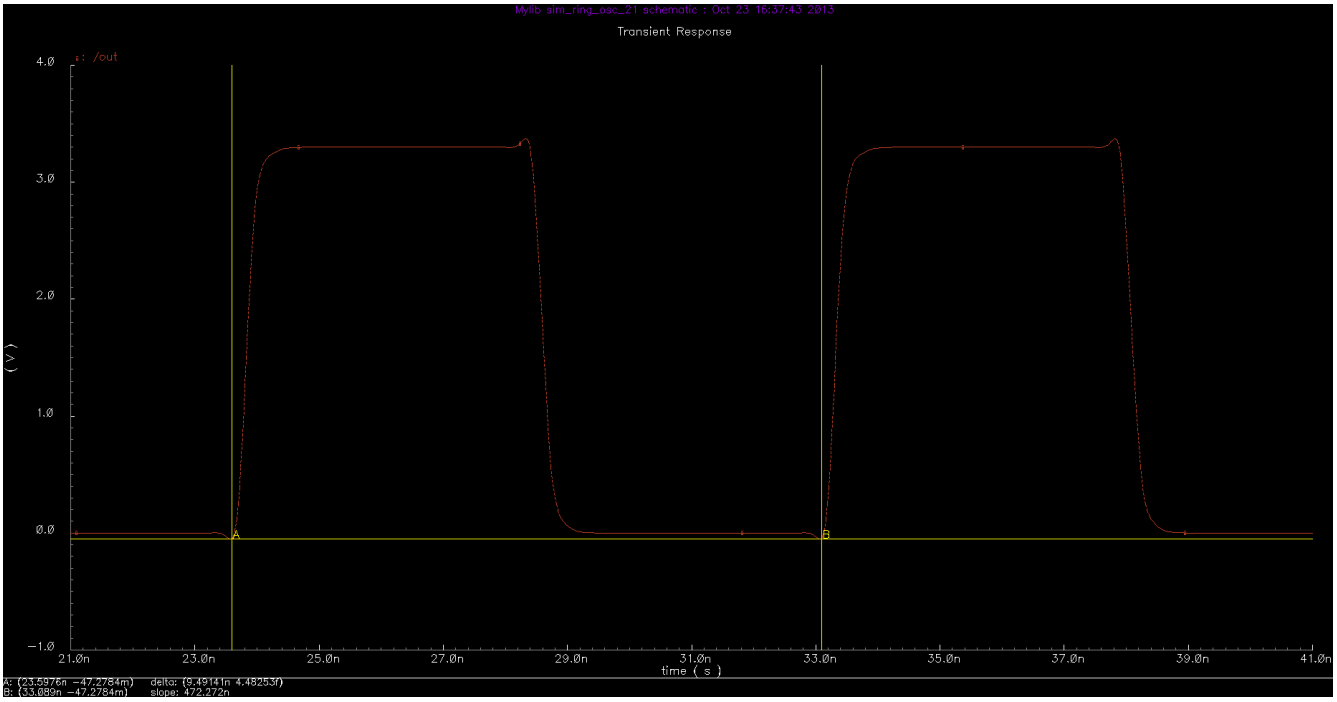

Figure 22. Waveform generated by the ring oscillator showing period = 9.5 ns, freq = 105.4 MHz