Lab Assignment #6

Instructor: Dr. Ioannis Savidis
TA: Ying Teng E-Mail:yt74@drexel.edu

Drexel University
Electrical and Computer Engineering
Nov 6th, 2013 (Wednesday)

1 Objectives

The objectives of this assignment are to learn:

- The design of a one-bit `Full Adder` using CMOS gates;
- The functionality and characteristics of a one-bit `Full Adder`;

2 Assignments

The lab assignment for this week is to design a one-bit `Full Adder`.

- The input bit `A` and the input bit `B` are the two addend bits. The input bit `C` is the carry-in bit. The output bit O_0 and the output bit O_1 are, respectively, the least significant bit and the most significant bit of the result. The logic function of a one-bit `Full Adder` can be presented as follows:

$$O_0 = A \oplus B \oplus C \tag{1}$$

$$O_1 = AB + AC + BC \tag{2}$$

- Design the one-bit `Full Adder` using the cells (`Inverter`, `NAND`, `AND`) and modules (`MUX`) designed in previous labs. An illustration of the gate-level one-bit full adder is shown in Figure 1. Note that the figure is only used as a reference. Your design does not have to be the same as that shown in Figure 1. It is however recommended that you design an *XOR* gate as a standard cell first to reduce routing of wires during layout.

3 Assignment

The lab assignment is due next Friday (Nov 15th). The report should include:

1. The schematic and the layout view of the one-bit `Full Adder`;
2. Simulation results verifying the functionality of the one-bit `Full Adder` for both the schematic and the layout;
3. Timing information of the `Adder` (propagation delay, rise/fall time).

`NOTE:` Pay attention when using standard cells for your designs. In addition to the correctness and functionality of the design, good, compact wiring will be an important aspect of your evaluation.

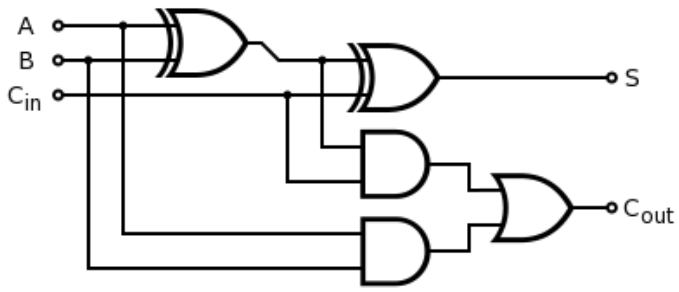

Figure 1: A schematic of the one-bit *Full Adder*.