Drexel University
Electrical and Computer Engineering Department

ECEC 471
Introduction to VLSI Design

Lab Assignment 6
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Lab 6 completes schematic and layout based simulations to characterize single bit full adder functionality. Special attention is paid to timing characteristics such as propagation delay and rise/fall time.

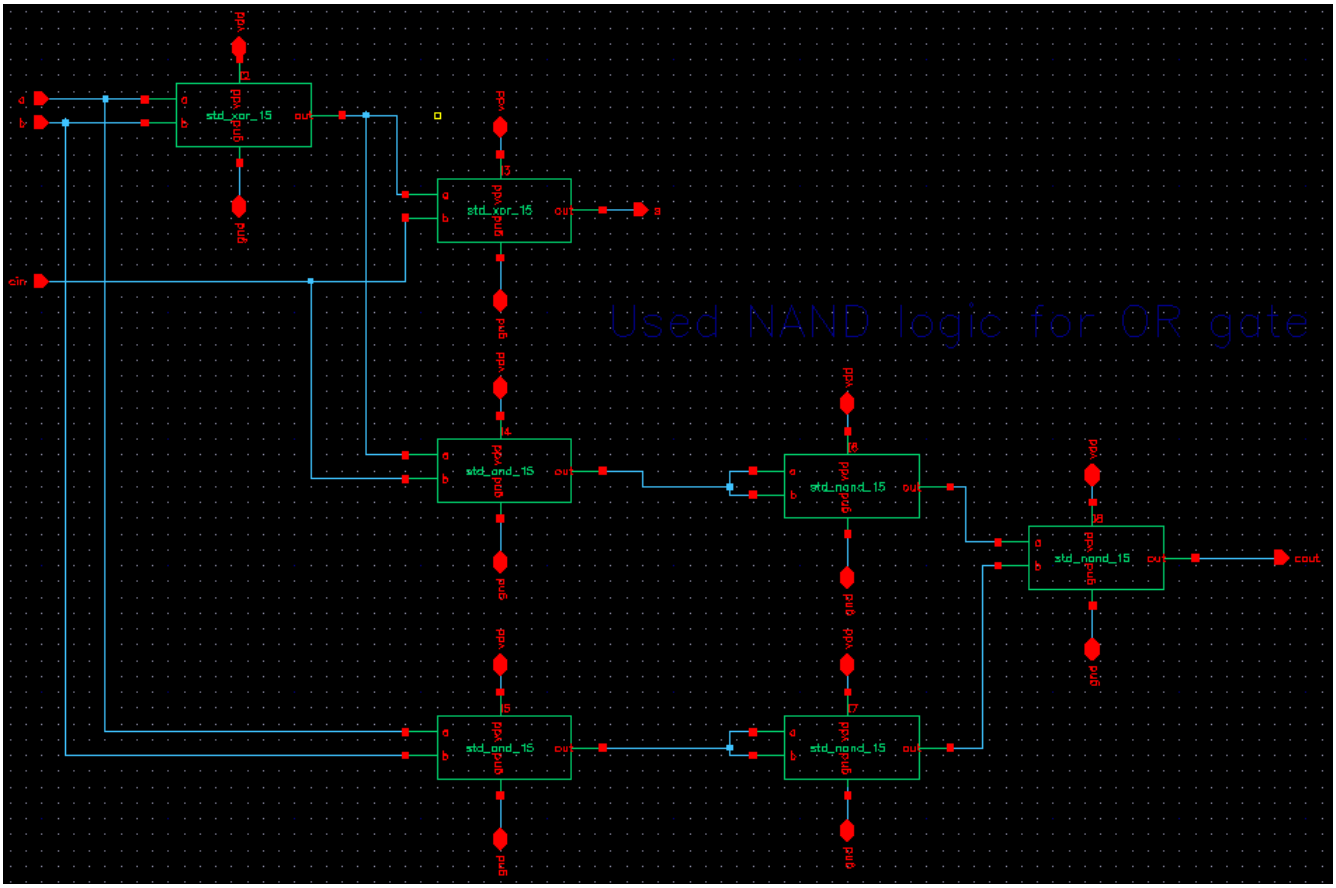

Fig. 1. Schematic view of the one-bit Full Adder.

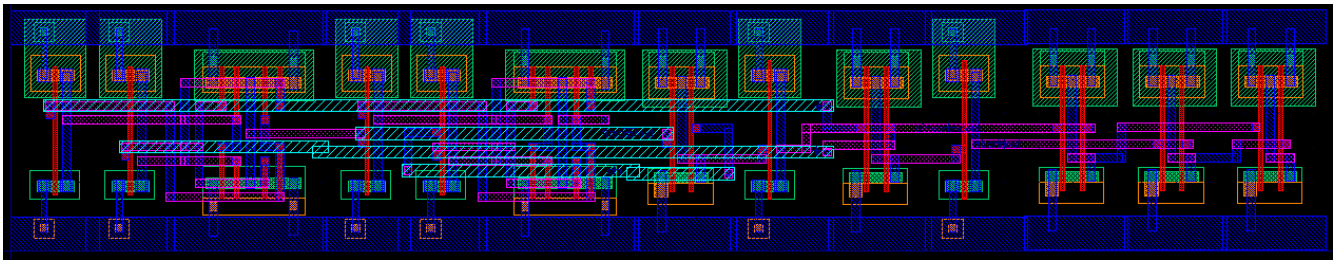

Fig. 2. Layout view of the one-bit Full Adder. (Full view)

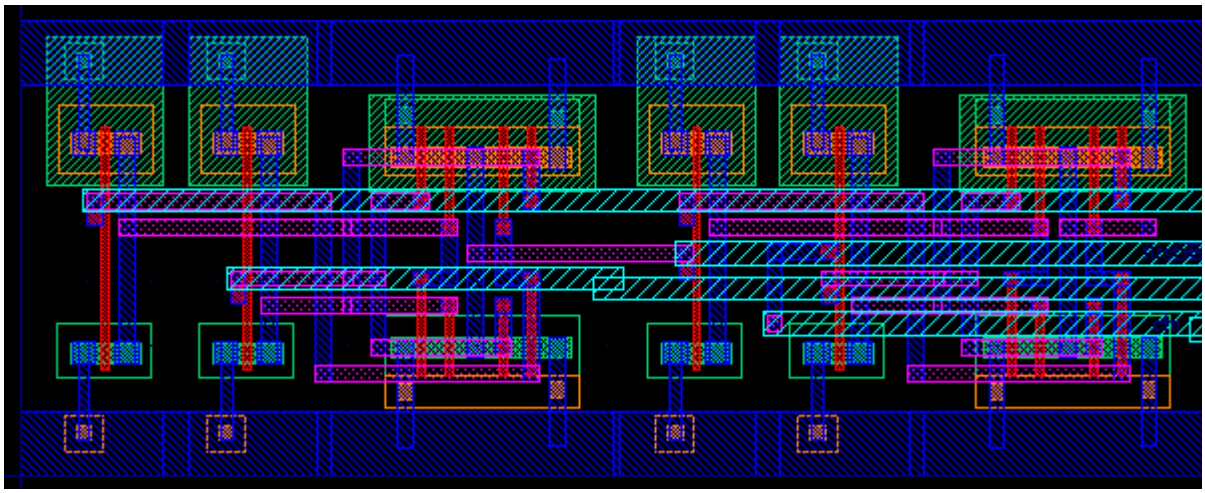

Fig. 3. Layout view of the one-bit Full Adder. (First half / left side view)

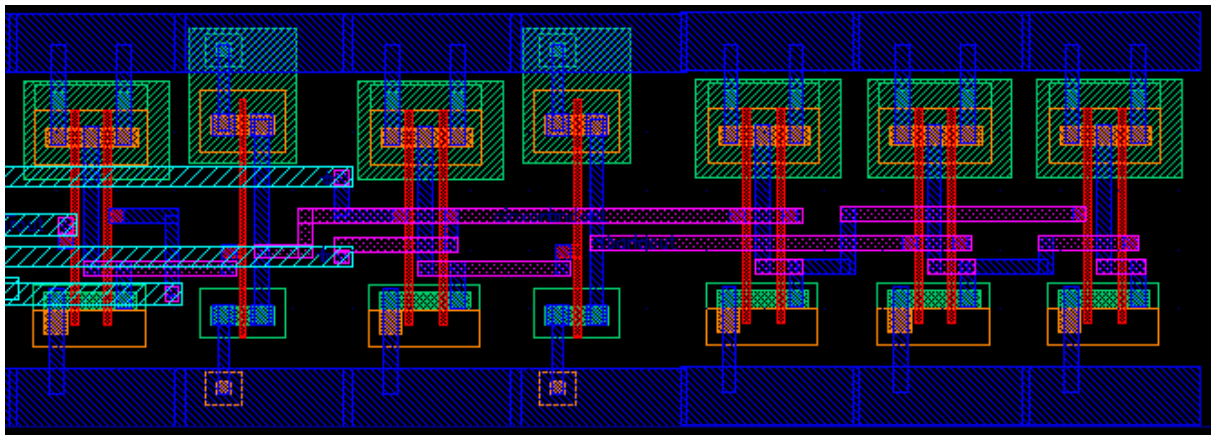

Fig. 4. Layout view of the one-bit Full Adder. (Second half / right side view)

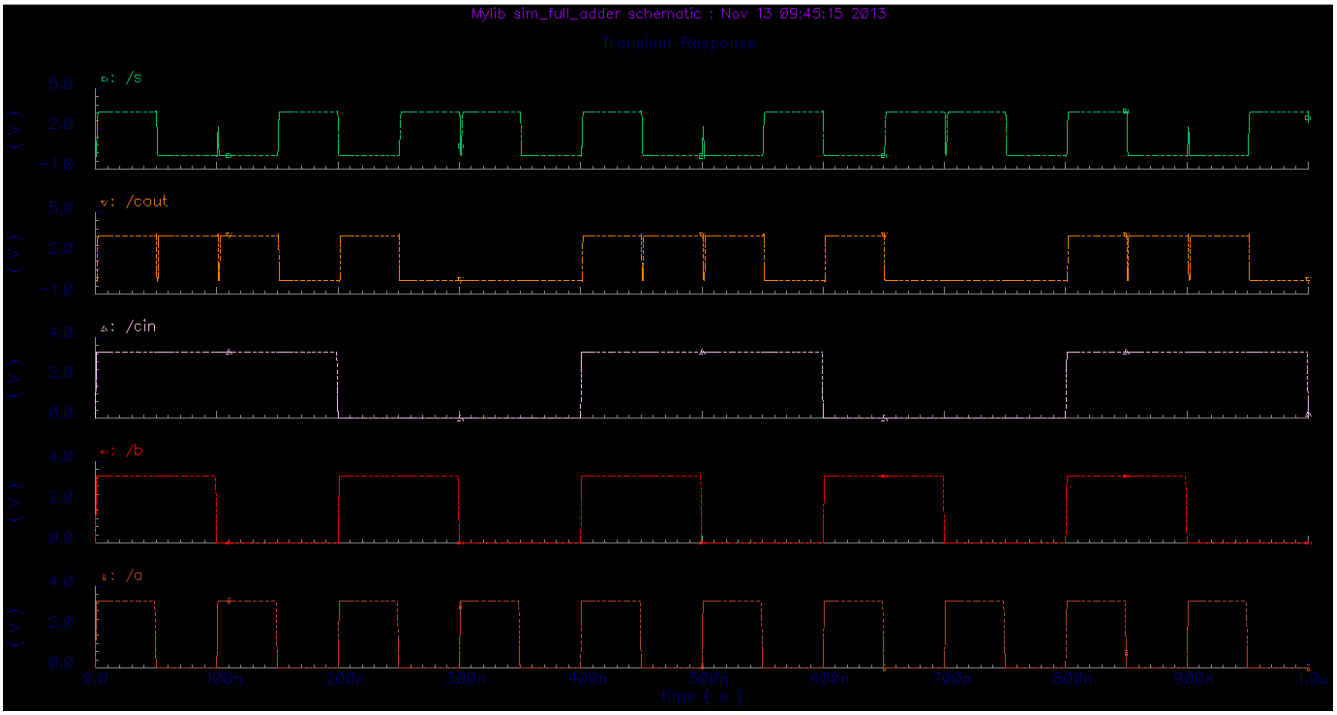

Fig. 5. Simulation results verifying the functionality of the one-bit Full Adder for schematic.

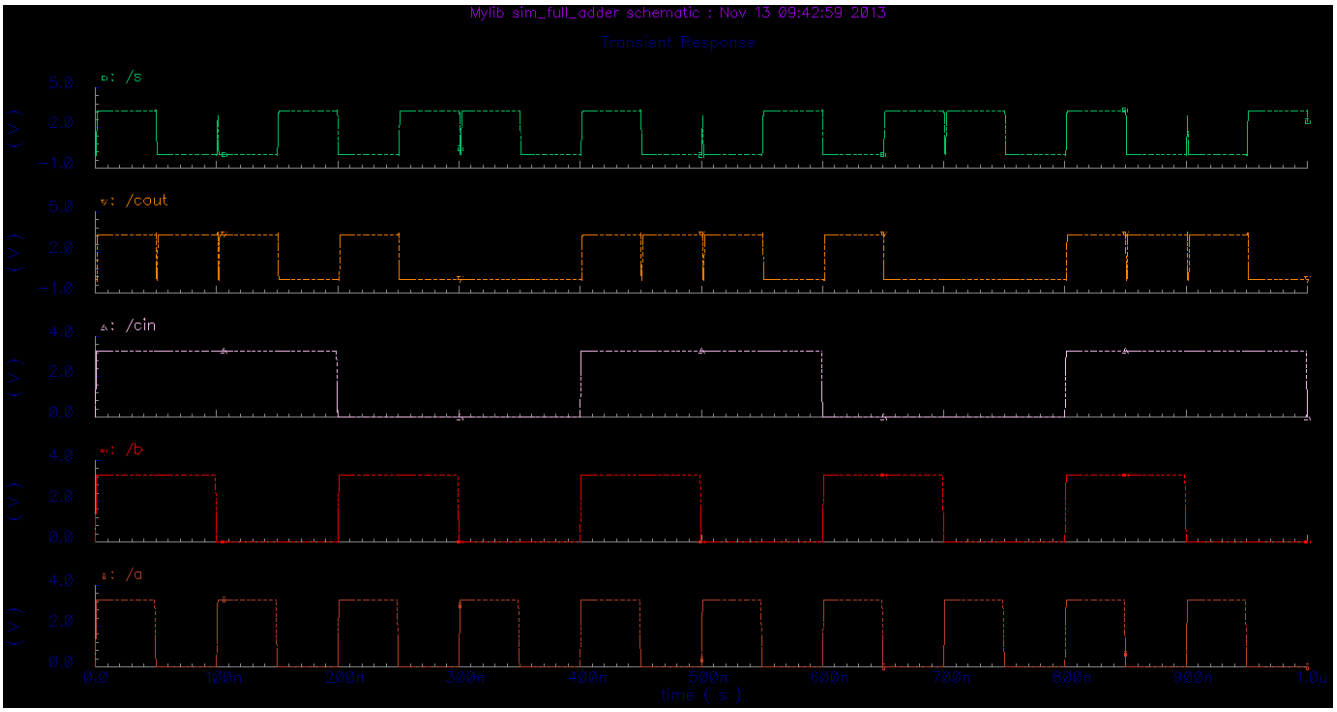

Fig. 6. Simulation results verifying the functionality of the one-bit Full Adder for layout.

Per Prof. Savidis, a subset of possible input patterns were examined. The table below contains the input patterns characterized and timing information. 'R' indicates a rising signal, 'H' a high signal, 'F' a falling signal, and 'L' a low signal. Zeros in the propagation delay columns indicate that the input signal specified was not switching at the time or was not critical to the propagation delay (i.e. output transition occurred before input transition).

Table. 1. Timing Information of the Adder
(Note: The period of signals A, B, and CIN, are 100ns, 200ns, 400ns respectively)

					Propagation Time (ns)				**Transition Time (ps)**	
A	**B**	**CIN**	**S**	**COUT**	**Last Output to Transition**	**A**	**B**	**CIN**	**S**	**COUT**
R	R	R	R	R	COUT	1.097	1.097	1.097	680.448	241.330
F	H	H	F	H	S	1.057	0.000	0.000	479.065	0.000
F	L	H	R	F	COUT	1.586	0.000	0.000	725.405	208.373
R	R	F	F	R	COUT	1.096	1.096	2.093	374.658	239.236
F	H	L	R	F	S	1.409	0.000	0.000	673.345	211.265
F	L	L	F	L	S	1.254	0.000	0.000	369.260	0.000

Table. 2. Timing Information of the Adder
(Note: The period of signals A, B, and CIN, are 400ns, 200ns, 100ns respectively)

					Propagation Time (ns)				**Transition Time (ps)**	
A	**B**	**CIN**	**S**	**COUT**	**Last Output to Transition**	**A**	**B**	**CIN**	**S**	**COUT**
R	R	R	R	R	COUT	1.107	1.107	1.107	677.684	245.437
H	H	F	F	H	S	0.000	0.000	0.596	379.196	0.000
H	L	F	R	F	COUT	0.000	0.000	0.836	687.703	206.646
F	R	R	F	R	COUT	2.874	1.880	1.880	514.099	305.658
L	H	F	R	F	COUT	0.000	0.000	0.829	673.390	206.802
L	L	F	F	L	S	0.000	0.000	0.596	386.891	0.000