# INVERTER TUTORIAL

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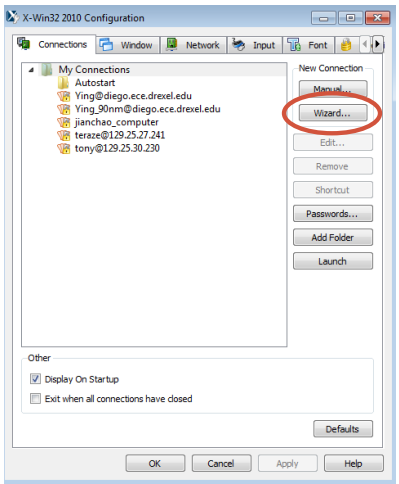
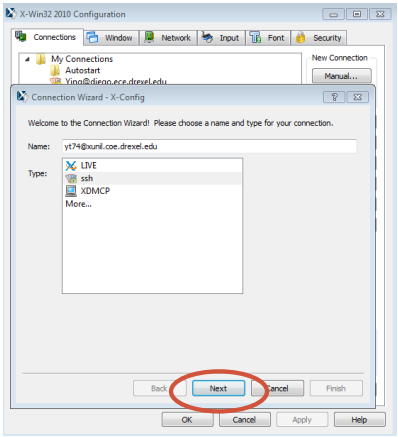
## 1 Login to **xunil**

- Start X-win32 and click on “Wizard”



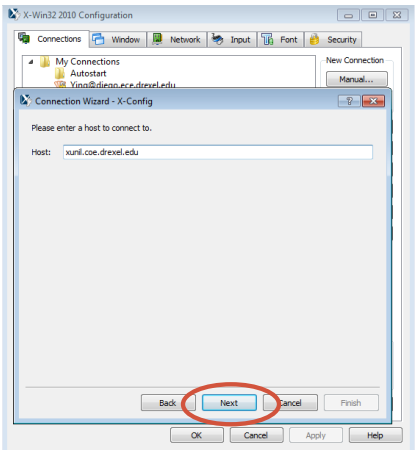
# 1 Login to **xunil**

- Name your server. This name should be easy for you to recognize.
- Type: select **ssh**
- Hit **next**



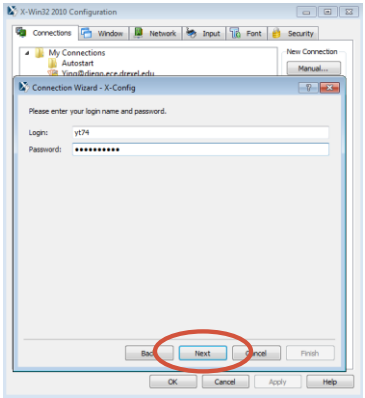

# 1 Login to **xunil**

- Input the server's address: **xunil.coe.drexel.edu**
- Hit **next**



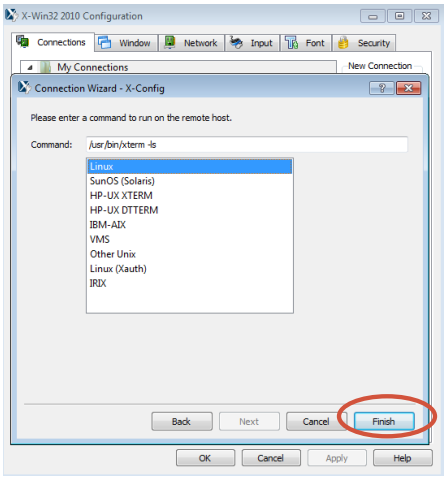
# 1 Login to **xunil**

- Input your **username** and **password**
  - Username: **drexelone username**
  - Password: **drexelone password**
- Hit **next**



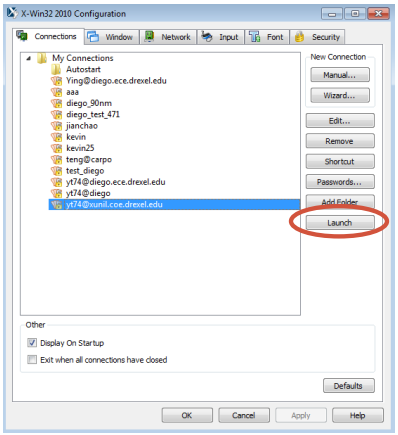

# 1 Login to **xunil**

- Choose **Linux**
- Hit **finish**



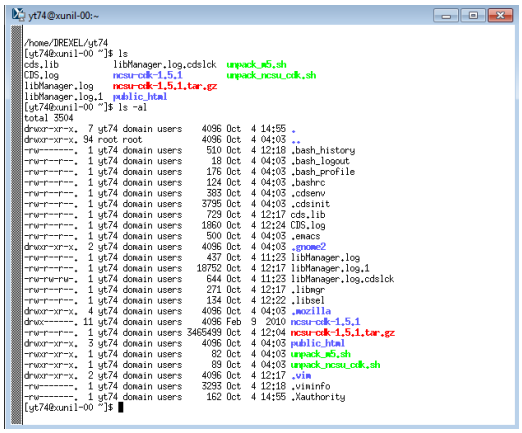
# 1 Login to **xunil**

- Come back to the **connections** panel and choose the connection which has been just created.
- Hit **launch** to login to xunil



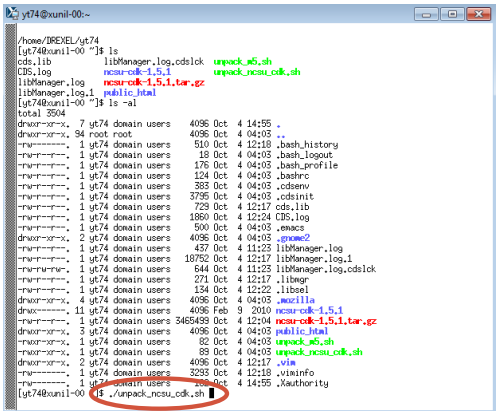

# 1 Login to **xunil**

- Linux commands:
  - pwd: print working directory
  - cd: change directory
  - ls: list



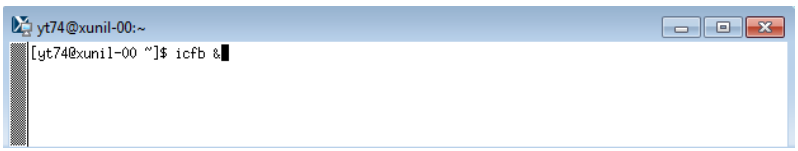
# 1 Login to **xunil**

- Run unpack_nesu_cdk.sh by command
- ./unpack_ncsu_cdk.sh
- Hit enter



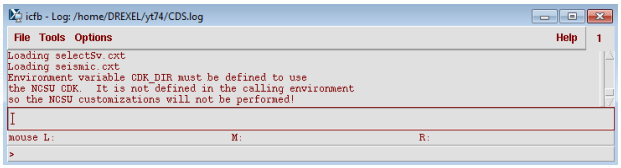

# 2 Using Cadence simulator

- Start cadence: type "**icfb &**" in the terminal, then hit "enter".
- The symbol "&" indicates the simulator is launched in the background. After launching Cadence, we can still input commands in the terminal. On the other hand, if the Cadence simulator is launch with command "**icfb**", we cannot type any command in the same terminal window until exit from Cadence.

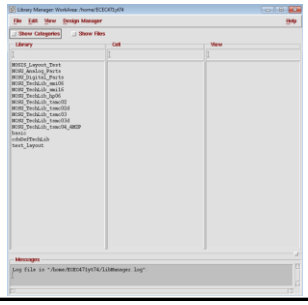


# 2.1 Panels in icfb

- CIW (Command interpreter window)

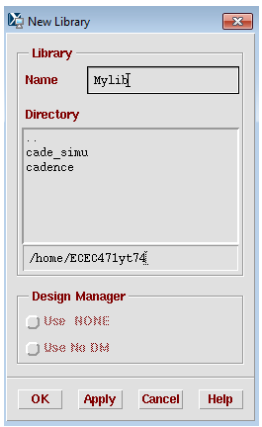



- In the CIW, select **Tools ->Library Manager…** The **"library manager"** will pop up.



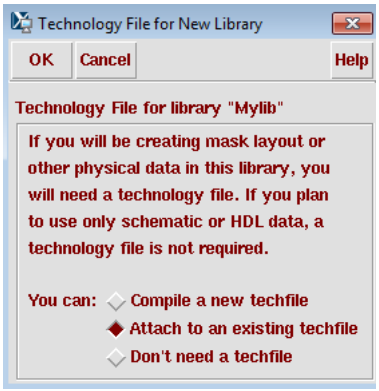
# 2.2 Create a new library

- 2.2.1 Create a new library
- In library Manager window, choose "**File-> New-> library…**"
- Enter the name of your library in the "New Library" window, such as: Mylib
- "/home/ECEC471yt74" shows the directory where your library is created.
- Hit "OK"



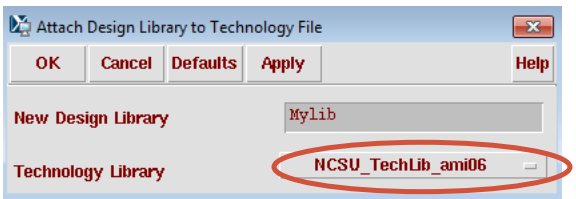
# 2.2 Create a new library

- After you hit “OK”, the **“Technology File for New Library”** will pop up.
- Select **“Attach to an existing techfile”.**
- Hit **“OK”.**



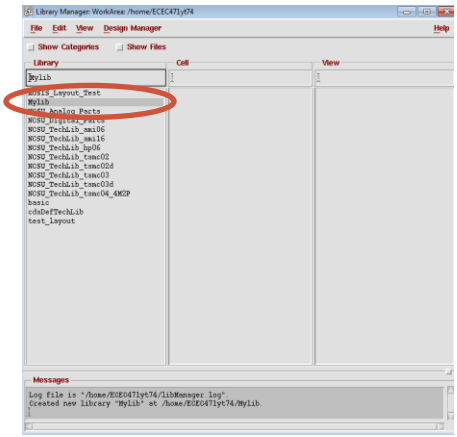

# 2.2 Create a new library

- After you hit “OK”, the **“Attach Design Library to Technology File”** will pop up.
- Select **“NCSU_TechLib_ami06”.**
- Hit **“OK”.**



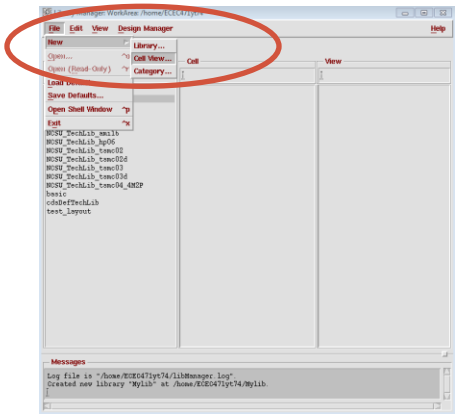
# 2.2 Create a new library

- The new library “Mylib” is created and you can see it in the library manager.



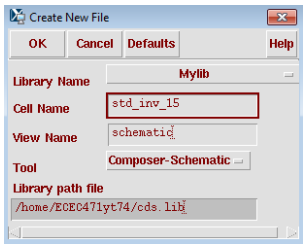

# 2.3 Create a new schematic view

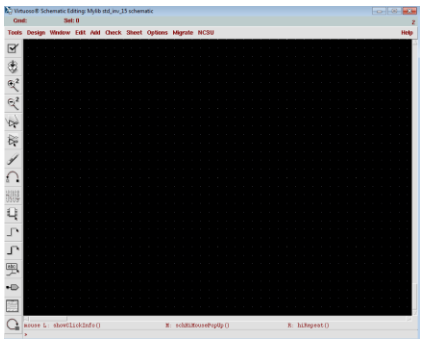
- In the “Library Manager”, select “Mylib” in the “Library” column.
- Click on “**File-> New->Cellview…**”



# 2.3 Create a new schematic view

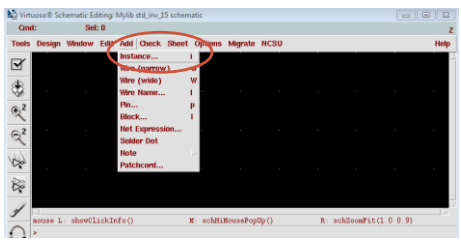
- The "**Create New File**" window will pop up.
- Library name: Mylib
- Tool: Composer-Schematic
- Hit "OK"
- Schematic window pops up.

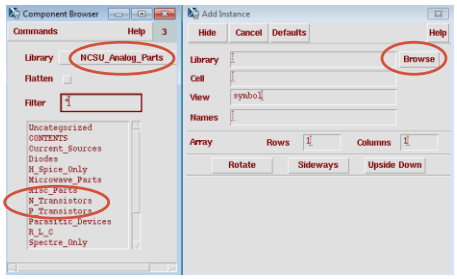


# 2.4 Create a schematic view of inverter

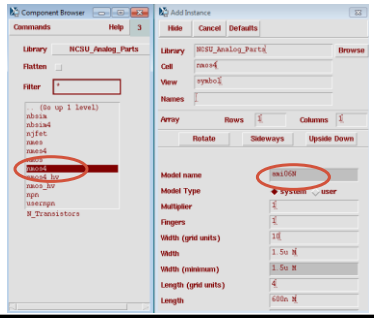
- Add instance:
  - To add an instance into your schematic, e.g. an NMOS device, activate the schematic window, click "Add-> instance…"(or type i)
  - The "add instance" and "component Browser" dialogue boxes appear.
  - If the "Component Browser" does not appear, click on "browse" in the "Add instance" dialogue box to start it.



# 2.4 Create a schematic view of inverter

- In “Component Browser”:
  - Choose library “**NCSU_Analog_Parts**”.
  - Click on **N_Transistors** (once) to descend into this folder.
  - Choose **nmos4** as your NMOS model type.
  - Hit on nmos4 once, then all the parameters of this model will appear in the “Add instance” window.
  - Check the model name: **ami06N**

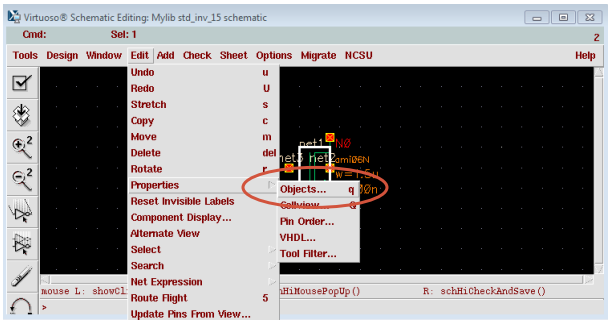



# 2.4 Create a schematic view of inverter

- To place this instance into your schematic:
  - Activate schematic window, click left button of your mouse.
  - Note that in Cadence schematic composers and layout editor, a command **WILL NOT** terminate until the user terminate it or start a new command. After you place the NMOS instance, you can see there is another NMOS instance ready to be place. To terminate the current operation(which is add instance), press **ESC**.

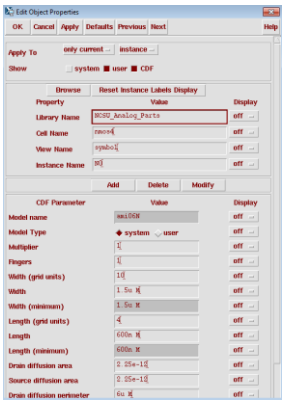
# 2.4 Create a schematic view of inverter

- Set properties of the instance
  - Activate your schematic window.
  - Select the object by clicking on it
  - Click Edit -> properties-> Objects…(or type q)



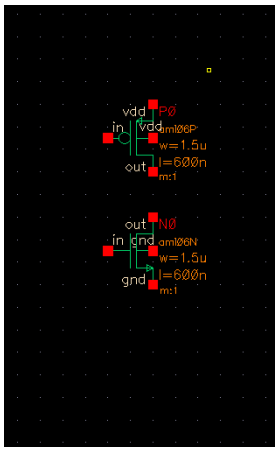

# 2.4 Create a schematic view of inverter

- The "**Edit Object Properties**" window will pop up.
- You can change the length or width of the transistor.
- PMOS is added into the schematic in a similar way.



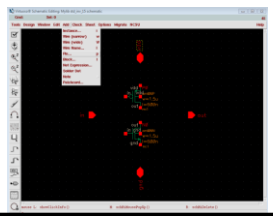
## 2.4 Create a schematic view of inverter

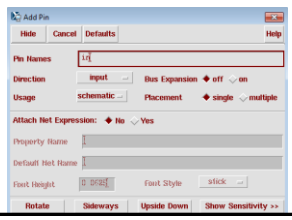
- After adding the PMOS and NMOS, the schematic should look like this:




## 2.4 Create a schematic view of inverter

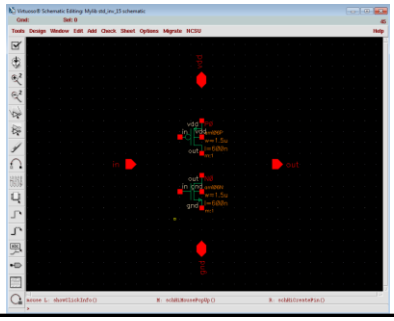
- Adding pins and labels:
  - To specify the input/output behavior of the circuit, input/output pins are added.
  - Click on "**Add->Pins…**"(or type p) in the schematic window.
  - The "Add Pin" dialogue box will appear
  - Choose **Direction**(e.g. input) and **enter the pin name**(e.g. in).
  - Click OK.
  - Place the pin in the schematic window the same way as place an instance.





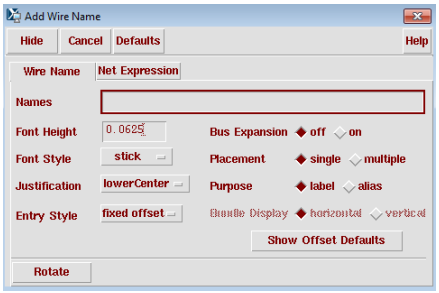
## 2.4 Create a schematic view of inverter

- Pin name: in  Pin type: input
- Pin name: out  Pin type: output
- Pin name: vdd  Pin type: inputoutput
- Pin name: gnd  Pin type: inputoutput
- After adding pins, the circuit looks like this:



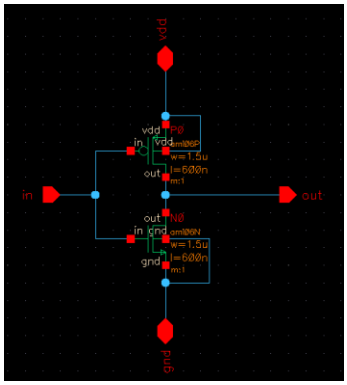
## 2.4 Create a schematic view of inverter

- Add label to a wire is similar as adding pins.
  - Click on "**Add->Wire Name…**"(or type l) in the schematic window, the "**Add Wire Name**" window will appear
  - Enter the name for a piece of wire and attach to a wire in the schematic window.



# 2.4 Create a schematic view of inverter

- Add wire:
  - Click on “Add ->Wire(narrow)” (or type w) in the schematic window.
  - The “Add Wire” dialogue box will appear. Hit “Hide” to go back to the schematic window.
  - A diamond shape will appear on the mouse arrow when the mouse arrow in on the port of an instance(red square) or a pin. Click once as the starting point of the wire, release the mouse, and click once at another port as the ending point of this piece of wire.




# 2.4 Create a schematic view of inverter

- Check and save your design
  - Click on “Design-> Check and Save”.
  - Check the CIW to see whether there is any errors in your design.

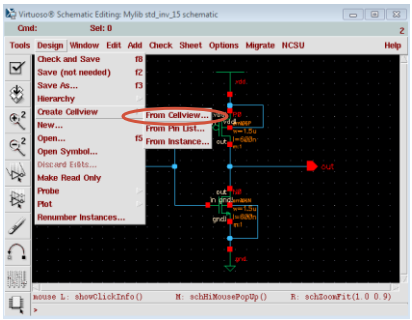
- Bindkeys:
  - i: Add instance
  - q: Edit properties
  - w: Add wire
  - p: Add a pin
  - l: label a wire
  - z: zoom in
  - Z: zoom out by 2X
  - f: fit the schematic in your schematic window
  - right mouse button: repeat last command

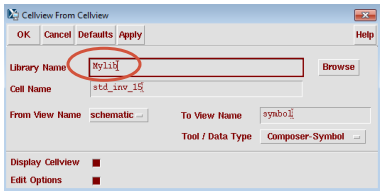
# 2.5 Create a symbol view of inverter

- Symbols are created for hierarchical design. At a higher level of abstraction, we would like to use a symbol to replace the details of a cell. Thus, a symbol of a cell should define all the inputs and outputs of that cell. Next, we introduce how to create a symbol from an existing schematic.

# 2.5 Create a symbol view of inverter

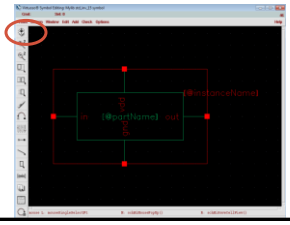
- Click on "**Design-> Create Cellview-> From Cellview**".
- The "**Cellview From Cellview**" window will pop up. We can use the default setup in this window to create the symbol.
- Hit "OK"



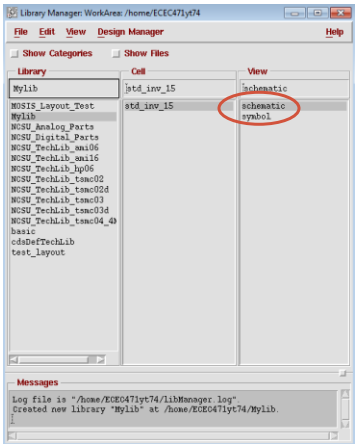
# 2.5 Create a symbol view of inverter

- Another window will pop up contains a default symbol picture. It has a red box that encloses the green colored inverter symbol. This red box defines the actual size a symbol will occupy, if you were to use this inverter in another design. You can change the size of this box. It is good custom to exactly fit the symbol within the red box. The red square dots indicate the pin connections. [@InstanceName] and [@PartName] are display variables, which you may delete or keep. The following picture shows the symbol. If you need to do some modifications to the symbol, remember to click “check and save”. The red circle is the quick button for “check and save”.




# 2.5 Create a symbol view of inverter

- Now if you go back to “Library Manager” window, the cell “std_inv_15” now has two views: schematic and symbol.



## 2.6 Simulation with spectre

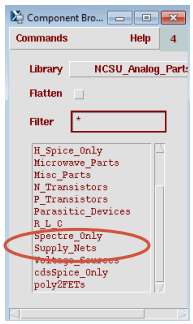
- Spectre is a Cadence version of the SPICE circuit simulator. The syntax of Spectre is compatible with SPICE simulation. By Comparison to Verilog-XL, Spectre lets you simulate transient behavior of your circuit at the transistor level. Next, we will perform transistor level simulations for the inverter schematic and observe its transient and DC behaviors.

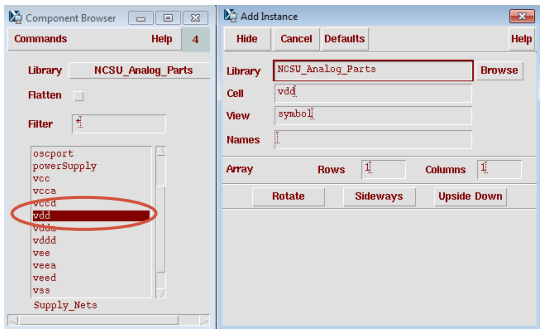
## 2.6 Simulation with spectre

- Create a new cell "**sim_inv**" in the library you created (In library manager) with "schematic" view, using “File->New->CellView” on the library manager window.
- Add the following components into your "**sim_inv1**“ schematic:
  - The symbol of “**std_inv_15**” from your own library.
  - The symbols for **VDD and GND** from “NCSU_Analog_Parts”.
  - The symbol for **vdc, vpulse** from “NCSU_Analog_Parts”.
  - The symbol for **cap** from “NCSU_Analog_Parts”.
- Connect the circuit.

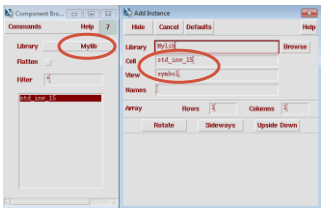
# 2.6 Simulation with spectre

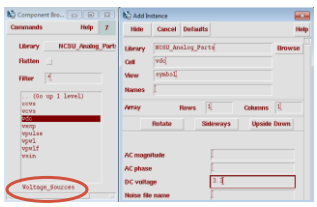
- Adding supply nets
  - The global supply nets (such as VDD and GND) are in the **NCSU_Analog_parts** library, **supply_nets** folder.
  - Add these supply nets into the schematic using the same way as adding NMOS and PMOS.

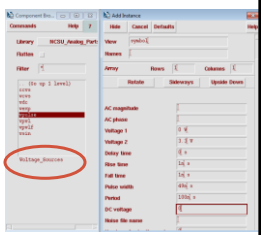


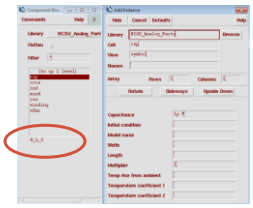



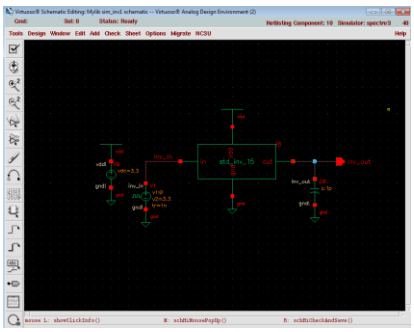

# 2.6 Simulation with spectre





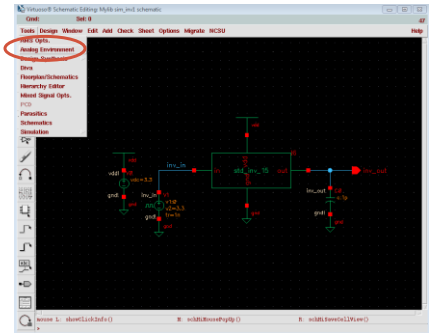


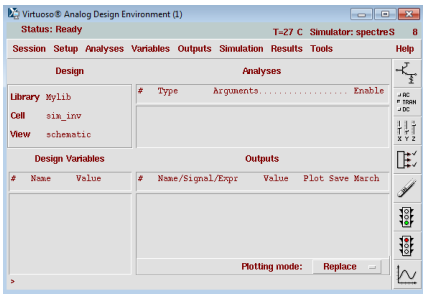




# 2.6 Simulation with spectre

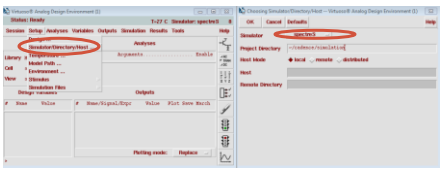
- Simulation in Analog Environment
  - Activate the schematic window of sim_inv.
  - click on "**Tools->Analog Environment**".

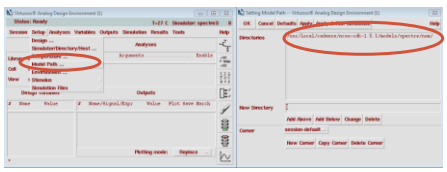





# 2.6 Simulation with spectre

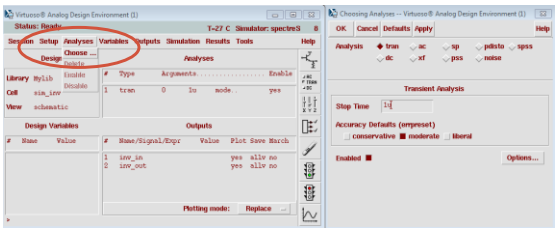
- Verify simulation settings of the "Analog Design Environment".
  - Click on "**Setup->Simulator/Directory/Host…**", make sure the simulator is "**SpectreS**".
  - Click on "**Setup->Model Path**", make sure the right model files are included for simulation.





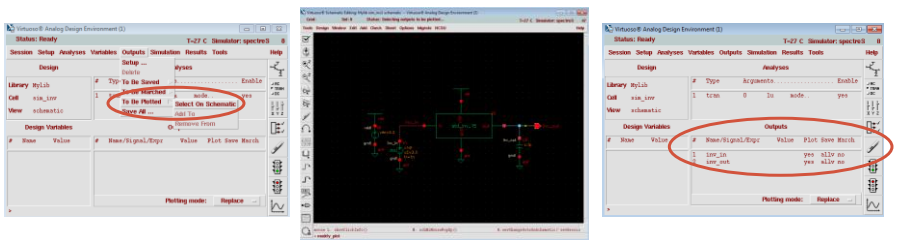
# 2.7 Transient Simulation with spectre

- Choose the simulation type.
- Click on "**Analyses->Choose…**".
- "**tran**" is chosen as the default analysis. Write the "Stop Time" of approximately 10cycles.
- Click OK.



# 2.7 Transient Simulation with spectre

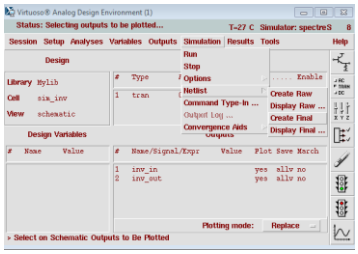
- Now, it is time to determine the nodes that will be observed.
- Click on "**Outputs->To Be Plotted->Select on Schematics**".
- This will let you choose the nodes to be observed. Focus the schematics window and click on the wires at the input and output of the inverter.

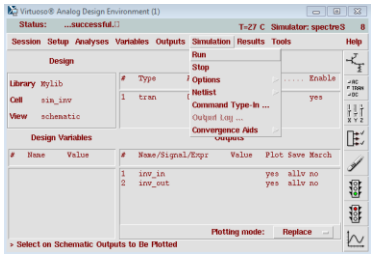


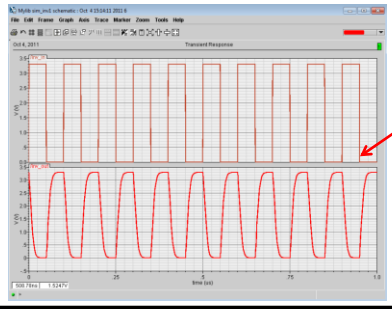
# 2.7 Transient Simulation with spectre

- There are 2 types of signals to be observed after the simulation: voltage and current.
- If you click on **wire**, you select that wire's **voltage** as the observed signal. If you click on the **node** like the input of the inverter, you select the **current** of that node as the observed signal. You see a circle on that node. **You will work on voltage here.**
- Once this is done, go to the Analog Design Environment Window and click "**Simulation->Netlist->Create Final**".
- Then the netlist of the schematic is extracted. Then click "**Simulation->run**". Wait for a few seconds and after the simulation is finished, a waveform window will automatically appear.

# 2.7 Transient Simulation with spectre



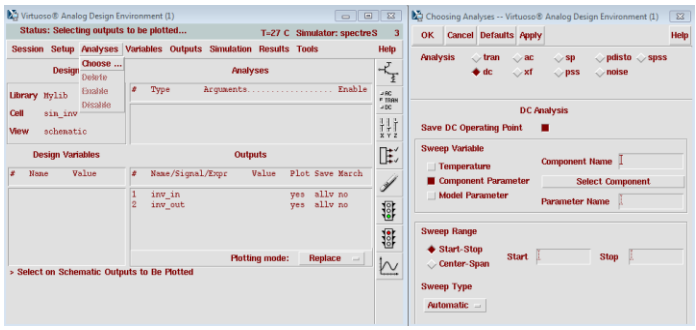
Set background white
Set the line as bold

# 2.7 DC Simulation with spectre

- DC simulation is used to analyze the performance of the output of the inverter along with the changing its input.
- The purpose of doing DC simulation is find the point where **inv_out=inv_in=vdd/2** through adjusting the size of PMOS and NMOS. When reaching this point, the inverter is called a **symmetrical inverter**.

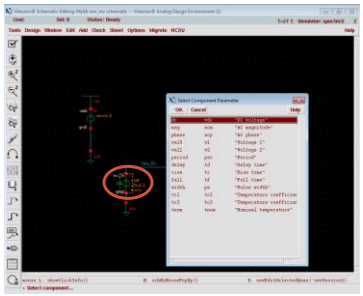
# 2.7 DC Simulation with spectre

- Go to the Analog Design Environment window, click on Analyses->Choose…, chosen “DC” as the simulation type.
- “Sweep Variable”, choose “**Component Parameter**”.



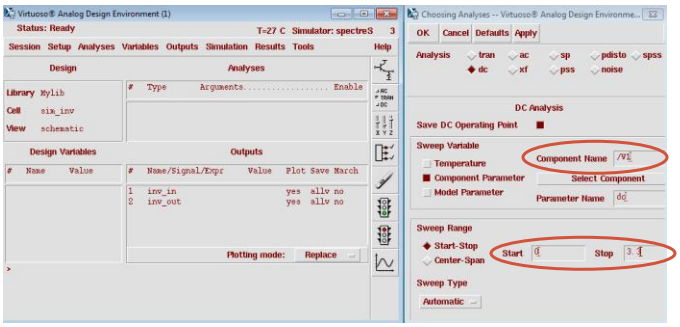
# 2.7 DC Simulation with spectre

- Click on "**Select Component**" will activate the schematic window.
- Click on the input voltage source, then the "**select component Parameter**" window will pop up.
- Choose "**DC**". Hit "OK".



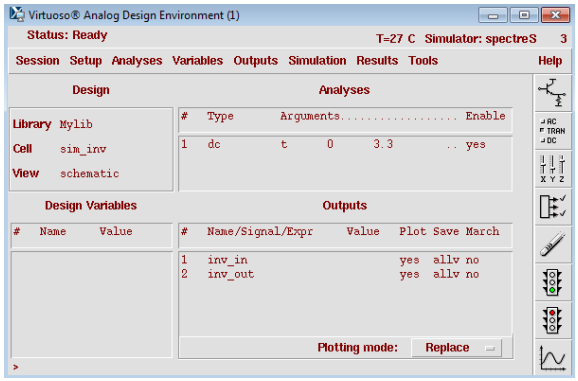
# 2.7 DC Simulation with spectre

- Now the "Component Name" is the input source of the inverter and the "Parameter Name" is "DC".
- We also need to set the "Sweep Range". Let the simulator the sweep the input voltage from "0v—3.3v".



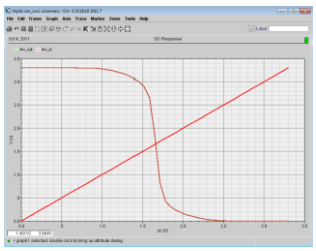
# 2.7 DC Simulation with spectre

- Now the Analog Design Environment window looks like this:




# 2.7 DC Simulation with spectre

- Once this is done, click "**Simulation->netlist->Create Final**" to extract the netlist;
- Click on "**Simulation->Run**" to run the simulation.
- Wait for a few seconds and after the simulation is finished, a waveform window will automatically appear.
- You can put a marker at the crossing point of input and output voltage of the inverter.

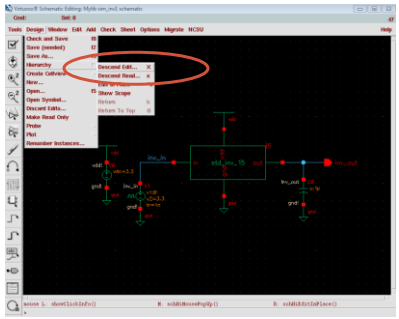


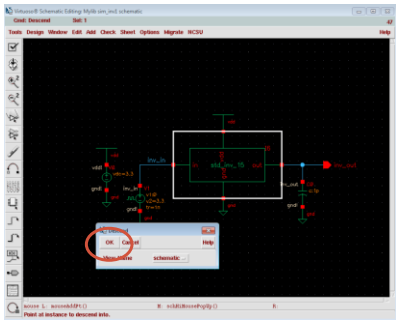
## 2.8 Find the symmetrical inverter

- In order to build a symmetrical inverter, we need to adjust the size of the MOSFET. Since only the ratio of PMOS width and NMOS width affect the performace of the inverter, here, we choose only modify the width of PMOS while keep the width of NMOS unchanged.
- How do we choose a proper number for the width of PMOS?
- We will set the width of PMOS as a variable, and assign a bunch of numbers to it to run simulations and pick one fits our requirements best to be the desired width of PMOS.

## 2.8 Find the symmetrical inverter

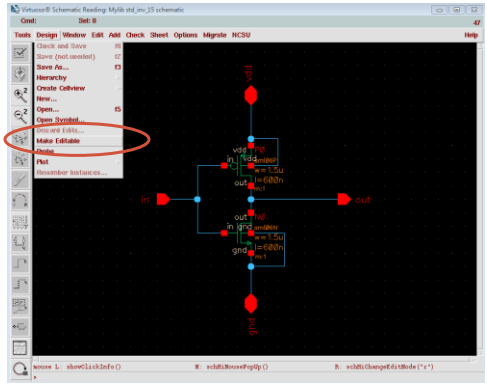
- Go back to the schematic window, select the inverter block, click on "**Design->Hierarchy->Descend Edit…**".
- Then the "Descend" window pops up. Hit "OK" will descend you to the lower level schematic of this circuit, which is the schematic of the inverter we have just build.





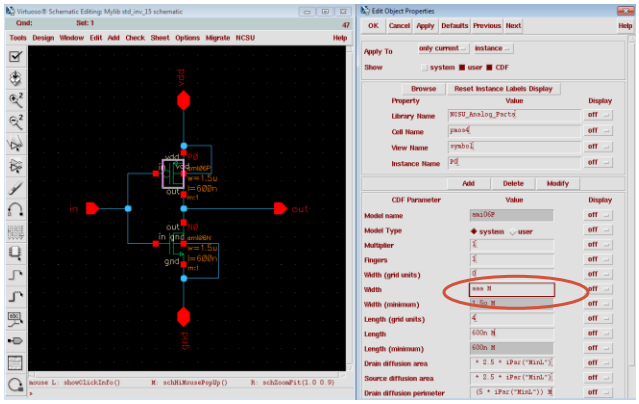
# 2.8 Find the symmetrical inverter

- If the left quick buttons are greyed, you need to hit “Design->Make Editable” to activate the schematic in this level. This is a default setting for protecting the lower level circuits.



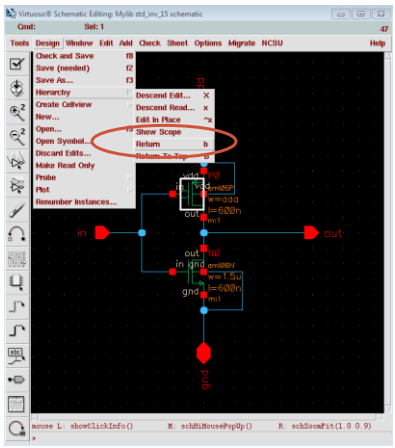
# 2.8 Find the symmetrical inverter

- Select the PMOS and hit “q” to edit its property.
- Hit “OK”.
- Hit “check and save” (every time you make modifications).



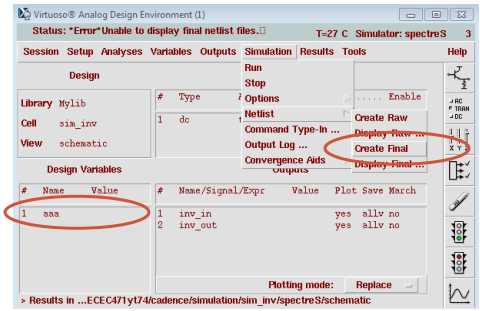
# 2.8 Find the symmetrical inverter

- Then hit “Design->Hierarchy->Return” or “b” to return to the upper level. In the upper level, hit “check and save” again.



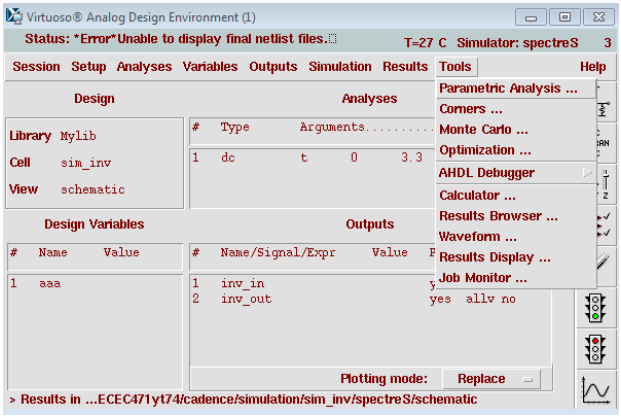

# 2.8 Find the symmetrical inverter

- Now we begin to do the simulation,
- Go to the “Analog Design Envionment” window, go to “Simulation->netlist->create final”.
- After extracting the netlist, “aaa” is listed in the “design variables” table.



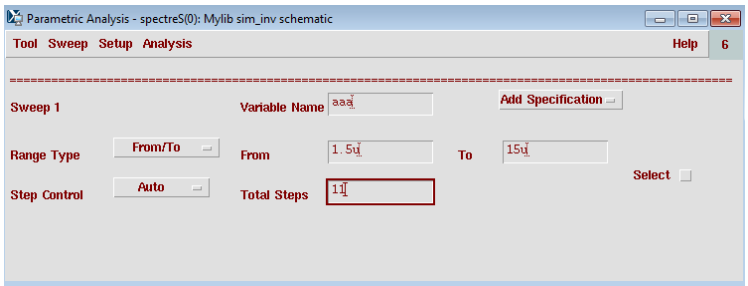
# 2.8 Find the symmetrical inverter

- Then hit “Tools->Parametric Analysis”.



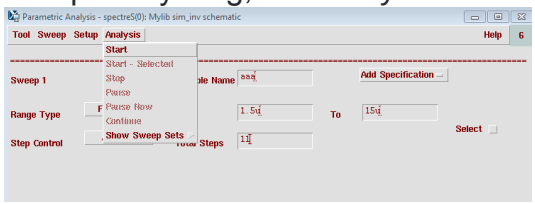

# 2.8 Find the symmetrical inverter

- In the “Parametric Analysis” window, fill in the “Variable Name”: the variable name of the width of PMOS (aaa as an example).
- Then fill in the sweep range. “from” should be equal or greater than 1.5u, which is required by the process. “to” is the final number that will be simulated with.



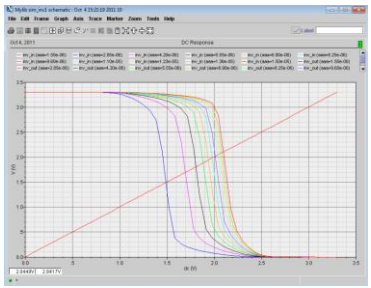
# 2.8 Find the symmetrical inverter

- Be careful about the “Total Steps”!!
- The width value used for simulation is calculated by:
  - **Width=From+(To-From)/Total Steps**
- Since the smallest incremental step of width is 0.15u, you need to make sure:
  - **(To-From)/Total Steps=n*0.15u (n is interger)**
- Thus, the tested value is valid.
- After you setup everything, hit “Analysis->Start”.




# 2.8 Find the symmetrical inverter

- The simulation results looks like this:



- Then you can choose the best width of PMOS from these simulation results. If you think neither of them meets your requirements, then you can shrink the span between “From” and “To”, redo the parametric analysis.

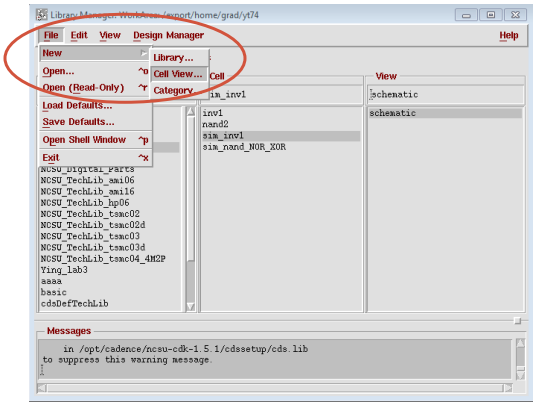
# 3 Build your layout

- Part 3 demonstrates:
  - The physical design (layout)
  - Design rule check (DRC)
  - Parameter extraction(PEX)
  - Layout vs. schematic (LVS)

  using the design rules for the AMI C5N (λ=0.3) fabrication process.
- It is important that you always have a verified functional schematic before beginning layout. If the schematic is not correct, the layout will also be incorrect. The layout should contain:
  - The same pin names and same connections.
  - Same transistors in same size as those in the schematic.
- In this tutorial the NMOS and PMOS transistors both use the minimum size transistor dimensions (W = 1.5um and L = 0.6um) for the AMI C5N process.

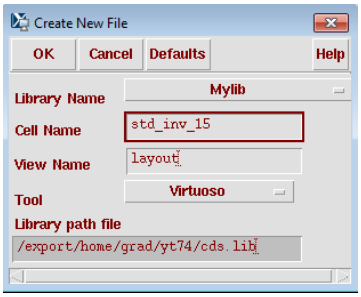
# 3.1 Create a new layout view

- In the Library Manager window
- Select your library in the left column.
- Select File->New->Cellview



# 3.1 Create a new layout view

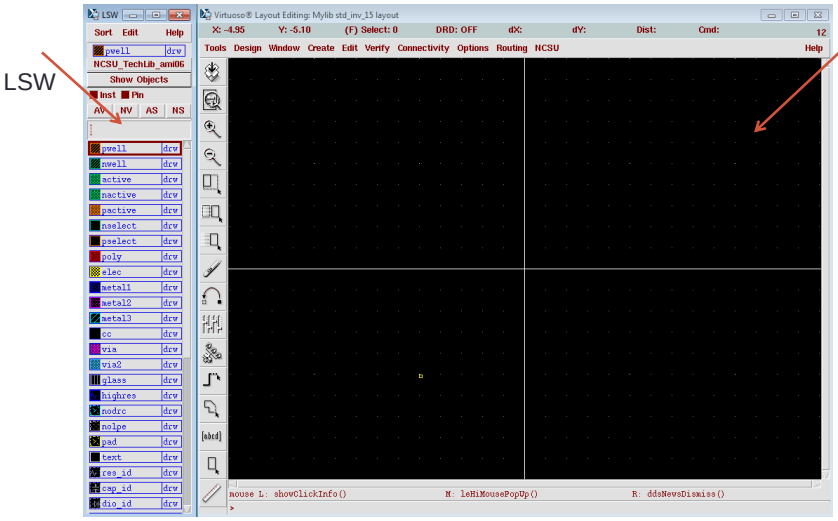
- A dialog box Create New File will pop up.
- Library name: your design library
- Cell Name: Same as the one you already have schematic and symbol *e.g. std_inv_15*
- View name: Virtuoso




# 3.1 Create a new layout view

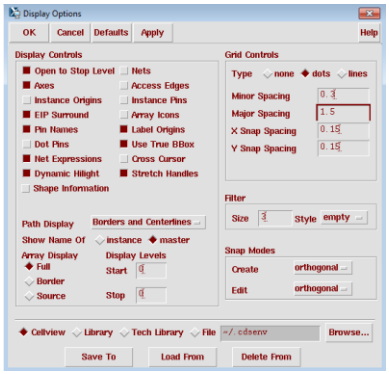
- Two design windows (Virtuoso and LSW) will pop-up.
- The Layer Selection window (LSW) lets the user select different layers of the mask layout. Virtuoso will always use the layer selected in the LSW for editing. The LSW can also be used to determine which layers will be visible and which layers will be selectable. To select a layer, simply click on the desired layer within the LSW.
- Virtuoso is the main layout editor of Cadence design tools. Commonly used functions can be accessed by pressing the buttons/icons of the toolbar on the left side of this window. There is an information line at the top of the window which shows (from left to right) the X and Y coordinates of the cursor, number of selected objects, the distance traveled in the X and Y directions, the total distance, and the command currently in use. This information can be very handy while editing. At the bottom of the window, another line shows the function of each mouse button. Note that the mouse button functions will change according to the command you are currently executing. The default mouse mode is selection, and as long as you do not choose a new mode you will remain in that mode. To quit from any mode or command and return to the default selection mode, the 'ESC' key can be used.

# 3.1 Create a new layout view



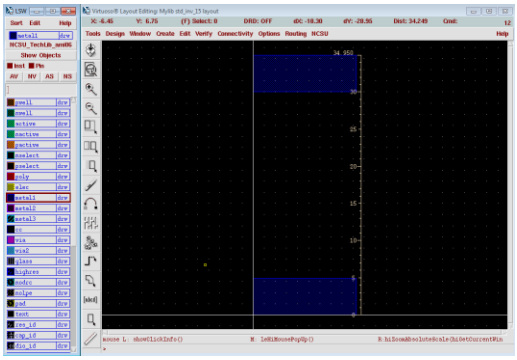

# 3.2 Build the layout of inverter std cell

- Display setup
- In the Virtuoso Layout Editing window,
- select Options->Display (or type e). The Display Options window will pop up.
- Type in the following settings:
  - Minor Spacing 0.3
  - Major Spacing 1.5
  - X Snap Spacing 0.15
  - Y Snap Spacing 0.15
- Then click OK.



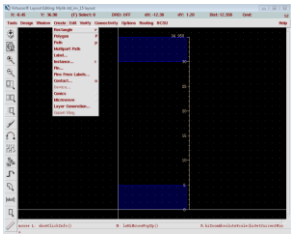
# 3.2 Build the layout of inverter std cell

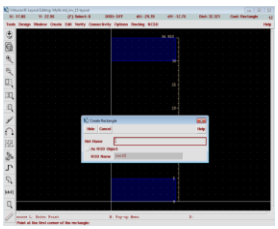
- Create VDD and GND rails.
- Metal1(drw) is used to create VDD and GND rails
- The standard cell pitch (height from bottom of the GND rail to top of the VDD rail) is 35um.



# 3.2 Build the layout of inverter std cell

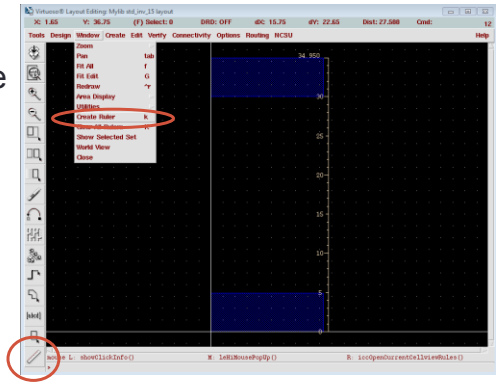
- Create rectangle
  - In the Virtuoso Layout Editing window, select Create->Rectangle (or type r).
  - The dialog box Create Rectangle will pop up. Hit Hide.
  - Go back to the Virtuoso Layout Editing window, click once left mouse, release the mouse, the shape of the rectangle changes along with you mouse.
  - Then click left mouse once again to finish build the rectangle.





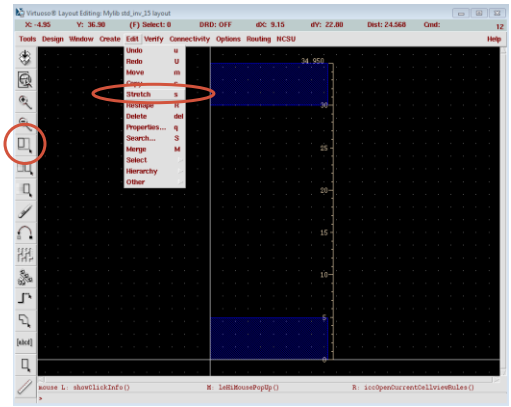
# 3.2 Build the layout of inverter std cell

- Useful editing tools
- Ruler: You can find ruler from
  - Windows->Create Ruler
  - The bottom of the menu bar
  - Or hit k
- Move, copy, delete,… are the same as in schematic.



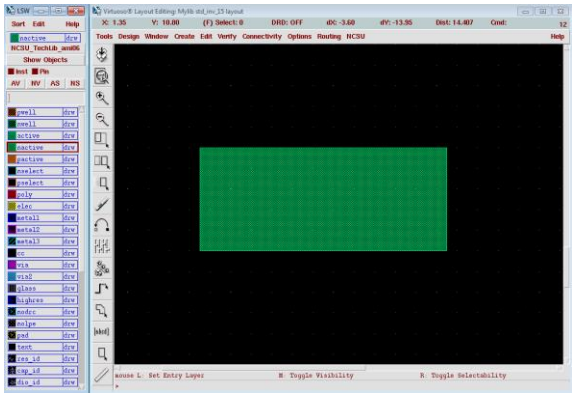
# 3.2 Build the layout of inverter std cell

- Useful editing tools
- Stretch:
  - Edit->Stretch
  - From the menu bar
  - Or just hit s
- How to use stretch?
  - Hit s
  - On the dialog box Stretch, hit hide.
  - Go back to the Virtuoso Layout Editing window, click on one edge of a rectangular with left mouse, release the mouse, the edge moves around with your mouse. Then click again to finish stretch.



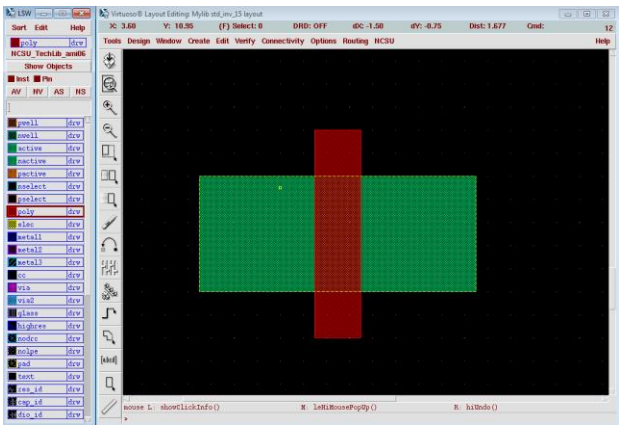
# 3.2 Build the layout of inverter std cell

- Draw the n-active region



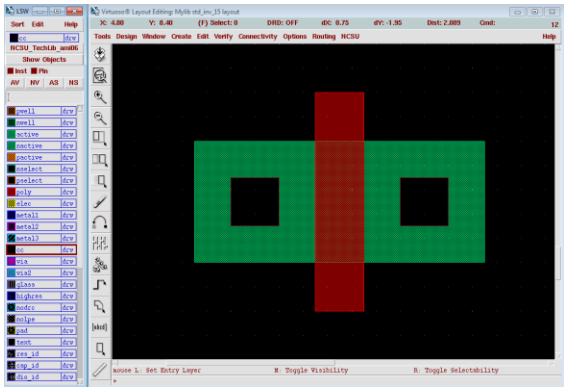
# 3.2 Build the layout of inverter std cell

- Draw the gate poly



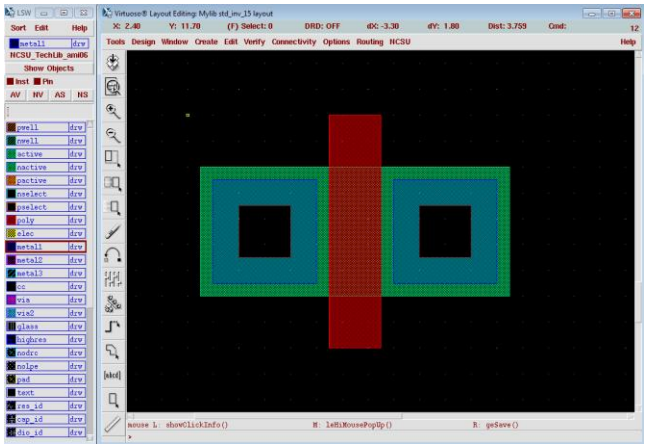
# 3.2 Build the layout of inverter std cell

- Create contacts
- These contacts are used to connect the active region and metal 1.



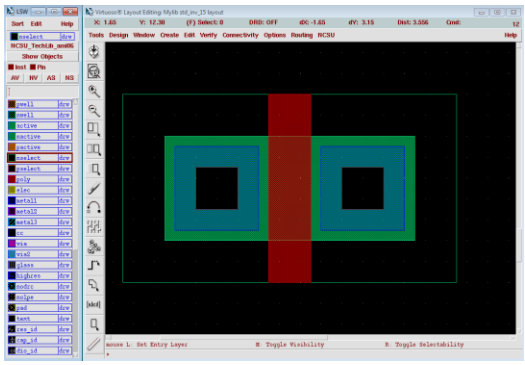
# 3.2 Build the layout of inverter std cell

- Cover contacts with metal1



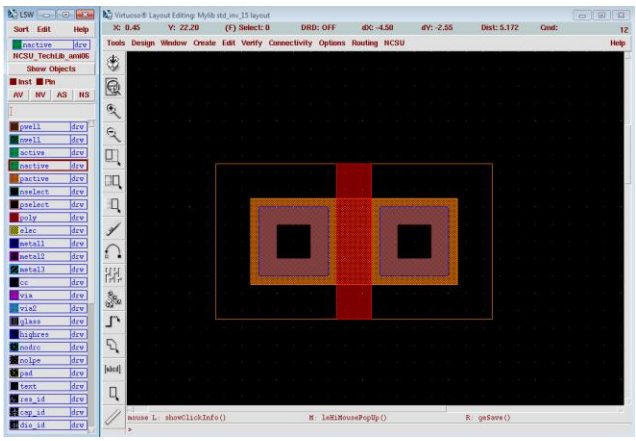
# 3.2 Build the layout of inverter std cell

- Create N-select layer
- Each active region must be specified as n-type or p-type. This is accomplished by a defining the window of n-select (or p-select) around each n-type (or p-type) transistor.



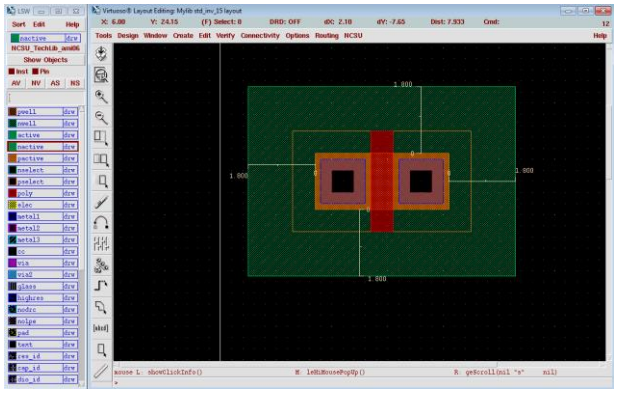
# 3.2 Build the layout of inverter std cell

- Create the PMOS.



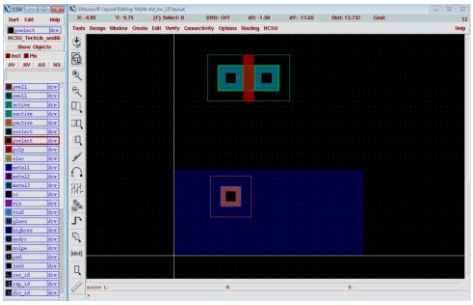
# 3.2 Build the layout of inverter std cell

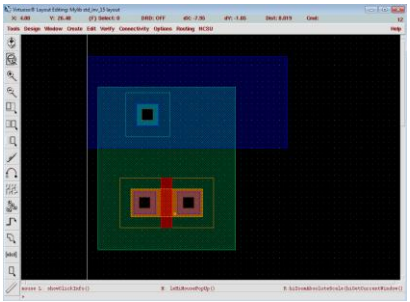
- Create the N-WELL for the PMOS
- The N-WELL should enclosure the active region by 1.8um



# 3.2 Build the layout of inverter std cell

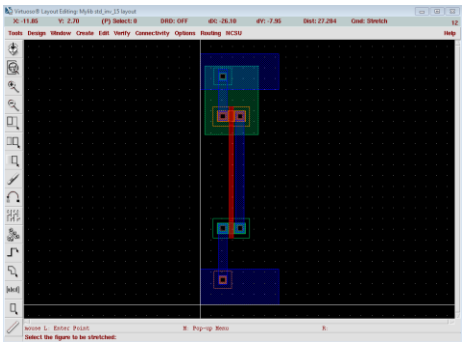
- Create substrate/Well contacts
- The body terminals of the NMOS and PMOS transistors are the substrate and n-well, respectively. These terminals must be tied to the proper supply rail, substrate to GND and n-well to VDD.





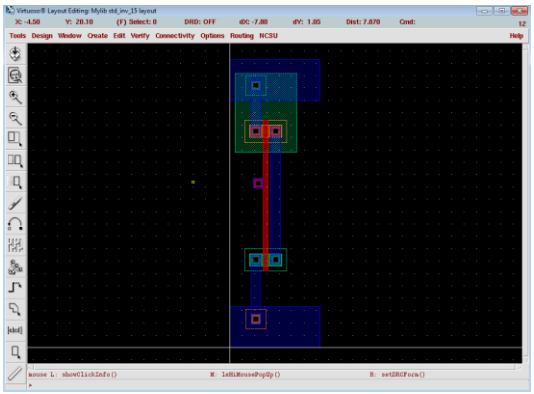
# 3.2 Build the layout of inverter std cell

- Make the connections
  - Connect gate
  - Connect Source of PMOS to VDD
  - Connect Source of NMOS to GND
  - Tie two Drains together
- The connection should be identical with schematic



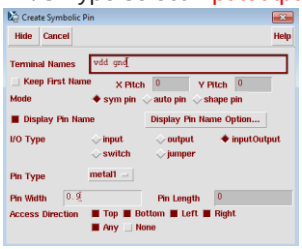
# 3.2 Build the layout of inverter std cell

- Make I/O nodes available in Metal1
  - As a standard practice that will help when connecting multiple cells (logic gates), we need to ensure that all of our input and output nodes have a connection in Metal1.



# 3.2 Build the layout of inverter std cell

- Add Pins to I/O nodes
- In the Virtuoso Layout Editing window select
- Create -> Pin to open the Create Symbolic Pin window.
  - Set the **global power pins**.
    - In the Terminal Names field, enter vdd gnd which are the names of the two global power pins. Put both names in this field, separate by a space.
    - Check sym pin and Display Pin Name. In I/O Type select inputoutput. For Pin Type select metal1.

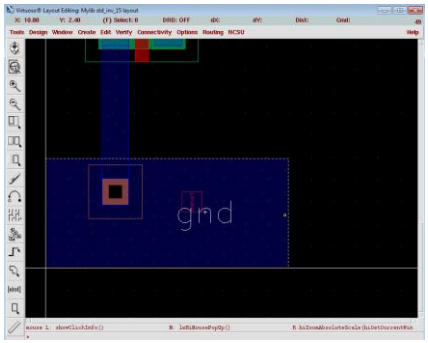


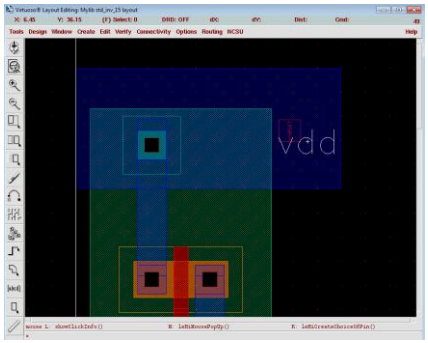

# 3.2 Build the layout of inverter std cell

- Set the **global power pins**.
  - In the Virtuoso Layout Editing window, move the mouse over the VDD rail of the inverter. Be sure to place your mouse over metal1 layer and not other layers (e.g., active) on the VDD rail. Click on the middle of the VDD rail to place the pin. Click again to place the symbol vdd -- you may move the mouse prior to clicking to place the name in any location.
  - Now move the mouse to the GND rail, place the gnd pin the same way you placed vdd. Note that because you entered both names (vdd and gnd) as Terminal Names, you can place both in the same order you entered the names.

# 3.2 Build the layout of inverter std cell

- Set the **global power pins.**



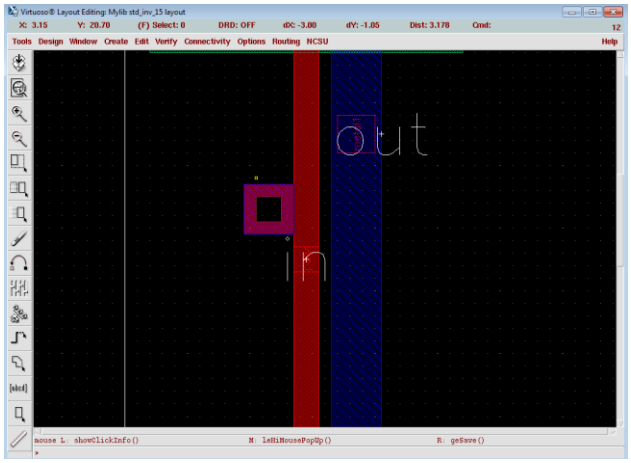




# 3.2 Build the layout of inverter std cell

- Set the **I/O pins.**
  - Go to Create Symbolic Pin window and input pin name in in the Terminal Names field. This name should be identical to your schematic. Change the I/O Type to input. Change the pin type to poly.
  - In the Virtuoso Layout Editing window, move the mouse over the middle of the input poly layer and place the pin.
  - Repeat the process to place the output pin on the output metal1. Use out in Terminal Names , output in I/O Type and metal1 in pin type.

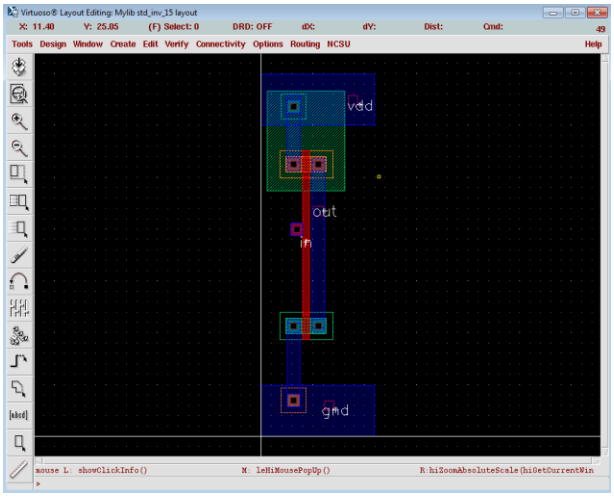
# 3.2 Build the layout of inverter std cell

- Set the **I/O pins.**




# 3.2 Build the layout of inverter std cell

- The whole layout of the inverter.



## 3.2 Build the layout of inverter std cell

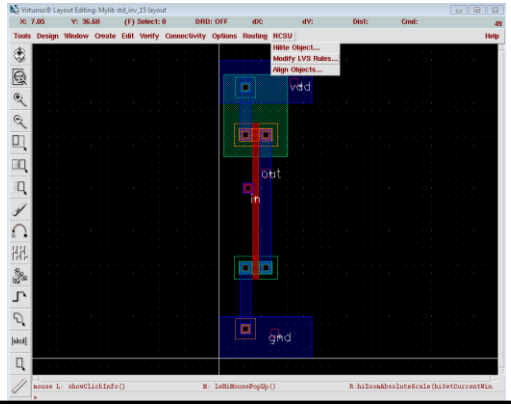
- Minimize the width of the layout
  - There is no strict guidelines for minimize the width.
  - Rules of thumb:
    - Let the VDD and GND rails extend beyond the boundary of p-select/n-select, active region, poly for easy connection (when you connects multiple standard cells in one row.)
    - PMOS in one row can share a N-WELL but not the active region or p-select.
    - NMOS in one row cannot share the n-select.

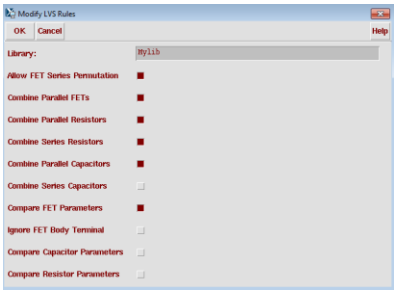
## 3.3 Design Rule Check (DRC)

- Layout must be drawn according to strict design rules. An automatic program checks every polygon in your design against these design rules and report violations.
- This process is Design Rule Checking (DRC) and MUST be done for every layout to ensure it will function properly when fabricated.
- Do DRC frequently along with you adding layers into your layout.

# 3.3 Design Rule Check (DRC)

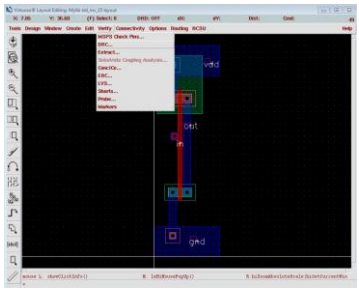
- In the Virtuoso Layout Editing window select NCSU => Modify LVS Rules.
- Check “Compare FET parameter”!

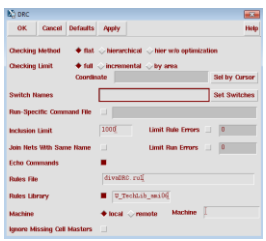



# 3.3 Design Rule Check (DRC)

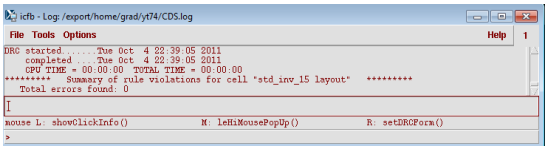
- In the Virtuoso Layout Editing window select Verify => DRC. The DRC options dialog box will pop up. The default options for the DRC are adequate for most situations.
- Click OK.
- DRC results and progress will be displayed in the CIW.



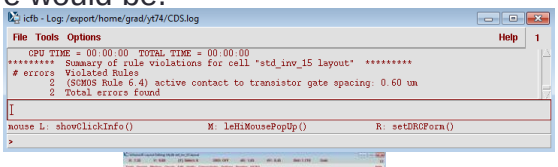



# 3.3 Design Rule Check (DRC)

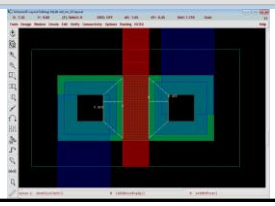
- No errors ➔ COOL!!




- Have errors, CIW shows what the smallest size/distance/enclosure would be.

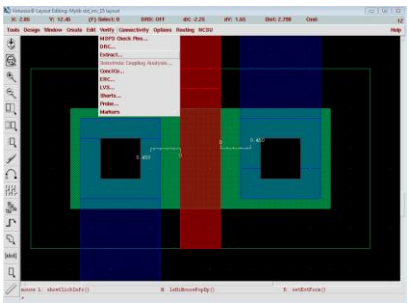


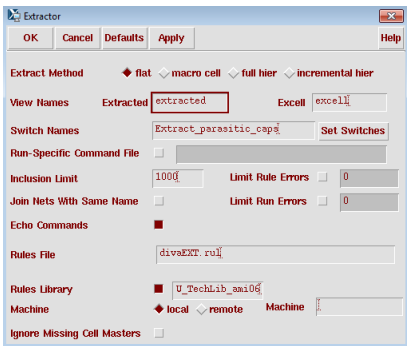

- It is displayed in layout too.



# 3.4 Layout Parameter Extraction(LPE)

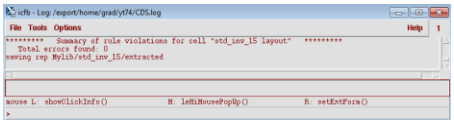
- In the Virtuoso Layout Editing window select Verify => Extract. The window named extractor with extraction options will appear.
- Click Set Switches and select Extract_parasitic_caps.
- Click on OK.



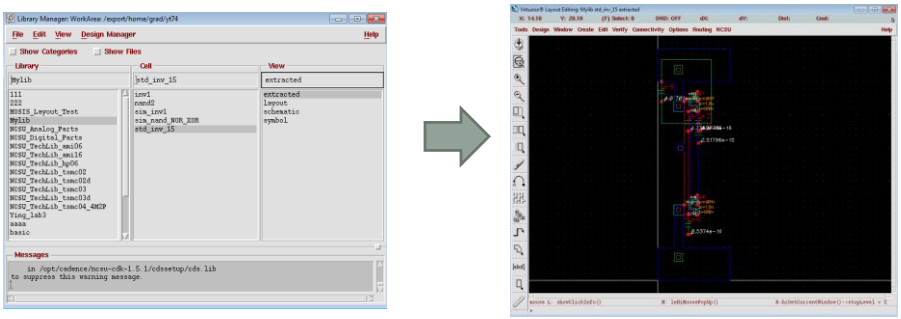


# 3.4 Layout Parameter Extraction(LPE)

- After LPE, you can see the result in the CIW

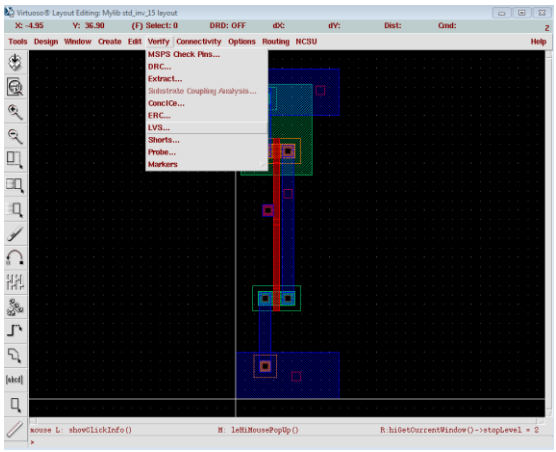


- There is an extracted view shown in the library



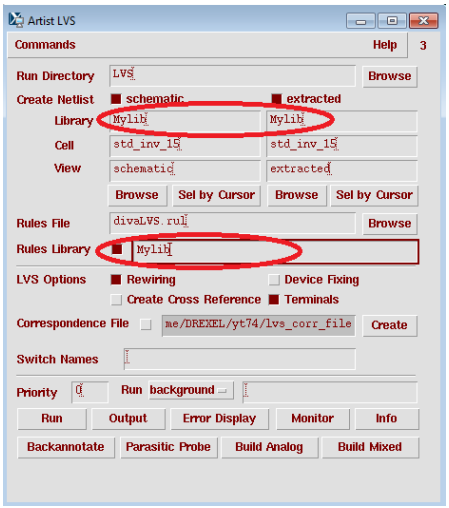
# 3.5 Layout vs. Schematic (LVS)

- In the Virtuoso Layout Editing window select Verify => LVS to open the LVS window.



# 3.5 Layout vs. Schematic (LVS)

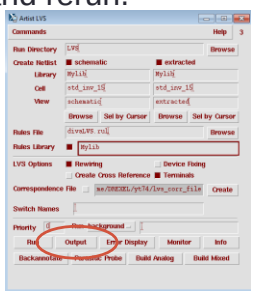
- Set the Artist LVS window like the following:
  - The "Rule Library" and the "Library" name are both your library name.
  - Tick "Rewiring" and "Terminals".
  - Do not tick "Correspondence file".
  - Leave "Switch Names" blank.
- Hit Run




# 3.5 Layout vs. Schematic (LVS)

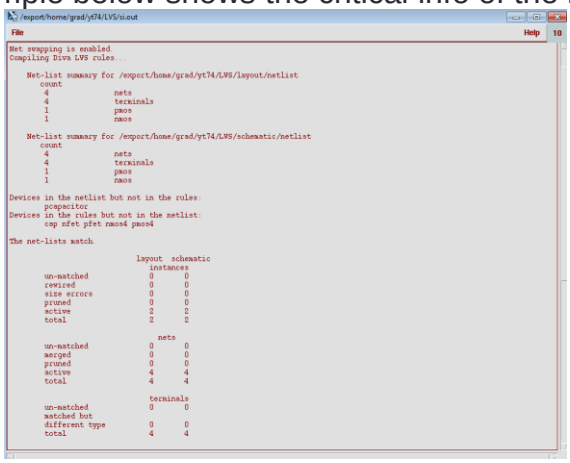
- If layout and schematic match, you would get a popup message as:


- If not match, find the reason, modify it and rerun.
- The result info can be seem at:



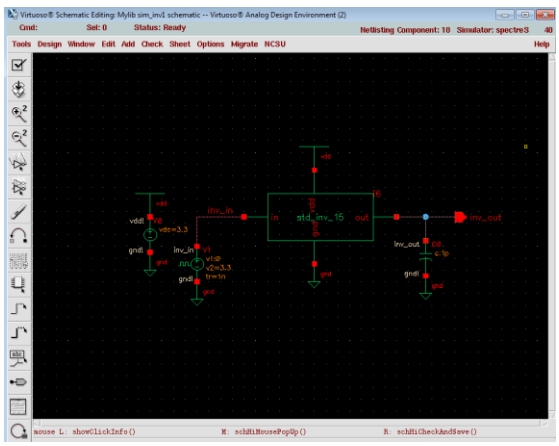
# 3.5 Layout vs. Schematic (LVS)

- Click on output, the info window will pop up.
- The sample below shows the critical info of the LVS.



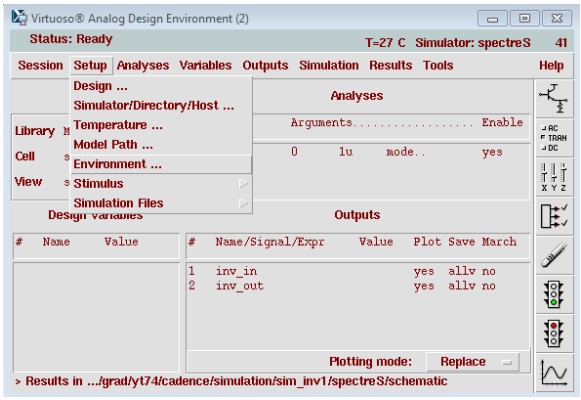

# 3.6 Post simulation

- Open the sim_inv schematic we have used for front end simulation.



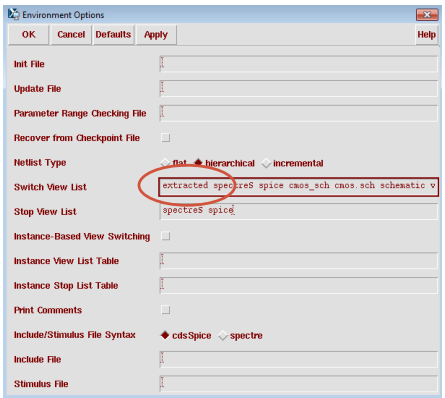
# 3.6 Post simulation

- Click on Tools=>Analog Environment to start ADE.
- Click on Setup=>Environment …




# 3.6 Post simulation

- In the Environment Option window make changes to the Switch View List
- Add extracted at the beginning.

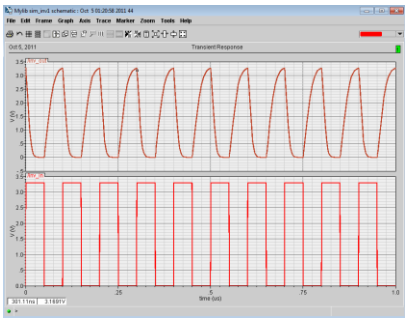


# 3.6 Post simulation

- Follow the same steps as front end simulation
  - Select simulation type: transient simulation
  - Select output nodes.
  - Extracted netlist: You can see the netlist on the pop up window. There are more capacitances, which are the parasitic capacitances.
  - Run simulation.

# 3.6 Post simulation

- The simulation results is as follows:



- You are required to compare the frontend sim and the backend sim results. You can changing the load cap to see the difference of these two results.