Fall 2013 **Introduction to VLSI Design**

Lab Assignment #5

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Drexel University
Electrical and Computer Engineering
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1 Objective

The goal of this assignment is learn how to build a CMOS gate using transistors. The major goals are to learn:

- The basic principles of designing the *Nand* and the *And* gates;
- The characteristics of *Nand* and the *And* CMOS gates.

2 Assignments

The objective of this laboratory is to design and simulate the `Nand` and the `And` gate.

2.1 Design an `Nand` Gate

1. Design a two input `Nand` gate, where the inputs are labeled `a` and `b`, and the output is labeled `out`. Make sure the total cell height is 35um for standard cell design. Choose `Vdd` and `Gnd` with width of 5um. Draw the Schematic and Layout of `Nand` Gate as shown in Figure 1 and Figure 2, respectively.
2. Check design using DRC.
3. Verify your design using LVS.
4. Simulate Schematic and Layout.

2.2 Design an `And` Gate

1. Design an `And` gate in schematic view as shown in Figure 3.
2. In layout view, connect the designed `Nand` and `Inverter` to form an `And` gate in a logic row as shown in Figure 4.
3. Perform DRC and LVS check.
4. Simulate the `And` gate.

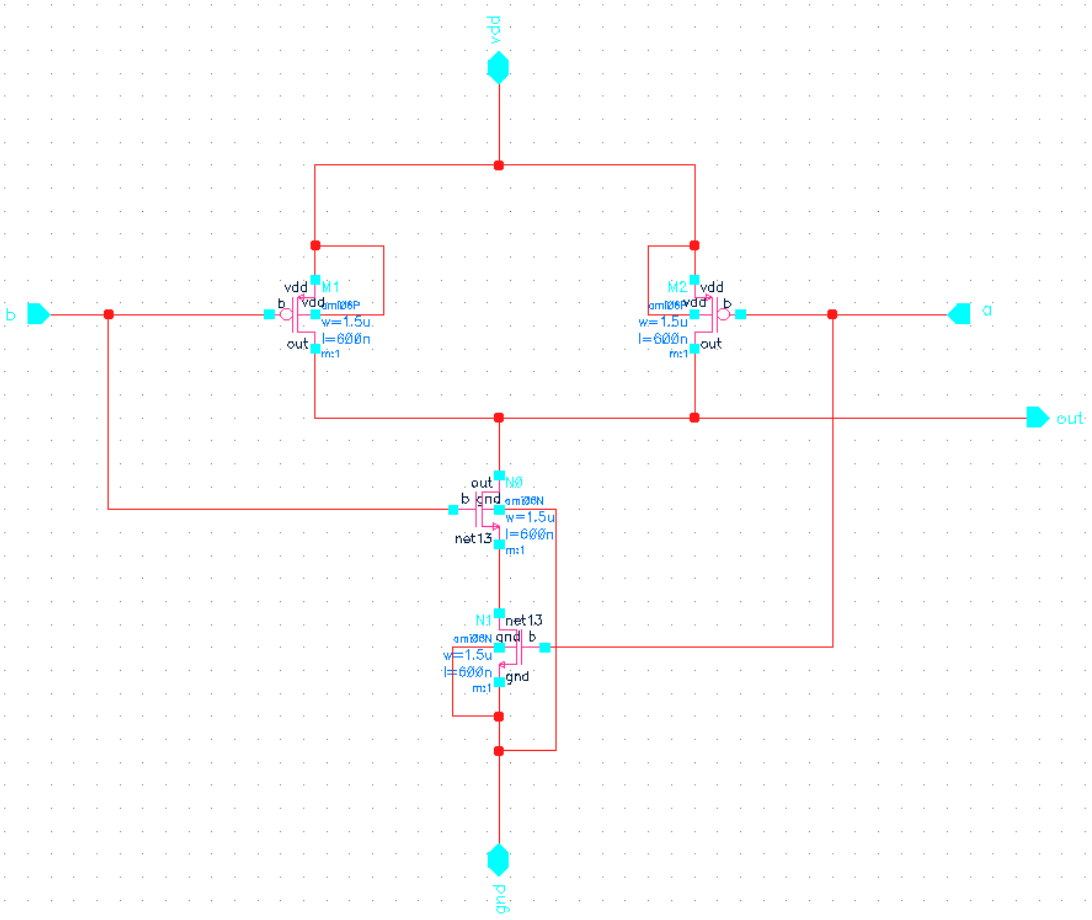

Figure 1: A schematic illustration of the *Nand* gate.

2.3 Deliverables

Lab 5 is due by Friday Nov. 1st at 5 pm. Your report should include the following:

- The schematic view and the layout view of both the `Nand` gate and the `And` gate. Use rulers to measure the dimension of the `Nand` gate and the `And` gate in layout views.
- Show DRC and LVS results for both the `Nand` gate and the `And` gate.
- Perform transient simulations on both the schematic views and the layout views of the `Nand` gate and the `And` gate to check the functionality, respectively.
- Measure the worst-case propagation delay, rise and fall time for an ideal pulse input (Use markers in the waveform analyzer to demarcate the various timing properties) for both `Nand` and `And` gates based on the simulation results.
- Perform a DC simulation on the schematic view of the `Nand` gate to plot the V_{in} versus V_{out} curve. Use markers to show the switching threshold. Size the `PMOS` to make the `Nand` symmetrical.

- Since both the designed `Inverter` and `Nand` are symmetrical, perfrom a DC simulation on the `And` gate to observe if it is also a symmetrical gate (Use markers to show the result).

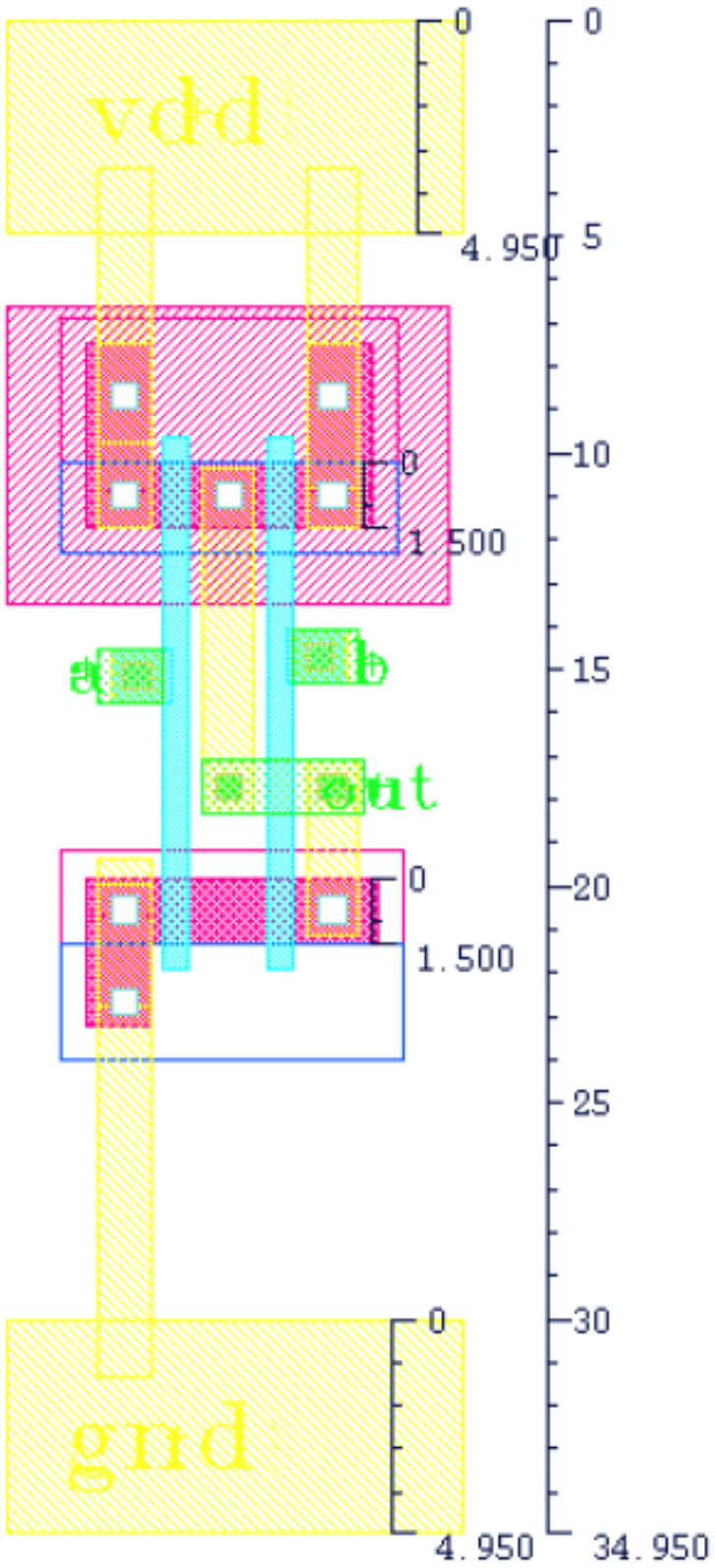

Figure 2: A layout illustration of the *Nand* gate.

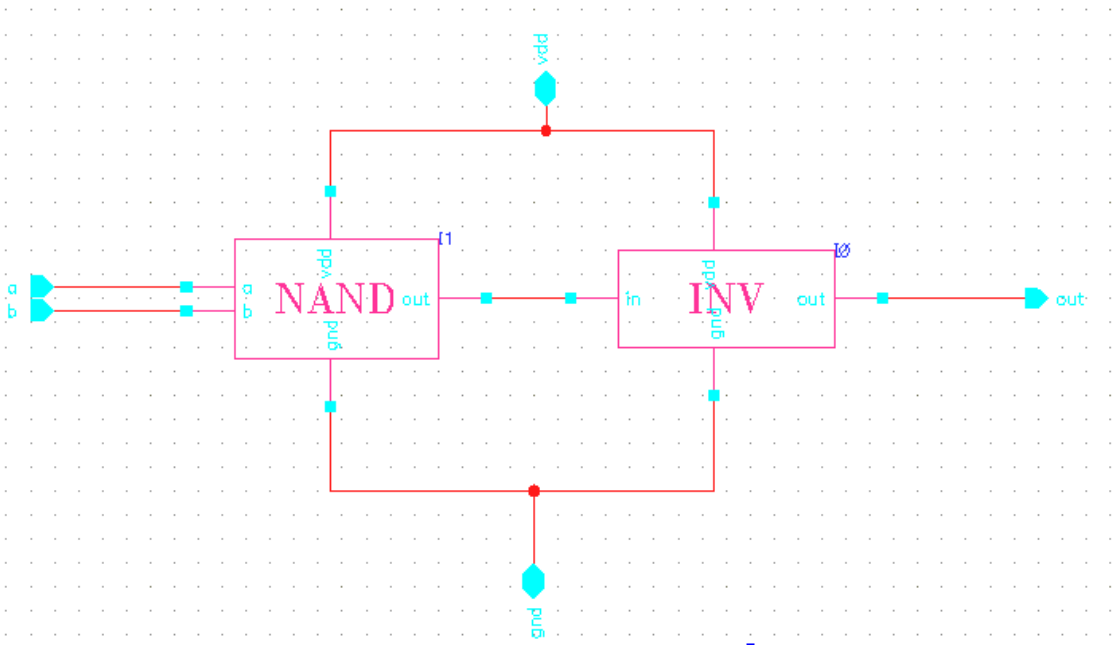

Figure 3: A schematic illustration of the *And* gate.

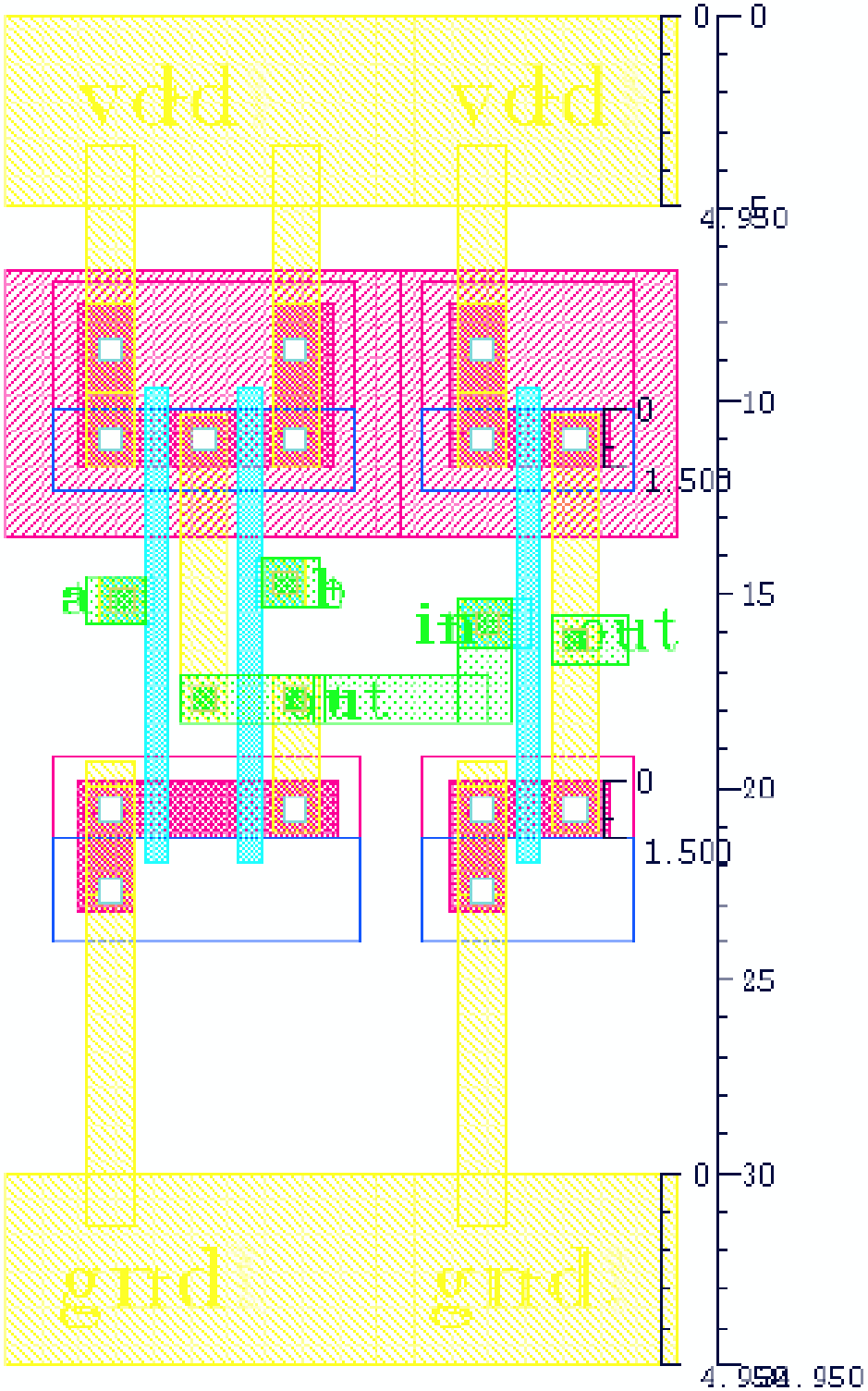

Figure 4: A layout illustration of the *And* gate.