Fall 2013 **Introduction to VLSI Design**

Lab Assignment #3

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Oct 16th, 2013 (Wednesday, week 4)

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1 Objective

The primary objective of this laboratory is to learn how to perform gate sizing in Cadence custom design tools, specifically **Virtuoso**. The goal is to create a symmetrical inverter, where the rise (t_r) and fall (t_f) times of the inverter are equal. The DC simulation of the inverter is studied as well. Laboratory tasks include:

- Sizing the inverter from Laboratory #2 such that the switching threshold is half of *Vdd*;
- Complete DC simulation on the schematic to verify the switching threshold;
- Modify the layout of the inverter to reflect the change in inverter size;
- Perform DC simulation on the layout to verify the switching threshold (with and without parasitic extraction).

2 Procedure

While sizing the inverter, the channel length of the *PMOS* and *NMOS* transistors is minimum sized (the default value). Only the channel width of the transistor is changed.

1. Perform a DC sweep simulation on the inverter, sweeping the channel width of the *PMOS* to deterine the point where the switching threshold is half of *Vdd*.
2. Change the channel width of the inverter to the desired value on the schematic, and simulate the modified inverter to verify the switching threshold.
3. Change the layout of the inverter to match the corresponding transistor dimensions on the schematic.
4. Perform DRC and LVS verification on the layout.
5. Perform a simulation on the layout (with and without parasitic extraction) to verify the switching threshold.

3 Lab reports

Lab reports are due next Wednesday before the class. Unless explicitly stated, lab reports are typically due one week after the Wednesday laboratory session. **Electronic submission in pdf or doc format through email** is accepted.

The report of this Inverter lab should include the following:

1. The DC sweep simulation plot which is used to choose the channel width;
2. The channel widths of the transistors you have chosen;
3. The screen shot of the Layout view and the Extracted view of the symmetrical Inverter;
4. The layout DRC and LVS verification results;
5. The DC simulation results for both the Schematic and Layout views;
6. The transient simulation result for the newly designed symmetrical Inverter. Mark the timing information on the plot including the rise time t_r, fall time t_f and propagation delay t_{prop};