Fall 2013 **Introduction to VLSI Design**

Lab Assignment #6

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1 Objective

The objective of this lab assignment is to build a 2-to-1 `Multiplexer` using previously designed standard cells.

2 Assignments

Same as the previous labs. In this lab assignment you will complete the schematic and layout of a `Multiplexer`.

2.1 Design a `Multiplexer`

Follow these steps to complete the multiplexer design:

1. Test the functionality of the `Inverter` and the `Nand` gate you designed previously.
2. Design a 2-to-1 MUX in the schematic view using the previously designed standard cells (*Inverter*, *NAND*, and *AND*) as shown in Figure 1. Simulate the multiplexer design and make sure the functionality is correct.
3. Complete the layout of the `Multiplexer` using the standard cell layout as shown in Figure 2 and perform transient simulation.

`NOTE:` Pay attention when using standard cells for your designs. In addition to the correctness and functionality of the design, good, compact wiring will be an important aspect of your evaluation.

2.2 Lab Reports

The correct functionality of the multiplexer and good routing are desired. Your report should include:

1. Schematic and Layout views, and simulation results of the Schematic and Layout verifying the functionality of the multiplexer.
2. Measure the worst case propagation delay, rise time, and fall time for the Schematic and Layout.

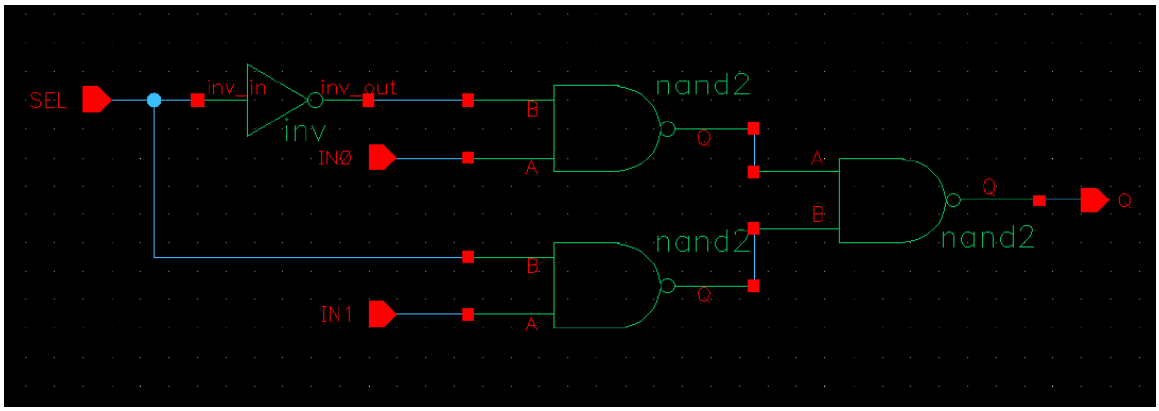

Figure 1: A schematic illustration of the *2-to-1 Mux*.

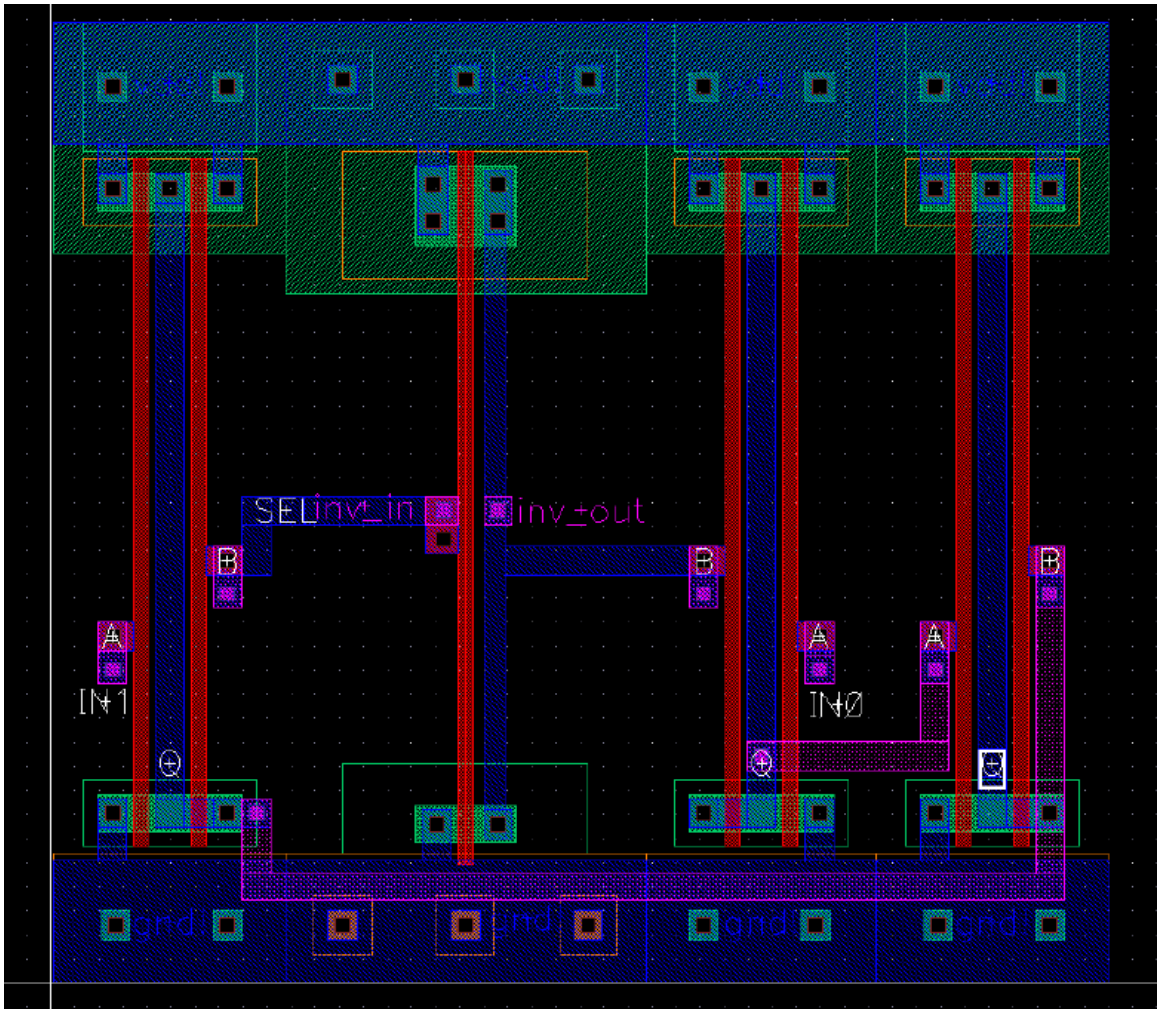

Figure 2: A layout illustration of the *2-to-1 Mux*.