IBM Microelectronics

CMRF7SF Process Design Kit Release Notes
Cadence Parasitic Extraction Component

Owning Department: KRYV

fdrytech@us.ibm.com
IBM Corporation
1000 River Road
Essex Junction, VT 05452

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1.0 Scope

This document describes the Cadence Parasitic Extraction Component of the V2.0.0.0 CMRF7SF Process Design Kit (PDK) Release.

An analog and mixed-signal design methodology has been developed to design circuits using the IBM Microelectronics CMRF7SF technology. Specific updates to the Cadence Parasitic Extraction release are discussed within.

Please send questions, comments, concerns or problems to the Application Engineering Support email address: ***fdrytech@us.ibm.com***. Include the technology, design kit version, and tool information in your problem report.

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2.0 Cadence Parasitic Extraction Component

Please refer to the CMRF7SF Design Manual for ground rule and process details. The design manual is located in the IBM_PDK/cmrf7sf/**V2.0.0.0xx**/doc directory. Additional design kit component release notes are available in the respective tool/doc subdirectories.

2.1 Contents

This kit includes the necessary parasitic extraction file structure to support the four CMRF7SF top-metal options, AM,ML,DM, the five metal stacks for each one of these options and MZ for only one stack (7LM).

16 directories are therefore:

$KIT/V2.0.0.0**xx**/Assura/QRC/3LM
$KIT/V2.0.0.0**xx**/Assura/QRC/4LM
$KIT/V2.0.0.0**xx**/Assura/QRC/5LM
$KIT/V2.0.0.0**xx**/Assura/QRC/6LM
$KIT/V2.0.0.0**xx**/Assura/QRC/7LM
where **xx** is AM or ML

$KIT/V2.0.0.0**DM**/Assura/QRC/4LM
$KIT/V2.0.0.0**DM**/Assura/QRC/5LM
$KIT/V2.0.0.0**DM**/Assura/QRC/6LM
$KIT/V2.0.0.0**DM**/Assura/QRC/7LM
$KIT/V2.0.0.0**DM**/Assura/QRC/8LM

$KIT/V2.0.0.0**MZ**/Assura/QRC/7LM

Where $KIT is the install path.

Each directory include the following files :

- qrcTechFile
- RCXspiceINIT
- RCXdspfINIT -> symbolic link to RCXspiceINIT
- Techgen_cmd
- lvsfile
- _p2lvsfile
- _procfile

There are also symbolic links pointing to the corresponding files in the .../Assura/LVS directories :

- LVSinclude.rsf
- bind.vldb
- bind.rul -> symbolic link to bind.vldb
- compare.vldb
- compare.rul -> symbolic link to compare.vldb
- deviceInfo.rul
- bind.cdl
- compare.cdl
- extract.rul -> symbolic link to the appropriate extractx.rul

2.2 Important Notice

Supported tool releases :

The component files were created under Cadence version 6.15.500-12 and Assura version 4.12.020-615.610, and tested under that same versions.

The users should install **QRC version 11.1.2-p106**, under which we have developed and tested this component.

This release requires the installation of the **V2.0.0.0 LVS release**.

The released PEX supports only **low-resistivity substrate (LR)** for AM, ML, DM and MZ release.

The current CMRF7SF Cadence parasitic extraction flow supports only Cadence Assura LVS inputs (remark that QRC is capable of supporting Mentor Graphics Calibre LVS input files, this is not currently implemented in this kit)

Set-up :

The Parasitic Extraction files in this kit are split into one directory per metal option. Included in these directories are symbolic links to the appropriate files. When using the kit, each metal option is mapped to its particular directory by the assura_tech.lib file.

The format of the assura_tech.lib file is : “DEFINE user_stack_name TechDir_path” ,
where user_stack_name is the user choice of a name for the stack, and TechDir_path is the path to the directory containing the parasitic extraction files and symbolic links (ex: see below for 6AM stack option)

```
DEFINE    QRC_7RF_6AM    $KIT/V2.0.0.0AM/Assura/QRC/6LM
```

The assura_tech.lib file should be placed in the run directory.

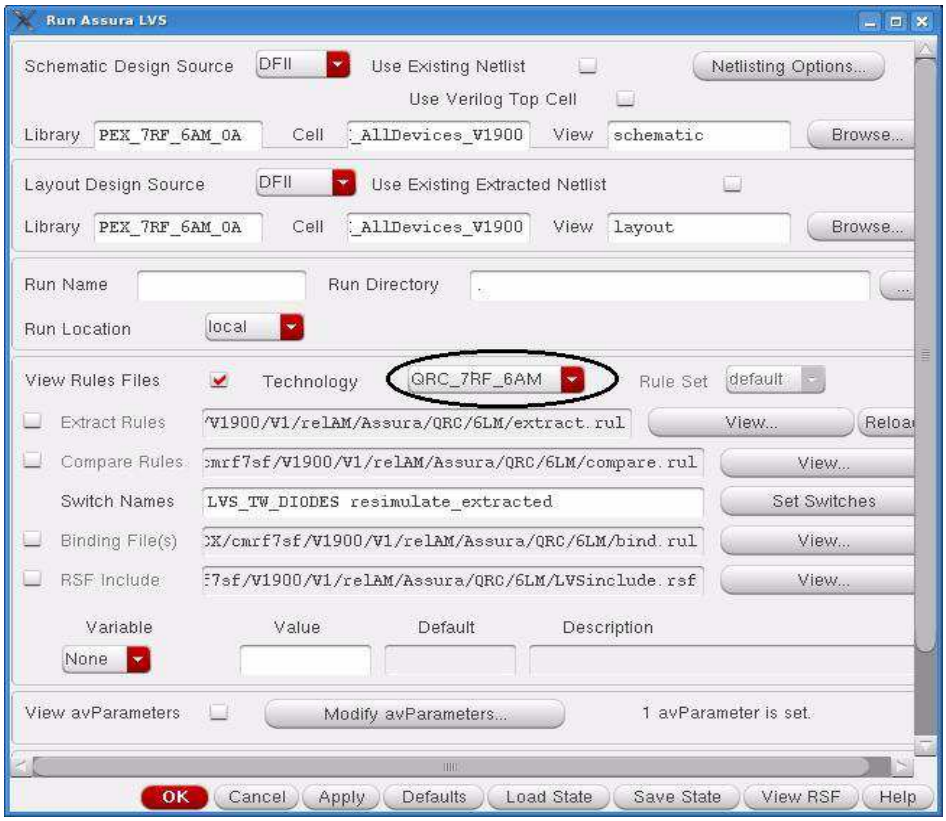
In the Assura LVS form and Assura QRC form, the choice is available under the Technology button.

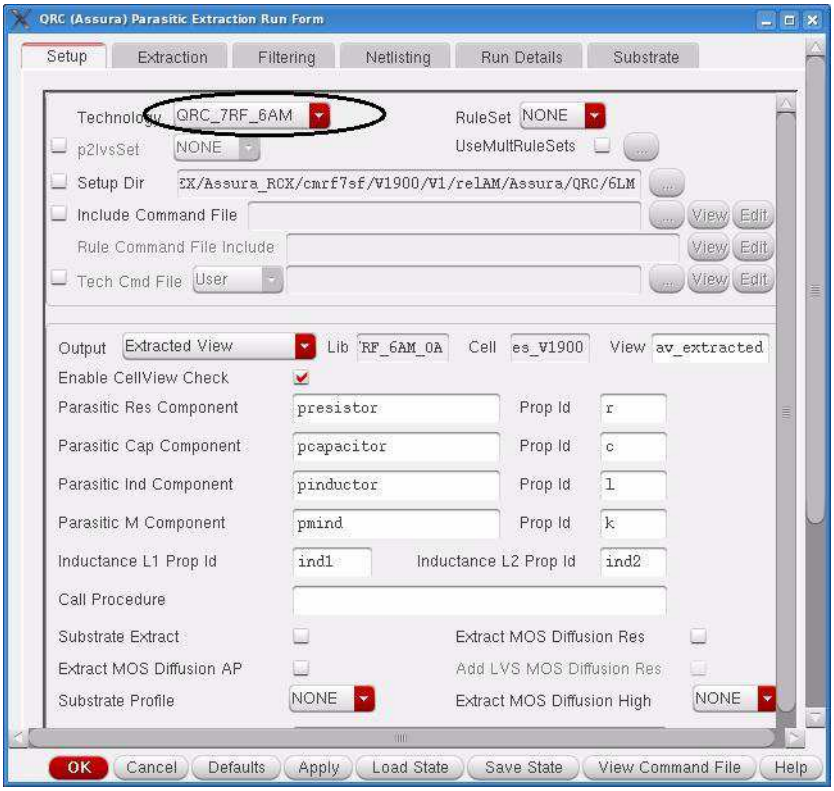
Post-extraction netlisting and simulation :

In order to obtain a valid post-extraction simulation netlist (Spectre or Spice) the customer should use the setup shown in the above figure. Note that the 'Extracted View' field should be used in the Output pull-down menu.

And then the resulting “av_extracted” view can then be simulated in the Cadence Virtuoso Analog Device Environment (ADE).

All other approaches will result in an incorrect netlist.





3.0 Validation procedures & results

Parasitic Extraction accuracy :

Prior to kit shipment, IBM has developed a validation procedure that compares, on a battery of testcases the results of the Cadence Parasitic Extraction tools versus “golden” results.

Double/miss-counting : Netlists are performed on wired devices, for each element of the device library. A comparison between extracted and modeled parasitics is done to evaluate possible double or lack of parasitic extraction. All errors are fixed or documented.

Resistance extraction :

Resistance extraction accuracy has been verified by comparison to design manual equations, the comparison is within our target (+/-1%).

- meshR option :

This option allows to extract parasitics resistances with more accuracy.
To use this option you need a license XL and Cadence QRC Advanced Analysis (AA) GXL Option (QRCX310), see **QRC Product Licensing.**
Explanation : The current is considered like uniform and model extraction is (R x L) / W with L > W. Indeed, this model works well for most of the net (long and "narrow") but it loses accuracy for large shapes such SQUARE . In this case the meshR increases the accuracy of Rparasitics and the size of the netlist.

Capacitance extraction :

Our tescases consist on a stack of parallel wires at minimum pitch for which we compute wire capacitance. We have observed that results of Assura QRC versus a golden field solver are beyond our specifications.

The QRC extracted capacitance is in a range of +/- 10% for 98% of the testcases compared to a golden theorical field solver reference (QuickCap).

For relML and relMZ, the “QRCFS Extraction Mode” AND “QRCFS Extraction Mode with QRCFS High” option, the results compared to a golden theorical field solver reference (QuickCap) are in the range of +/- 10% for 100% of the testcases compared to a golden theorical field solver reference (QuickCap).

For relAM and relDM, the “QRCFS Extraction Mode” AND “QRCFS Extraction Mode with QRCFS High” option, the results compared to a golden theorical field solver reference (QuickCap) are in the range of +/- 10% for 99% of the testcases compared to a golden theorical field solver reference (QuickCap).

Inductance extraction :

The QRC extracted inductances are within +/- 5% compared to our reference field solver (QuickInd).

For mutual inductances extraction with wide metal wire, validation should be made with the “LadderNetwork” option.

Case of parasitic extractions in the vicinity of modeled devices / double counting:

The library of devices from the V2.0.0.0 release has been tested against possible double / miss counting.

No issue has been found during this test.

Netlisting (post extraction):

Only the "av_extracted" view output is supported, to obtain a valid "Spectre or Spice" output for netlisting, the "Extracted View" option must be selected, and then netlisted with analog environment menu (Cadence methodology).

4.0 Important notes on usage and Known Limitations

Tool limitations

- **Resistance extraction**
  The override cheesing option (Mx_exclude) is not enabled.

- **Capacitance extraction**

  We have observed that the capacitance extraction on a library element without wiring can cause QRC fail (e.g. MIMs with vias, but without external connections) if the Design Capacitor Models and Parasitic Capacitor Models switch is not set to “Include Model”, in the QRC Assura run form / Netlisting Tab.

  If two devices are situated close to each other, and each contains mx_model and mx_resistive in the blocage region then the coupling capacitance between the two devices is not accounted for.

- **Device parasitic extraction**

  For coupledwire and singlewire devices, the parasitic extraction of metal outside the pcell wired between the shielded metal mx and the signal metal mx is not extracted.

  For rflines, inductors and singlewire, the coupling capacitance between the device and a neighbor wire is not extracted.

Process variation :

The PEX decks have been validated ONLY in nominal case.

Mx Fill process :

There are two ways to take parasitic effect of Metal FILL shapes when using QRC.

- **Automatic estimation Way**:
  To estimate the parasitic effects of Metal Fill shapes through this way, set "Enable Virtual Metal Fill" button to ON state in QRC form (under Netlisting tab). The QRC decks will then estimate those Metal Fill shapes according to IBM "post-cheese and fill" algorithms (Layout Rules for IBM-Generated FILL and HOLE Shapes in Design Manual), and include their parasitic capacitance into "av_extracted" view.
  There is no need to manually add Metal Fill shapes into layout for this automatic way.

- **Manual Way**:
  For this way, the user has to place the xxFILL shapes into layout according to Layout Rules for IBM-Generated FILL and HOLE Shapes, or leaves IBM to peform automatic fill of metal layers into layout and ask for post design-service GDS file to evaluate the impact of xxFILL shapes. For this approach, LVS should run with "INCLUDE_Mx/PC_Fill_in_PEX" switch ON to take these shapes into account in QRC.

  Note : Do Not use the two methodologies in conjunction to avoid the risk of double counting for fill effect.

5.0 What's been updated in V2.0.0.0.

New device supported :

- device1p
- p5pcdcap50

Drop voltage issues

Drop voltage issues has been improved in some cases this patch.

- **Issues**

  LVS extraction decks use the stamping statement to pass the connectivity from metal 1 to the different well. This methodology present advantages for LVS validation but can have undesirable effect when using QRC. Consequence is to mask the real drop voltage on M1 layer.

  In the LVS rules , the different "substrates" layers [nwell, pwell, ns and substrate] are typically modeled as fully conductor (non-resistive) to preserve the correct layer connectivity. However, full conductivity of the substrates layers (R=0) has the undesirable side effect of shorting out the metal resistor above the substrates layers through any vias that make contact to the substrate. As such, there could be considerable resistance loss in the power lines (which may have many connections to the substrates layers).

- **Work around**

  A specific QRC setting allows to improve the m1 resistive network (long well contact / ring cases)

  => In the QRC form, fill the "Ignore Vias" field from the "Netlisting" tabs.

This command specifies that all vias belonging to the specified comma-separated list of layers, that occur on any of the comma-separated list of nets, should be eliminated from resistance extraction.
This command is intended to suppress vias connecting to the substrate to prevent the substrate from shorting parasitic resistors on nets connecting to the substrate. This has the advantage of reducing the extracted parasitics by eliminating many possible via resistors from the power or ground net, and reducing the RC networks as a result.
Specify the via layers and the substrate nets to achieve this result.

For example fill into the **Ignore Vias** fill form :

- **Layers** : ca6 *
- **Nets** : vcc

***ca6** is a LVS reserved keyword. This derived layer has to be used when using the "ignore vias" methodology. The via "ca6" allows connectivity between M1 and all the well nodes (nw, ns, pwell) to correctly extract the M1 parasitics resistance .

Process

- High Resistivity substrate is not supported any more.