SDE Upgrade
WP5 ECRs

WP5 Proposal

EA UUB production status:

ECRs (Feb 2016) for the next UUB version:

- Present UUB block Schematic.
- ECRs integrated for EA.
- ECRs not integrated for EA.

New ECRs for next UUB version:

EA UUB production status

ECRs (Feb 2016) added by WP5 for EA

WP	ECR nb.	Description	For EA	WP5 proposale for KIT Prod.	BOM Modif.	Retro-fit
WP1	1-1	Replace type 3 FE design by Type 1 or 2 (2 last channels)	Yes	Simplest modification	√	√
	1-2	Low gain on type 1 FE design at -12 dB	Yes	Ok	√	
	1-3	Gain optimization on 3 last ADC chan. (on type 1 & 2, 3 boards only)	Yes	Ok	√	
	1-4	Remove zero resistors as jumper to exclude external VREF on ADCs	Yes	Cut wire		√
	1-5	Siegen solution for enable of - 3.3 V problem	Yes	Seems not work. Other propasal made and seems work		√
	1-6	Add tantalum capacitors on offset output	Yes	Ok		√
	1-7	Precision & quality resistors for offset and VREF generators	Yes	No. Seems not need (TBC)		
	1-8	Passive components final values on filter and amplifiers and capacitors position	Yes	Ok		√
	1-9	Remove last SMA connector	No	N/A		
WP2	2-1	Remove the ADC overflow bits (useless)	No	N/A		
WP4	4-1	Add 10uF capacitors filter on microcontroller Vref+	Yes	Ok		√
	4-2	Change SC ADC impedances on PMT_TMon lines to 1 kΩ	Yes	Ok	√	
	4-3	3.3 to 1.8V conversion for microcontroller NMI-FPGA line	No	N/A		
	4-4	Connect microcontroller PS_SRST_B line to 3.3V	Yes	Ok, NCR_2-49		√
WP5	5-1	Ethernet LED connection	No	N/A		
	5-2	Radio reset routed to micro-controller	No	Should be made		√
	5-3	Replace Jitter cleaner with fan-out and new VXO to go to 1ps jitter, 3.3V on DAC	No	N/A		
	5-4	Replace QSPI flash memory (to be tested)	Yes	Ok		√
	5-5	Remove LVDS buffers on EXT I/O and on board connectors	Yes	Ok	√	
	5-6	New power supply connector (stronger)	No	N/A		
	5-7	Modify bad footprints (see list)	No	N/A		
	5-8	Use adapted size stencil sheet for PCB	Yes	KIT		
	5-9	Update the BOM	Yes	Ok	√	
	5-10	Additional ground plane on top and bottom of the PCB	No	N/A		
	5-11	Change holes position on PCB	No	N/A		
	5-12	Remove stiffener	Yes	Ok	√	
	5-13	DC/DC ramp capacitor value optimization	Yes	Ok	√	
	5-14	Correction on USB PHY component	Yes	Ok		√
	5-15	Correction on clock DAC voltage	Yes	Ok		√
	5-16	Optimized ADCs SDIO Configuration (power down)	No	N/A		
	5-17	Optimize passive components values and sizes (prod. center recom.)	Yes	Ok	√	
	5-18	Replace pin connectors by SMT models (prod. center recom.)	No	N/A		
WP7	7-1	LED controller logic integration into FPGA	Yes	Ok	√	√

After WP 1 & 5 discussions: Not integrated

Modification made during EA

: Not integrated for the 21 UUBs production

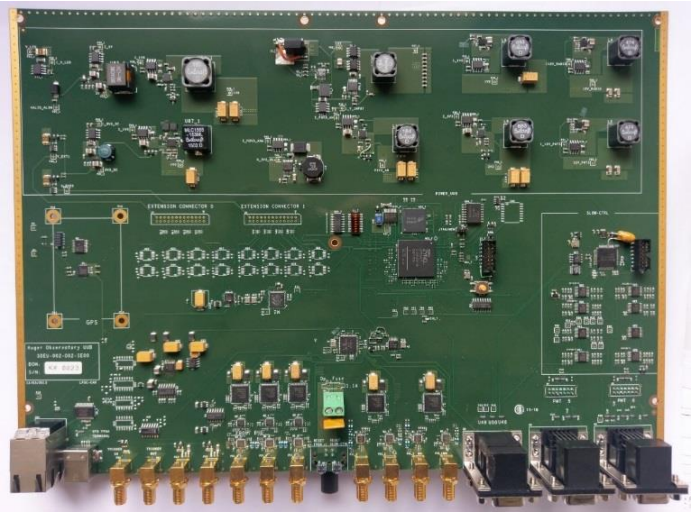
Status

3 March 2016, PCB specifications provided by WP5 for PCB manufacturing

Middle of March, 22 PCBs and BOM files sent to KIT

Begin of June 16, 21 UUBs sent to Grenoble:

- 67 NCRs.
- Middle June, Only 2 UUBs was fully tested (WP1 & WP5).
- End of June, 4 UUBs sent to Malargüe.



Begin September 16, EA:

- 12 UUBs available, retro-fitted and tested at Malargüe (WP5).
- EA test: 7 NCRs (4 UUB NCRs & 3 Cable NCRs).
- 13 Watts power consumption (with BULLET radio)

End March 2017, WP5 provides specifications for layout:

Middle of June 2017, 5 prototypes delivered:

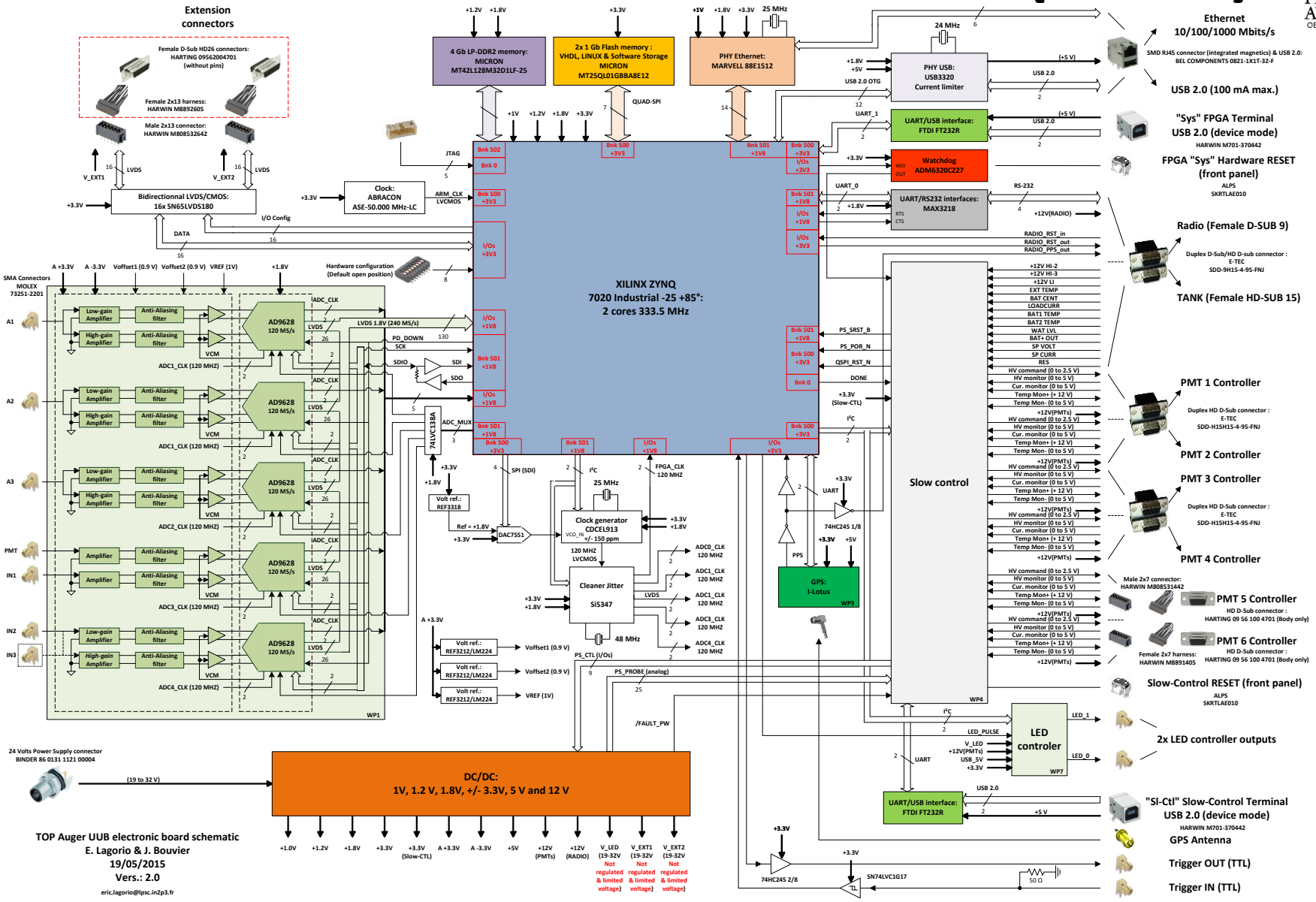
End 2017, Mass production ???:

Next prototypes must FULLY tested before mass-Prod

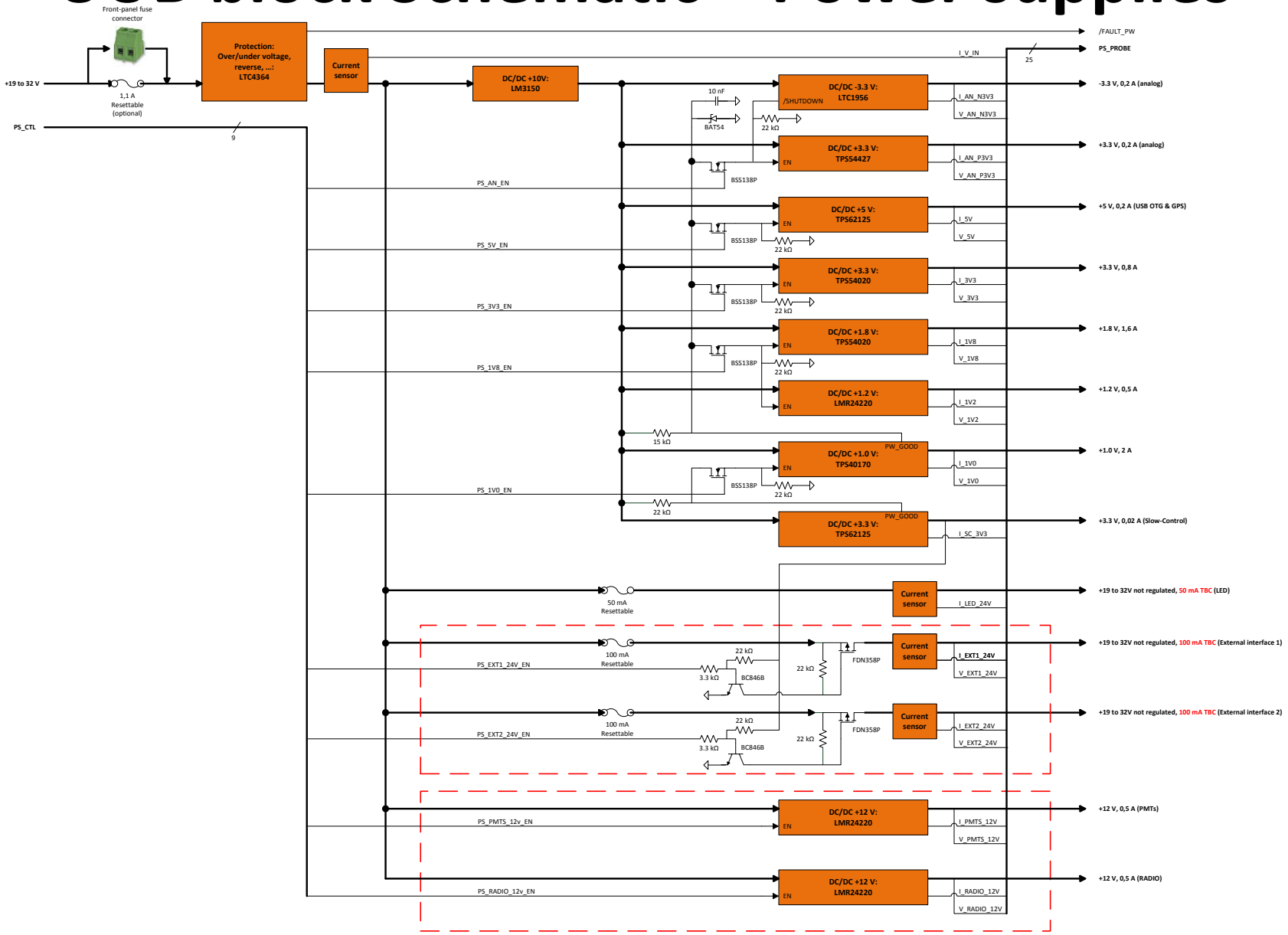
ECRs (Feb 2016) for the next UUB version

- Present UUB block Schematics
- ECRs not integrated for EA

UUB block Schematic – main (v1.12)



UUB block Schematic – Power supplies



ECR (Feb 2016) not integrated for EA

ECR 1-9, Remove Last SMA connector:

In layout, but mounted or D.N.M. with BOM

ECR 2-1, Remove the ADC overflow bit:

Already in layout. Why remove it?

ECR 4-3, 3,3V to 1,8V conversion NMI-FPGA line:

Micro-controller pin configured in open-collector.

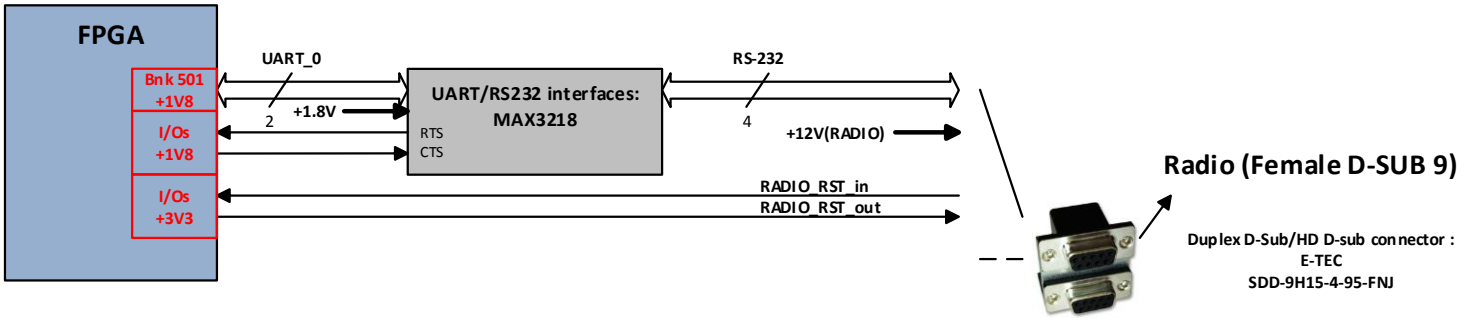
Compliant with Micro-controller input threshold. No voltage translator needed.

ECR 5-1, Ethernet LED connection:

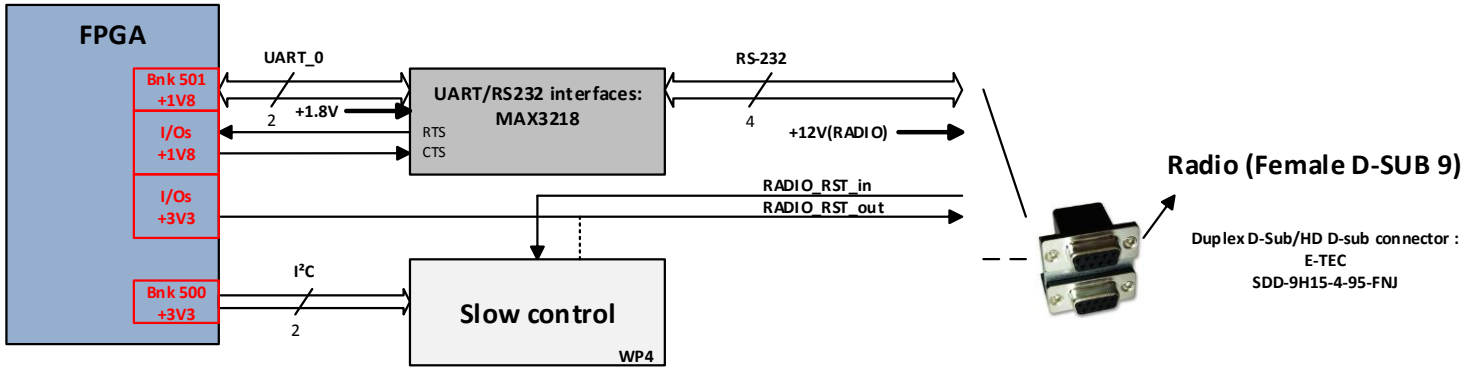
Schematic error

ECR (Feb 2016) not integrated for EA

ECR 5-2, Radio RESET routed to Micro-controller (P. Allison)



In present UUB design: RADIO_Rest_IN signal from radio is managed by FPGA



RADIO_Rest_IN signal from radio is managed by Slow-Control as the other Resets (fpga & QSPI Flash memories).

ECR (Feb 2016) not integrated for EA

ECR 5-3, Jitter Cleaner replacement by Fanout:

WHAT DO WE NEED: Acceptable SNR (noise) MUST BE define before the choice. MORE JITTER = MORE NOISE

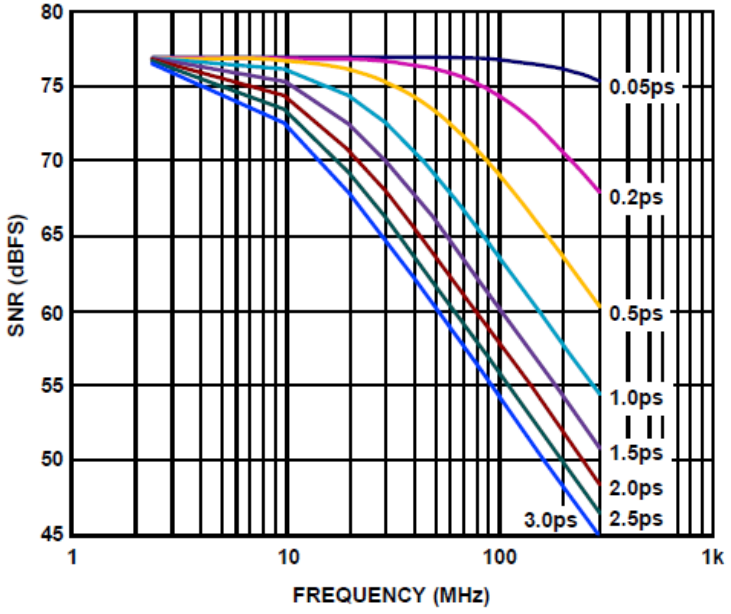
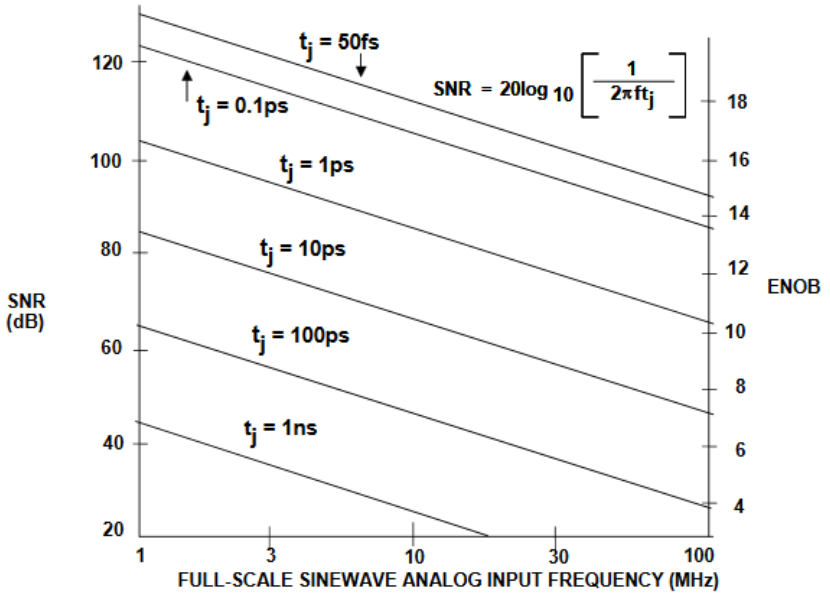


Figure 58. SNR vs. Input Frequency and Jitter

Analog Devices AD9628 datasheet rev. C



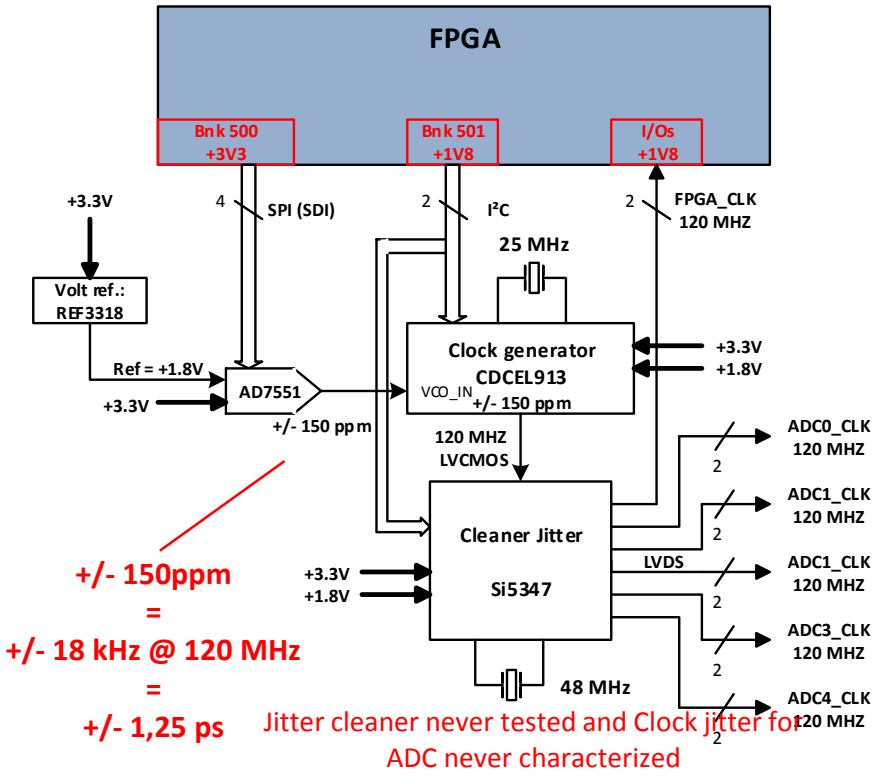
Lower power consumption OR Lower noise

To remove Jitter cleaner -> risk of increase of noise

ECR (Feb 2016) not integrated for EA

ECR 5-3, Jitter Cleaner replacement by Fanout:

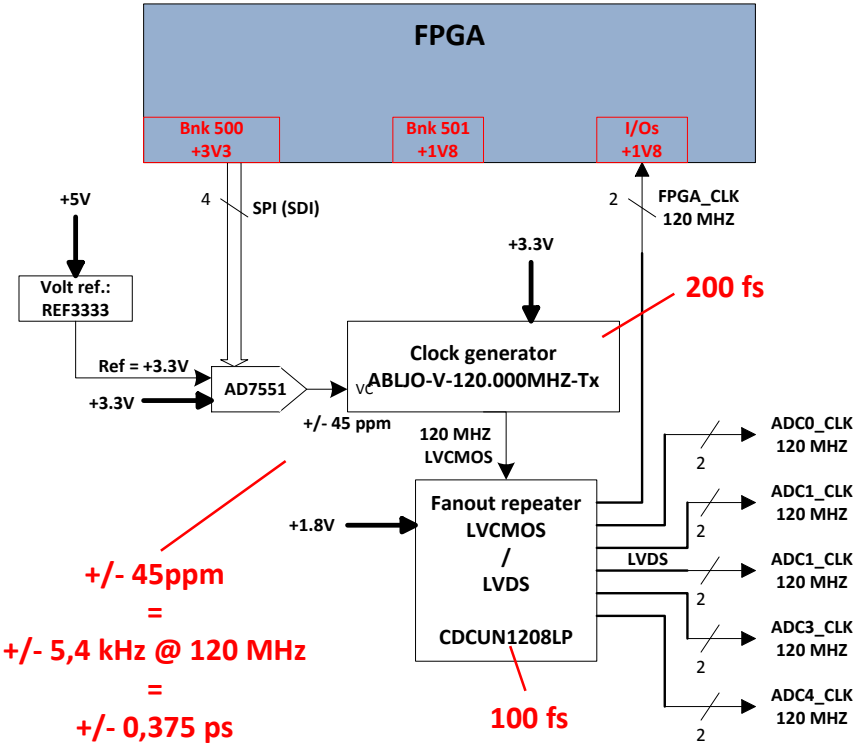
In present UUB



Jitter cleaner never tested and Clock jitter for ADC never characterized

Compliant with ADCs 100fs specs
Clocks Jitter Estimate : 0,1 ps Max
+/- 150 ppm frequency control (+/- 18 kHz)
Configurable
Power: 700mW

Alternate proposal



Outside ADCs specs.
Clocks Jitter estimate : 0,3 ps RMS
+/- 45 ppm frequency control (+/- 5,4 kHz)
No configuration
Power: 252 mW

ECR (Feb 2016) not integrated for EA

ECR 5-6, Power supply connector:

Describe in New ECR 15.11 & ECR 15.12

ECR 5-7, Bad footprints:

Done

ECR 5-10, Additional Ground plane on Top and Bottom PCB layers:

Describe in New ECR 15.03

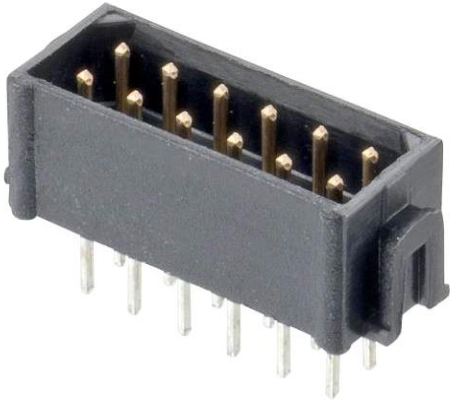
ECR 5-11, Change holes position on PCB:

Describe in New ECR 5.11 & ECR 2-13

ECR (Feb 2016) not integrated for EA

ECR 5-18, Change through-hole pin connector by SMT:

J4, J5, J7 & J9 are used for PMT and extension cable plug : could be snatched



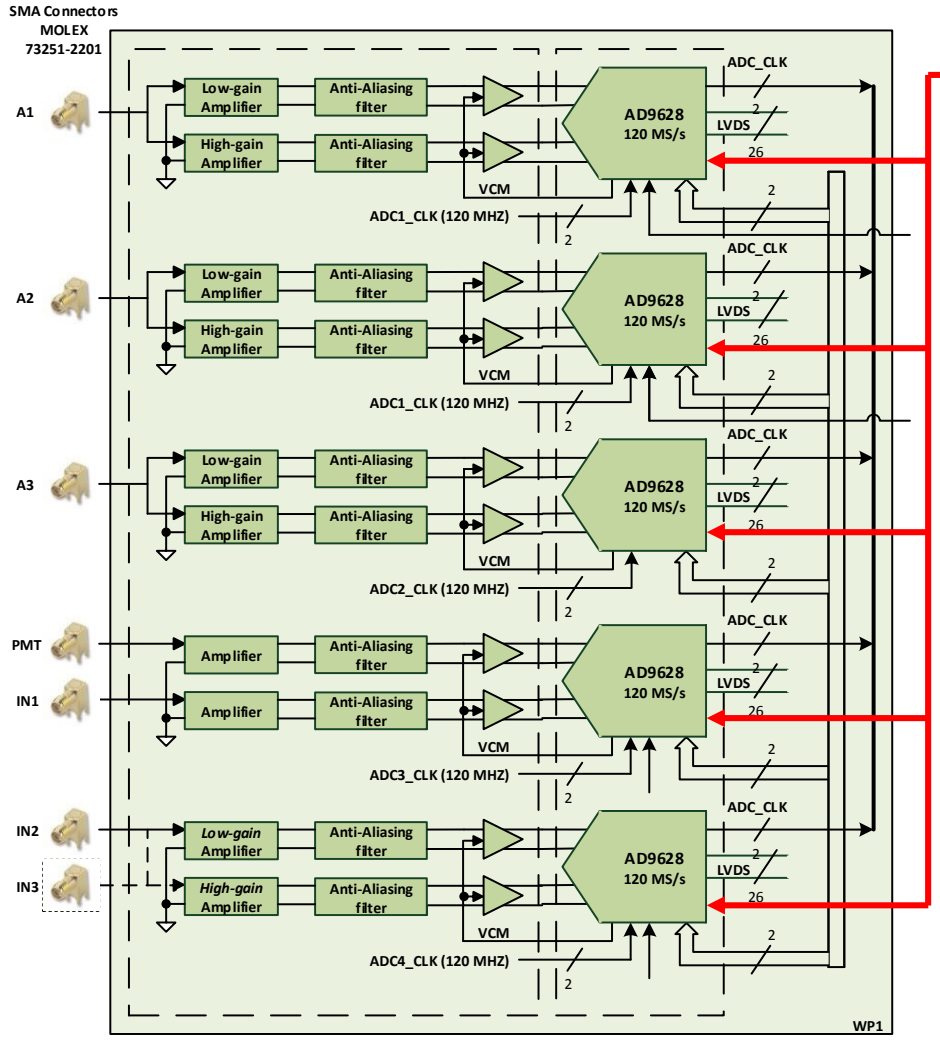
Through-hole = Strong

SMT = fragile

Can't be production problem. Basic connector.

ECR (Feb 2016) not integrated for EA

ECR 5-16, Optimized ADCs SDIO configuration:



Power_down (1 FPGA pin)

ADCs power down enable from FPGA:

- ADCs initialization.
- Low power when UUB starts.
- Better component's life.

New ECRs for the next UUB version

ECR (Dec 2016)

ECR 11.1, Add LC filters for +/-3,3V power supplies for Front-end amplifiers:

A DC/DC is an extremely noisy component.

ECR 14-1, -3,3V monitoring schematic:

Error in the schematic (NCR n° 2-52).

ECR 14-2, Change digital pressure sensor:

The BMP180 component is obsolete (NCR n° 2-61).

ECR 14.3, : Analog temperature sensor ESD protection:

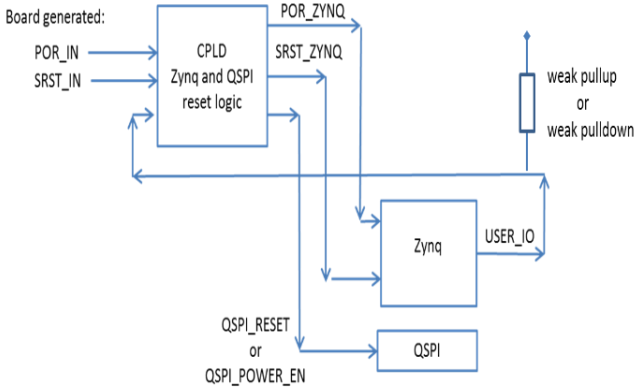
Remove ESD protection for temperature sensor 12V power supply pin (NCR n° 2-66).

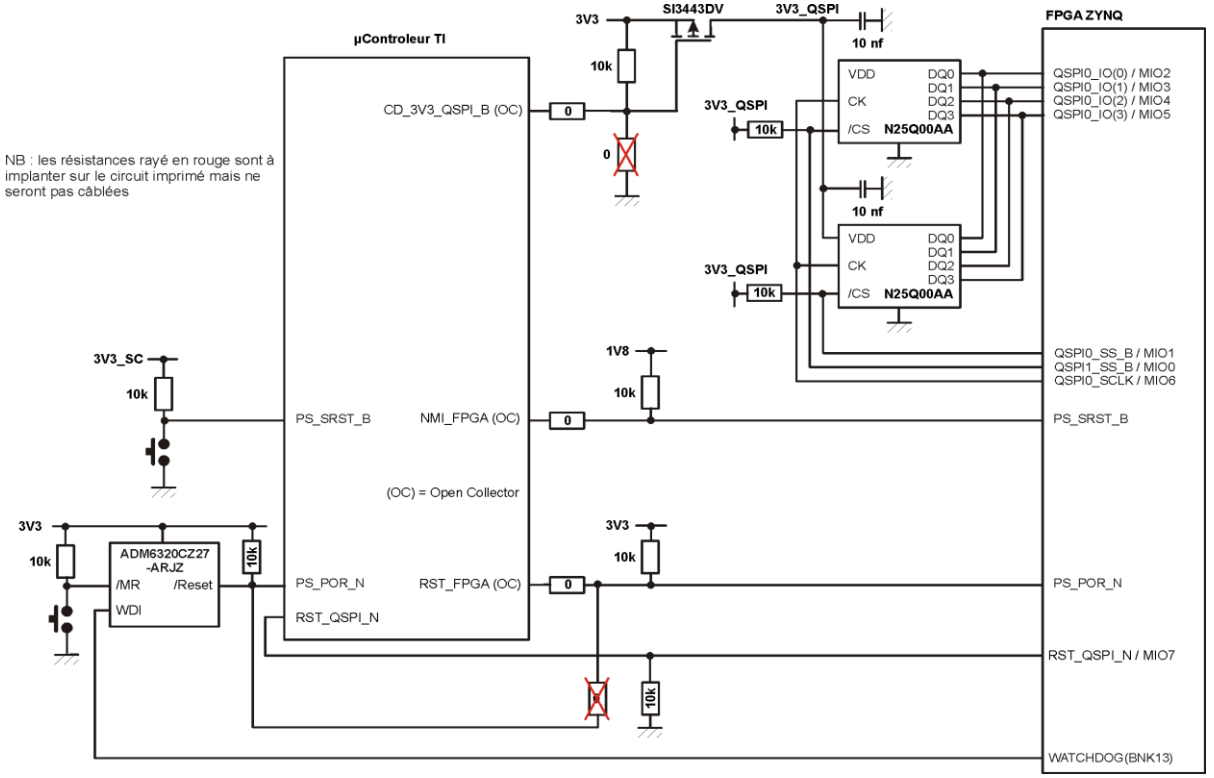
ECR (Dec 2016)

ECRs 14.4, 14.9 & 14.10, Resets specifications:

Never clearly specified:

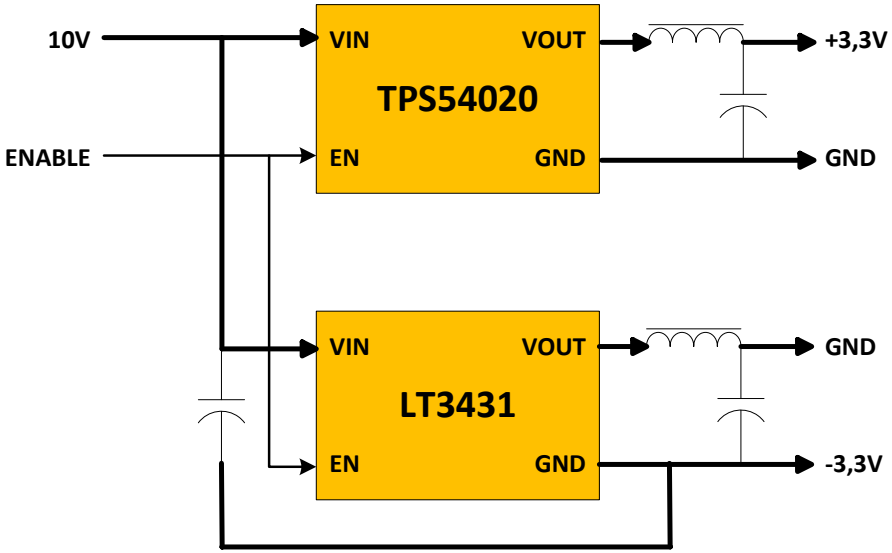
- Watchdog: Reset UUB (FPGA+SC) or only FPGA?
- "Radio" Reset: UUB (FPGA+SC) or only FPGA?

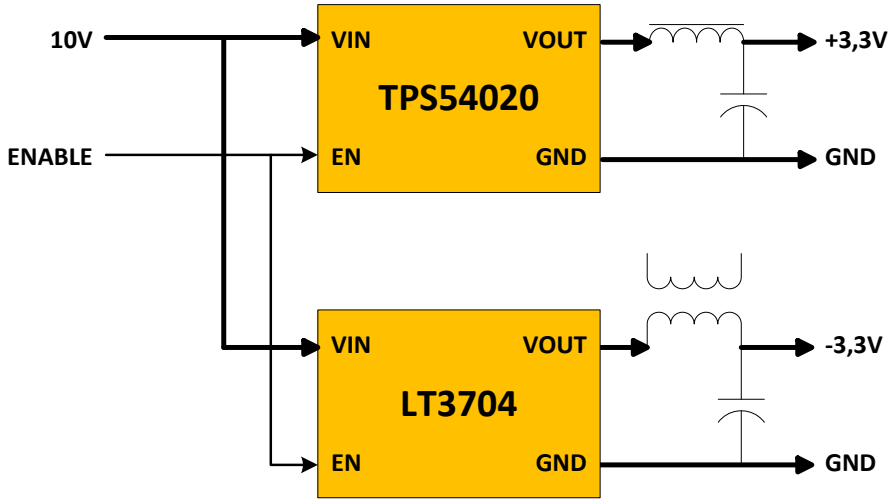




ECR (Dec 2016)

ECR 15-1, -3,3V DC/DC to be changed :





Charge pump technology
-3,3V is DC/DC voltage reference
-3,3V Enable, ERC 1-15(Feb 2016)

Not Charge pump technology: **less noisy**
¨Enable¨ NCR suppressed

Positive voltage -> negative voltage, noisy and low efficiency

ECR (Dec 2016)

ECR 15.2, RAM Layout must be modified:

Decoupling capacitor layout should be optimized to reduce noise

ECR 15.3, shielding plane on Top and Bottom layers for PCB:

Could decrease noise.

ECR 15.3, shielding ring for front-end on PCB:

Could decrease noise.

ECR (Dec 2016)

ECR 15.4 & 15.27, Optimized all DC/DC layout 1/2:

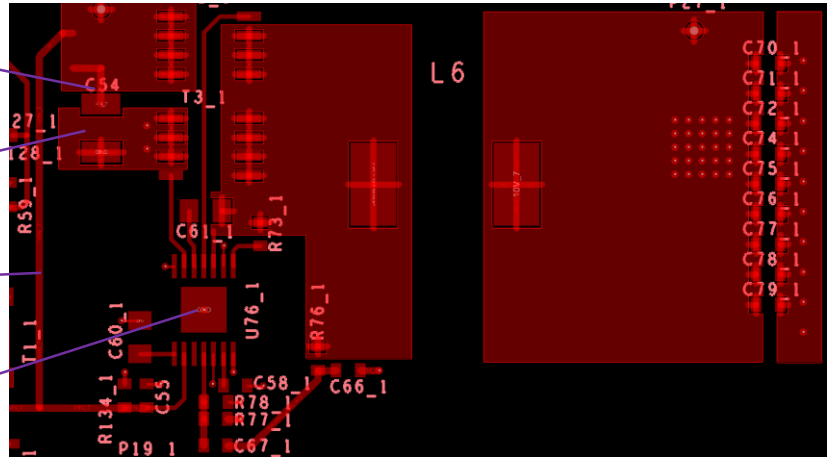
Change present 10V DC/DC LMR3150?

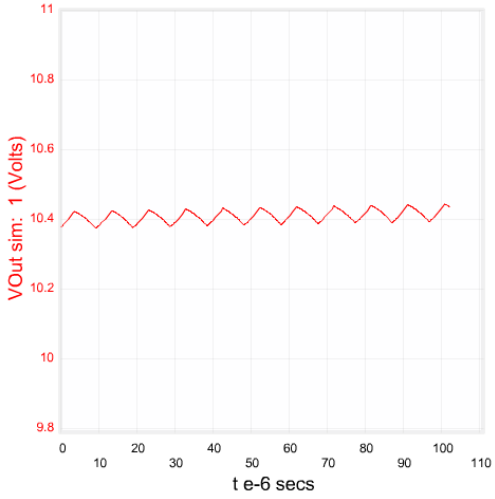
Design: adjust capacitor value

Layout: bad return current for input capacitor

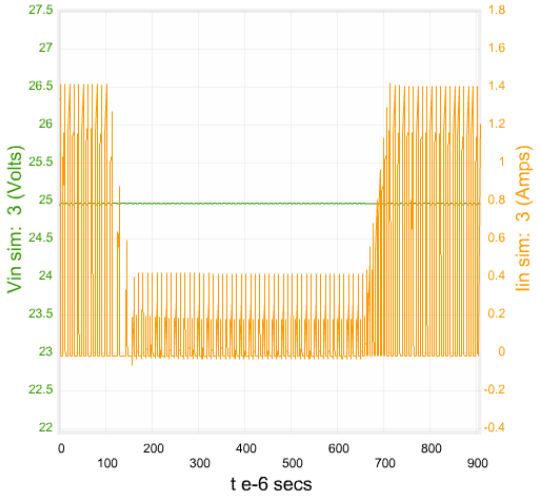
Layout: input 24V wire too thin (R bigger = more noise)

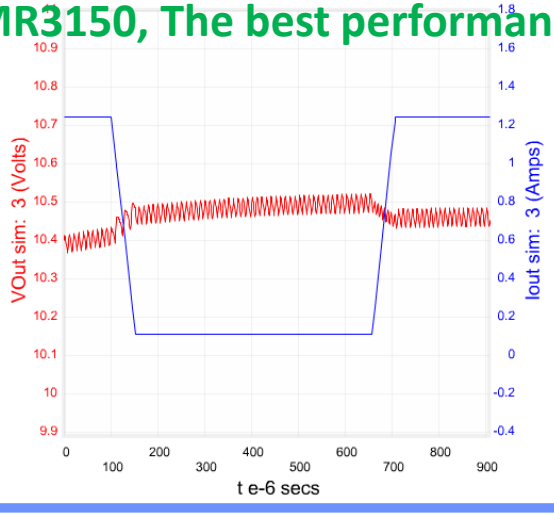
Layout: No GND junction center on DC/DC pad. Too few vias.

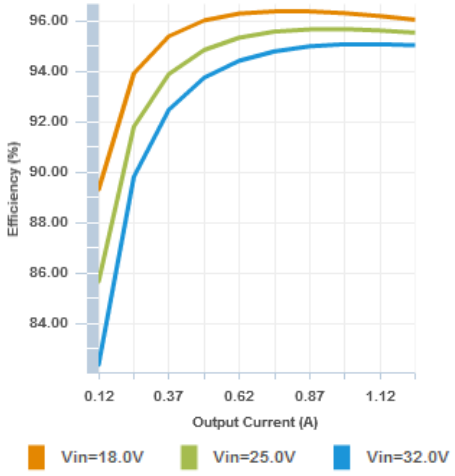




LMR3150, The best performances



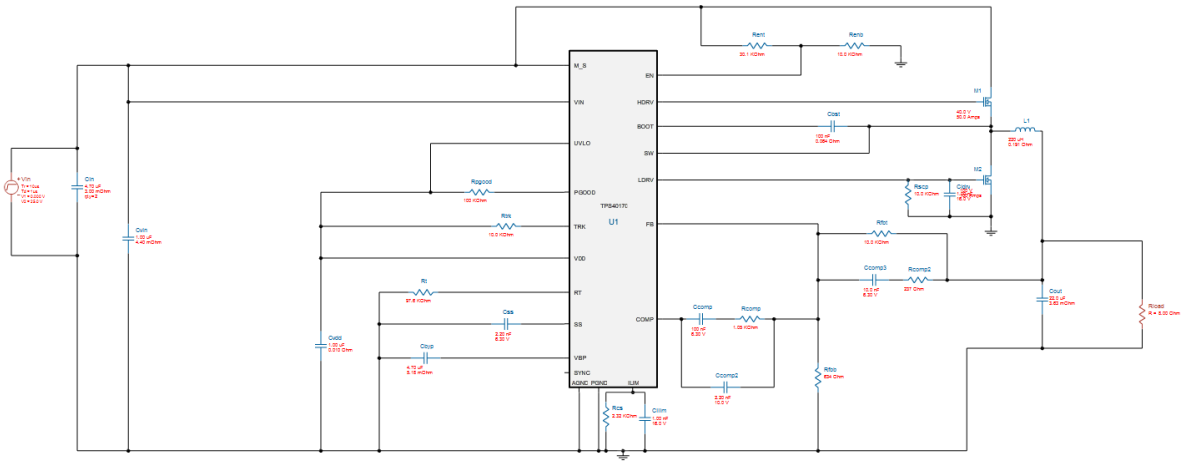


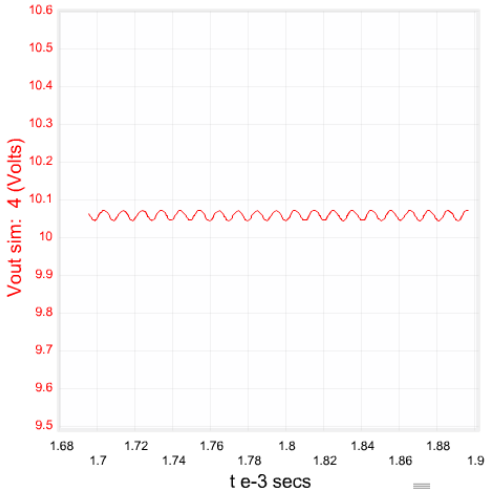


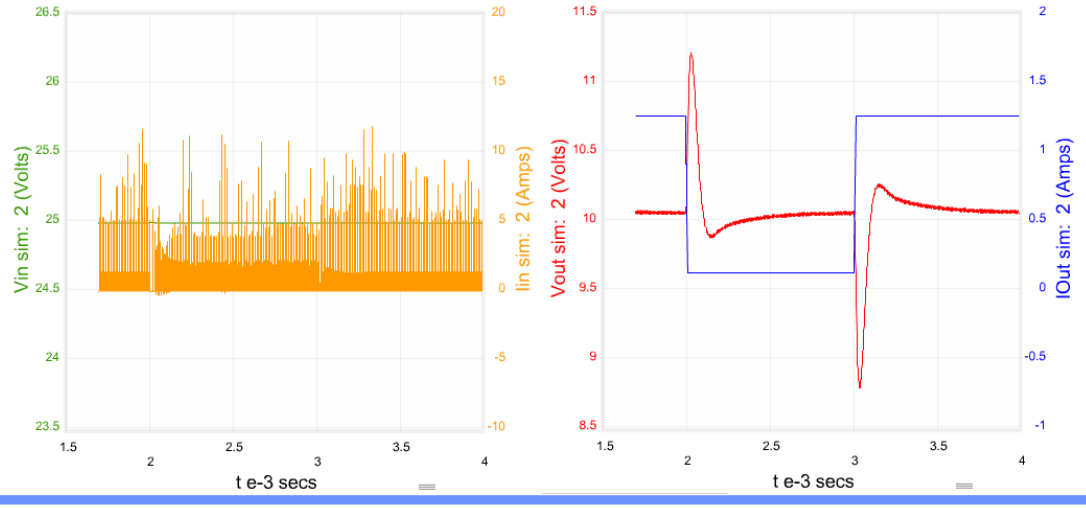
ECR (Dec 2016)

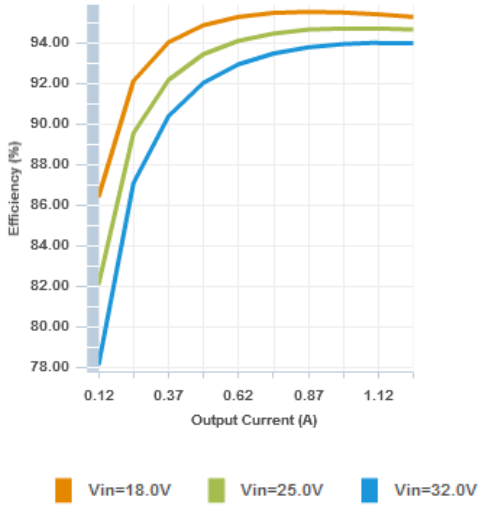
ECR 15.4 & 15.27, Optimized all DC/DC layout 2/2:

TPS40170, lower performance than LMR3150









ECR (Dec 2016)

ECR 15.5, Removed Digital External connector blocks:

Must stay on layout, without components on PCB.

Must be removed only if FPGA I/Os are useful.

Front Panel ???

ECR 15.6, Removed PMT6 connector:

Must stay on layout, with components on PCB.

Front Panel ???

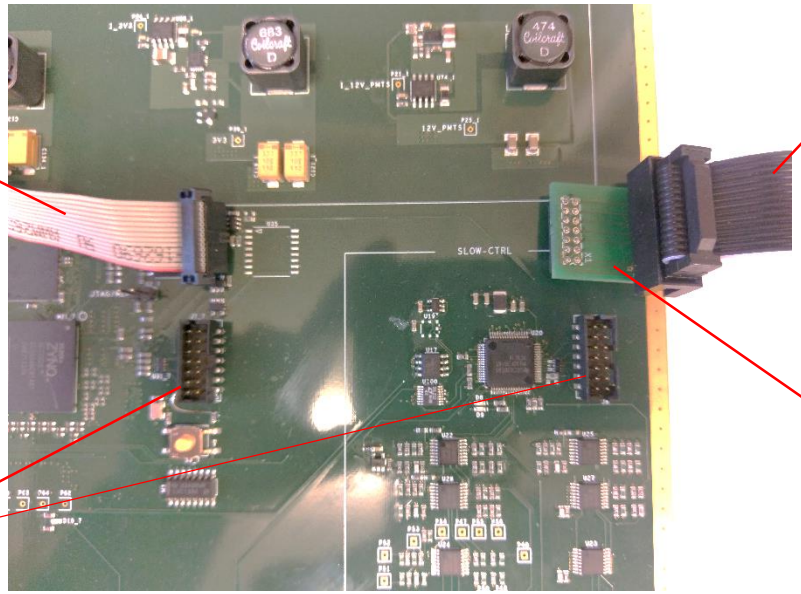
ECR 15.7, Changed J4 & J5 PMT connectors on PCB:

Less wire mechanical constraints in plug connector.

ECR (Dec 2016)

ECR 15.8, Change Slow-control JTAG connector:

Requested at first by KIT production center, but it is a problem for maintenance. Need to be changed to 2,54 mm pitch connector.



Xilinx JTAG probe:
2x7 pins 2 mm pitch

TI JTAG probe:
2x7 pins 2,54 mm pitch

2 mm to 2,54m converter daughter board

Connector on board:
2x7 pins 2 mm pitch

ECR (Dec 2016)

ECR 15.9, Remove FPGA Reset Switch on Front-panel:

Useless for maintenance. Use a switch somewhere on board.

ECR 15.10, Changed front-panel :

Stronger and IP57.

NCR n° 2-41, problems after manufacturing .

Old

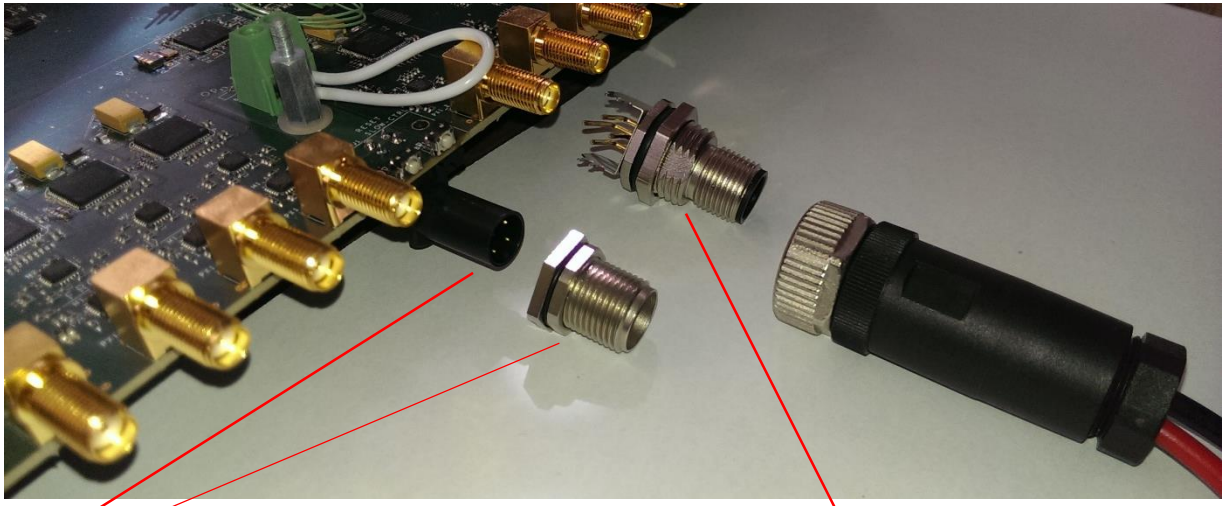
New

ECR (Dec 2016)

ECR 15.11, Change Power supply connector:

only one part and more robust. Less mechanical constraints.

Same plug.



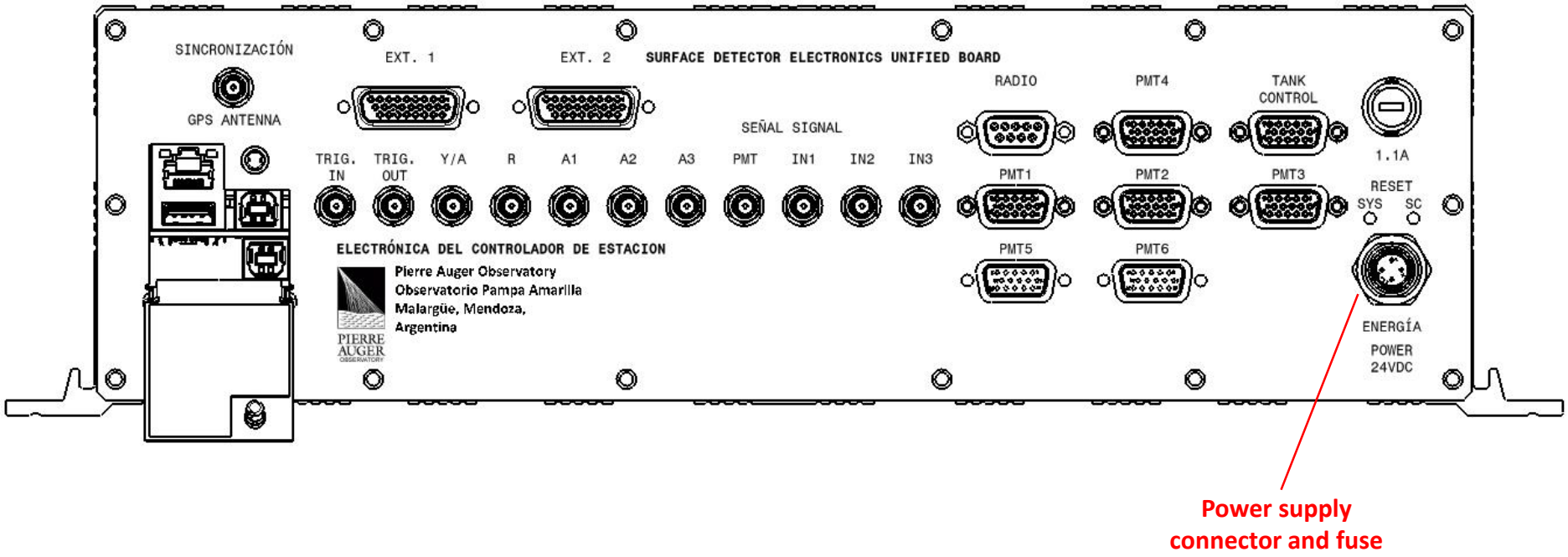
Present version:
2 parts

next version:
1 parts

ECR (Dec 2016)

ECR 15.12, Change Power supply connector position:

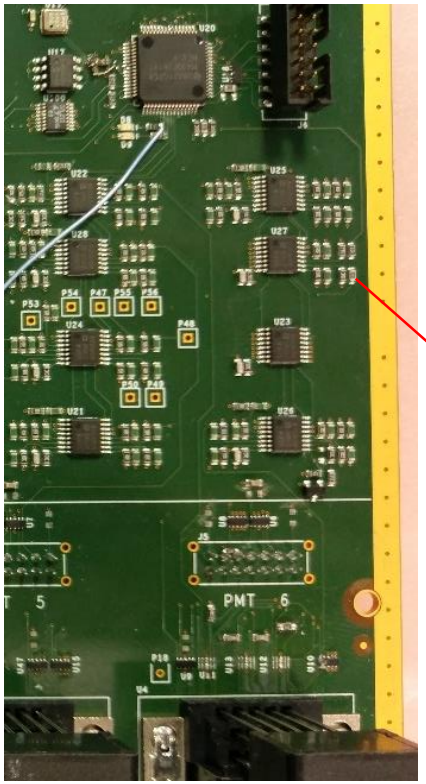
Away from Front-end area on PCB to lower the noise (actual position -> specification request).



ECR (Dec 2016)

ECR 15.13, Move Slow-control layout block:

Slow-control block must be moved to the left. Resistor could be in short-cut if they are too close the box.



Passive component could be in contact with box

ECR (Dec 2016)

ECR 15.14, 0402 package for Front-end & FPGA only:

Easier for maintenance.

ECR 15.15, Change 8x multi-switch reference:

Difficult to find. Footprint will change, new specs ?

ECR 15.17, Change "Radio" 12V & "PMTs" 12V DC/DC:

LMR24220 component does not have short-cut protection (NCR n°2-59). Changed by TPS54A20, but 80% of estimate efficiency only.

ECR 15.18, Change all tantalum capacitors:

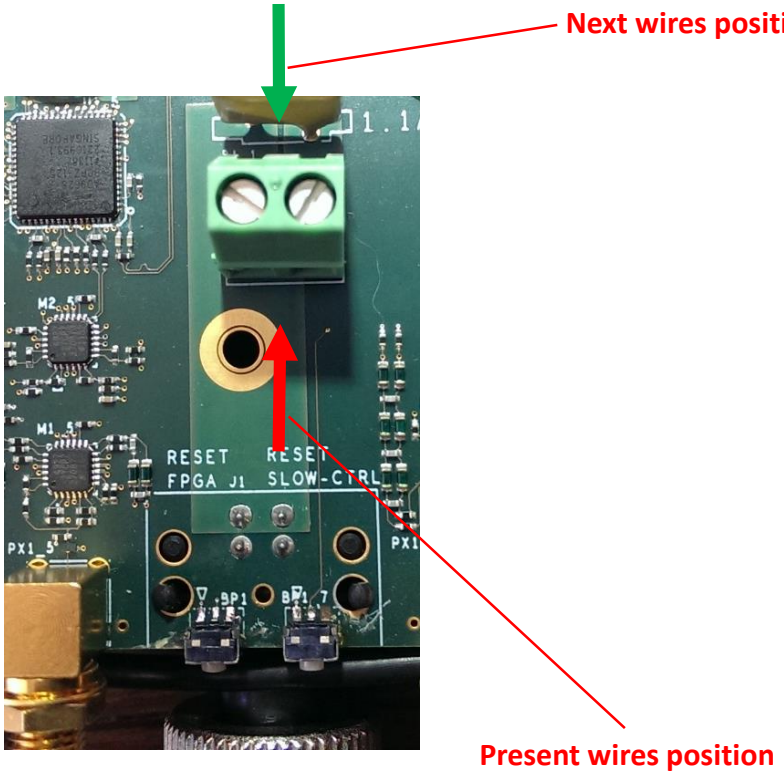
Change all tantalum capacitors by ceramic capacitors.

Less noisy and no burn risk.

ECR (Dec 2016)

ECR 15.16, Fuse wires connection to board:

Reverse screw connector for fuse wires (NCR n° 2-58).



ECR (Dec 2016)

ECR 15.19, Change LP-DDR2 component:

MT42L128M32D1-LF-25WT obsolete the 21/12/2016 (NCR n° 2-63). It could be changed by EDB4432BBPA-1D-F-R. Layout will change and not certified by Xilinx

ECR 15.20, "Radio" RS232 ESD protection:

Remove RCLAMP0524J.TCT ESD protection for MAX3218 RS232 interface (NCR n° 2-64). This component has already protection.

ECR (Dec 2016)

ECR 15.21, FPGA "start" Jumper :

The S2_7 jumper should be:

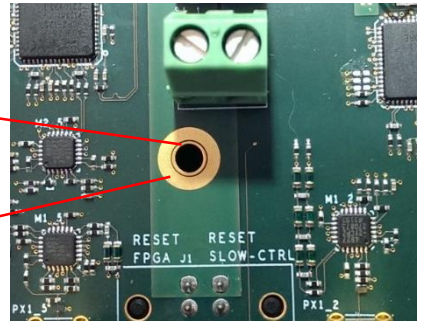
OPEN = Flash memory start

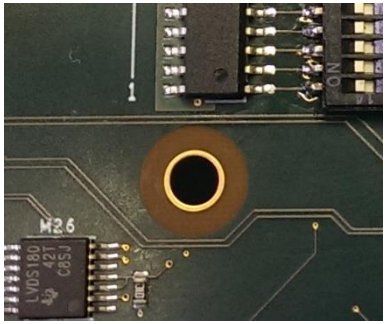
CLOSE = JTAG start

Open is stable connection. Jumper is not

ECR 5.11, Move or remove holes on PCB:

Holes was put on PCB in compliance with the UB. They are used only for debugging. Not used in SDE box.





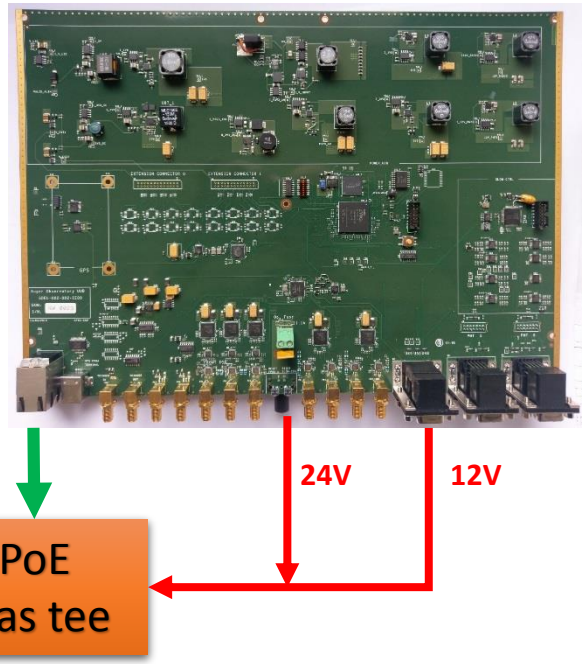
ECR (Dec 2016)

ECR 15.22, Ethernet PoE integration:

Combo connector Eth + USB with PoE: does not exist

No other solution than bias Tee

Auger Radio
OR
BULLET Radio
OR
Remove connector



ECR (Dec 2016)

ECR 15.23, Bigger PCB thickness:

The present PCB thickness is 1.52 mm (layout constraints). For mechanical constraints it could be good to increase to 1.8 mm maximum, if it is compliant with layout constraints.

Design Cross Section

Subclass Name	Type	Material	Thickness (MM)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MM)	Single Impedance (ohm)	Coupling Type	Spacing (MM)	Differential Impedance (ohm)	Unused Pin Pad Suppression	Unused Via Pad Suppression
	SURFACE	AIR		0	1	0									
TOP	CONDUCTOR	COPPER	0.04	595900	1	0			0.17	0	EDGE	0.13	0		
	DIELECTRIC	FR-4	0.1	0	4.3	0.035									
GND_1	PLANE	COPPER	0.0175	595900	1	0.035		Yes							
	DIELECTRIC	FR-4	0.2	0	4.3	0.035									
INT_1	CONDUCTOR	COPPER	0.0175	595900	1	0.035			0.19	0	EDGE	0.20	0		
	DIELECTRIC	FR-4	0.15	0	4.3	0.035									
ALIM_1	PLANE	COPPER	0.0175	595900	1	0.035		Yes							
	DIELECTRIC	FR-4	0.1	0	4.3	0.035									
INT_2	CONDUCTOR	COPPER	0.0175	595900	1	0.035			0.127	0	EDGE	0.13	0		
	DIELECTRIC	FR-4	0.2	0	4.3	0.035									
INT_3	CONDUCTOR	COPPER	0.0175	595900	1	0.035			0.13	0	EDGE	0.13	0		
	DIELECTRIC	FR-4	0.1	0	4.3	0.035									
ALIM_2	PLANE	COPPER	0.0175	595900	1	0.035		Yes							
	DIELECTRIC	FR-4	0.15	0	4.3	0.035									
INT_4	CONDUCTOR	COPPER	0.0175	595900	1	0.035			0.131	0	EDGE	0.20	0		
	DIELECTRIC	FR-4	0.2	0	4.3	0.035									
GND_2	PLANE	COPPER	0.0175	595900	1	0.035		Yes							
	DIELECTRIC	FR-4	0.1	0	4.3	0.035									
BOTTOM	CONDUCTOR	COPPER	0.04	595900	1	0			0.15	0	NONE				
	SURFACE	AIR		0	1	0									

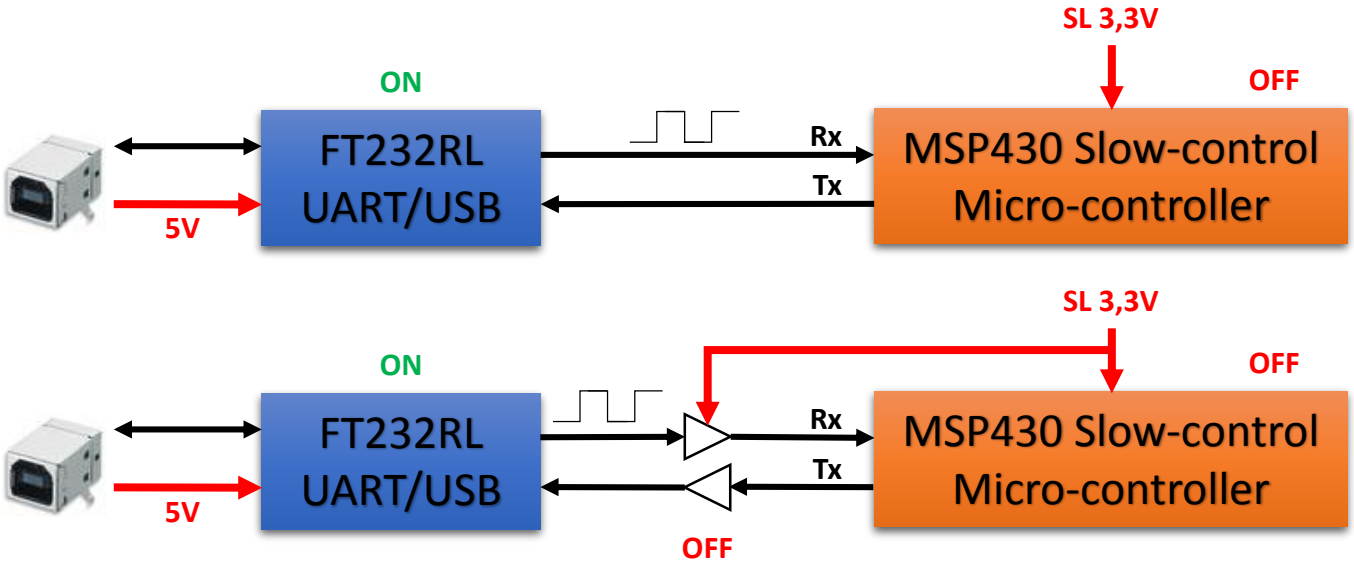
Total Thickness: 1.52 MM

Thickness is final PCB manufacturer dependent

ECR (Dec 2016)

ECR 15.24, Start problem Slow-control micro-controller:

Sometime, the micro-control stopes during start sequence (NCR n° 2-67). Only when a PC is connected before the UUB turn ON.



This must be made also for FPGA UART.

ECR (Dec 2016)

ECR 15.25, Reset switch label positions:

Change label position. They are in reverse position. Modification in layout.

ECR 5.12 (feb 2016), Stiffener integration:

It was removed because it was not useful for EA . But for the mass-production, its status is still open.

ECR 12.3, VHDL code optimization:

During EA, the consumption increased around 1,5 Watts, when the final VHDL code was integrated. The power consumption is strongly VHDL dependent.

ECR (Dec 2016)

- **ECR 15.26, Front-panel window:**

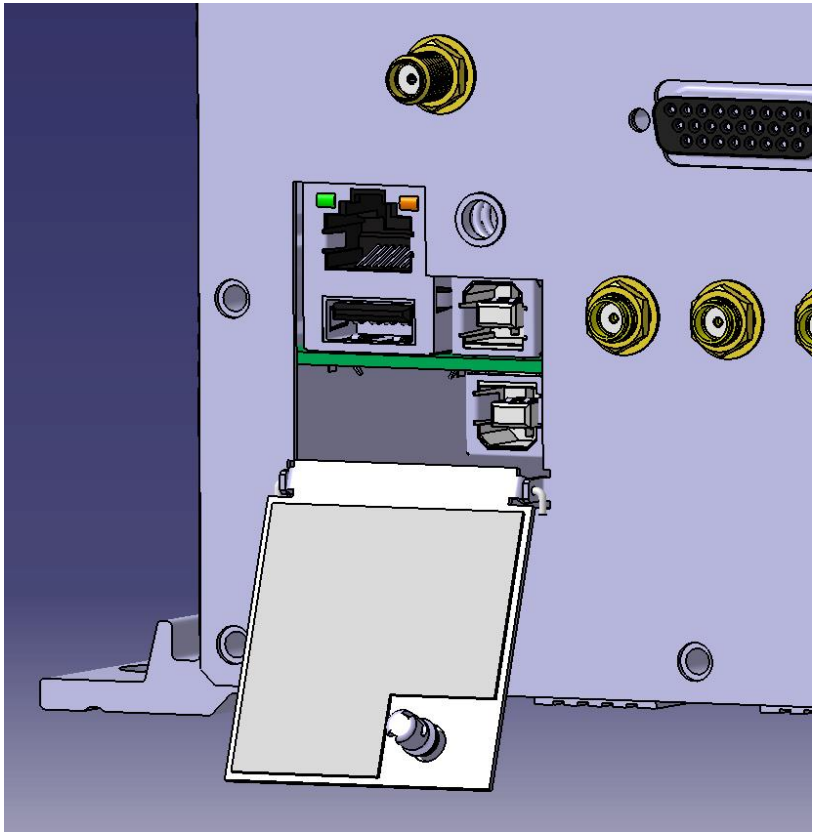
  The Front-panel window is still not defined or confirmed. Presently only the WP5 proposal is available.

WHAT?

HOW ?

WHO?

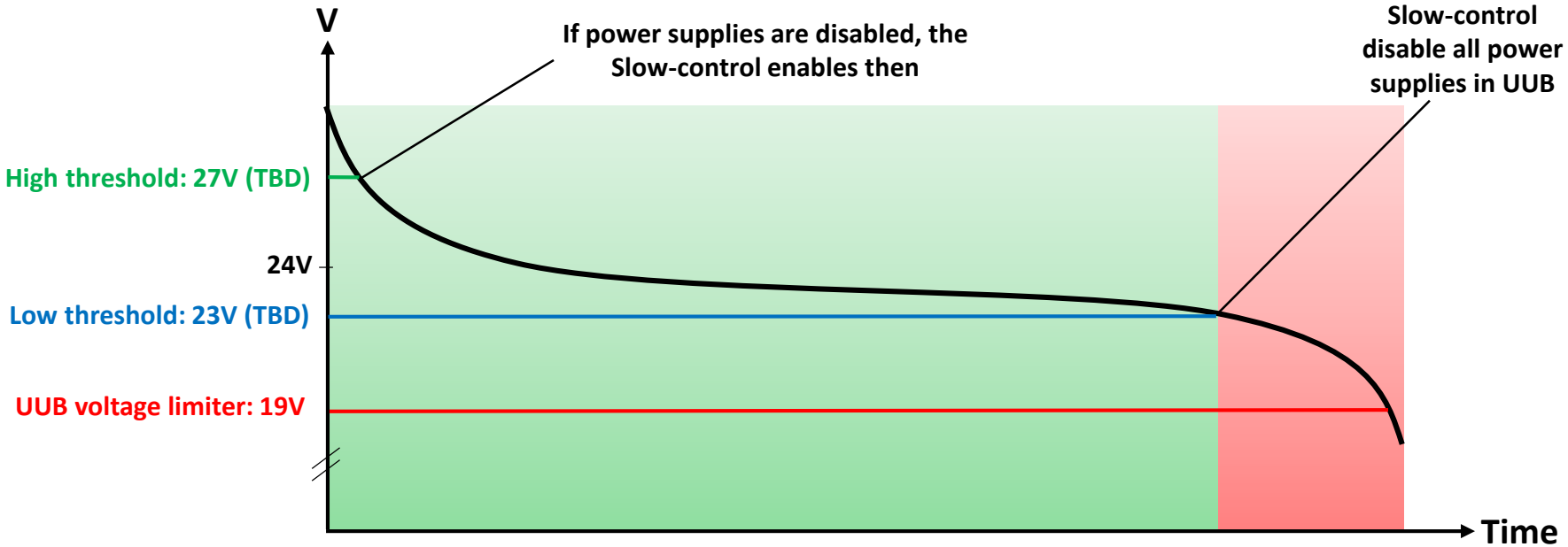
WHEN?



ECR (Dec 2016)

ECR 15.29, Solar power system Slow-control management:

If the battery voltage is too low, the electronic will twinkle. Could damage electronic and battery.



Battery Discharging curve

No hardware modification, only Slow-control software.

ECR (Dec 2016)

ECR 15.34, FPGA cooling solution:

The FPGA must be cooled.

Cooling must be specified

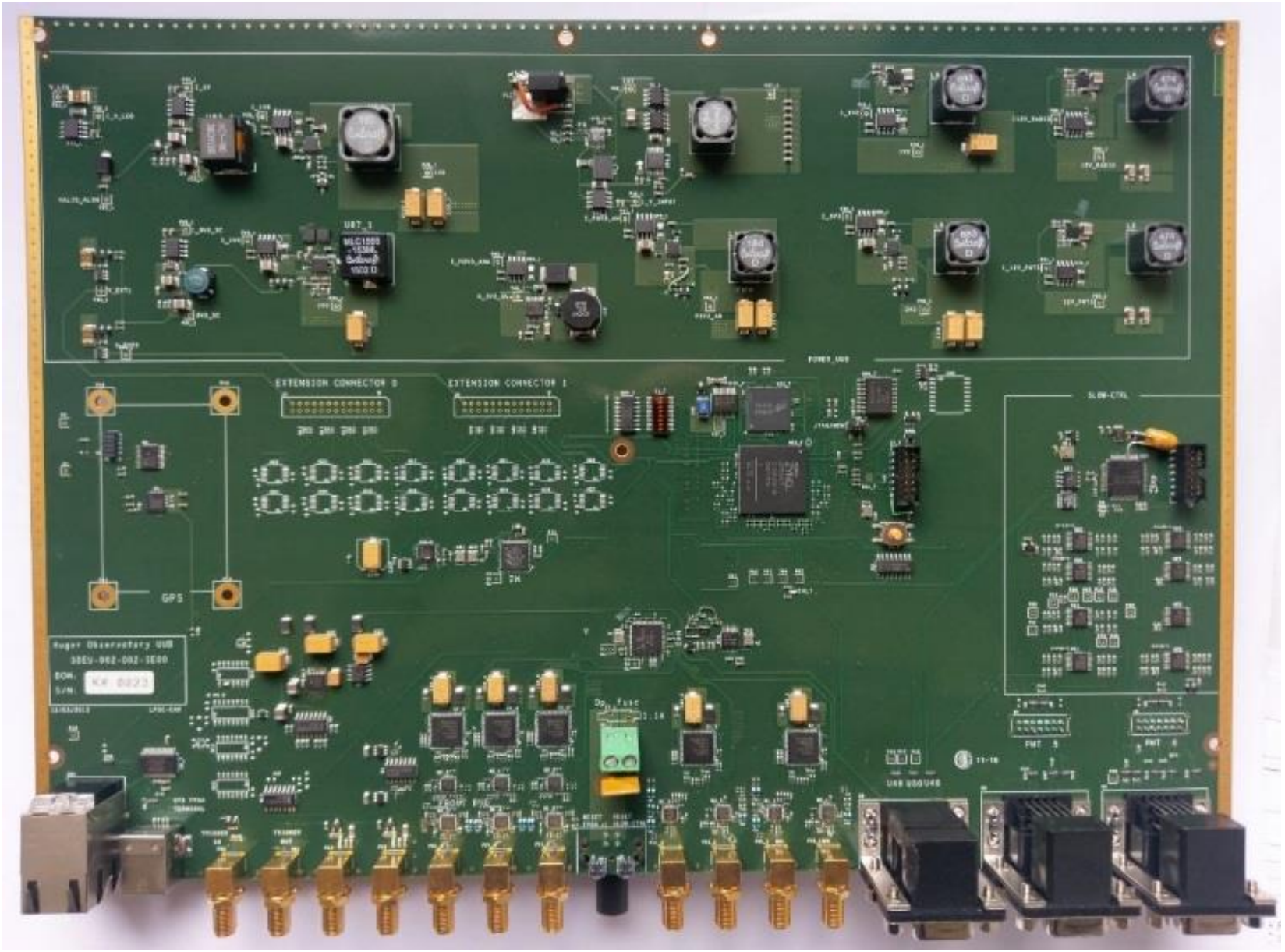
Possible component:

Wakefield-Vette 901-19-2-23-2-B-0 and thermic glue or clip (Layout must be modified)

19x19x23 mm, natural convection: 10,55 C°/W

Conclusion

- All WPs design (Schematic & BOM) must be validated by them. Layout will start when all WP designs will be validated.
- WPs must check obsolescence status for their design.
- Only corrections must be integrated for the new UUB version. New good ideas has schedule impact (manufacturing, test, validation,…), mass production is foreseen end 2017.


EXTENSION CONNECTOR 0
EXTENSION CONNECTOR 1
GPS
SLOW-CTRL