Pierre Auger Observatory

Surface Detector Electronics Upgrade

UUB Pre Prototype Production Report

UUB Model version: SDE-002-002-IE00

Document written by: E. Lagorio *Institute:* LPSC Grenoble	*verified by:* P. Stassi
Date: *24 November 2016*	*Date:* *19 November 2016*
ATRIUM Reference: *120770*	*Project Reference:* *WP05-LPSC-20D*

Table of Content

1 Global modifications: 5
1.1 TOP side modifications: 5
1.2 BOTTOM side modifications: 6
2 WP5 modifications: 7
2.1 Valid_Alim modification: 7
2.2 Voltage limiter: 8
2.3 120 MHz Oscillator control DAC: 8
2.4 USB interface modification: 10
2.5 USB VBUS resistor: 11
2.6 USB Power supply: 12
2.7 -3,3 Volts power supply enable: 13
2.8 FPGA boot configuration jumper: 15
2.9 GPS antenna voltage configuration: 15
3 Slow-control modifications (WP4): 17
3.1 Reset/Done modification: 17
3.2 Vref decoupling capacitors: 18
3.3 Slow-Control Reset Pull-up: 18
3.4 Watchdog modification: 19
4 LED-CONTROLER (WP6): 20
4.1 I²C interface: 20
4.2 Logic integration: 20
5 Front-end (WP1): 21
5.1 Offset 1 & 2 wrong decoupling capacitors positions: 21
5.2 Offset 1 & 2 decoupling capacitors: 22
5.3 Vref modifications: 24
5.4 Type 3, input impedance modifications: 25
5.5 OFFSET_1 & OFFSET_2 Vref values: 26
6 EngineEring array modifications: 28
6.1 "Radio RS232" ESD protection: 28
6.2 Slow-control ESD protection and Temperature sensor power supply modification (WP4 & 5): 28
6.3 TRIGGER in modification: 30
6.4 "RADIO Reset" modification: 31
7 MATERIAL: 32
7.1 Bill Of Material: 32

ACRONYMS

ADC	Analog to Digital Converter
BGA	Ball Grid Array
BOM	Bill Of Material
CR	Configurational Requirement
DC	Direct Current
ER	Environmental Requirement
FPGA	Full Programmable Gate Array
FR	Functional Requirements
GPS	Global Positioning System
ICD	Interfaces Control Document
IR	Interface Requirements
n/a	non applicable
OR	Operational Requirements
PBS	Product Breakdown Structure
PCB	printed Circuit Board
PR	Physical Requirements
QR	Quality Requirements
SDE	Surface Detector Electronics
SR	Support Requirements
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UB	Unified Board
UUB	Upgraded Unified Board
UHE	Ultra High Energy
UHECR	Ultra High Energy Cosmic Ray
VM	Verification Matrix

DOCUMENT CHANGE RECORD

Issue	Revision	Issue Date	Changes Approved by	Modified Pages Numbers, Change Explanations and Status
20	A	08/03/16	E. Lagorio	First version
20	B	22/08/16	P. Stassi	First diffusion
20	C	18/09/16	E. Lagorio	Engineering Array modifications (page 5, 6, 28, 29, 30 and 31)
20	D	24/11/2016	E. Lagorio	Bad value for R139_1

1 GLOBAL MODIFICATIONS:

This document describes all the retro-fitting action on the boards after their manufacturing. This manufacturing must be made with SDE-002-002-IE00-VA01 13 April 2016 BOM version.

Below find the location of the modifications on the UUB board, TOP and BOTTOM sides. All modifications are specifically described.

1.1 TOP side modifications:

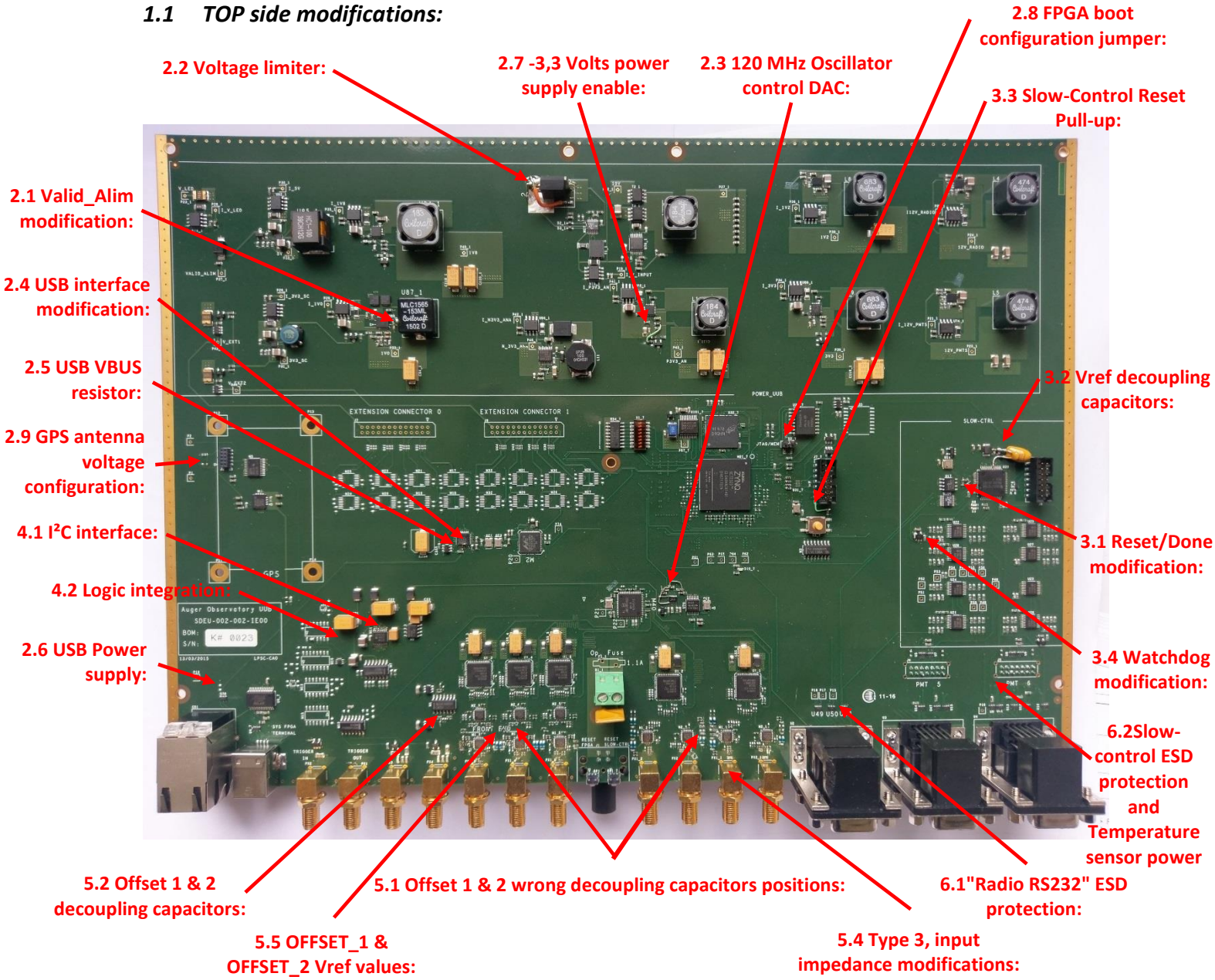

Figure 1: TOP side Modifications.

1.2 BOTTOM side modifications:

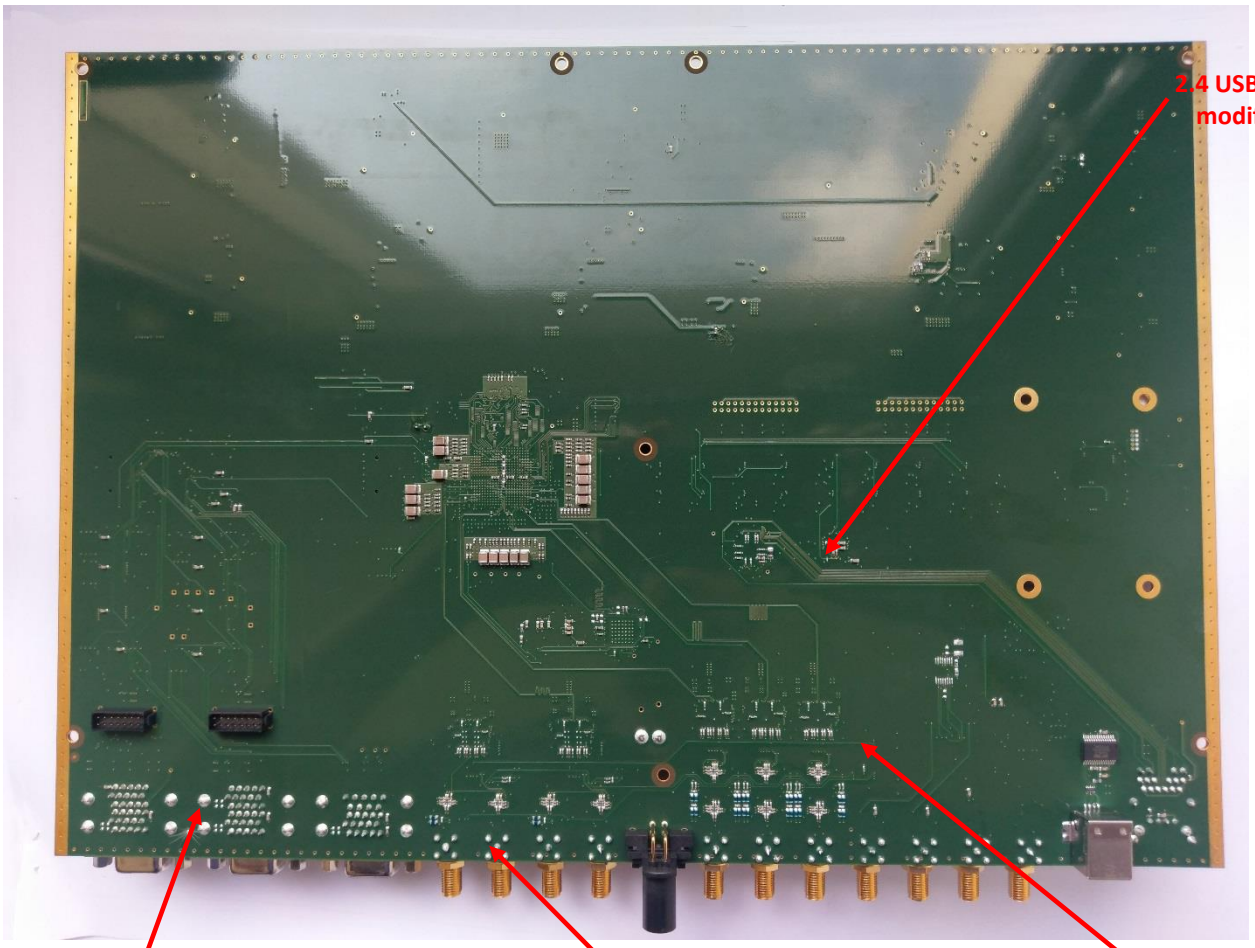

Figure 2: BOTTOM side Modifications.

2 WP5 MODIFICATIONS:

2.1 Valid_Alim modification:

The Valid_Alim is generated by 1 Volt DC/DC converter, from its “power good” pin.
R100_1 is removed.
A 1,5 K Ohms 1 % resistor, 0603 package must be added between VDD (U86_1 pin 10) and PGOOD (U86_1 pin 11).

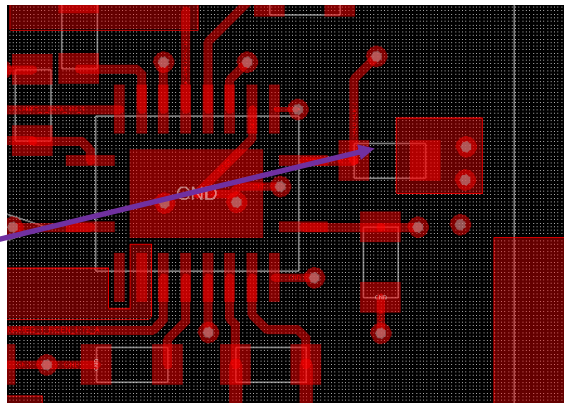

Figure 3: R100 removed

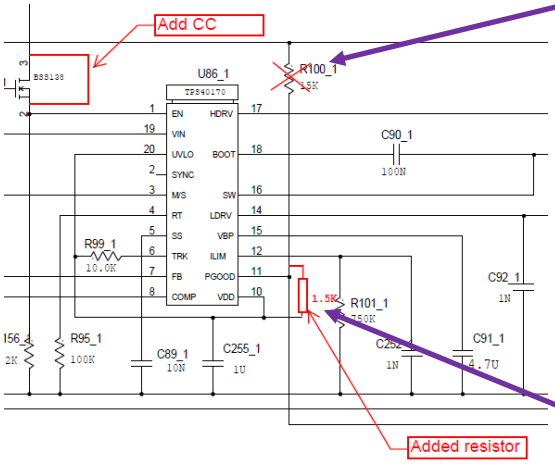

Figure 4: Valid_Alim modification in schematic (page 11)

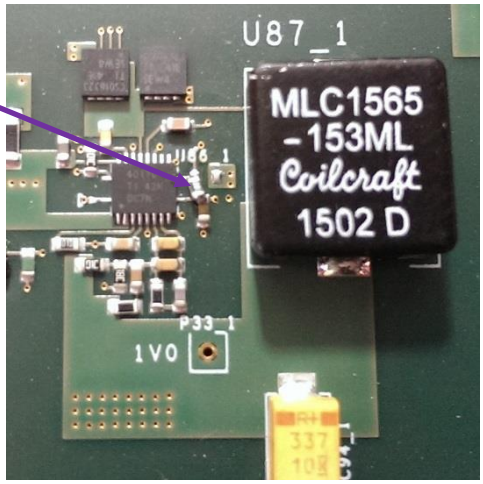

Figure 5: 1,5 k Ohms resistor, and 0603 package added.

The added components:

- R1_X, 1.5 KOhms 1% 0603 (available in UUB BOM, ref.: RES-068)

Number of operation: 1

2.2 Voltage limiter:

Wrong footprint for Q4_1 transistor. Pins 2 & 3 must be swapped.

Transistor Pin 3 must be soldered to footprint pin 2

Transistor Pin 2 must be soldered to footprint pin 3

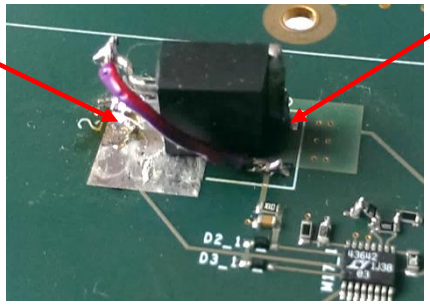

Figure 6: Pin 2 &3 Swap connection.

The connection between transistor pin 1 to the footprint must be made by a wire.

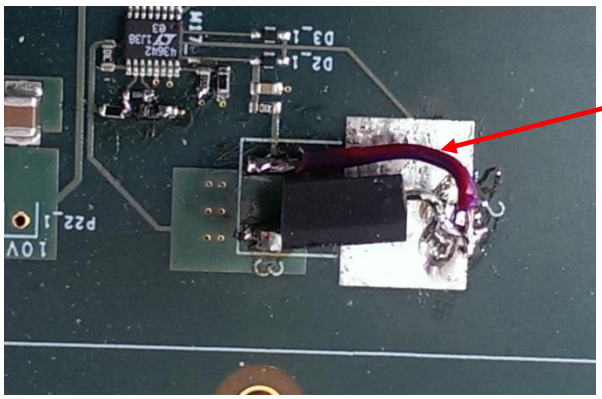

Figure 7: Pin 1 wire connection.

Number of operation: 1

2.3 120 MHz Oscillator control DAC:

DAC7551 IOVDD pin must be connected to 3,3 Volt (1,8 volt previously) power supply and the pull-up resistors R382, R383, R384, R385 & R386 too.

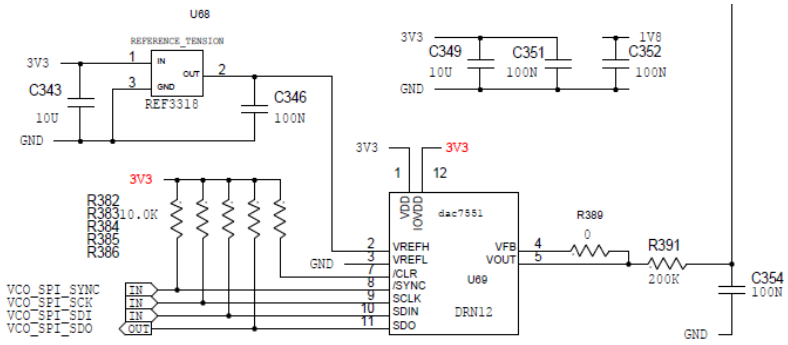

Figure 8: DAC7551 Power supply modifications (Schematic page 6).

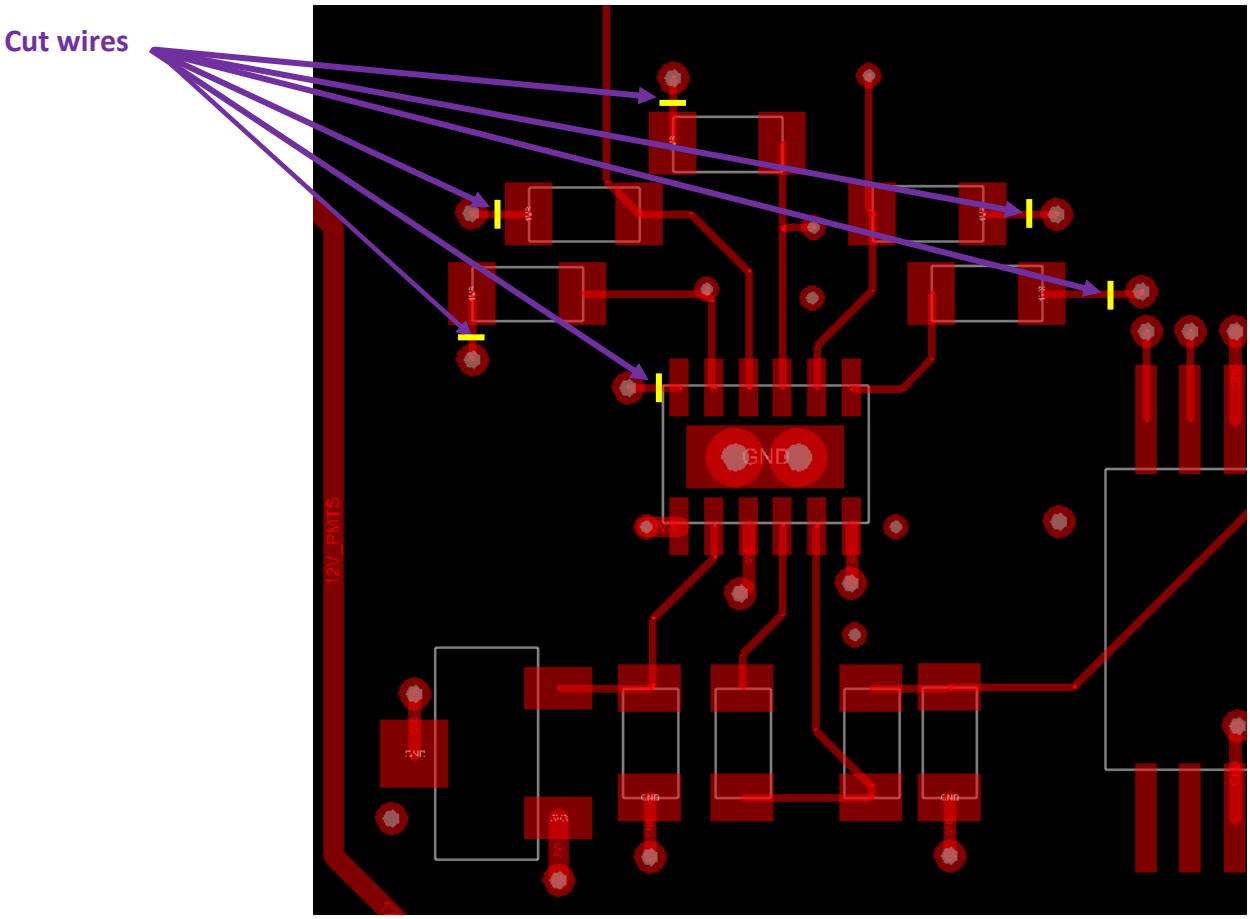

Figure 9: Cut DAC7551 1,8 Volts Power supply wires.

3,3 Volts power supply modifications. Add wire between U69 pin 12 and resistor R382, R383, R384, R385 & R386

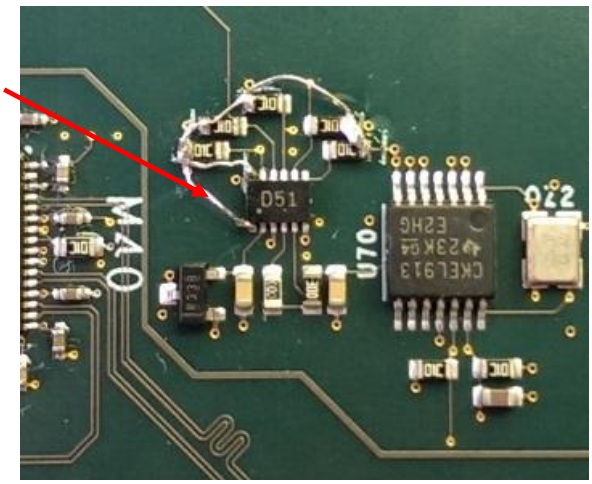

Figure 10: DAC7551 Power supply modifications on UUB

Number of operation: 8

2.4 USB interface modification:

U36 pin 20 must be disconnected from 3,3 Volts and connected to U36 pin 23.

U36 pin 23 must be disconnected from 1,8 Volts and connected to 3,3 Volts.

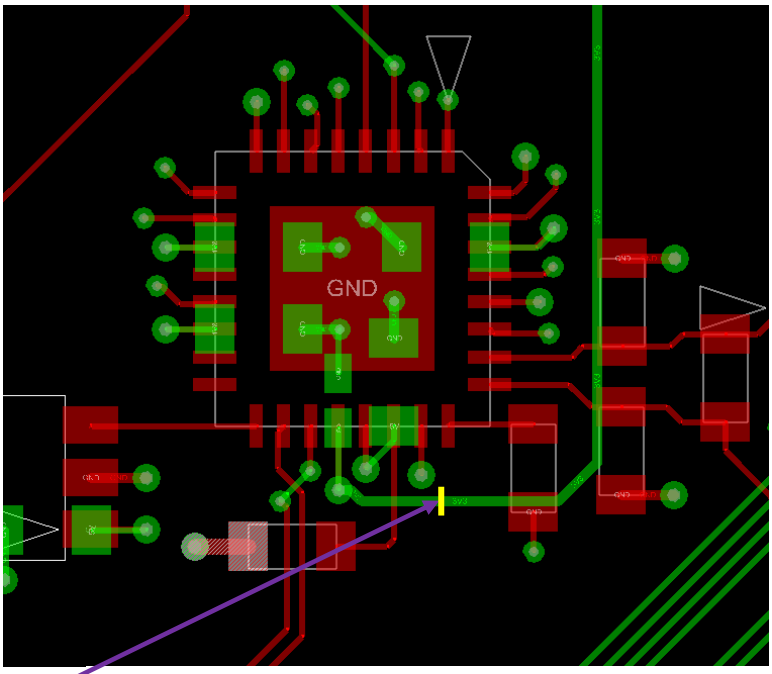

Figure 11: 3,3 Volts wire cut.

Cut wires

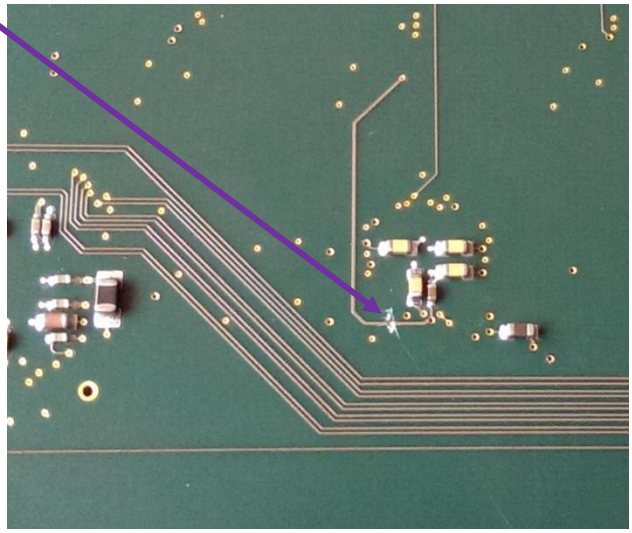

Figure 12: 3,3 Volts wire cut on bottom side.

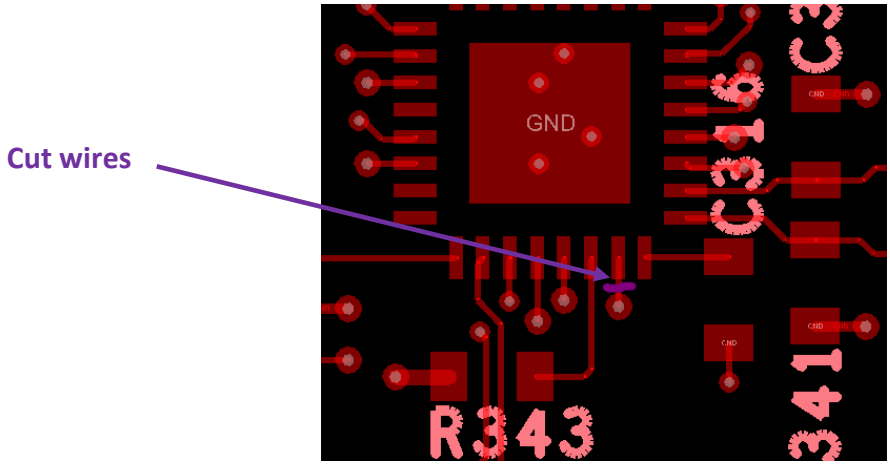

Figure 13: 1,8 Volts wire cut.

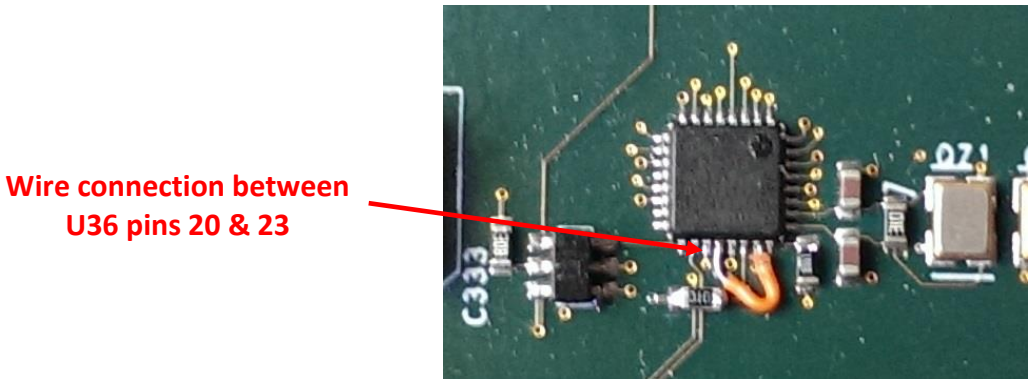

Figure 14: U36, pins 20 & 23 wire connection.

Number of operation: 3

2.5 USB VBUS resistor:

The VBUS R343 resistor value is bad in the Bill Of Material. It must be 1 kOhms instead 10 kOhms (NCR n° 2-43).

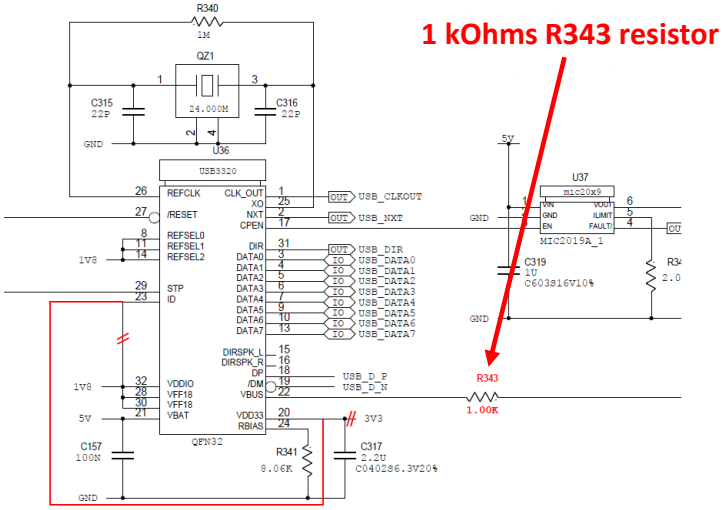

Figure 15: R343 resistor value changed to 1 kOhms (Schematic page 4).

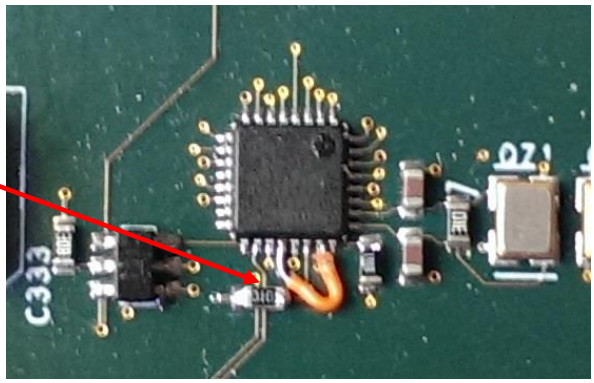

Figure 16: 1 kOhms R343 resistor on board.

Number of operation: 2

2.6 USB Power supply:

The FE5 coil has been forgotten in the BOM. A 0 Ohm resistor or a short-cut could be put (NCR n° 2-42).

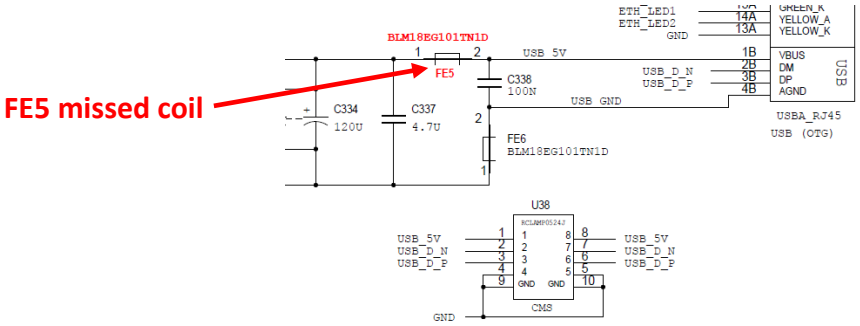

Figure 17: Missed FE5 coil (Schematic page 4).

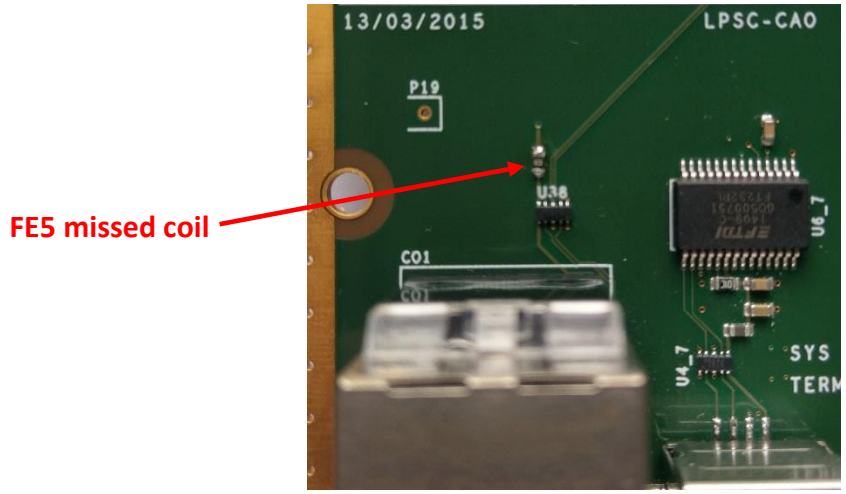

Figure 18: Missed FE5 on board.

Number of operation: 1

2.7 -3,3 Volts power supply enable:

For the SDE-002-002-IE00 UUB board only, the +/- 3,3 Volts Enable will be send from the Slow-Control micro-controller (3,3Volts) to U97_1 +3,3V DC/DC pin15 (EN) and U18_1 -3,3V DC/DC pin 15 (/SHDN). The +3,3V DC/DC output will enable the -3,3V DC/DC enable.

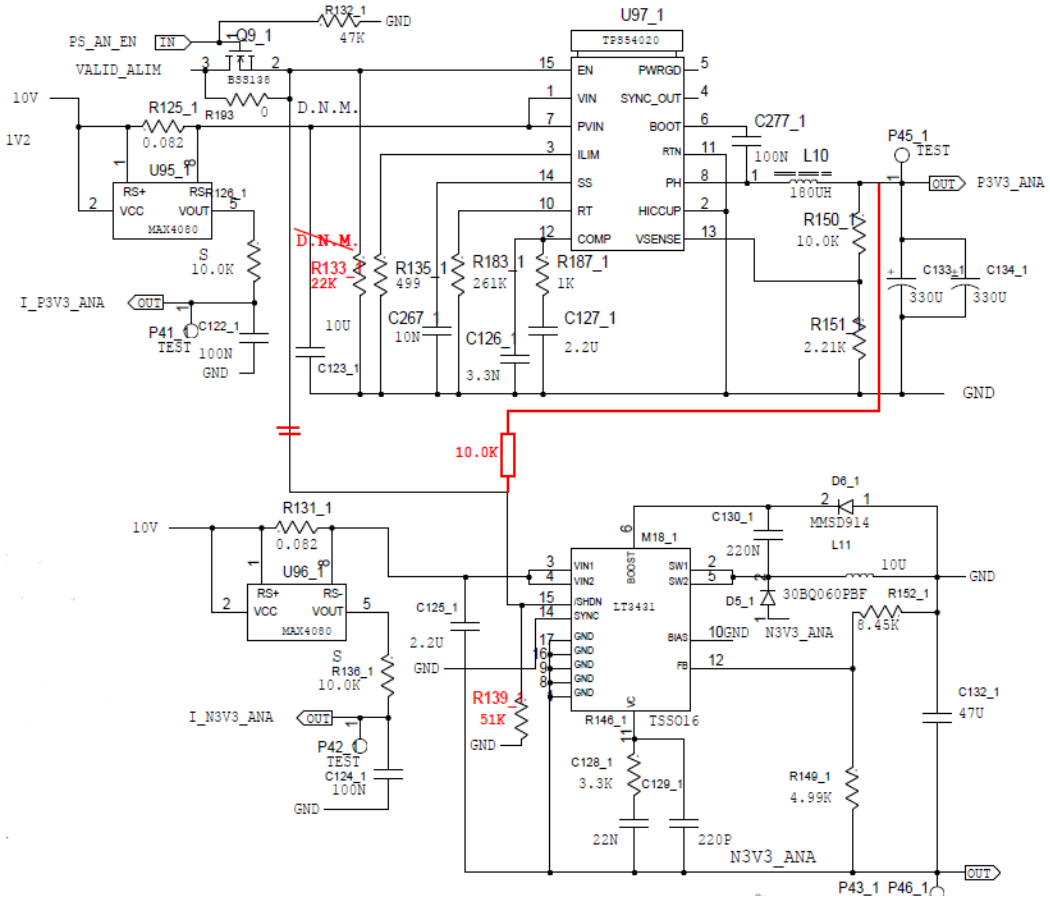

Figure 19: +/- 3,3 Volts Enable modification (Schematic page 10).

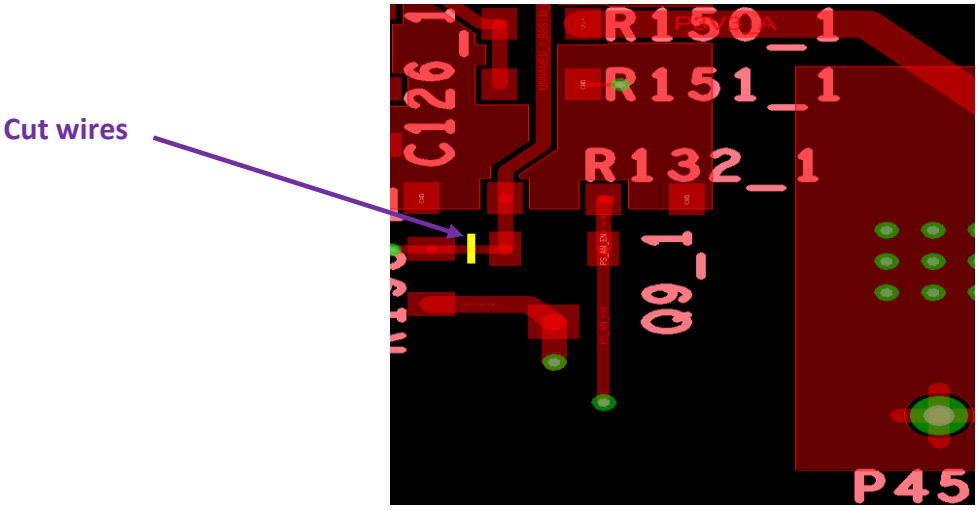

Figure 20: Wire cut.

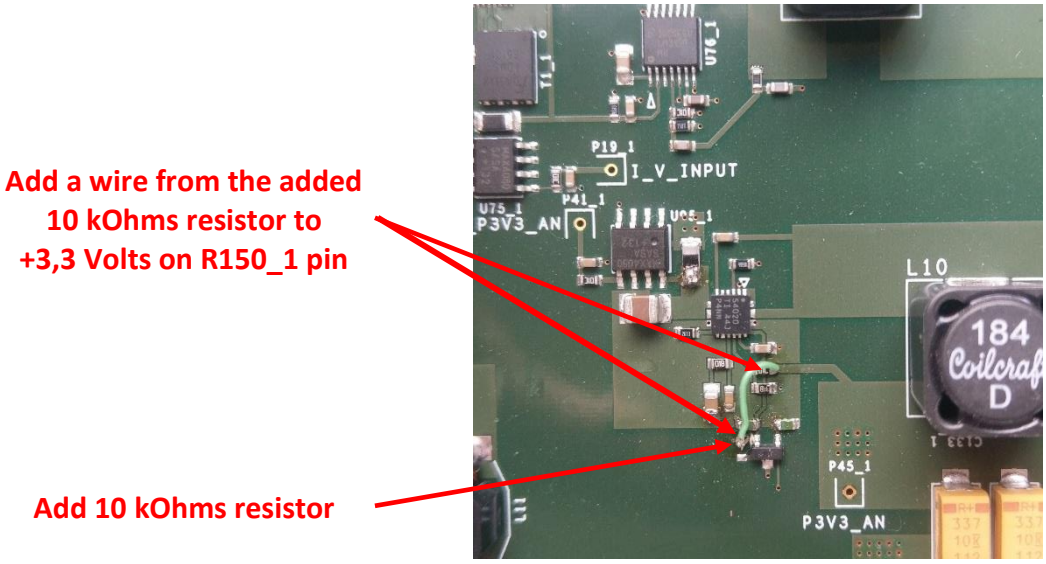

Figure 21: Top side modifications.

R139_1 resistor value must be changed from 22 kOhms to 51 kOhms.

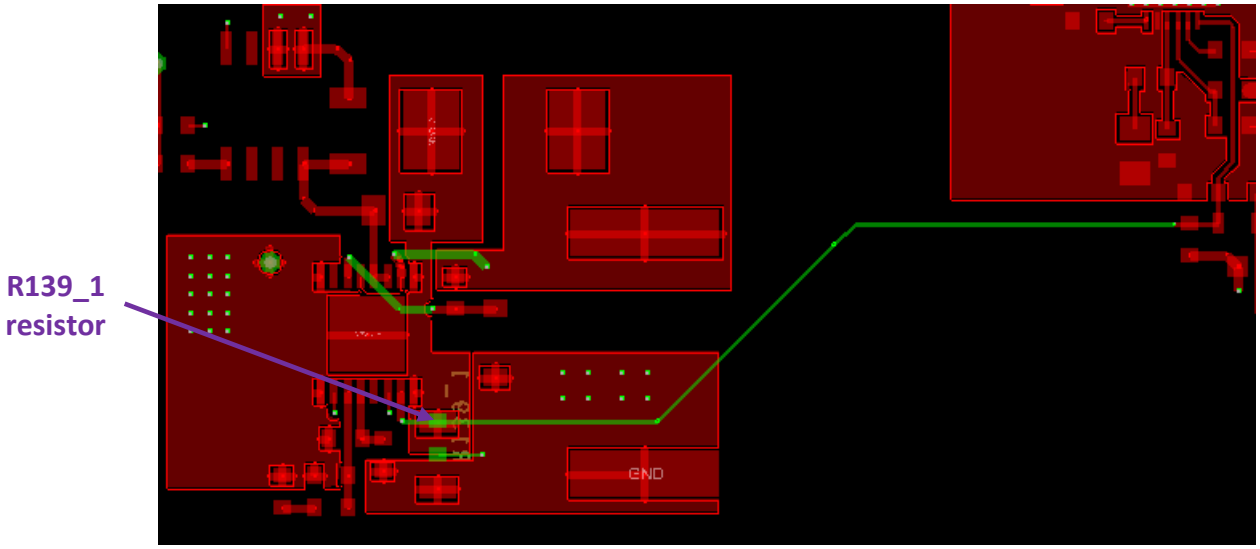

Figure 22: BOTTOM side R139_1 resistor value modification.

The added components:

- R2_X, 10 KOhms 1% 0603 (available in UUB BOM, ref.: RES-017)

Number of operation: 5

2.8 FPGA boot configuration jumper:

The boot configuration jumper (S2_7) has been forgotten in the Bill Of Material (NCR n° 2-1). It must be added.

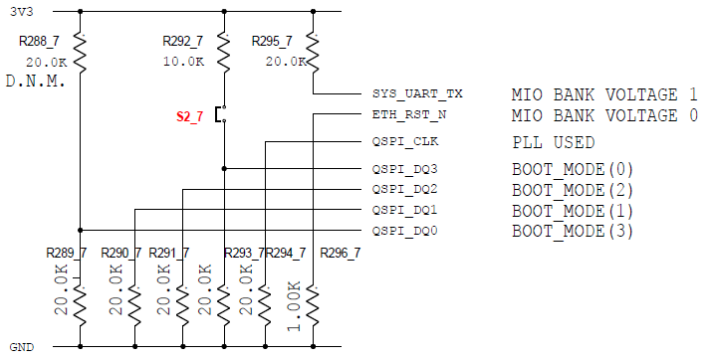

Figure 23: FPGA boot configuration jumper (Schematic page 23).

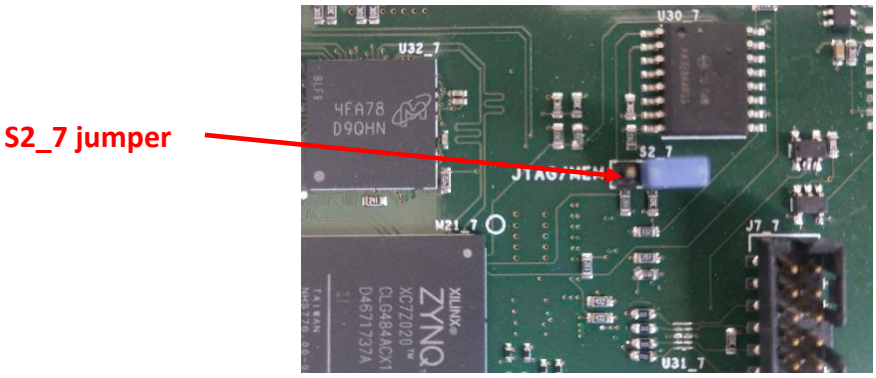

Figure 24: FPGA boot configuration jumper added on board.

Added components:

- S2_7, xxx (available in UUB BOM, ref.: CON-**XXX**)

Number of operation: 1

2.9 GPS antenna voltage configuration:

The GPS antenna could be powered by 2 types of voltages, 3 Volts or 5 Volts. On the board this choice is made by R1 and R2 0 Ohm resistors. Presently, the 2 resistors are soldered on board (NCR n° 2-2). R2 resistor must be removed.

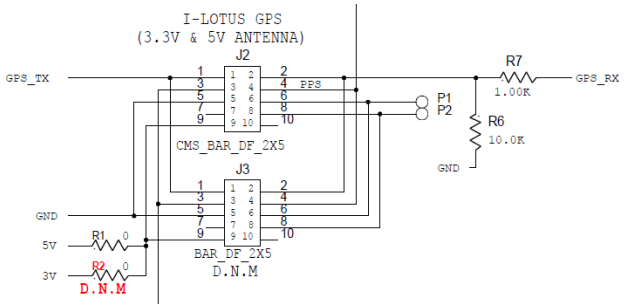

Figure 25: GPS antenna configuration resistor (Schematic page 3).

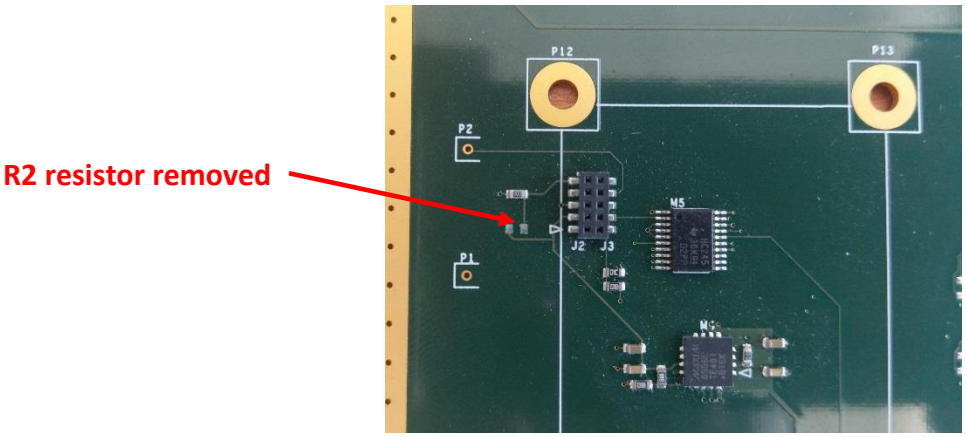

Figure 26: GPS antenna voltage configuration on board.

Number of operation: 1

3 SLOW-CONTROL MODIFICATIONS (WP4):

3.1 Reset/Done modification:

4,7 kOhms 1% and 0603 package Pull-up resistor must be added between 3V3_SLOW_CTRL and U20 pin 23 (schematic page 12).

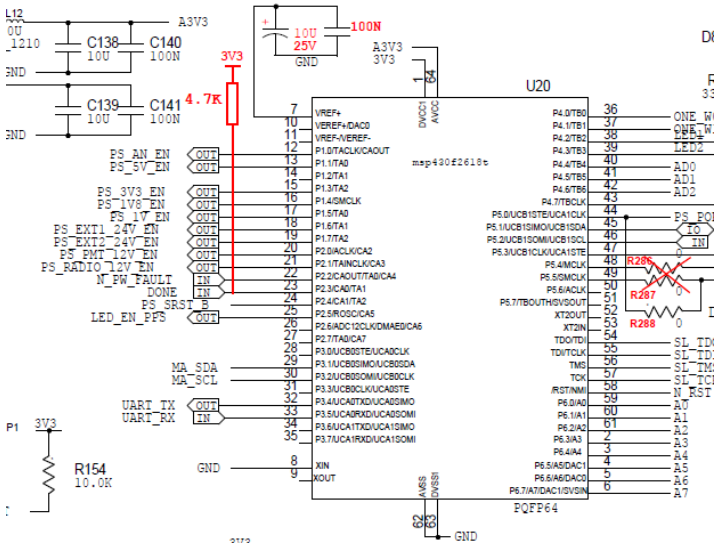

Figure 27: Slow-Control RESET configuration resistors (Schematic page 12).

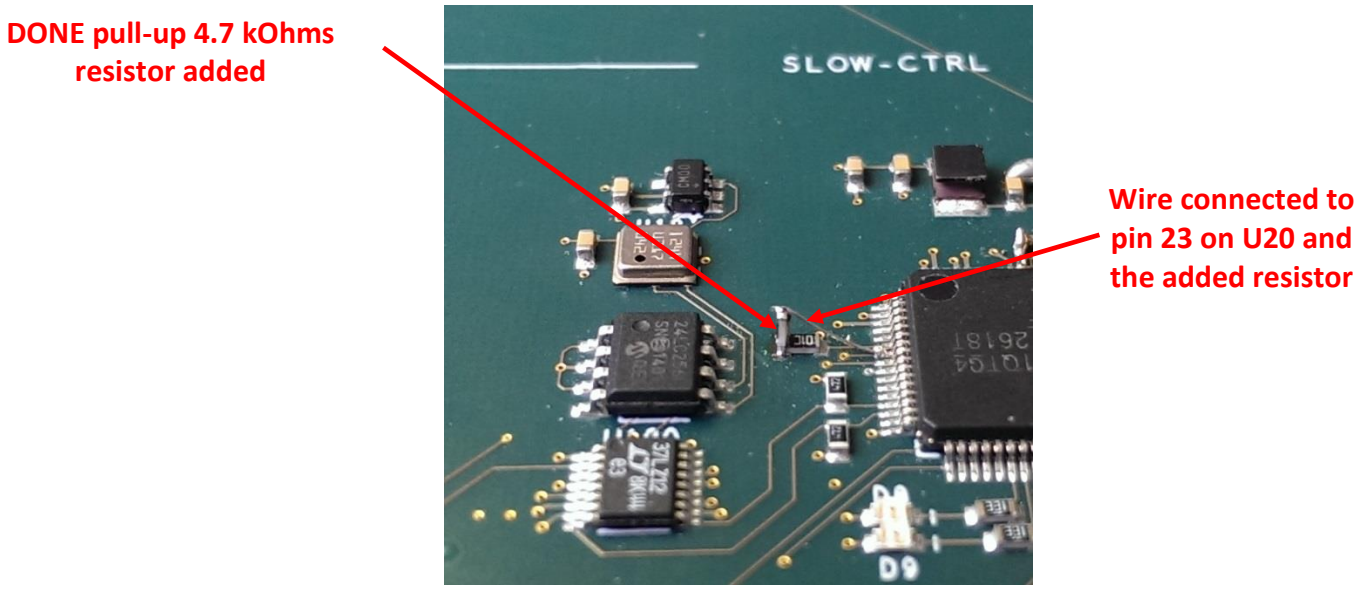

Figure 28: Slow-Control RESET & DONE configuration resistors on board.

The added components:

- R3_X, 4,7 KOhms 1% 0603 (available in UUB BOM, ref.: RES-043)

Number of operation: 2

3.2 *Vref decoupling capacitors:*

Connect 10 µF 25 Volts and 100nF capacitors in parallel to U20 pin 7 and C138 & C140 ground pins.
Be careful to 10µF polarity connected to U20 pin 7.

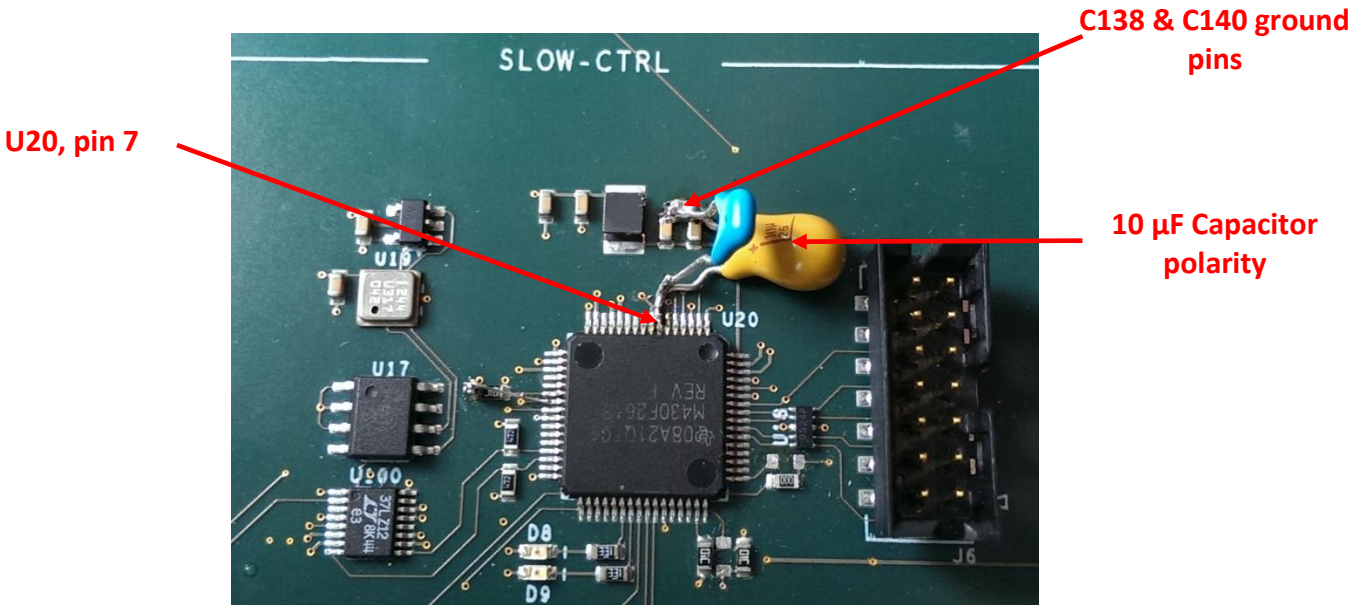

Figure 29: Vref decoupling capacitors.

The added components:

- C2_X capacitor: 10 µF 35 Volts trad — ref.: KEMET T350G106K035AT.
- C1_X capacitor: 100 nF 50 Volts trad — ref.: VISHAY K104K15X7RF53L2.

Number of operation: 2

3.3 *Slow-Control Reset Pull-up:*

3,3 Volts is missing on Slow-Control Reset Pull-up R297_7 resistor. One pin is unconnected. It must be connected to 3,3 Volts power supply.

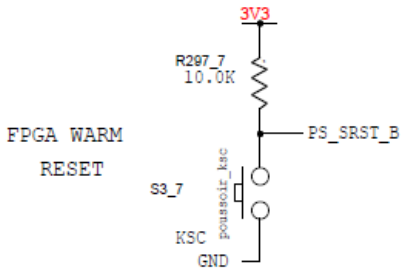

Figure 30: R297_7 pull_up resistor power supply on (Schematic page 12).

A wire must be connected from R297_7 resistor pin to the J7_7 connector pin 2 (3,3 Volts) (NCR n° 2-49).

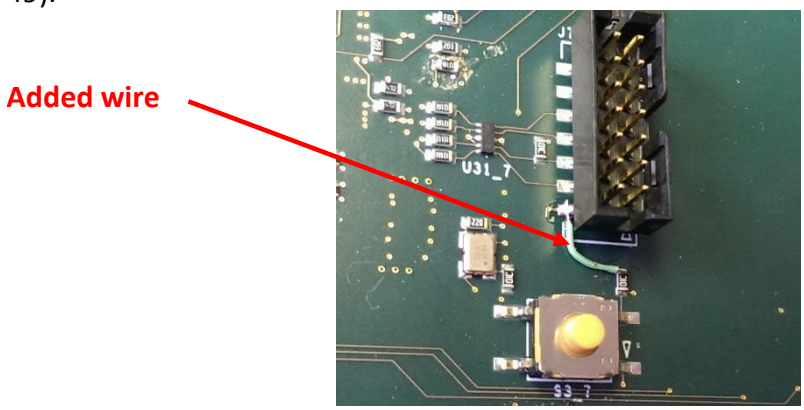

Figure 31: 3,3 Volts connection to 3,3 volts power suplly.

Number of operation: 1

3.4 Watchdog modification:

A pull-up resistor is missing in the schematic. A 10 kOhms resistor must be added between 1 and 5 pins for M34 components (NCR n° 2-22).

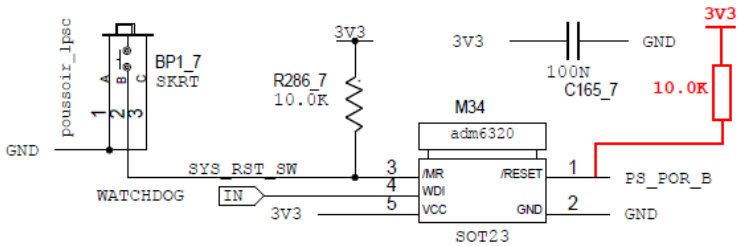

Figure 32: Pull-up resistor added on watchdog output (Schematic page 12).

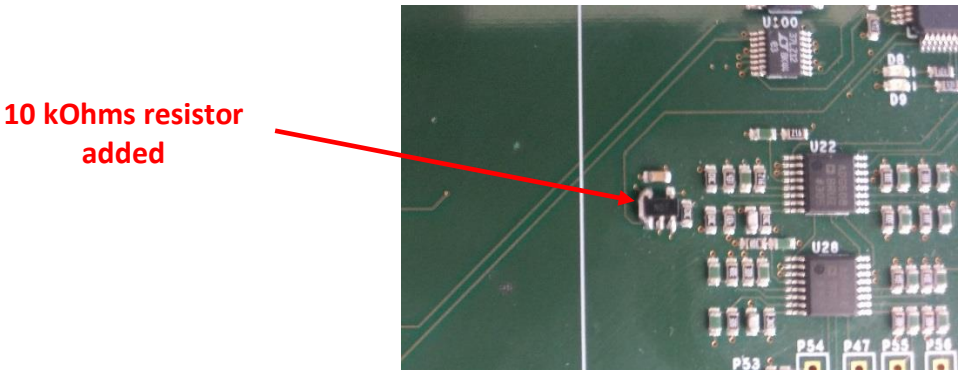

Figure 33: Watchdog 10 kOhms resistor pull-up on board.

The added components:

- R4_X, 10 KOhms 1% 0603 (available in UUB BOM, ref.: RES-017)

Number of operation: 1

4 LED-CONTROLER (WP6):

4.1 I²C interface:

Error in the schematic, SCL & SDA pins must be swapped.

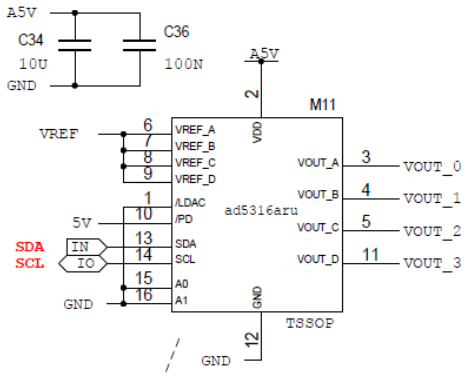

Figure 34: SCL & SDA wires must be swapped (Schematic page 7).

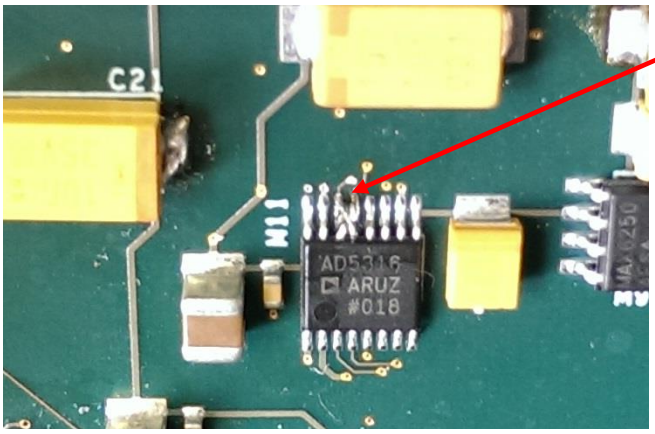

Figure 35: SCL & SDA wires must be swapped on board

Number of operation: 2

4.2 Logic integration:

A short-cut must be made between M14 pins 2 and 3.

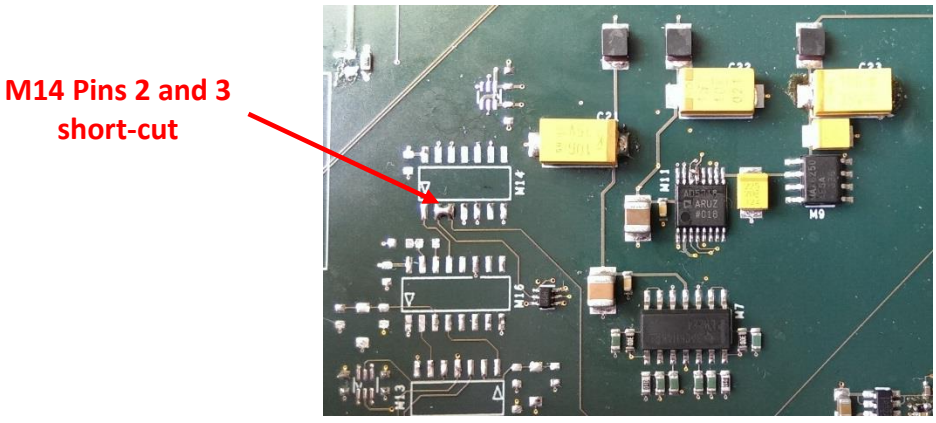

Figure 36: SCL & SDA wires must be swapped on board

Number of operation: 1

5 FRONT-END (WP1):

5.1 Offset 1 & 2 wrong decoupling capacitors positions:

Offset 1 & 2 decoupling capacitors are in the wrong position in the schematic. These capacitors are: C5_1, C8_1, C5_2, C8_2, C5_3, C8_3, C5_4, C8_4, C5_5 & C8_5.

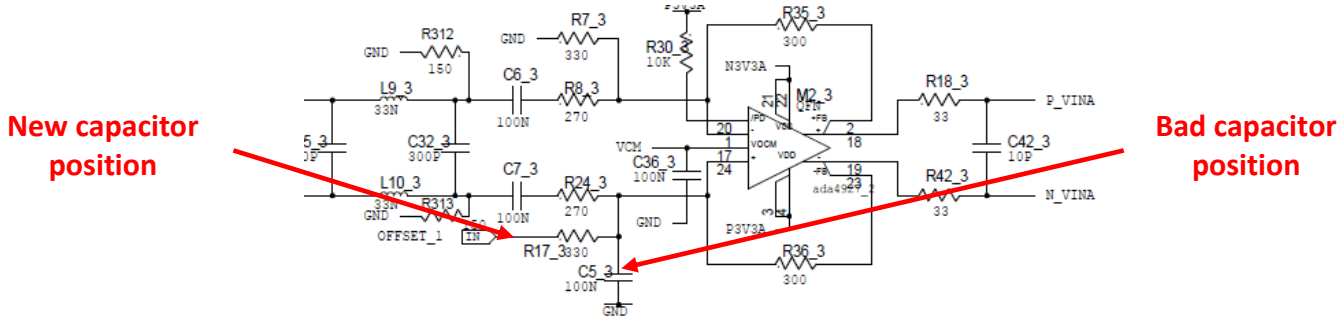

Figure 37: OFFSET_1 C5_3 decoupling capacitors in wrong place (Schematic page 18).

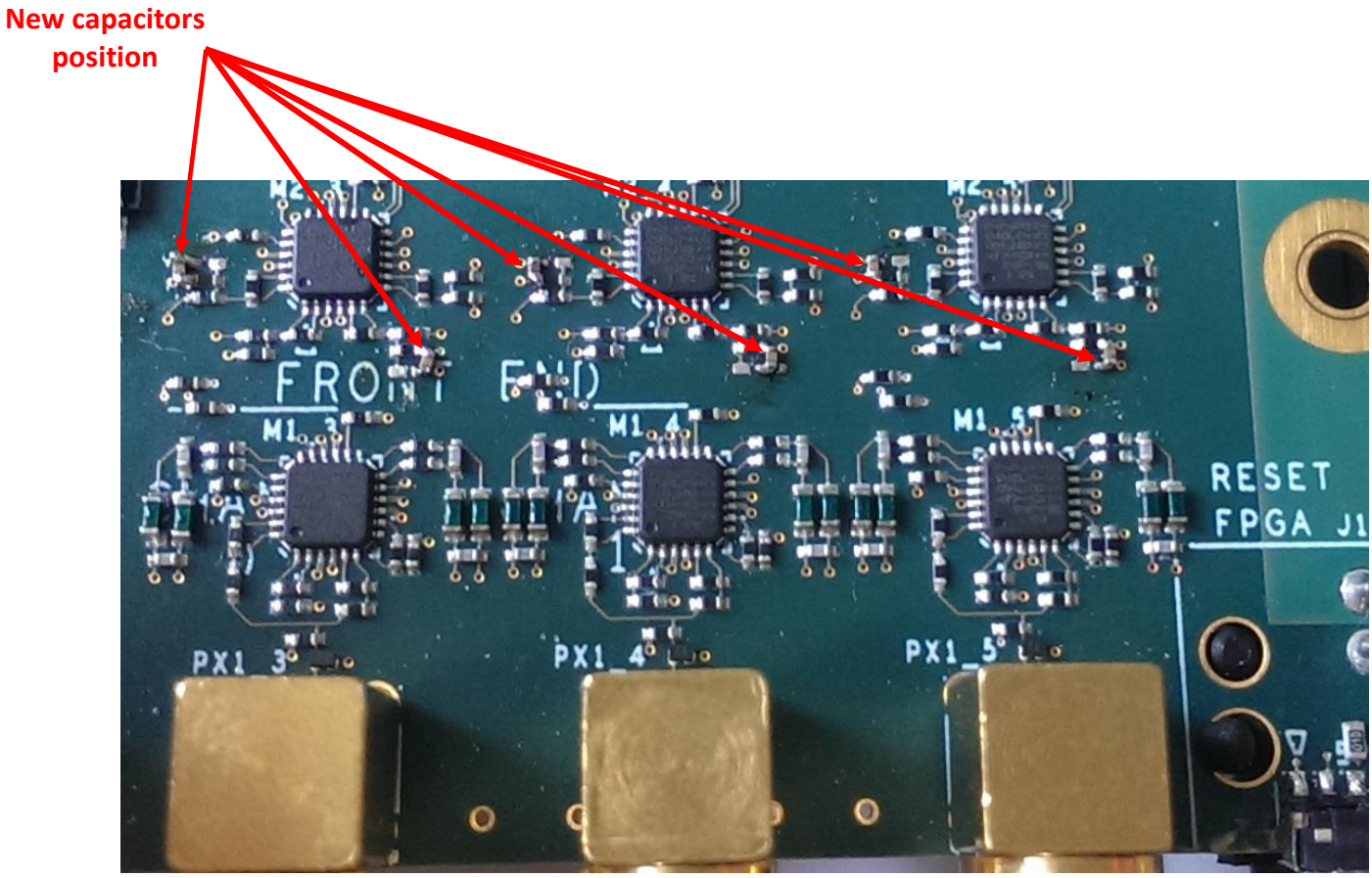

Figure 38: OFFSET_1 & OFFSET_2 C5_3, C8_3, C5_4, C8_4, C5_5 & C8_5 decoupling on board.

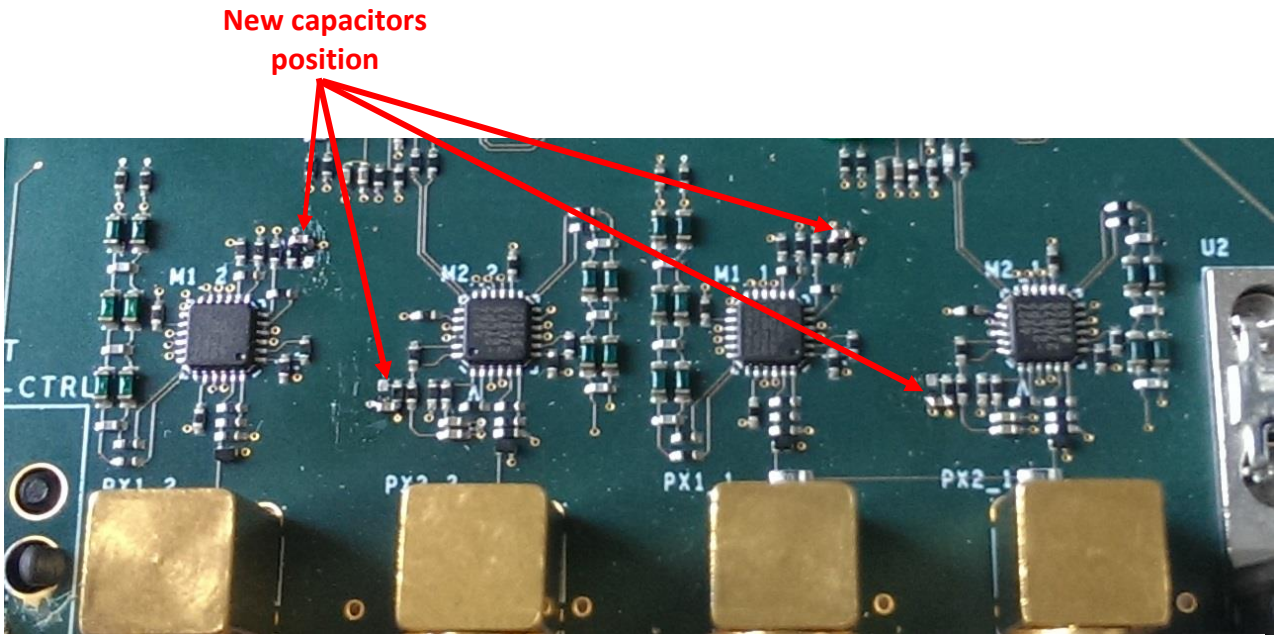

Figure 39: OFFSET_1 & OFFSET_2 C5_1, C8_1, C5_2 & C8_2 decoupling on board.

The added components:

- C5_1,C8_1,C5_2,C8_2,C5_3,C8_3,C5_4,C8_4,C5_5,C8_5, 100 nF 10V 10% 0402 (available in UUB BOM, ref.: CAP-004)

Number of operation: 10

5.2 Offset 1 & 2 decoupling capacitors:

4 Tantalum or ceramic decoupling capacitors must be soldered on board on each OFFSET signal. 2 on amplifier Offset outputs. The 2 others must be close the ADCs.

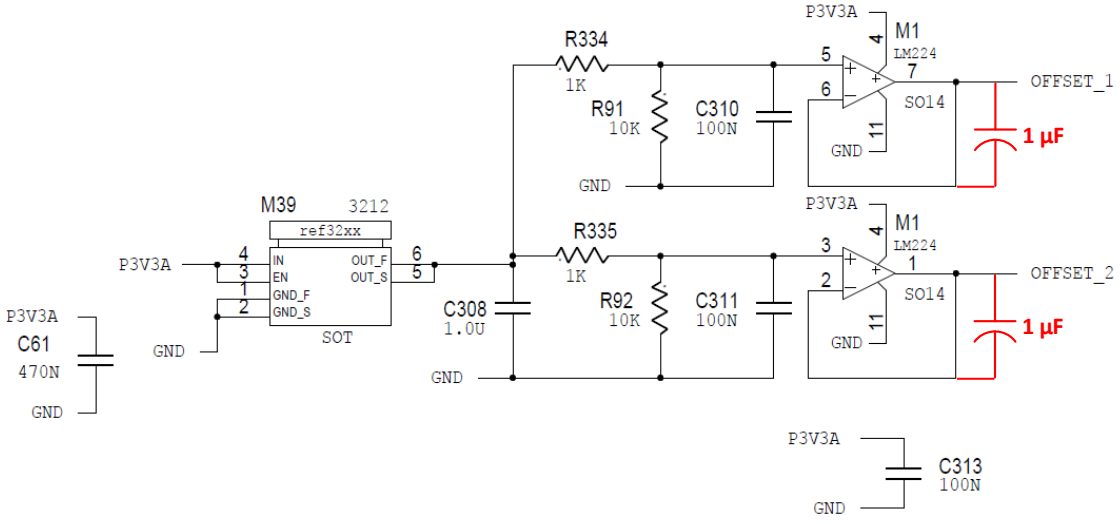

Figure 40: OFFSET_1 & OFFSET_2 amplifiers decoupling (Schematic page 15).

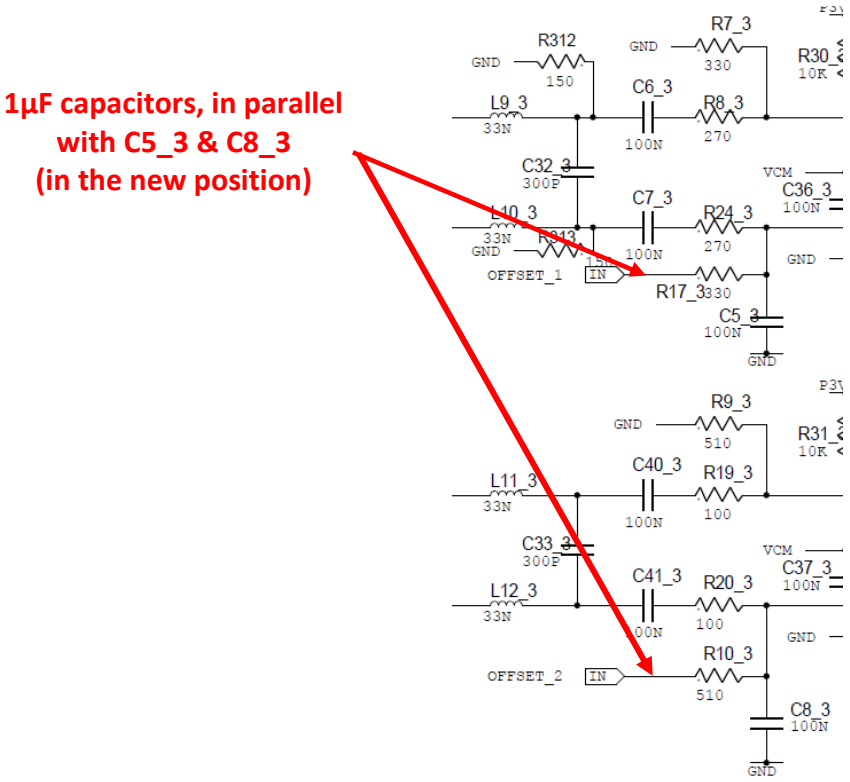

Figure 41: OFFSET_1 & OFFSET_2 decoupling close ADC (Schematic page 18).

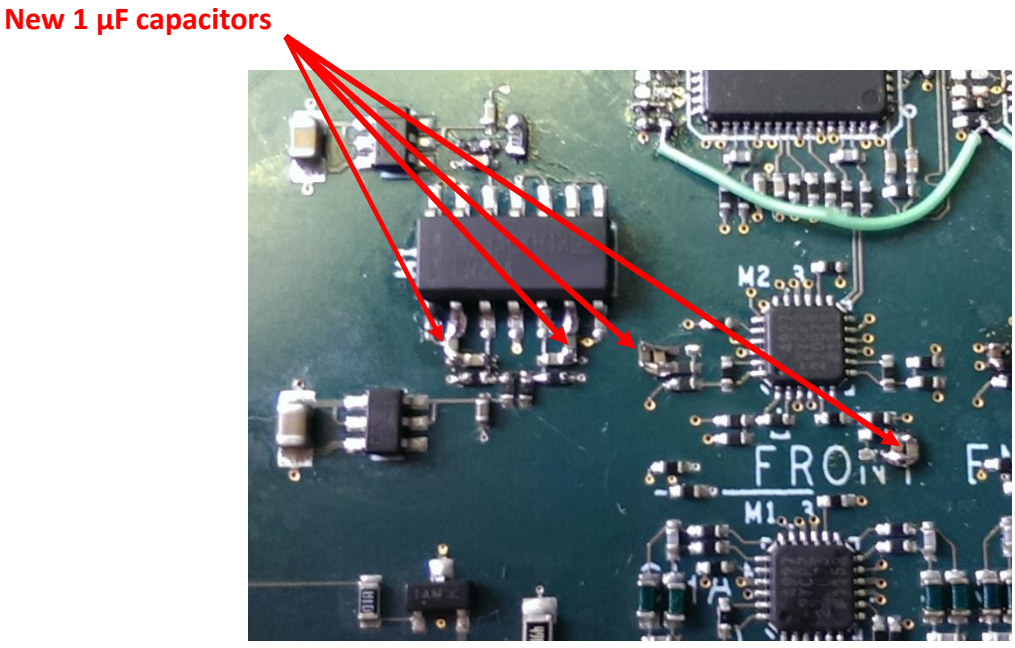

Figure 42: OFFSET_1 & OFFSET_2 amplifier decoupling and close ADC on board.

The added components:

- C3_X, C4_X, C5_X and C6_X, 1 µF 16 V 0402 (available in UUB BOM, ref.: CAP-012)

Be careful with the capacitor's polarity, it is a Tantalum technology.
Number of operation: 4

5.3 Vref modifications:

Vref wire provides 1 Volt to all ADCs. A wire cut must be made just after the M1 output pin.

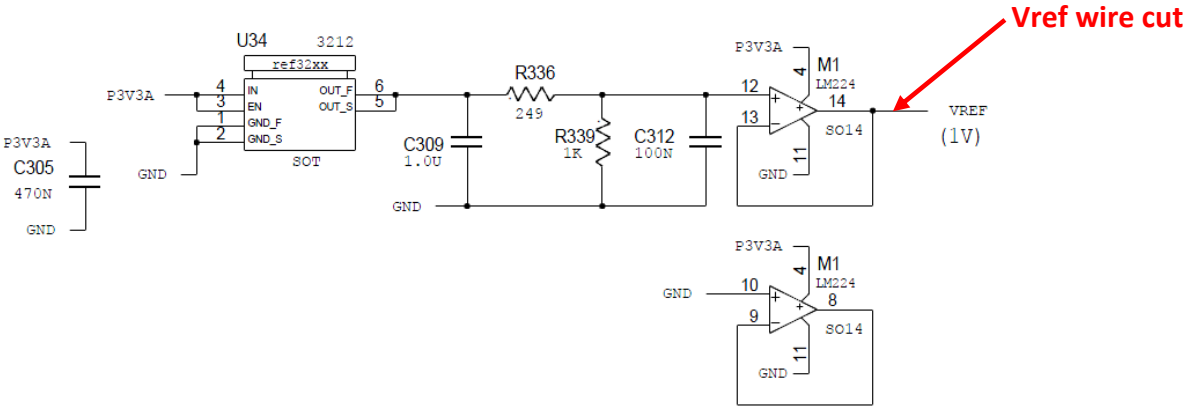

Figure 43: Disconnected Vref provided by M1 amplifier (Schematic page 15).

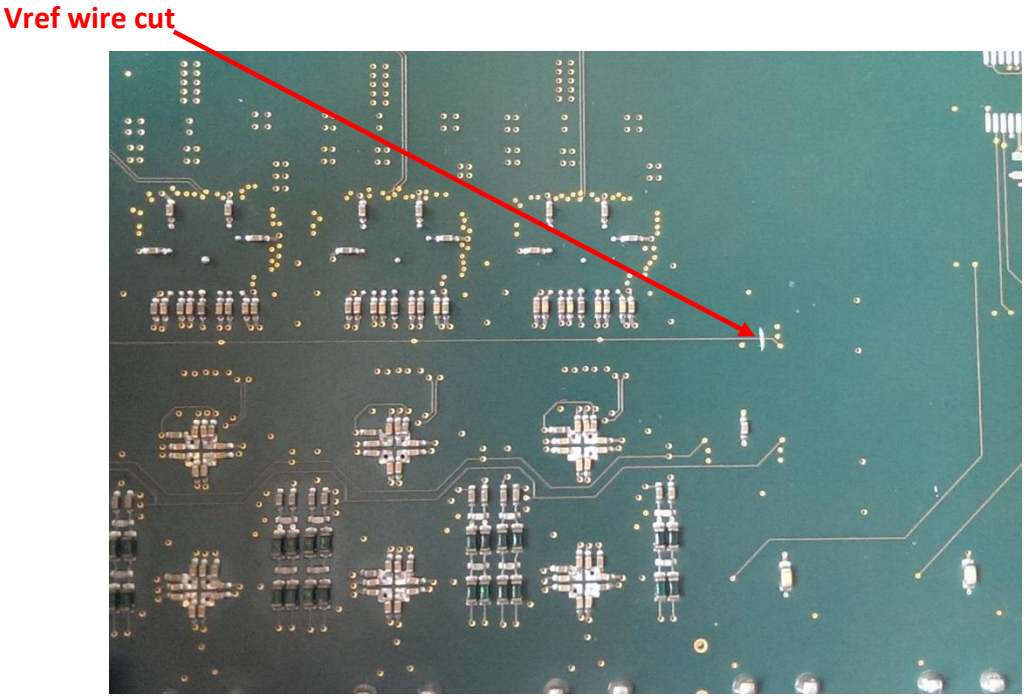

Figure 44: Vref Disconnected cut on board.

Number of operation: 1

5.4 Type 3, input impedance modifications:

For SSD detector the type 3 front-end design must be implanted with a type1 Bill Of Material. For the impedance adaptation a wire must be cut and a resistor 200 Ohms and 51 Ohms 0603 package added.

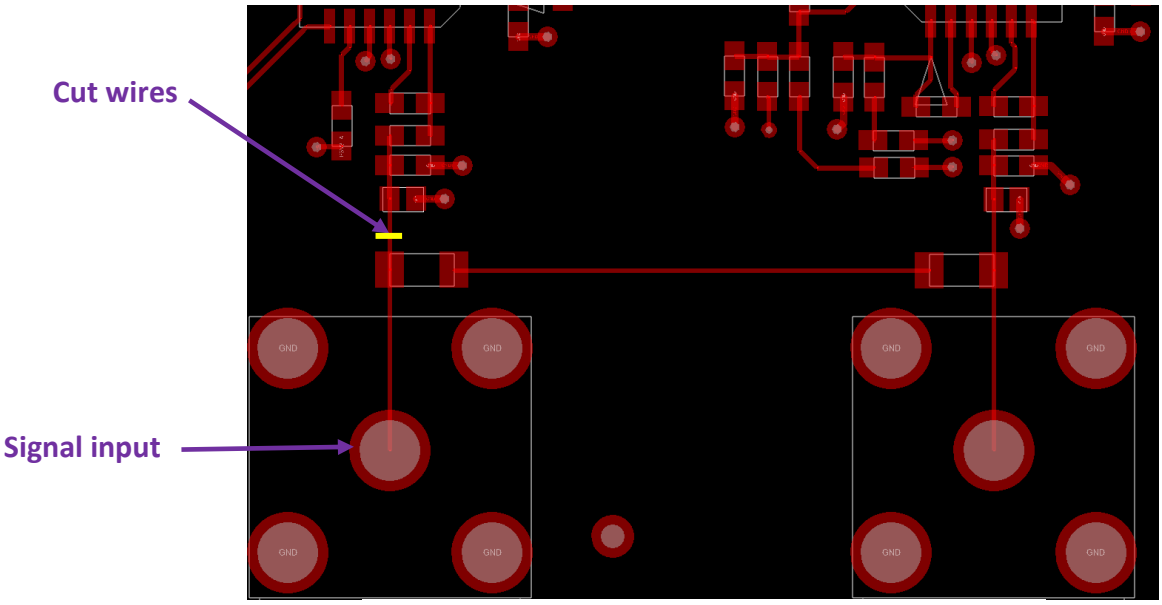

Figure 45: SSD analog input Wire Cut.

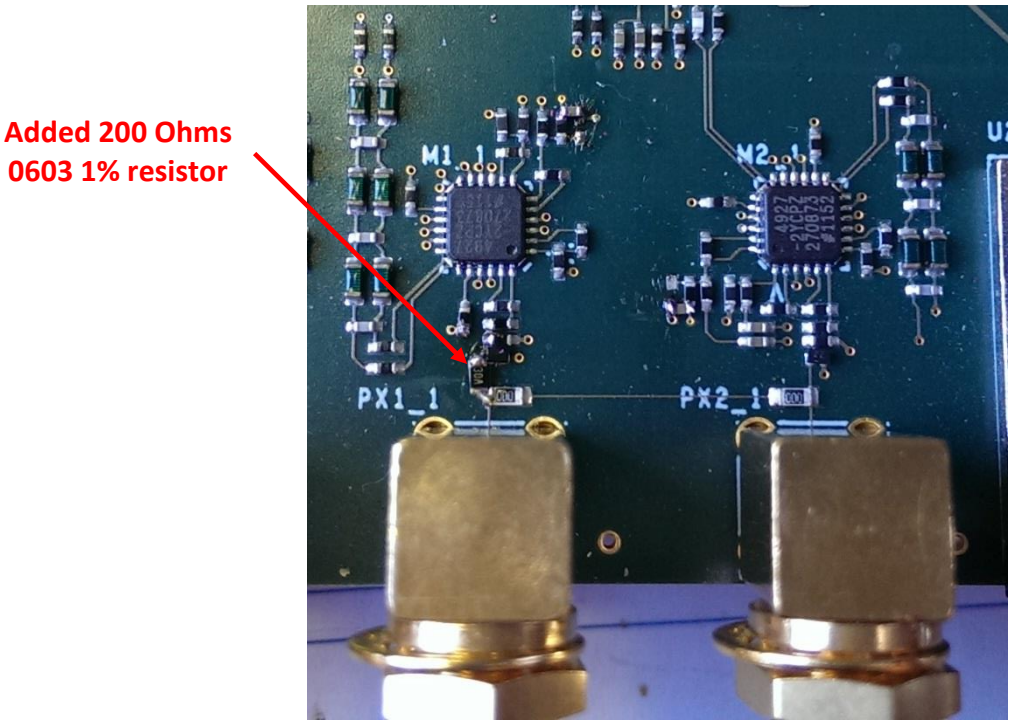

Figure 46: 200 Ohms resistor added.

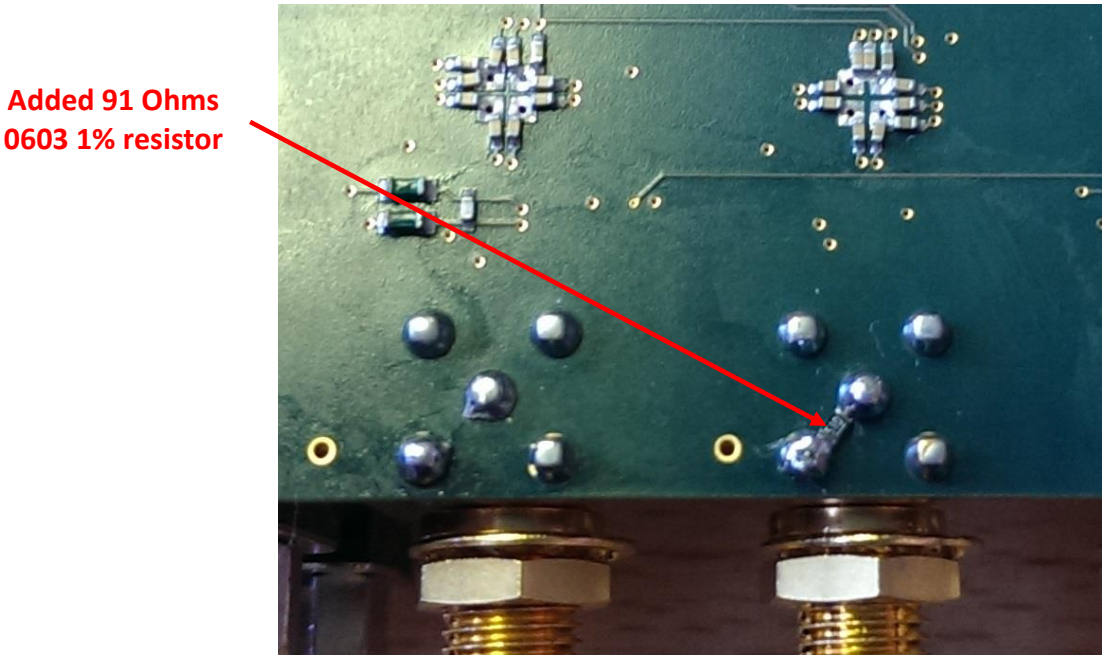

Figure 47: 91 Ohms resistor added.

The added components:

- R5_X, 91 Ohms 1% 0603 (available in UUB BOM, ref.: RES-121)
- R6_X, 200 Ohms 1% 0603 (available in UUB BOM, ref.: RES-112)

Number of operation: 3

5.5 OFFSET_1 & OFFSET_2 Vref values:

The Reference Voltage value must be changed. R91 resistor value must be 2,4 kOhms and R92 1,3 kOhms in 0402 1% (NCRs n° 2.-47 & 2-48)

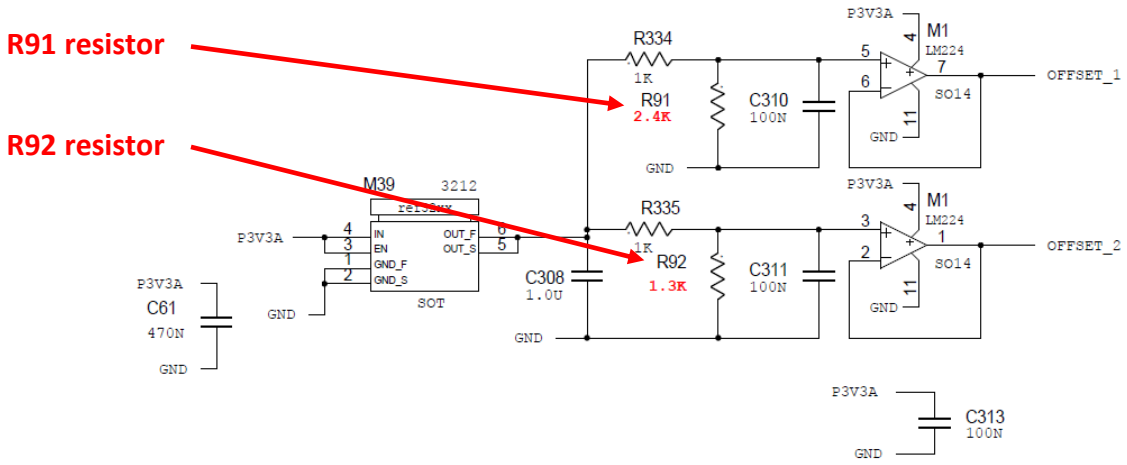

Figure 48: New resistor value for R91 an R92 (Schematic page 15).

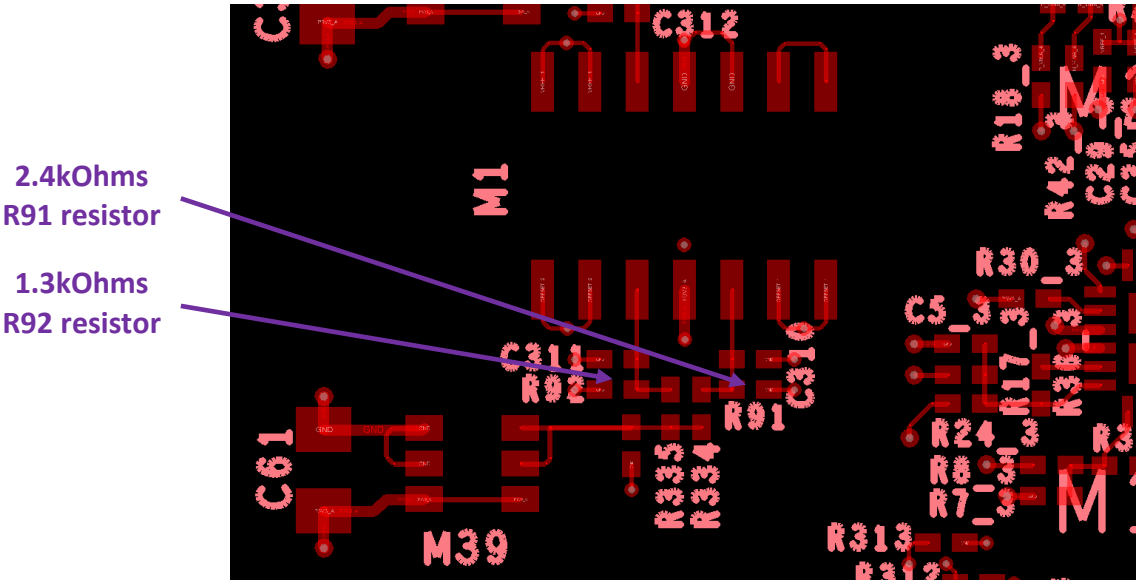

Figure 49: New resistor value for R91 an R92.

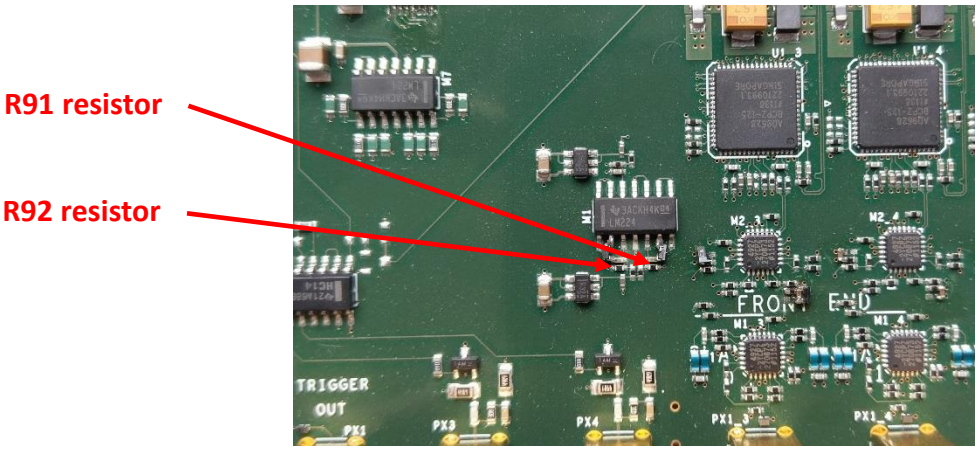

Figure 50: New resistor value for R91 an R92.

The changed component value:

- R91, 2,4 kOhms 1% 0402 (available in UUB BOM, ref.: RES-121)
- R92, 1,3 kOhms 1% 0402 (available in UUB BOM, ref.: RES-123)

Number of operation: 4

6 ENGINEERING ARRAY MODIFICATIONS:

During the Engineering Array, several modifications have been made in the electronic UUB design.

6.1 "Radio RS232" ESD protection:

The RCLAMP0524J.TCT ESD component modifies the "Radio RS232" signal. The U48 & U50 must be removed. The MAX3218 RS232 interface has already 15kVolts ESD protection.

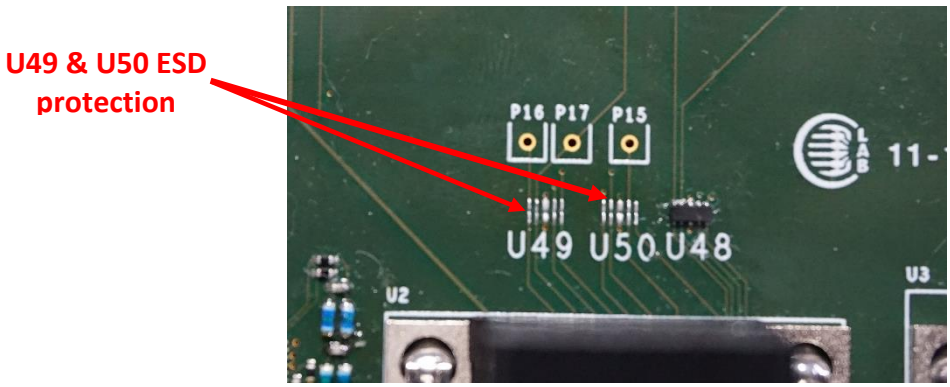

Figure 51: Removed U49 & U50 ESD RCLAMP components.

Number of operation: 2

6.2 Slow-control ESD protection and Temperature sensor power supply modification (WP4 & 5):

The RCLAMP0524J.TCT ESD component modifies signals for PMT and Tank devices. Wires must be cut, R13, R14, R19, R20 & R21 resistors and U11, U12 & U13 must be removed.

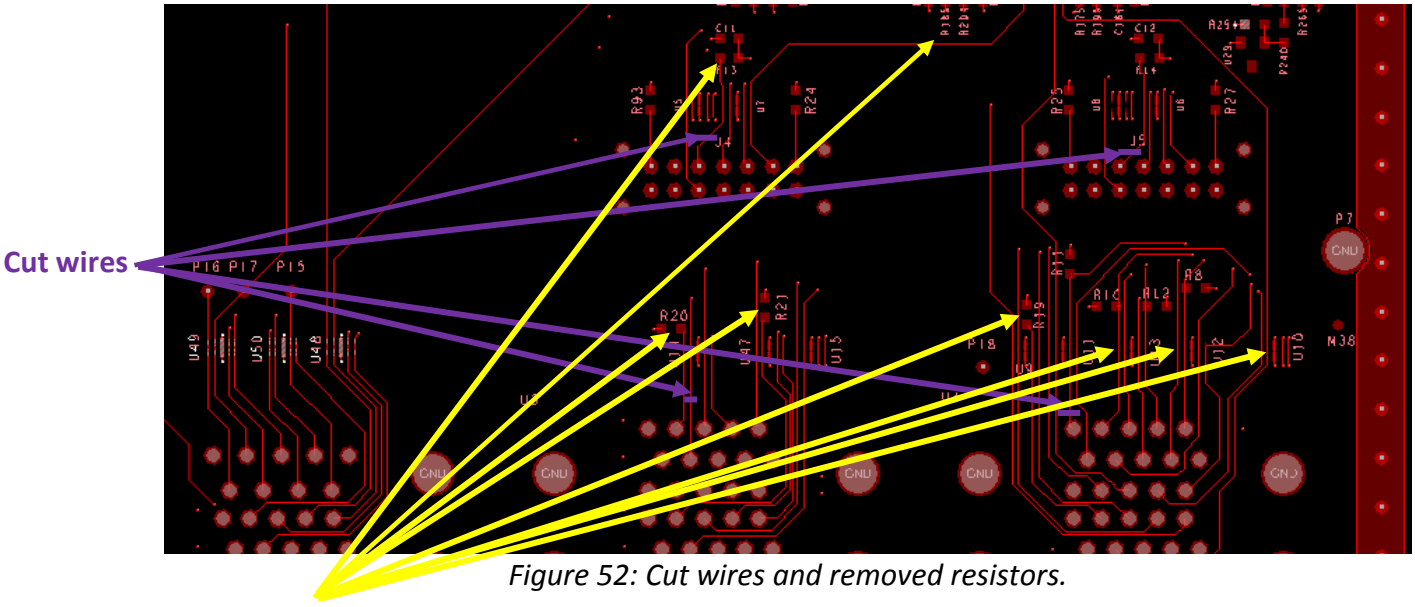

Figure 52: Cut wires and removed resistors.

Removed 1kOhms Resistor R13, R14, R19, R20, R21, U11, U12 & U13

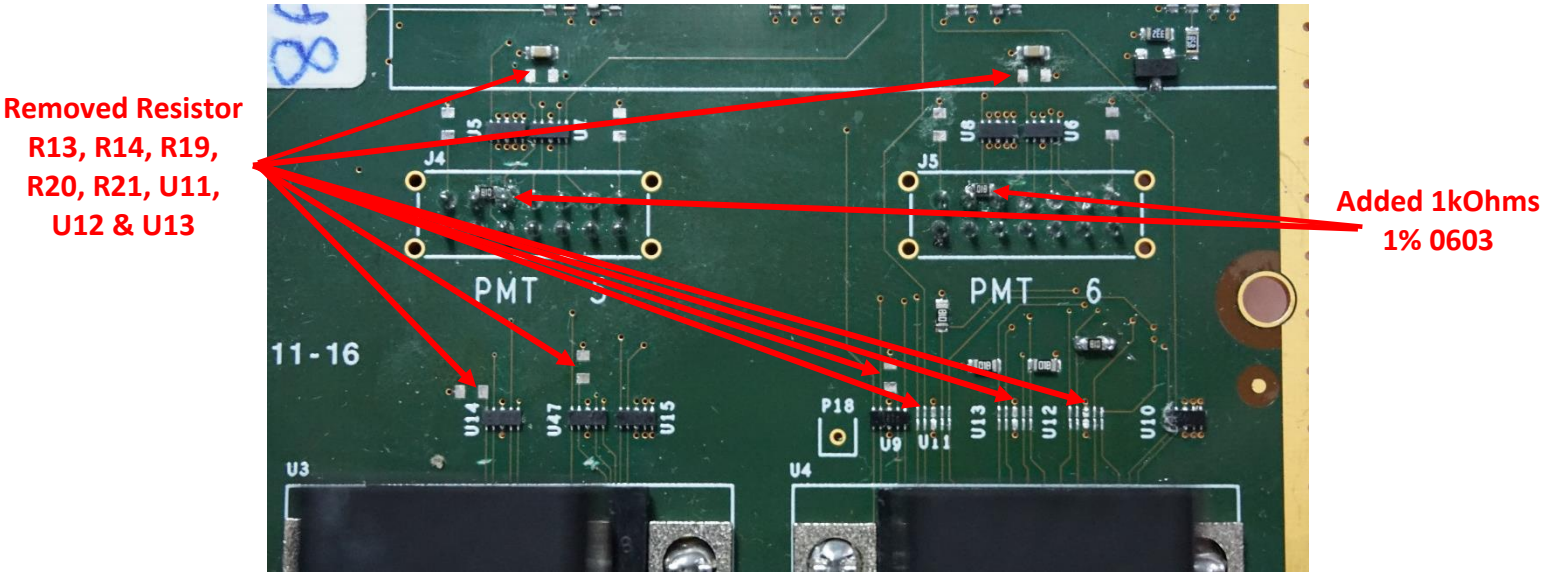

Figure 53: Cut wires, resistors & ESD removed and R7_X & R8_X added resistors on top side.

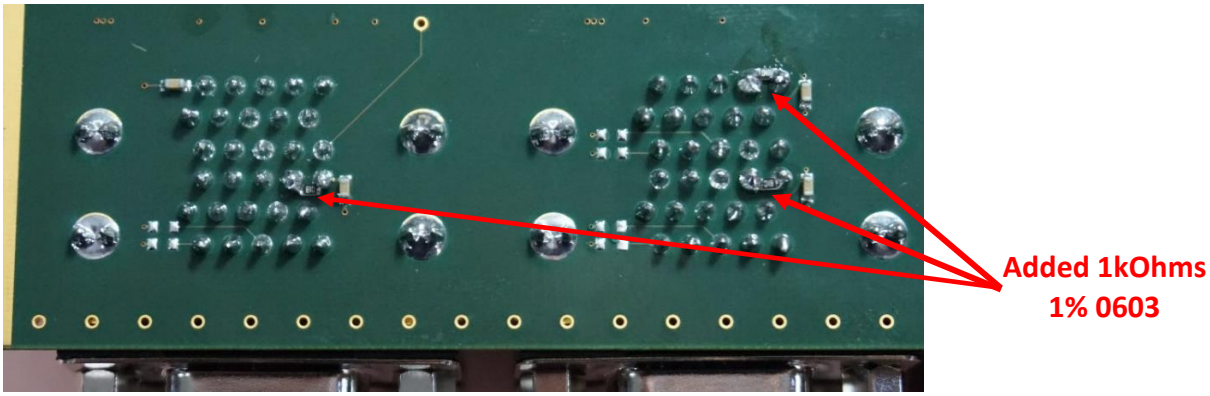

Figure 54: resistors added on bottom side.

The added components:

- R7_X, R8_X, R9_X, R10_X and R11_X, 1 kOhms 1% 0603 (available in UUB BOM, ref.: RES-014)

Number of operation: 18

The Temperature sensor power supply adjustment R8 resistor must be changed. The value was 22 kOhms 1% 0603 and it must be 1 kOhms 1% 0603.

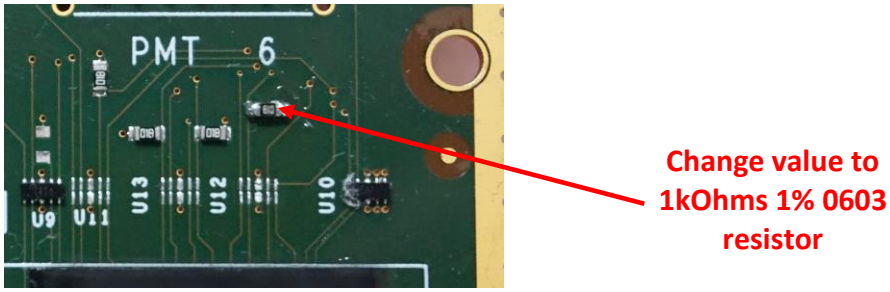

Figure 55: resistors changed on top side.

The changed component value:

- R8, 1 kOhms 1% 0603 (available in UUB BOM, ref.: RES-014)

Number of operation: 2

The -3,3 Volts monitoring schema is not conform (NCR n° 2-52). For the Engineering Array the 10 kOhms R242 resistor must be removed.

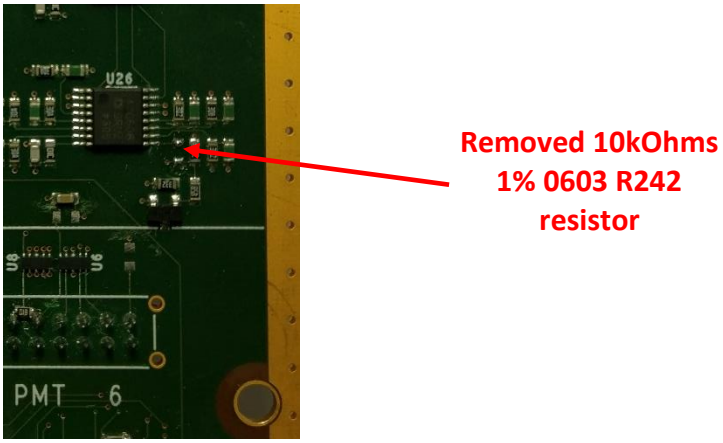

Figure 56: resistors changed on top side.

Number of operation: 1

6.3 TRIGGER in modification:

The input 50 Ohms R29 resistor must be removed, but kept on board. There is too many attenuation on the signal.

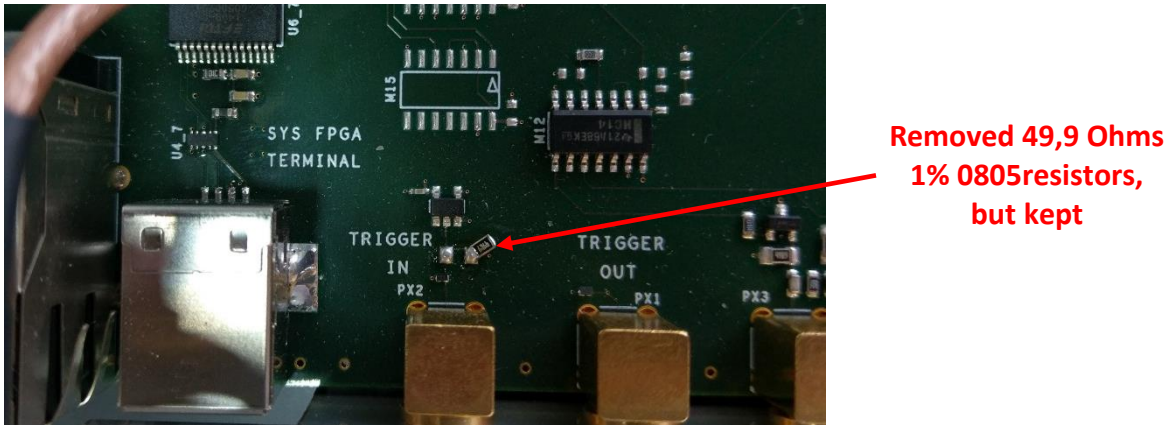

Figure 57: R29 resistors removed on top side.

Number of operation: 2

6.4 "RADIO Reset" modification:

The "RADIO Reset" was managed by FPGA, but now it must be managed by the Slow-Control. It's already managed the UUB's Reset.

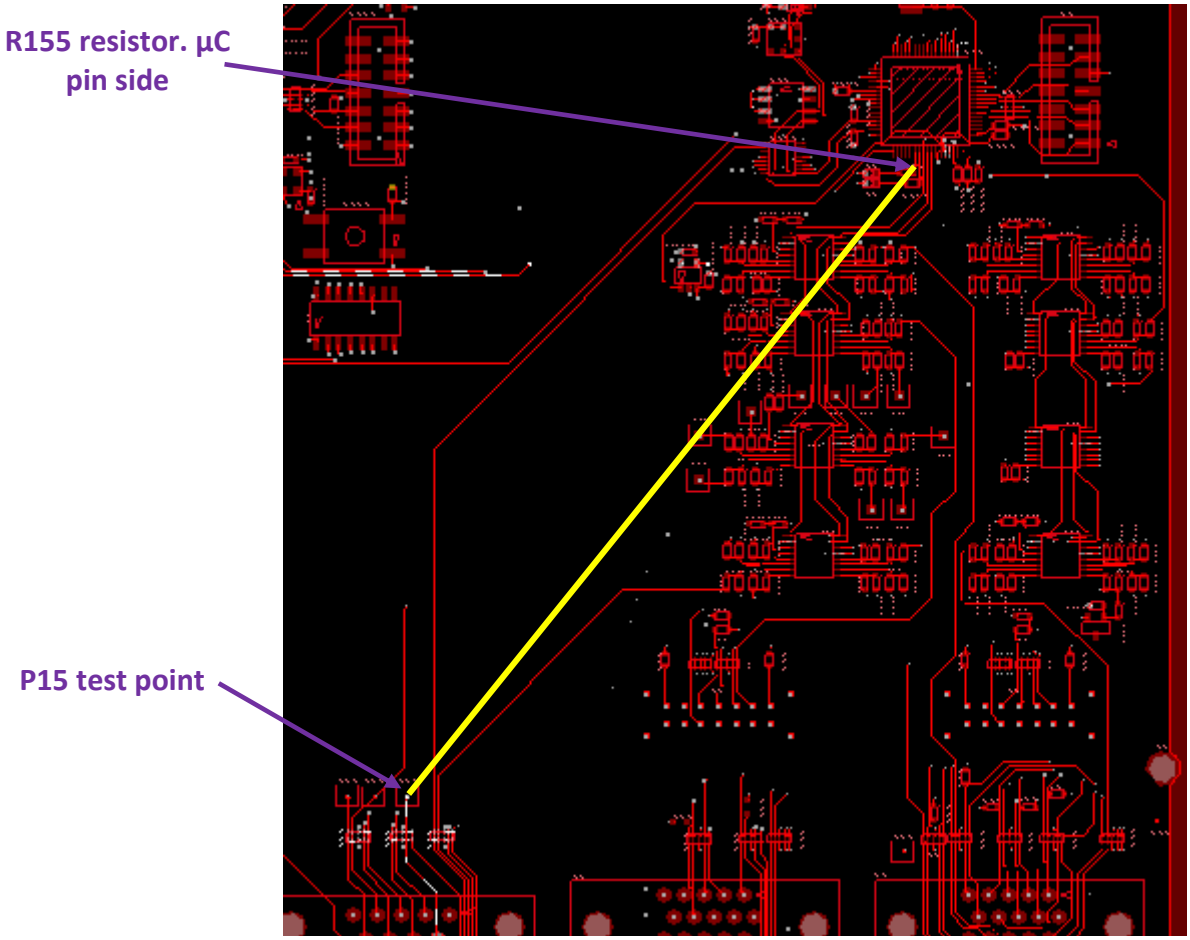

Figure 58: "RADIO Reset" Wire connection between P15 test point and R155resistor.

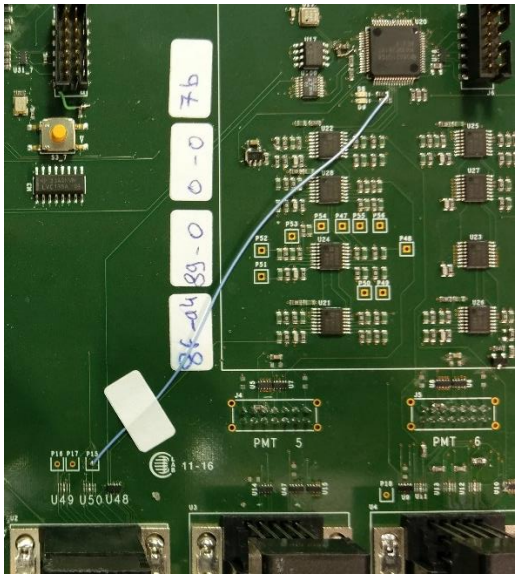

Figure 59: "RADIO Reset" Wire on top side.

7 MATERIAL:

7.1 Bill Of Material:

Auger ID Ref.	*Component reference*	*Description*	*Design reference*	*Qty*	*Manufacturer 1*	*Manufacturer 1 Part number*	*Manufacturer 2*	*Manufacturer 2 Part number*	*Manufacturer 3*	*Manufacturer 3 Part number*	*Manufacturer …*	*Manufacturer … Part number*	*Work Package in charge*
CAP-004	CAPA-100N,C402S10V10%	Capacitor 100 nF 10V ±10% X5R 0402 ceramic -55°C to +85°C	C5_1,C8_1,C5_2,C8_2,C5_3,C8_3,C5_4,C8_4,C5_5,C8_5	10	AVX	0402ZD104KAT2A	MURATA	GRM155R61A104KA01D	KEMET	C0402C104K8PACTU			WP1, WP5
CAP-069	CAPA-100N,CER50V10%	Capacitor 100 nF 50V ±10% X7R TRAD 2,54 mm ceramic -55°C to +125°C	C1_X	1	VISHAY	K104K15X7RF53L2							WP4
CPL-011	CPOL-1U,TAN35V	Capacitor 10 µF 35V ±20% TRAD 2,54 mm Tantalum -55°C to +105°C	C2_X	1	KEMET	T350G106K035AT							WP4
CPL-012	CPOL-10U,0402S16V10%	Capacitor 10 µF 16V ±20% 0402 Tantalum -55°C to +125°C	C3_X,C4_X,C5_X,C6_X	4	VISHAY	TMCJ1C105MTRF							WP1
RES-014	RGEN-1.00K,S100MW1%	Resistor 1 Kohm ±1% 100mW E24 series 0603 package, -55°C to +125°C	R8, R343 R7_X, R8_X, R9_X, R10_X, R11_X	7	TE Connectivity	1622866-1	YAGEO	RC0603FR-071KL					WP1, WP5, WP7
RES-017	RGEN-10.0K,S100MW1%	Resistor 10 Kohm ±1% 100mW E24 series 0603 package, -55°C to +125°C	R2_X,R4_X	2	YAGEO	RC0603FR-0710KL	BOURNS	CR0603-FX-1002ELF					WP4, WP5, WP7
RES-043	RGEN-4.70K,S100MW1%	Resistor 4,7 kohm ±1% 100mW E24 series 0603 package, -55°C to +125°C	R3_X	1	YAGEO	RC0603FR-074K7L	BOURNS	CR0603-FX-4701ELF	Rohm Semiconductor	MCR03FZPFX4701			WP4, WP5
RES-068	RGEN-1.5k,S100MW1%	Resistor 1.5 kohm ±1% 100mW E24 series 0603 package, -55°C to +125°C	R1_X	1	Bourns	CR0603-FX-1501ELF	VISHAY	CRCW06031K50FKEA	YAGEO	RC0603FR-071K5L			WP4
RES-112	RGEN-200,S100MW1%	Resistor 200 ohm ±1% 100mW E24 series 0603 package, -55°C to +125°C	R6_X	1	YAGEO	RC0603FR-07200RL	VISHAY	CRCW0603200RFKEA	PANASONIC	ERJ-3EKF2000V			WP1, WP4
RES-121	RGEN-91,S63MW1%	Resistor 51 ohm ±1% 100mW E96 series 0603 package, -55°C to +125°C	R5_X	1	YAGEO	RC0603FR-0751RL	VISHAY	CRCW060351R0FKEA	PANASONIC	ERJ-3EKF51R0V			
	RGEN-2,4K,S63MW1%	Resistor 2,4 kohm ±1% 63mW E96 series 0402 package, -55°C to +125°C	R91	1									
	RGEN-1,3K,S63MW1%	Resistor 1,3 kohm ±1% 63mW E96 series 0402 package, -55°C to +125°C	R92	1									