ZYNC 7020 Ports MOI Usage - 17 October 2014 version – LPSC Grenoble – Joël BOUVIER

Component: XA7Z020clg484-1I (industrial version)

Integrated components used:

- Quad SPI Flash (programming flash memory)
- Ethernet 0 (Ethernet link)
- USB 0 (USB2.0 OTG link)
- UART 0 (radio RS232 link) with RTSn & CTSn (38400 8 N 1)
- UART 1 (SYS FPGA Terminal link) (9600 8 N 1)
- I2C 0 (SLOW CONTROL interface)
- I2C 1 (CLOCK GENERATOR interface)
- SPI 0 (ADC AD9628 interface)
- SPI 1 (CLOCK GENERATOR DAC control interface)

Descripted components used:

- UART 2 (RS232 GPS link) (9600 8 N 1)
- GPIO_1(0) Watchdog : watchdog hardware trigger (input/output)
- GPIO_2(7..0) Config(7..0) : 8 configuration switches (output)

Zynq peripherals configuration

Quad SPI Flash	MIO 1 .. 6
Ethernet 0	MIO 16 .. 27
	tx_clk MIO 16
	txd[3] MIO 20
	txd[2] MIO 19
	txd[1] MIO 18
	txd[0] MIO 17
	tx_ctl MIO 21
	rx_clk MIO 22
	rxd[3] MIO 26
	rxd[2] MIO 25
	rxd[1] MIO 24
	rxd[0] MIO 23
	rx_ctl MIO 27
	MDIO MIO 52 .. 53
	mdc MIO 52
	mdio MIO 53
USB 0	MIO 28 .. 39
	clk MIO 36
	dir MIO 29
	stp MIO 30
	nxt MIO 31
	data[0] MIO 32
	data[1] MIO 33
	data[2] MIO 34
	data[3] MIO 35
	data[4] MIO 28
	data[5] MIO 37
	data[6] MIO 38
	data[7] MIO 39
UART 0	MIO 46 .. 47
	rx MIO 46
	tx MIO 47
UART 1	MIO 8 .. 9
	rx MIO 9
	tx MIO 8
I2C 0	MIO 14 .. 15
	scl MIO 14
	sda MIO 15
I2C 1	MIO 48 .. 49
	scl MIO 48
	sda MIO 49
SPI 0	MIO 40 .. 45
	SS[0] MIO 42
	SS[1] MIO 43
	SS[2] MIO 44
SPI 1	MIO 10 .. 15
	SS[0] MIO 13
GPIO	MIO

MIO configuration Table

MIO Pin	FPGA Pin	Peripheral	Signal	Direction	Comment	IO type
--	F7	System	PS_CLK	in	System Clock	LVCMOS 3.3V
--	B5	System	PS_POR_n	in	Power On Reset	LVCMOS 3.3V
0	G6	GPIO	ETH_RST_n	out	/reset pour le PHY ethernet	LVCMOS 3.3V
1	A1	Quad SPI Flash	qspi0_ss_b	out	FLASH memory "progr."	LVCMOS 3.3V
2	A2	Quad SPI Flash	qspi0_io[0]	inout	FLASH memory "progr."	LVCMOS 3.3V
3	F6	Quad SPI Flash	qspi0_io[1]	inout	FLASH memory "progr."	LVCMOS 3.3V
4	E4	Quad SPI Flash	qspi0_io[2]	inout	FLASH memory "progr."	LVCMOS 3.3V
5	A3	Quad SPI Flash	qspi0_io[3]	inout	FLASH memory "progr."	LVCMOS 3.3V
6	A4	Quad SPI Flash	qspi0_sclk	out	FLASH memory "progr."	LVCMOS 3.3V
7	D5	GPIO	USB_RST_n	out	/Reset pour le PHY USB	LVCMOS 3.3V
8	E5	UART 1	tx	out	SYS Terminal Interface	LVCMOS 3.3V
9	C4	UART 1	rx	in	SYS Terminal Interface	LVCMOS 3.3V
10	G7	SPI 1	mosi	out	DAC Clock Interface	LVCMOS 3.3V
11	B4	SPI 1	miso	in	DAC Clock Interface	LVCMOS 3.3V
12	C5	SPI 1	sclk	inout	DAC Clock Interface	LVCMOS 3.3V
13	A6	SPI 1	ss[0]	inout	DAC Clock Interface	LVCMOS 3.3V
14	B6	I2C 0	scl	inout	Interface Slow Control	LVCMOS 3.3V
15	E6	I2C 0	sda	inout	Interface Slow Control	LVCMOS 3.3V
--	C9	System	PS_SRST_B	In	Connected to 1V8 through a 10 KΩ resistor	LVCMOS 1.8V
--	F8	System	PS_MIO_VREF	in	Connected to 1V8 through a 10 KΩ resistor	LVCMOS 1.8V
16	D6	Ethernet 0	tx_clk	out	Ethernet 10/100/1000	LVCMOS 1.8V
17	E9	Ethernet 0	txd[0]	out	Ethernet 10/100/1000	LVCMOS 1.8V
18	A7	Ethernet 0	txd[1]	out	Ethernet 10/100/1000	LVCMOS 1.8V
19	E10	Ethernet 0	txd[2]	out	Ethernet 10/100/1000	LVCMOS 1.8V
20	A8	Ethernet 0	txd[3]	out	Ethernet 10/100/1000	LVCMOS 1.8V
21	F11	Ethernet 0	tx_ctl	out	Ethernet 10/100/1000	LVCMOS 1.8V
22	A14	Ethernet 0	rx_clk	in	Ethernet 10/100/1000	LVCMOS 1.8V
23	E11	Ethernet 0	rxd[0]	in	Ethernet 10/100/1000	LVCMOS 1.8V
24	B7	Ethernet 0	rxd[1]	in	Ethernet 10/100/1000	LVCMOS 1.8V
25	F12	Ethernet 0	rxd[2]	in	Ethernet 10/100/1000	LVCMOS 1.8V
26	A13	Ethernet 0	rxd[3]	in	Ethernet 10/100/1000	LVCMOS 1.8V
27	D7	Ethernet 0	rx_ctl	in	Ethernet 10/100/1000	LVCMOS 1.8V
28	A12	USB 0	data[4]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
29	E8	USB 0	dir	in	Interface USB2.0 OTG	LVCMOS 1.8V
30	A11	USB 0	stp	out	Interface USB2.0 OTG	LVCMOS 1.8V
31	F9	USB 0	nxt	in	Interface USB2.0 OTG	LVCMOS 1.8V
32	C7	USB 0	data[0]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
33	G13	USB 0	data[1]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
34	B12	USB 0	data[2]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
35	F14	USB 0	data[3]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
36	A9	USB 0	clk	in	Interface USB2.0 OTG	LVCMOS 1.8V
37	B14	USB 0	data[5]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
38	F13	USB 0	data[6]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
39	C13	USB 0	data[7]	inout	Interface USB2.0 OTG	LVCMOS 1.8V
40	E14	SPI 0	sclk	inout	Interface AD9628	LVCMOS 1.8V
41	C8	SPI 0	miso	in	*Not used*	LVCMOS 1.8V
42	D8	SPI 0	ss[0]	out	selection AD9628(0)	LVCMOS 1.8V
43	B11	SPI 0	ss[1]	out	selection AD9628(1)	LVCMOS 1.8V
44	E13	SPI 0	ss[2]	out	selection AD9628(2)	LVCMOS 1.8V
45	*B9*	*SPI 0*	*mosi*	*out*	Interface AD9628	*LVCMOS 1.8V*
46	D12	UART 0	rx	in	Interface "Radio"	LVCMOS 1.8V
47	B10	UART 0	tx	out	Interface "Radio"	LVCMOS 1.8V
48	D11	I2C 1	scl	inout	Interface Clock Generator	LVCMOS 1.8V
49	C14	I2C 1	sda	inout	Interface Clock Generator	LVCMOS 1.8V
50	D13	TP0	gpio[50]	inout	*Test_point*	LVCMOS 1.8V
51	C10	TP1	gpio[51]	inout	*Test_point*	LVCMOS 1.8V
52	D10	Ethernet 0	mdc	out	Ethernet 10/100/1000	LVCMOS 1.8V
53	C12	Ethernet 0	mdio	inout	Ethernet 10/100/1000	LVCMOS 1.8V

Bank 502 Configuration : LPDDR2 memory Interface

Bank Pin	FPGA Pin	Signal	Direction	Comment	IO type
/DRST	F3		Output	unused	
/CS	P6	/LPDDR_CS	Output	LPDDR2 Chip Select	HSUL_12
CKE	V3	LPDDR_CKE	Output	LPDDR2 Clock Enable	HSUL_12
/WE	R4		Output	unused	
/RAS	R5		Output	unused	
/CAS	P3		Output	unused	
DM(0)	B1	LPDDR_DM(0)	Output	Data byte Mask 0	HSUL_12
DM(1)	H3	LPDDR_DM(1)	Output	Data byte Mask 1	HSUL_12
DM(2)	P1	LPDDR_DM(2)	Output	Data byte Mask 2	HSUL_12
DM(3)	AA2	LPDDR_DM(3)	Output	Data byte Mask 3	HSUL_12
DQS(0)	C2	LPDDR_DQS(0)	I/O	Positive differential data strobe 0	DIFF_HSUL_12
/DQS(0)	D2	/LPDDR_DQS(0)	I/O	Negative differential data strobe 0	DIFF_HSUL_12
DQS(1)	H2	LPDDR_DQS(1)	I/O	Positive differential data strobe 1	DIFF_HSUL_12
/DQS(1)	J2	/LPDDR_DQS(1)	I/O	Negative differential data strobe 1	DIFF_HSUL_12
DQS(2)	N2	LPDDR_DQS(2)	I/O	Positive differential data strobe 2	DIFF_HSUL_12
/DQS(2)	P2	/LPDDR_DQS(2)	I/O	Negative differential data strobe 2	DIFF_HSUL_12
DQS(3)	V2	LPDDR_DQS(3)	I/O	Positive differential data strobe 3	DIFF_HSUL_12
/DQS(3)	W2	/LPDDR_DQS(3)	I/O	Negative differential data strobe 3	DIFF_HSUL_12
VRP	N7	LPDDR_VRP	--	connected to Gnd through a 40 Ω resistor	analog
VRN	M7	LPDDR_VRN	--	connected to 1V2 through a 40 Ω resistor	analog
CK	N4	LPDDR_CK	Output	Positive differential 400 MHz clock	DIFF_HSUL_12
/CK	N5	/LPDDR_CK	Output	Negative differential 400 MHz clock	DIFF_HSUL_12
ODT	P5		Output	unused	
VREF0	H7	LPDDR_VREF	--	Vref = 1V2 / 2	analog
VREF1	P7	LPDDR_VREF	--	Vref = 1V2 / 2	analog
BA(0)	M6		Output	unused	
BA(1)	L6		Output	unused	
BA(2)	L7		Output	unused	
A(0)	M4	LPDDR_A(0)	Output	LPDDR address line 0	HSUL_12
A(1)	M5	LPDDR_A(1)	Output	LPDDR address line 1	HSUL_12
A(2)	K4	LPDDR_A(2)	Output	LPDDR address line 2	HSUL_12
A(3)	L4	LPDDR_A(3)	Output	LPDDR address line 3	HSUL_12
A(4)	K6	LPDDR_A(4)	Output	LPDDR address line 4	HSUL_12
A(5)	K5	LPDDR_A(5)	Output	LPDDR address line 5	HSUL_12
A(6)	J7	LPDDR_A(6)	Output	LPDDR address line 6	HSUL_12
A(7)	J6	LPDDR_A(7)	Output	LPDDR address line 7	HSUL_12

Bank Pin	FPGA Pin	Signal	Direction	Comment	IO type
A(8)	J5	LPDDR_A(8)	Output	LPDDR address line 8	HSUL_12
A(9)	H5	LPDDR_A(8)	Output	LPDDR address line 9	HSUL_12
A(10)	J3		Output	unused	
A(11)	G5		Output	unused	
A(12)	H4		Output	unused	
A(13)	F4		Output	unused	
A(14)	G4		Output	unused	
DQ(0)	D1	LPDDR_D(0)	I/O	LPDDR2 Data line 0	HSUL_12
DQ(1)	C3	LPDDR_D(1)	I/O	LPDDR2 Data line 1	HSUL_12
DQ(2)	B2	LPDDR_D(2)	I/O	LPDDR2 Data line 2	HSUL_12
DQ(3)	D3	LPDDR_D(3)	I/O	LPDDR2 Data line 3	HSUL_12
DQ(4)	E3	LPDDR_D(4)	I/O	LPDDR2 Data line 4	HSUL_12
DQ(5)	E1	LPDDR_D(5)	I/O	LPDDR2 Data line 5	HSUL_12
DQ(6)	F2	LPDDR_D(6)	I/O	LPDDR2 Data line 6	HSUL_12
DQ(7)	F1	LPDDR_D(7)	I/O	LPDDR2 Data line 7	HSUL_12
DQ(8)	G2	LPDDR_D(8)	I/O	LPDDR2 Data line 8	HSUL_12
DQ(9)	G1	LPDDR_D(9)	I/O	LPDDR2 Data line 9	HSUL_12
DQ(10)	L1	LPDDR_D(10)	I/O	LPDDR2 Data line 10	HSUL_12
DQ(11)	L2	LPDDR_D(11)	I/O	LPDDR2 Data line 11	HSUL_12
DQ(12)	L3	LPDDR_D(12)	I/O	LPDDR2 Data line 12	HSUL_12
DQ(13)	K1	LPDDR_D(13)	I/O	LPDDR2 Data line 13	HSUL_12
DQ(14)	J1	LPDDR_D(14)	I/O	LPDDR2 Data line 14	HSUL_12
DQ(15)	K3	LPDDR_D(15)	I/O	LPDDR2 Data line 15	HSUL_12
DQ(16)	M1	LPDDR_D(16)	I/O	LPDDR2 Data line 16	HSUL_12
DQ(17)	T3	LPDDR_D(17)	I/O	LPDDR2 Data line 17	HSUL_12
DQ(18)	N3	LPDDR_D(18)	I/O	LPDDR2 Data line 18	HSUL_12
DQ(19)	T1	LPDDR_D(19)	I/O	LPDDR2 Data line 19	HSUL_12
DQ(20)	R3	LPDDR_D(20)	I/O	LPDDR2 Data line 20	HSUL_12
DQ(21)	T2	LPDDR_D(21)	I/O	LPDDR2 Data line 21	HSUL_12
DQ(22)	M2	LPDDR_D(22)	I/O	LPDDR2 Data line 22	HSUL_12
DQ(23)	R1	LPDDR_D(23)	I/O	LPDDR2 Data line 23	HSUL_12
DQ(24)	AA3	LPDDR_D(24)	I/O	LPDDR2 Data line 24	HSUL_12
DQ(25)	U1	LPDDR_D(25)	I/O	LPDDR2 Data line 25	HSUL_12
DQ(26)	AA1	LPDDR_D(26)	I/O	LPDDR2 Data line 26	HSUL_12
DQ(27)	U2	LPDDR_D(27)	I/O	LPDDR2 Data line 27	HSUL_12
DQ(28)	W1	LPDDR_D(28)	I/O	LPDDR2 Data line 28	HSUL_12

Bank Pin	FPGA Pin	Signal	Direction	Comment	IO type
DQ(29)	Y3	LPDDR_D(29)	I/O	LPDDR2 Data line 29	HSUL_12
DQ(30)	W3	LPDDR_D(30)	I/O	LPDDR2 Data line 30	HSUL_12
DQ(31)	Y1	LPDDR_D(31)	I/O	LPDDR2 Data line 31	HSUL_12
VCCO		1V2	Power		

Notes:

- In yellow, signals which cannot be permuted
- In green, test signals
- The internal DDR memory controller cannot handle more than 1 Gbytes.
- On the Vref analog inputs, a voltage equal to half the supply voltage of the LPDDR2 memory, 0.6V, must be applied
- Pin DDR_VRP is connected to Gnd through a resistor of 40 ohms.
- Pin DDR_ is connected to 1V2 through a resistor 40 ohms
- On the ZQ pin of the memory LPDDR there must be a resistor of 240 ohms
- It is not necessary to put matching resistors on the signals between the memory and the FPGA, the adaptation is within the memory component (using the value of the resistor connected to pin ZQ)
- The decoupling capacitors on the memory component are 100nF (case 0402) to be implemented to the nearest power pins of the component.
- The impedance of the wires between the FPGA and the memory component are:
    - 50 ohms for single lines
    - 100 ohms for the differential lines
- Differences in length in wires connecting the FPGA and the memory component should not exceed 0635 mm or 5 ps delay (shorter / longer)

Pour le contrôleur mémoire les paramètres pour la mémoire MT42L128M32D1 est :

The memory controller settings parameters for MT42L128M32D1 memory are:

- Memory size 4Gbits
- CAS latency 7
- Cas WRITE LATENCY 0
- RAS TO CAS Delay 7
- .precharge time 8
- Trc 63
- Tras min 42
- Tfaw 50
- Cycle time 2,5 ns

Bank 13 Configuration

Bank Pin	FPGA Pin	Peripheral	Signal	Comment	IO type
0	R7	GPS	GPS_PPS		LVCMOS33
1P	V10	GPS_UART2	GPS_TX		LVCMOS33
1N	V9	GPS_UART2	GPS_RX		LVCMOS33
2P	V8	Trigger	TRIG_IN	External Trigger IN	LVCMOS33
2N	W8	Trigger	TRIG_OUT	External Trigger OUT	LVCMOS33
3P	W11	Watchdog	Watchdog	Watchdog rearmament out signal	LVCMOS33
3N	W10	TP14		*Test_point*	HCMOS33
4P	V12	Hard Conf.	HCONF(0)	bit configuration 0	LVCMOS33
4N	W12	Hard Conf.	HCONF(1)	bit configuration 1	LVCMOS33
5P	U12	Hard Conf.	HCONF(2)	bit configuration 2	LVCMOS33
5N	U11	Hard Conf.	HCONF(3)	bit configuration 3	LVCMOS33
6P	U10	Hard Conf.	HCONF(4)	bit configuration 4	LVCMOS33
6N	U9	Hard Conf.	HCONF(5)	bit configuration 5	LVCMOS33
7P	AA12	Hard Conf.	HCONF(6)	bit configuration 6	LVCMOS33
7N	AB12	Hard Conf.	HCONF(7)	bit configuration 7	LVCMOS33
8P	AA11	Radio	RADIO_RST_OUT	Reset signal to RADIO subsystem	LVCMOS33
8N	AB11	Radio	RADIO_RST_IN	Reset signal from RADIO subsystem	LVCMOS33
9P	AB10	Ext0 connector	EXT0_I0	Extension Connector 0	LVCMOS33
9N	AB9	Ext0 connector	EXT0_I1	Extension Connector 0	LVCMOS33
10P	Y11	Ext0 connector	EXT0_I2	Extension Connector 0	LVCMOS33
10N	Y10	Ext0 connector	EXT0_I3	Extension Connector 0	LVCMOS33
11P	AA9	Ext0 connector	EXT0_O0	Extension Connector 0	LVCMOS33
11N	AA8	Ext0 connector	EXT0_O1	Extension Connector 0	LVCMOS33
12P	Y9	Ext0 connector	EXT0_O2	Extension Connector 0	LVCMOS33
12N	Y8	Ext0 connector	EXT0_O3	Extension Connector 0	LVCMOS33
13P	Y6	Ext0 connector	EXT0_I4	Extension Connector 0	LVCMOS33
13N	Y5	Ext0 connector	EXT0_I5	Extension Connector 0	LVCMOS33
14P	AA7	Ext0 connector	EXT0_I6	Extension Connector 0	LVCMOS33
14N	AA6	Ext0 connector	EXT0_I7	Extension Connector 0	LVCMOS33
15P	AB2	Ext0 connector	EXT0_O4	Extension Connector 0	LVCMOS33
15N	AB1	Ext0 connector	EXT0_O5	Extension Connector 0	LVCMOS33
16P	AB5	Ext0 connector	EXT0_O6	Extension Connector 0	LVCMOS33
16N	AB4	Ext0 connector	EXT0_O7	Extension Connector 0	LVCMOS33
17P	AB7	Ext1 connector	EXT1_I0	Extension Connector 1	LVCMOS33
17N	AB6	Ext1 connector	EXT1_I1	Extension Connector 1	LVCMOS33
18P	Y4	Ext1 connector	EXT1_I2	Extension Connector 1	LVCMOS33
18N	AA4	Ext1 connector	EXT1_I3	Extension Connector 1	LVCMOS33
19P	R6	Ext1 connector	EXT1_O0	Extension Connector 1	LVCMOS33
19N	T6	Ext1 connector	EXT1_O1	Extension Connector 1	LVCMOS33
20P	T4	Ext1 connector	EXT1_O2	Extension Connector 1	LVCMOS33
20N	U4	Ext1 connector	EXT1_O3	Extension Connector 1	LVCMOS33
21P	V5	Ext1 connector	EXT1_I4	Extension Connector 1	LVCMOS33
21N	V4	Ext1 connector	EXT1_I5	Extension Connector 1	LVCMOS33
22P	U6	Ext1 connector	EXT1_I6	Extension Connector 1	LVCMOS33
22N	U5	Ext1 connector	EXT1_I7	Extension Connector 1	LVCMOS33
23P	V7	Ext1 connector	EXT1_O4	Extension Connector 1	LVCMOS33
23N	W7	Ext1 connector	EXT1_O5	Extension Connector 1	LVCMOS33
24P	W6	Ext1 connector	EXT1_O6	Extension Connector 1	LVCMOS33
24N	W5	Ext1 connector	EXT1_O7	Extension Connector 1	LVCMOS33
25	U7	USB0	USB_IFAULT	Overcurrent on the USB OTG port	LVCMOS33

Notes:

- In yellow, signals which cannot be permuted
- In green, test signals

Bank 33 Configuration: ADC Interface

Bank Pin	FPGA Pin	Signal	Comment	IO type
0	*U19*	UART0_CTSn	Interface "Radio"	HCMOS18
1P	T21	UART0_RTSn	Interface "Radio"	HCMOS18
1N	U21	TP2	*Test_point*	HCMOS18
2P	T22	ADC0_D4_P	ADC0, data D4 positive polarity	LVDS18
2N	U22	ADC0_D4_N	ADC0, data D4 negative polarity	LVDS18
3P	V22	ADC1_D2_P	ADC1, data D2 positive polarity	LVDS18
3N	W22	ADC1_D2_N	ADC1, data D2 negative polarity	LVDS18
4P	W20	ADC1_D6_P	ADC1, data D6 positive polarity	LVDS18
4N	W21	ADC1_D6_N	ADC1, data D6 negative polarity	LVDS18
5P	U20	ADC1_D7_P	ADC1, data D7 positive polarity	LVDS18
5N	V20	ADC1_D7_N	ADC1, data D7 negative polarity	LVDS18
6P	V18	ADC1_D3_P	ADC1, data D3 positive polarity	LVDS18
6N	V19	ADC1_D3_N	ADC1, data D3 negative polarity	LVDS18
7P	AA22	ADC1_D4_P	ADC1, data D4 positive polarity	LVDS18
7N	AB22	ADC1_D4_N	ADC1, data D4 negative polarity	LVDS18
8P	AA21	ADC1_D5_P	ADC1, data D5 positive polarity	LVDS18
8N	AB21	ADC1_D5_N	ADC1, data D5 negative polarity	LVDS18
9P	Y20	ADC1_D0_P	ADC1, data D0 positive polarity	LVDS18
9N	Y21	ADC1_D0_N	ADC1, data D0 negative polarity	LVDS18
10P	AB19	ADC0_D8_P	ADC0, data D8 positive polarity	LVDS18
10N	AB20	ADC0_D8_N	ADC0, data D8 negative polarity	LVDS18
11P	Y19	ADC1_D1_P	ADC1, data D1 positive polarity	LVDS18
11N	AA19	ADC1_D1_N	ADC1, data D1 negative polarity	LVDS18
12P	*Y18*	ADC_CLK_P	output Clock ADC	LVDS18
12N	*AA18*	ADC_CLK_N	output Clock ADC	LVDS18
13P	*W17*	LED_FLG	LED_SYNC	HCMOS18
13N	*W18*	LED_ASY	LED_SYNC	HCMOS18
14P	W16	ADC0_D6_P	ADC0, data D6 positive polarity	LVDS18
14N	Y16	ADC0_D6_N	ADC0, data D6 negative polarity	LVDS18
15P	U15	ADC0_D11_P	ADC0, data D11 positive polarity	LVDS18
15N	U16	ADC0_D11_N	ADC0, data D11 negative polarity	LVDS18
16P	U17	ADC0_OR_P	ADC0, data Over range positive polarity	LVDS18
16N	V17	ADC0_OR_N	ADC0, data Over range negative polarity	LVDS18
17P	AA17	ADC0_D7_P	ADC0, data D7 positive polarity	LVDS18
17N	AB17	ADC0_D7_N	ADC0, data D7 negative polarity	LVDS18
18P	AA16	ADC0_D5_P	ADC0, data D5 positive polarity	LVDS18
18N	AB16	ADC0_D5_N	ADC0, data D5 negative polarity	LVDS18
19P	V14	ADC0_D1_P	ADC0, data D1 positive polarity	LVDS18
19N	V15	ADC0_D1_N	ADC0, data D1 negative polarity	LVDS18
20P	V13	ADC0_D10_P	ADC0, data D10 positive polarity	LVDS18
20N	W13	ADC0_D10_N	ADC0, data D10 negative polarity	LVDS18
21P	W15	ADC0_D9_P	ADC0, data D9 positive polarity	LVDS18
21N	Y15	ADC0_D9_N	ADC0, data D9 negative polarity	LVDS18
22P	Y14	ADC0_D0_P	ADC0, data D0 positive polarity	LVDS18
22N	AA14	ADC0_D0_N	ADC0, data D0 negative polarity	LVDS18
23P	Y13	ADC0_D2_P	ADC0, data D2 positive polarity	LVDS18
23N	AA13	ADC0_D2_N	ADC0, data D2 negative polarity	LVDS18
24P	AB14	ADC0_D3_P	ADC0, data D3 positive polarity	LVDS18
24N	AB15	ADC0_D3_N	ADC0, data D3 negative polarity	LVDS18
25	U14	TP3	*Test_point*	HCMOS18

Notes:

- In yellow, signals which cannot be permuted
- In green, test signals

Bank 34 Configuration: ADC Interface

Bank Pin	FPGA Pin	Signal	Comments	IO type
0	*H15*	*TP4*	*Test_point*	HCMOS18
1P	J15	ADC1_D8_P	ADC1, data D8 positive polarity	LVDS18
1N	K15	ADC1_D8_N	ADC1, data D8 negative polarity	LVDS18
2P	J16	ADC1_D9_P	ADC1, data D9 positive polarity	LVDS18
2N	J17	ADC1_D9_N	ADC1, data D9 negative polarity	LVDS18
3P	K16	ADC1_D10_P	ADC1, data D10 positive polarity	LVDS18
3N	L16	ADC1_D10_N	ADC1, data D10 negative polarity	LVDS18
4P	L17	ADC1_D11_P	ADC1, data D11 positive polarity	LVDS18
4N	M17	ADC1_D11_N	ADC1, data D11 negative polarity	LVDS18
5P	N17	ADC2_OR_P	ADC2, data Over range positive polarity	LVDS18
5N	N18	ADC2_OR_N	ADC2, data Over range negative polarity	LVDS18
6P	M15	ADC2_D0_P	ADC2, data D0 positive polarity	LVDS18
6N	M16	ADC2_D0_N	ADC2, data D0 negative polarity	LVDS18
7P	J18	ADC2_D1_P	ADC2, data D1 positive polarity	LVDS18
7N	K18	ADC2_D1_N	ADC2, data D1 negative polarity	LVDS18
8P	J21	ADC2_D2_P	ADC2, data D2 positive polarity	LVDS18
8N	J22	ADC2_D2_N	ADC2, data D2 negative polarity	LVDS18
9P	J20	ADC2_D3_P	ADC2, data D3 positive polarity	LVDS18
9N	K21	ADC2_D3_N	ADC2, data D3 negative polarity	LVDS18
10P	L21	ADC2_D4_P	ADC2, data D4 positive polarity	LVDS18
10N	L22	ADC2_D4_N	ADC2, data D4 negative polarity	LVDS18
11P	K19	ADC2_D5_P	ADC2, data D5 positive polarity	LVDS18
11N	K20	ADC2_D5_N	ADC2, data D5 negative polarity	LVDS18
12P	L18	MST_CLK_P	Master Clock System	LVDS18
12N	L19	MST_CLK_N	Master Clock System	LVDS18
13P	*M19*	*TP5*	*Test_point*	HCMOS18
13N	*M20*	*TP6*	*Test_point*	HCMOS18
14P	N19	ADC2_D6_P	ADC2, data D6 positive polarity	LVDS18
14N	N20	ADC2_D6_N	ADC2, data D6 negative polarity	LVDS18
15P	M21	ADC2_D7_P	ADC2, data D7 positive polarity	LVDS18
15N	M22	ADC2_D7_N	ADC2, data D7 negative polarity	LVDS18
16P	N22	ADC2_D8_P	ADC2, data D8 positive polarity	LVDS18
16N	P22	ADC2_D8_N	ADC2, data D8 negative polarity	LVDS18
17P	R20	ADC2_D9_P	ADC2, data D9 positive polarity	LVDS18
17N	R21	ADC2_D9_N	ADC2, data D9 negative polarity	LVDS18
18P	P20	ADC2_D10_P	ADC2, data D10 positive polarity	LVDS18
18N	P21	ADC2_D10_N	ADC2, data D10 negative polarity	LVDS18
19P	N15	ADC2_D11_P	ADC2, data D11 positive polarity	LVDS18
19N	P15	ADC2_D11_N	ADC2, data D11 negative polarity	LVDS18
20P	P17	ADC1_OR_P	ADC1, data Over range positive polarity	LVDS18
20N	P18	ADC1_OR_N	ADC1, data Over range negative polarity	LVDS18
21P	T16	ADC3_D0_P	ADC2, data D0 positive polarity	LVDS18
21N	T17	ADC3_D0_N	ADC3, data D0 negative polarity	LVDS18
22P	R19	ADC3_D1_P	ADC3, data D1 positive polarity	LVDS18
22N	T19	ADC3_D1_N	ADC3, data D1 negative polarity	LVDS18
23P	R18	ADC3_D2_P	ADC3, data D2 positive polarity	LVDS18
23N	T18	ADC3_D2_N	ADC3, data D2 negative polarity	LVDS18
24P	P16	ADC3_D3_P	ADC3, data D3 positive polarity	LVDS18
24N	R16	ADC3_D3_N	ADC3, data D3 negative polarity	LVDS18
25	R15	TP7	*Test_point*	HCMOS18

Notes:

- In yellow, signals which cannot be permuted
- In green, test signals

Bank 35 Configuration: ADC Interface

Bank Pin	FPGA Pin	Signal	Comment	IO type
0	H17	*TP8*	*Test_point*	HCMOS18
1P	F16	ADC3_D5_P	ADC3, data D5 positive polarity	LVDS18
1N	E16	ADC3_D5_N	ADC3, data D5 negative polarity	LVDS18
2P	D16	ADC3_D4_P	ADC3, data D4 positive polarity	LVDS18
2N	D17	ADC3_D4_N	ADC3, data D4 negative polarity	LVDS18
3P	E15	ADC3_D6_P	ADC3, data D6 positive polarity	LVDS18
3N	D15	ADC3_D6_N	ADC3, data D6 negative polarity	LVDS18
4P	G15	ADC3_D7_P	ADC3, data D7 positive polarity	LVDS18
4N	G16	ADC3_D7_N	ADC3, data D7 negative polarity	LVDS18
5P	F18	ADC3_D8_P	ADC3, data D8 positive polarity	LVDS18
5N	E18	ADC3_D8_N	ADC3, data D8 negative polarity	LVDS18
6P	G17	ADC3_D9_P	ADC3, data D9 positive polarity	LVDS18
6N	F17	ADC3_D9_N	ADC3, data D9 negative polarity	LVDS18
7P	C15	ADC3_D10_P	ADC3, data D10 positive polarity	LVDS18
7N	B15	ADC3_D10_N	ADC3, data D10 negative polarity	LVDS18
8P	B16	ADC3_D11_P	ADC3, data D11 positive polarity	LVDS18
8N	B17	ADC3_D11_N	ADC3, data D11 negative polarity	LVDS18
9P	A16	ADC3_OR_P	ADC3, data Over range positive polarity	LVDS18
9N	A17	ADC3_OR_N	ADC3, data Over range negative polarity	LVDS18
10P	A18	ADC4_D0_P	ADC4, data D0 positive polarity	LVDS18
10N	A19	ADC4_D0_N	ADC4, data D0 negative polarity	LVDS18
11P	C17	ADC4_D1_P	ADC4, data D1 positive polarity	LVDS18
11N	C18	ADC4_D1_N	ADC4, data D1 negative polarity	LVDS18
12P	D18	*TP9*	*Test_point*	HCMOS18
12N	C19	*TP10*	*Test_point*	HCMOS18
13P	B19	*TP11*	*Test_point*	HCMOS18
13N	B20	*TP12*	*Test_point*	HCMOS18
14P	D20	ADC4_D2_P	ADC4, data D2 positive polarity	LVDS18
14N	C20	ADC4_D2_N	ADC4, data D2 negative polarity	LVDS18
15P	A21	ADC4_D3_P	ADC4, data D3 positive polarity	LVDS18
15N	A22	ADC4_D3_N	ADC4, data D3 negative polarity	LVDS18
16P	D22	ADC4_D4_P	ADC4, data D4 positive polarity	LVDS18
16N	C22	ADC4_D4_N	ADC4, data D4 negative polarity	LVDS18
17P	E21	ADC4_D5_P	ADC4, data D5 positive polarity	LVDS18
17N	D21	ADC4_D5_N	ADC4, data D5 negative polarity	LVDS18
18P	B21	ADC4_D6_P	ADC4, data D6 positive polarity	LVDS18
18N	B22	ADC4_D6_N	ADC4, data D6 negative polarity	LVDS18
19P	H19	ADC4_D7_P	ADC4, data D7 positive polarity	LVDS18
19N	H20	ADC4_D7_N	ADC4, data D7 negative polarity	LVDS18
20P	G19	ADC4_D8_P	ADC4, data D8 positive polarity	LVDS18
20N	F19	ADC4_D8_N	ADC4, data D8 negative polarity	LVDS18
21P	E19	ADC4_D9_P	ADC4, data D9 positive polarity	LVDS18
21N	E20	ADC4_D9_N	ADC4, data D9 negative polarity	LVDS18
22P	G20	ADC4_D10_P	ADC4, data D10 positive polarity	LVDS18
22N	G21	ADC4_D10_N	ADC4, data D10 negative polarity	LVDS18
23P	F21	ADC4_D11_P	ADC4, data D11 positive polarity	LVDS18
23N	F22	ADC4_D11_N	ADC4, data D11 negative polarity	LVDS18
24P	H22	ADC4_OR_P	ADC4, data Over range positive polarity	LVDS18
24N	G22	ADC4_OR_N	ADC4, data Over range negative polarity	LVDS18
25	H18	TP13	*Test_point*	HCMOS18

Notes:

- In yellow, signals which cannot be permuted
- In green, test signals

General information:

- The power of the Ethernet connector 10/100/1000 must be done through a filter, reference BLM21PG220S
- No Schottky diode used on the input pin RESETN of the Ethernet component PHY 88E1518
- The 125 MHz output pin of the PHY Ethernet component must remain "UNCONNECTED"

Revisions:

13/04/13 : initial version

12/06/13 : placement of signals UART0_CTSn & UART0_RTSn signals on "Bank pin" 0 1P of the bank 13 instead of two test points (the number of test points on the Banks in 1V8 is now 14)

26/06/13: assignment of Bank35 signals (the number of test points in 3.3V is 4, the total number of test points is 18).
The test points are in green

02/07/13 Adding of FPGA pin numbers for the Banks 13, 33, 34, 35, 500, 501 and 502
Upgrade of the signals of the Banks 500 and 501
Assigning and definition of output levels of des pins for Bank 502: LPDDR2 Memory Interface
Adding PS_MIO_VREF & PS_SRST_B signals in the "MIO configuration Table"

17/07/13 adding connection information between FPGA and memory LPDDR2
Update general information part
Network connector
port 25 of the Bank 35 receive over current signal of the USB OTG port (the number of test points is 17 now)
MOI (0) becomes signal / RST of the Ethernet PHY
MOI (7) becomes signal / RST of the USB OTG PHY

25/07/14 ports MIO50 (pin D13) & MIO51 (pin C10) becomes test points
port 13P of bank 13 becomes LED_FLG (Input)
port 13N of bank 13 becomes LED_ASY (Output)
port 8N of bank 35 becomes RESET_IN_RADIO
port 8P of bank 35 becomes RESET_OUT_RADIO
the number of test points is 15 now

30/07/14 correction, ports Vref (ADC) & SRST_B was defined twice in the MOI Configuration Table
Correction, BANK 13 : ADC0_D9_N signal was affected to the wrong pin
Correction, BANK 34 : ADC4_D4_P signal was affected to the wrong pin

06/08/14 update of Banks 13, 33, 34 et 35 pinout after evaluation board layout routing (EVAL_UUB)

17/10/14 Banks reallocation:
Bank 13 signals are transferred on Bank 33, Bank 33 signals are transferred on Bank 34, Bank 34 signals are transferred on Bank 35, and Bank 35 signals are transferred on Bank 13
MST_CLK signal is transferred from the Bank 35 to the Bank34 (port 12P & 12 N)