VHDL Lab 5:

Task 5.1

A screenshot of a computer program

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A screenshot of a computer program

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Task 5.2

Answer the following questions:

✓ Estimated clock period -> 6.816 ns

✓ Worst case latency -> 25ms

✓ Number of DSP48E utilized in the implementation -> 2

✓ Number of FFs utilized in the implementation -> 66

✓ Number of LUTs utilized in the implementation -> 371

A screenshot of a computer

Description automatically generated A screenshot of a computer

Description automatically generated

Task 5.3)

In FPGA programming, using VHDL provides fine control over hardware details and customization but involves a steep learning curve and potential challenges in debugging and optimization. On the other hand, High-Level Synthesis (HLS) with C++ offers rapid prototyping, code reusability, and abstracts hardware complexities, making it more accessible for software developers. However, automatic VHDL code generated by HLS tools may lack the level of optimization achievable through manual VHDL programming, and developers have limited control over intricate hardware details. While HLS code readability in Vitis HLS is generally enhanced by high-level constructs and tool-specific features, challenges may arise in understanding complex optimizations and debugging generated VHDL code. The choice between VHDL and HLS depends on project requirements, the need for control, and the expertise of the development team.