ENE5220 Digital Integrated Circuit

HW1 MOSFET Capacitance

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1 Introduction

An NMOS transistor is modeled using a predictive SPICE model for 45 nm technology, with a width of 100 nm and a length of 45 nm. Three different configurations, all utilizing identical NMOS transistors, are analyzed. In the first circuit, the capacitances of the gate, drain, and source are examined as the supply voltage V_S varies from 0 to 1.2 V. In the subsequent circuit models, the focus shifts to analyzing the rise and fall delays at the NMOS node connected to a resistor. Additionally, the equivalent capacitance circuit is calculated to approximate the NMOS behavior, where V_S ranges from 0 V to 1.2 V. The rise and fall times are both 1 ps, with a pulse width of 999 ps and a period of 2 ns.

2 Config 1

The NMOS model is biased as shown in Figure 1, with the bulk grounded, and the gate voltage V_G varying from 0 to 1.2 V. We delve into the relationship between the capacitances of the gate, drain, and source, and the gate voltage V_G.

2.1 Gate Capacitance VS. V_G

Figure 2 shows the relationship between gate capacitance and V_G. To generate this plot, we performed a DC analysis with V_G varying from 0 to 1.2 V and recorded the node capacitances C_{gg}, C_{gd}, and C_{gs}. The statement are as follows.

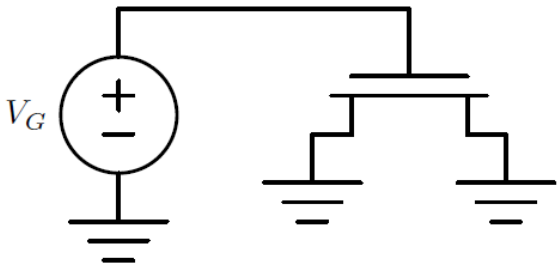

Fig. 1: NMOS model 1

```
.dc VVG 0 1.2 0.01 ** DC analysis
.print M1:CGGBO    ** Get Cgg, total gate capacitance
.print M1:CGDBO    ** Get Cgd
.print M1:CGSBO    ** Get Cgs
```

To Get the capacitance of C_gb, we use the relationship in equation (1).

$$|C_{gg}| = |C_{gd}| + |C_{gs}| + |C_{gb}| \tag{1}$$

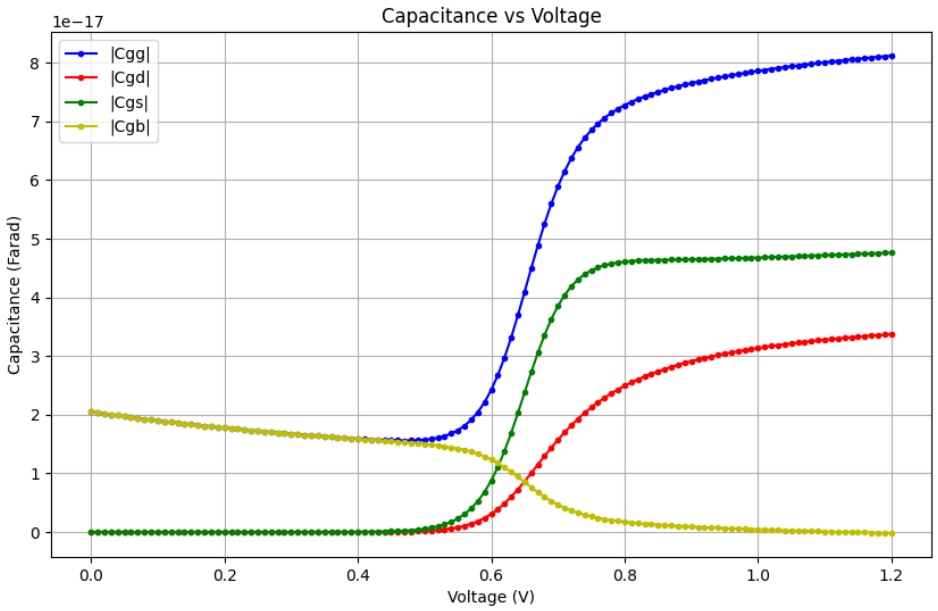

Fig. 2: Gate Capacitance VS. V_G

2.2 Bulk Capacitance VS. V_G

Figure 3 shows the relationship between bulk capacitance and V_G. To generate this plot, we performed a DC analysis with V_G varying from 0 to 1.2 V and recorded

the node capacitances C_{bg}, C_{bd}, and C_{bs}. The statement are as follows.

```
.dc VVG 0 1.2 0.01 ** DC analysis
.print M1:CBGBO    ** Get Cbg
.print M1:CBDBO    ** Get Cbd
.print M1:CBSBO    ** Get Cbs
```

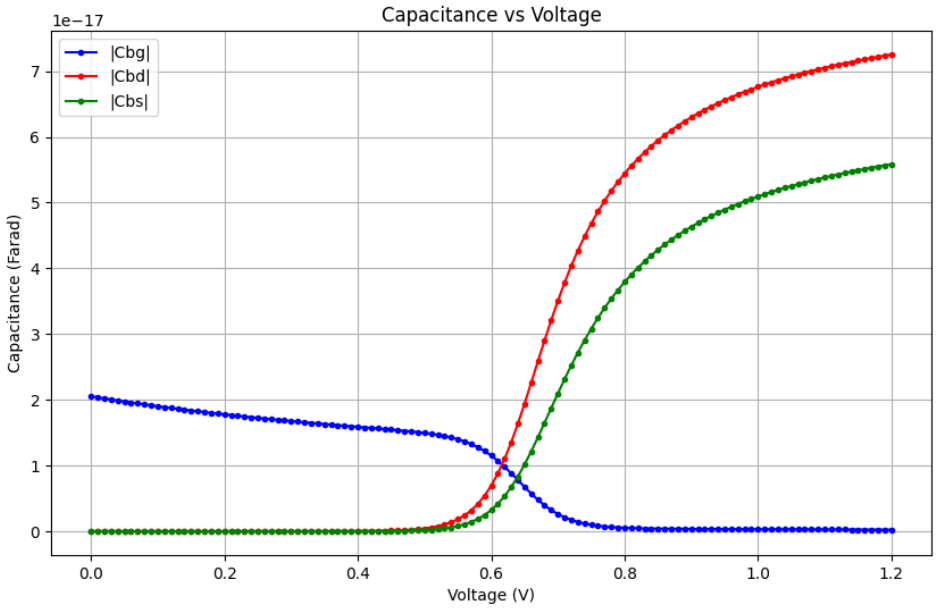

Fig. 3: Bulk Capacitance VS. V_G

2.3 Drain Capacitance VS. V_G

Figure 4 shows the relationship between drain capacitance and V_G. To generate this plot, we performed a DC analysis with V_G varying from 0 to 1.2 V and recorded the node capacitances C_{dd}, C_{dg}, and C_{ds}. The statement are as follows.

```
.dc VVG 0 1.2 0.01 ** DC analysis
.print M1:CDDBO    ** Get Cdd, total drain capacitance
.print M1:CDGBO    ** Get Cdg
.print M1:CDSBO    ** Get Cds
```

To Get the capacitance of C_db, we use the relationship in equation (2).

$$|C_{dd}| = |C_{dg}| + |C_{ds}| + |C_{db}| \tag{2}$$

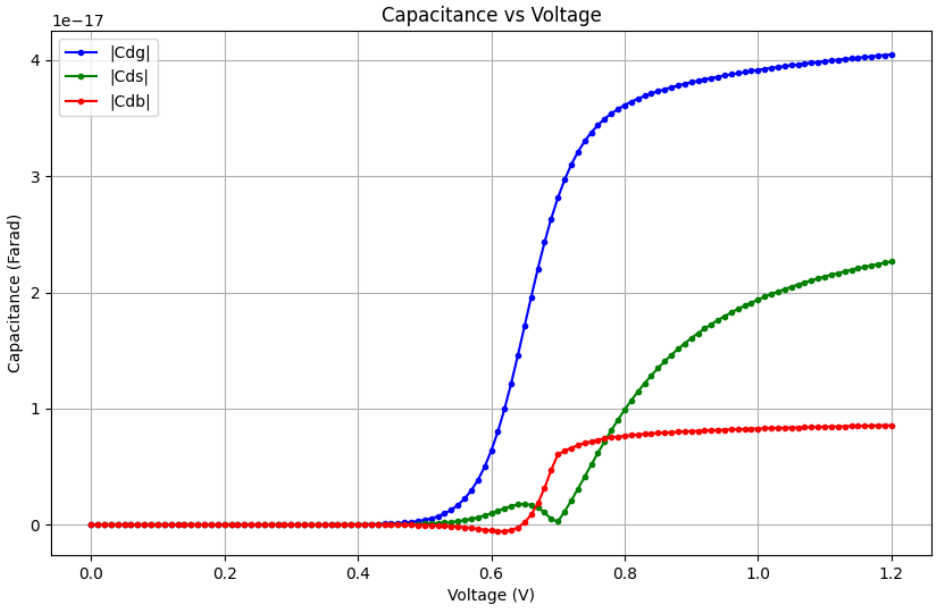

Fig. 4: Drain Capacitance VS. V_G

2.4 Observation

In Section (2.1), when the gate voltage, $V_G << 0$, the channel is in accumulation, and the total gate capacitance, C_{gg}, is dominated by the oxide capacitance.

$$|C_{gg}| = |C_{bg}|$$

and

$$|C_{gd}| = |C_{ds}| = 0$$

As V_G increases, the channel surface becomes depleted, and the gate capacitance is modeled as the depletion capacitance in series with the oxide capacitance, causing $|C_{gg}|$ to decrease slightly. When the channel enters strong inversion, i.e., when V_{GS} exceeds the threshold voltage ($V_T \approx 0.6\,V$), free electrons appear in the channel, causing $|C_{gs}|$ and $|C_{gd}|$ to increase, dominating $|C_{gg}|$. Consequently, the electron sheet under the gate leads to $|C_{gb}| \approx 0$.

Both the source and drain of the NMOS are grounded. Ideally, $|C_{gd}|$ and $|C_{gs}|$ should have the same value due to the symmetrical structure of the NMOS. However, from Figure 2, we observe that this is not the case. Most of the time, $|C_{gs}|$ is larger than $|C_{gd}|$. In my opinion, the model provided by the foundry does not have a

perfectly symmetrical structure.

In Section (2.2), when V_G is smaller than the threshold voltage ($V_T \approx 0.6\,V$), the channel is in depletion, leading to small values of $|C_{bd}|$ and $|C_{bs}|$. $|C_{bg}|$ slightly decreases because the gate capacitance is modeled as the depletion capacitance in series with the oxide capacitance. When V_G surpasses V_T, $|C_{bg}|$ becomes very small, while $|C_{bd}|$ and $|C_{bs}|$ increase drastically. From Figure 3, we can still observe the asymmetry in the real NMOS structure.

In Section (2.3), when V_G is smaller than the threshold voltage, $|C_{dg}|$, $|C_{ds}|$, and $|C_{db}|$ are nearly zero. As the channel enters strong inversion, the drain capacitances begin to increase. Several interesting phenomena can be observed in Figure 4. For $|C_{ds}|$, it slightly increases when $V_G > V_T$, but soon decreases before bouncing back to increase again. In my opinion, the NMOS enters the saturation region ($V_{DS} > V_{GS} - V_T$) at the bouncing point. Additionally, $|C_{db}|$ appears to become saturated as the NMOS moves into the saturation region.

Ideally, $|C_{dg}|$ and $|C_{gd}|$ should have the same value, as should $|C_{gb}|$ and $|C_{bg}|$. However, from Figures 5 and 6, this is not the case. These capacitances differ when V_G is around V_T. This occurs because capacitances in MOS devices are non-linear and voltage-dependent, particularly in strong inversion or saturation. The asymmetry in the NMOS structure and the differing voltage dependencies between the gate and drain terminals cause $|C_{gd}|$ and $|C_{dg}|$, as well as $|C_{gb}|$ and $|C_{bg}|$, to behave differently.

3 Config 2

The NMOS transistor can function as a MOS capacitor when properly configured. In this case, it is connected as shown in Figure 7, with the bulk terminal of the NMOS grounded.

3.1 Total Gate Capacitance and Charge VS. V_S

Figures 8 and 9 show the relationship between total gate capacitance, C_{gg}, and total gate charge, Q_g, and the supply voltage, V_S. To generate these plots, we

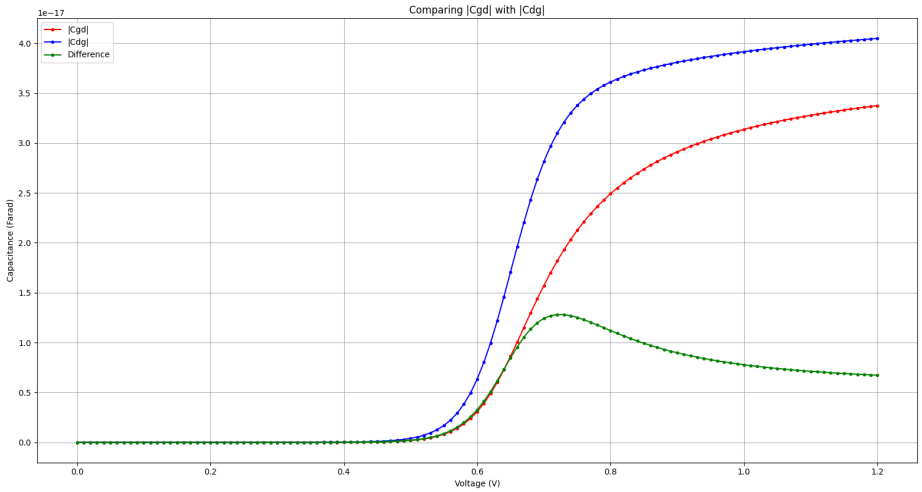

Fig. 5: Comparing C_{gd} with C_{dg}

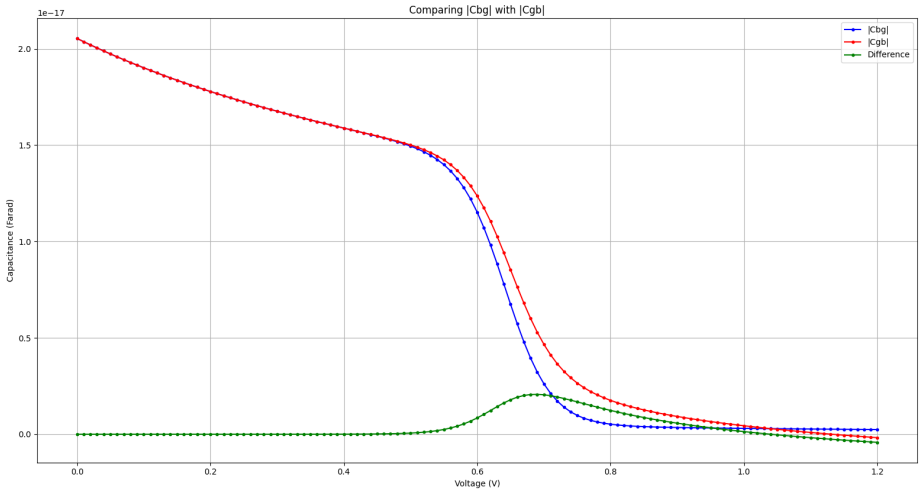

Fig. 6: Comparing C_{bg} with C_{gb}

performed a DC analysis with V_S varying from 0 to 1.2 V and recorded the node capacitance C_{gg} and charge Q_g. The statements are as follows.

```
.dc VVS 0 1.2 0.01 ** DC analysis
.print M1:CGGBO    ** Get Cgg, total gate capacitance
.print M1:QG     ** Get total gate charge
```

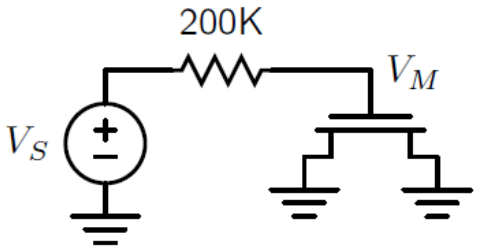

Fig. 7: NMOS model 2

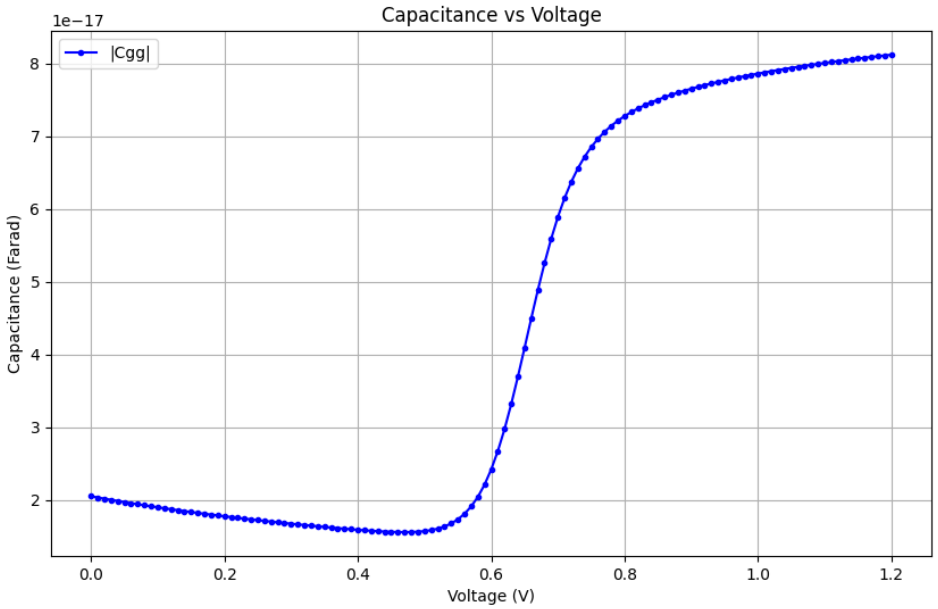

Fig. 8: Total Gate Capacitance VS. V_S

3.2 Rise and Fall Delays for V_M

To determine the rise and fall delays, a transient analysis is performed. The supply voltage, V_S, is applied as a pulse ranging from 0 V to 1.2 V, with rise and fall times of 1 ps, a pulse width of 999 ps, and a period of 2 ns. The trigger voltage is set to 0.6 V. The statements and results are as follows.

```
    ** Set supply voltage as as pulse
VVS VS 0 PULSE(0 1.2 10n 1p 1p 999p 2n)

.tran 0.1p 20n    ** Transient analysis

    ** measure rise delay
.measure tran tdr trig V(VS) val = 0.6 rise = 1
+                 targ V(VM) val = 0.6 rise = 1

    ** measure fall delay
```

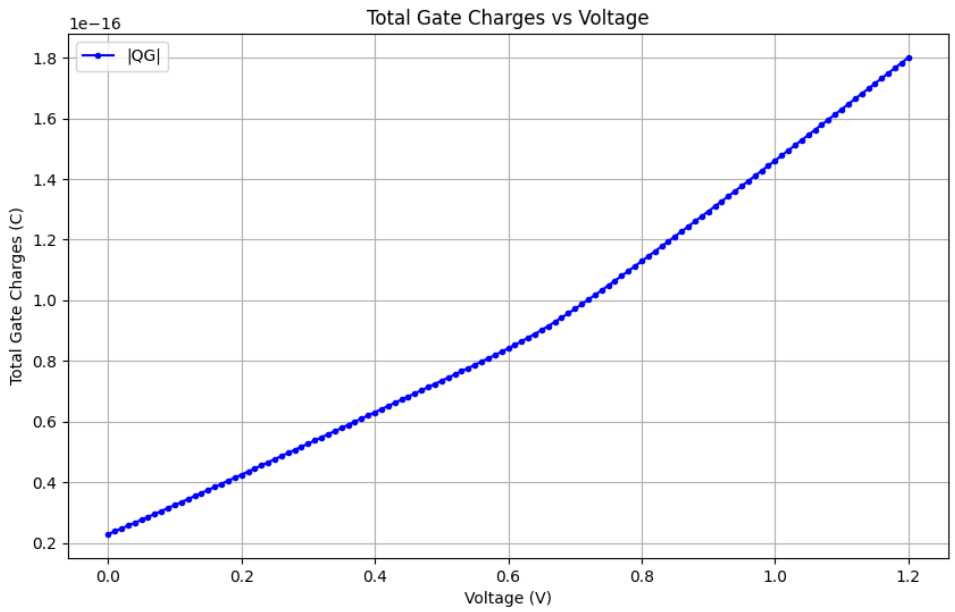

Fig. 9: Total Gate Charge VS. V_S

```
11    .measure tran tdf trig V(VS) val = 0.6 fall = 1
12    +                 targ V(VM) val = 0.6 fall = 1
```

- **Rise Delay:** 14.5264 ps
- **Fall Delay:** 21.6440 ps

3.3 Large Signal Equivalent Capacitance

We can apply Equation (3) to find the large signal equivalent capacitance.

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{High}) - Q_j(V_{Low})}{V_{High} - V_{Low}} = \frac{180.0138a - 22.9590a}{1.2 - 0} = 130.879\,aF \quad (3)$$

3.4 Rise and Fall Delays for V_M when NMOS is replaced by C_{eq}

We can repeat the procedure described in Section (3.2). The results are as follows.

- **Rise Delay:** 18.1376 ps

- **Fall Delay:** 17.9779 ps

3.5 Observation

From Figures 8 and 9 in Section (3.1), we observe that although the charge on the gate is accumulating, the total gate capacitance slightly drops when the channel approaches strong inversion. This is because the gate capacitance is modeled as the depletion capacitance in series with the oxide capacitance.

Table 1 summarizes the rise and fall delays of the NMOS circuit and the equivalent capacitance circuit. The rise delay of the NMOS is faster than that of the equivalent capacitance circuit, but the fall delay of the NMOS is slower. However, the average delay of both is nearly identical. Figure 10 shows the derivatives of charge for the NMOS gate and the equivalent capacitor, which explains the phenomena observed in Table 1. It is known that delay time is proportional to the product of resistance, R, and the equivalent capacitance, C_{eq}. Before V_M reaches the threshold voltage V_T, dQ_{NMOS}/dV_M is smaller than $dQ_{C_{eq}}/dV_M$. Since both share the same resistor, the rise delay of the NMOS is shorter than that of C_{eq}, and vice versa for the fall delay.

	Rise Delay, tdr (ps)	Fall Delay, tdf (ps)	Average (ps)
NMOS	14.5264	21.6440	18.0582
C_{eq}	18.1376	17.9779	18.0578
Error (%)	24.8596	16.9381	0.0002215

Table 1: Rise and Fall Delay for V_M

4 Config 3

The NMOS transistor is connected as shown in Figure 11, with the bulk terminal connected to ground.

4.1 Rise and Fall Delays for V_D

We can repeat the procedure described in Section (3.2). The results are as follows.

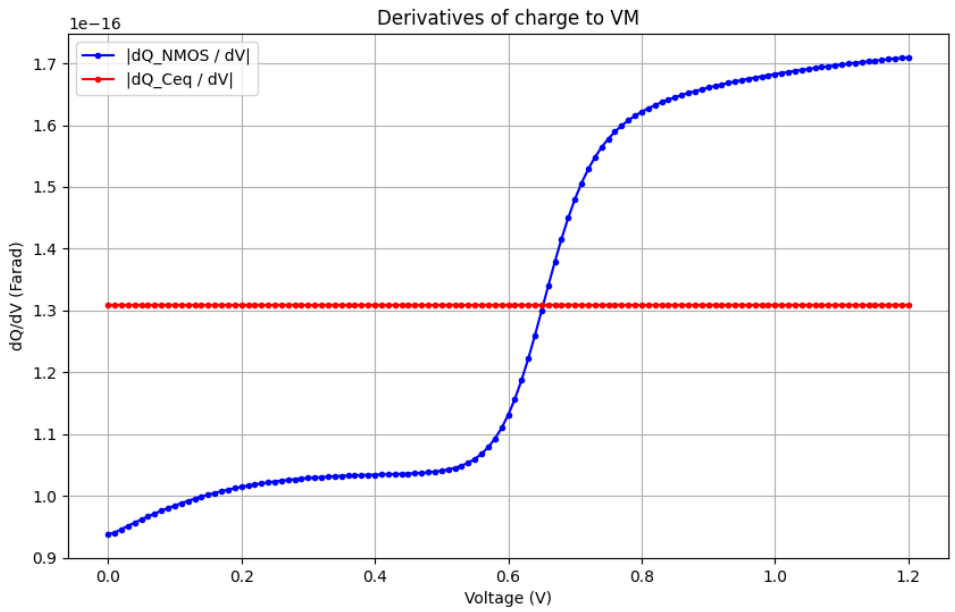

Fig. 10: Derivatives of Charge to V_M

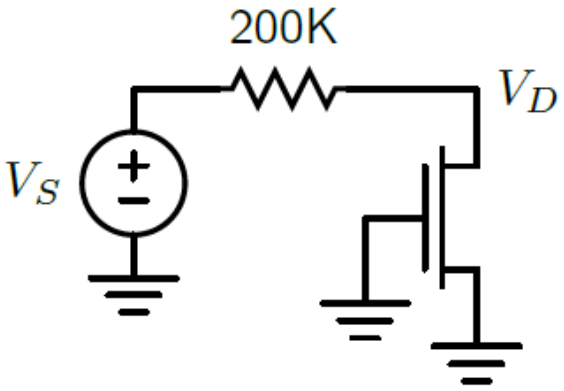

Fig. 11: NMOS model 3

- **Rise Delay:** 13.1347 ps
- **Fall Delay:** 11.3913 ps

4.2 Equivalent Capacitance

The average delay time we found in section (4.1) is $12.2630\,ps$ Then we can take advantage of the equation (4) to get the equivalent capacitance.

$$V_D = 1.2(1 - \exp^{\frac{-t}{RC_{eq}}}) = 0.6 \tag{4}$$

Where R = $200k\Omega$, t = $12.2630\,ps$. Then, we have,

$$\frac{-t}{RC_{eq}} = \ln 0.5 \tag{5}$$

$$C_{eq} = \frac{-12.2630\,ps}{200k\Omega * \ln 0.5} = 88.4588\,aF \tag{6}$$

Repeat the procedure described in Section (3.2). The results are as follows.

- **Rise Delay:** 12.4263 ps
- **Fall Delay:** 12.2953 ps

4.3 Obervation

Table 2 summarizes the rise and fall delay times of the NMOS and the equivalent capacitance. However, when comparing the derivatives of charges in the NMOS drain and the equivalent capacitance, significant differences are observed, as shown in Figure 12. This discrepancy cannot fully explain the phenomena observed in Table 2. Therefore, I calculated the equivalent capacitance using the large signal approximation, yielding:

$$C_{eq,Large} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{High}) - Q_j(V_{Low})}{V_{High} - V_{Low}} = \frac{28.9739\,\text{aC} - (-1.9589\,\text{aC})}{1.2 - 0} = 25.7773\,\text{aF} \tag{7}$$

We find that $C_{eq,Large}$ is approximately 30% of C_{eq} as discussed in Section (4.2). However, Figure 13 appears to better explain the phenomena observed in Table 2.

Let us further explore the decrease in dQ_{NMOS}/dV_D shown in Figure 13. Figure 14 reveals that there is still some leakage current from drain to source, even though the NMOS gate is grounded, indicating that the NMOS is not fully turned on. This leakage current results in the loss of charges that should have remained on the drain side, affecting its behavior as a capacitor.

	Rise Delay, tdr (ps)	Fall Delay, tdf (ps)	Average (ps)
NMOS	13.1347	11.3913	12.2630
C_{eq}	12.4263	12.2953	12.3680
Error (%)	5.3933	7.9359	0.7975

Table 2: Rise and Fall Delay for V_D

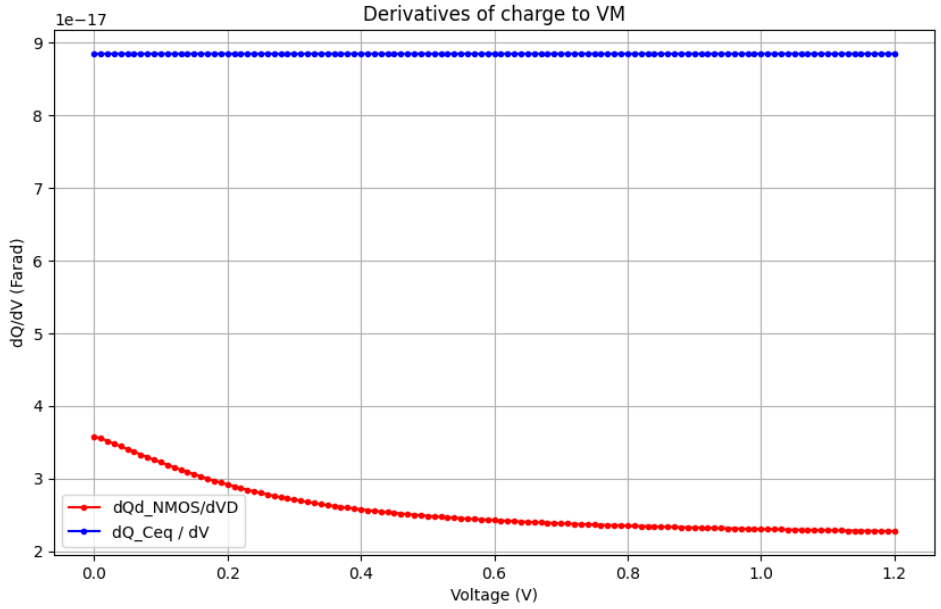

Fig. 12: Derivatives of Charge to V_D

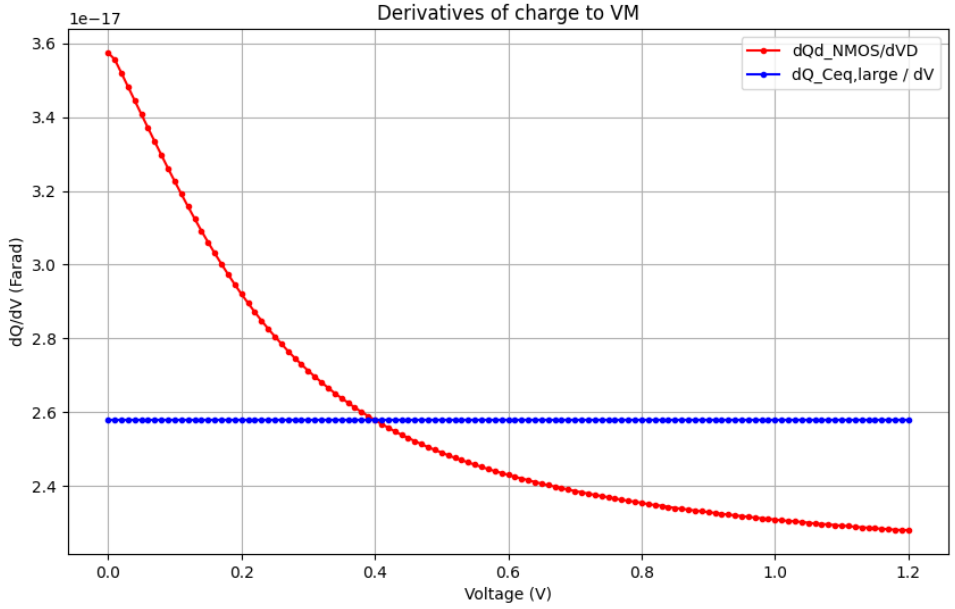

Fig. 13: Derivatives of Charge to V_D, large signal C_{eq}

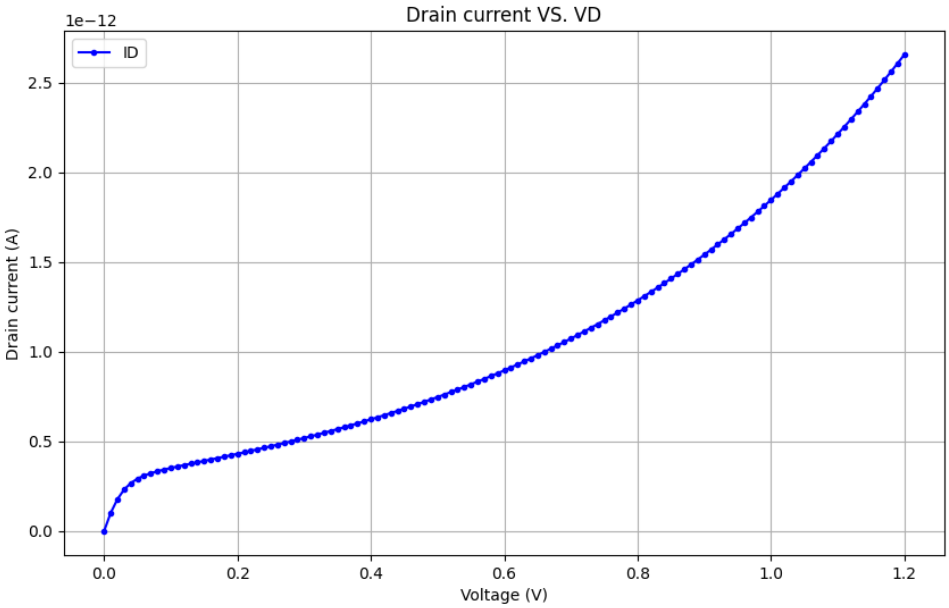

Fig. 14: Drain Current