ENE5220 Digital Integrated Circuit

HW2 INV Voltage Transfer Curves

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1 Introduction

A CMOS inverter, designed using 45nm technology, is a fundamental digital logic gate widely employed in modern integrated circuits. It consists of a PMOS and NMOS transistor in a complementary configuration, where the input signal controls the switching between the two transistors. When the input (**VIN**) is high, the NMOS turns on, pulling the output (**VOUT**) to ground; when the input is low, the PMOS turns on, pulling the output to the supply voltage, producing the characteristic inverting behavior.

To explore its behavior, a CMOS inverter is modeled using a predictive SPICE model, as shown in Figure 1. The widths of the PMOS and NMOS transistors can be adjusted, and using this model, we aim to examine key parameters such as switching voltage (V_M), voltage gain (g) at V_M, and noise margin for various transistor widths. Additionally, we investigate the trade-offs between power consumption and performance as the supply voltage decreases, with a focus on how these changes affect switching voltage, gain, and noise margin.

2 Analysis of CMOS Inverter with PMOS Width = 200nm and NMOS Width = 100nm

In this section, we analyze the behavior of a CMOS inverter with a PMOS transistor width of 200nm and an NMOS transistor width of 100nm. The analysis

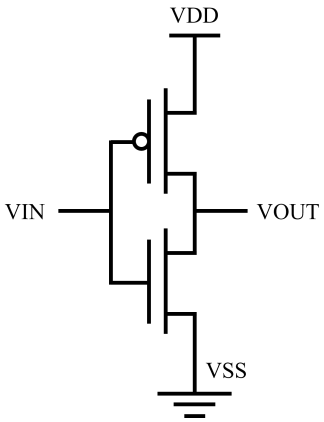

Fig. 1: CMOS inverter

involves several key performance parameters, including the voltage transfer characteristics, the switching voltage (V_M), and the voltage gain (g) at the switching threshold. Furthermore, we will use the gain and a piecewise linear approximation to calculate noise margins such as V_{IL}, V_{IH}, NML, and NMH. This analysis provides insight into the performance and robustness of the inverter, especially in terms of its switching behavior and noise tolerance.

2.1 Voltage Transfer Curve

The voltage transfer curve (VTC) of a CMOS inverter describes the relationship between the input voltage (V_{IN}) and the output voltage (V_{OUT}). It is a key characteristic that illustrates the inverter' s switching behavior, showing how the output transitions from one logic level to another as the input voltage varies. By plotting the VTC, we can identify critical points such as the switching voltage (V_M), and analyze the inverter's gain and noise margins, which are essential for evaluating its performance in digital circuits.

To generate the VTC, a DC analysis is performed by sweeping V_{IN} from 0 to 1.2 volts. The resulting plot is shown in Figure 2.

```
1    .dc VIN 0 1.2 100u       ** DC analysis
```

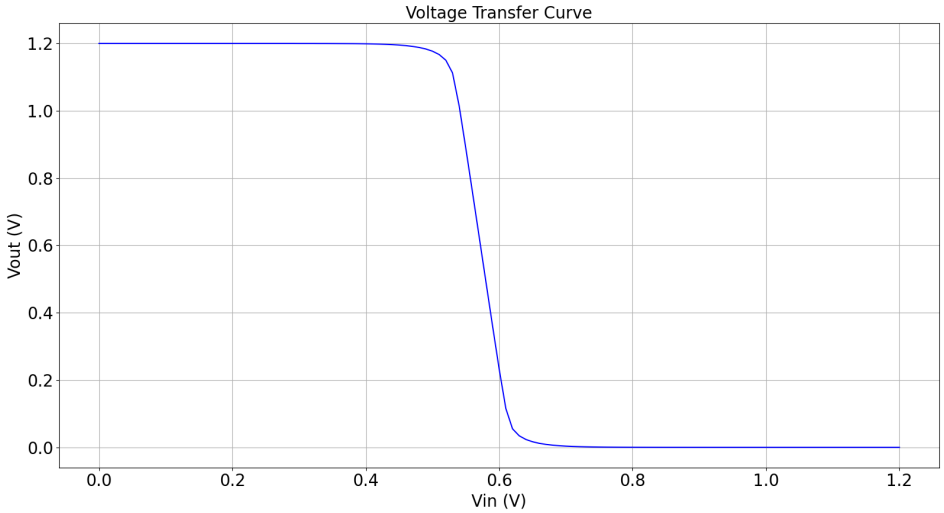

Fig. 2: Voltage Transfer Curves

2.2 switching voltage V_M

The switching voltage (V_M) of a CMOS inverter is the input voltage at which the output voltage is equal to the input voltage, as defined in Equation 1. This occurs when both the PMOS and NMOS transistors are in their saturation regions.

$$V_{IN} = V_{OUT} = V_M \tag{1}$$

To extract the switching voltage V_M, the following statement can be used during a DC analysis, and the desired result is $V_M = 573.8797\,mV$.

```
1   .measure dc VM when V(VOUT) = V(VIN) ** Measure the switching
      voltage
```

2.3 Gain g at the Switching Threshold

In this section, we analyze the voltage gain (g) of the CMOS inverter at the switching voltage (V_M). The gain is defined as the rate of change of the output voltage with respect to the input voltage. To extract the voltage gain (g) at the switching voltage (V_M), the following statement can be used during a DC analysis, and the desired result is $g = -13.2237$.

```
.measure dc g derivative V(VOUT) at VA ** Measure the gain at
   switching voltage
```

2.4 Calculation of V_{IL}, V_{IH}, NML, and NMH Using Gain and Piecewise Linear Approximation

In this section, we calculate the V_{IL}, V_{IH}, NM_L, and nNM_H of the CMOS inverter using the gain and a piecewise linear approximation of the voltage transfer curve. These parameters are defined and found in Equations 2, 3, 4, and 5. Once the voltage gain (g) and switching voltage (V_M) are determined, all these parameters can be derived.

$$V_{IH} = V_M - \frac{V_M}{g} = 0.5739 - \frac{0.5739}{-13.2261} = 0.6173\,\text{V} \tag{2}$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} = 0.5739 + \frac{1.2 - 0.5739}{-13.2261} = 0.5266\,\text{V} \tag{3}$$

$$NM_H = V_{DD} - V_{IH} = 1.2 - 0.6173 = 0.5827\,\text{V} \tag{4}$$

$$NM_L = V_{IL} = 0.5266\,\text{V} \tag{5}$$

Figure 3 illustrates the noise margin, showing the relationship between the input and output voltages. V_{IL} acts as the upper bound of the noise margin low. If the input voltage is smaller than V_{IL}, the output logic will be recognized as high. V_{IH} sets the lower bound of the noise margin high. If the input voltage is larger than V_{IH}, the output logic will be recognized as low. However, if the input voltages lie between V_{IL} and V_{IH}, the output logic remains undefined.

3 Impact of Different PMOS-to-NMOS Width Ratios on CMOS Inverter Performance

In this section, we explore the impact of varying the PMOS-to-NMOS width ratios on the performance of a CMOS inverter. By adjusting the width of the PMOS transistor while keeping the NMOS width constant, we investigate how key

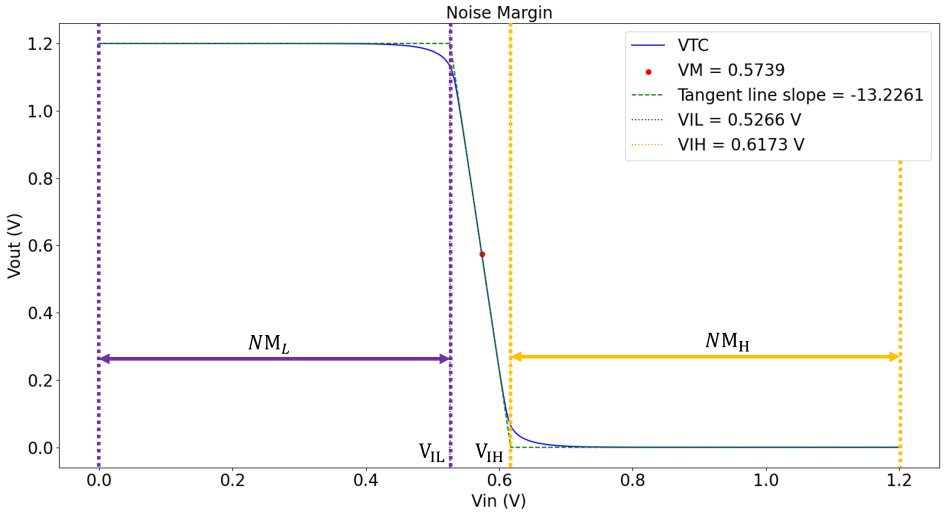

Fig. 3: Noise Margin for PMOS Width = 200nm and NMOS Width = 100nm

parameters such as the switching voltage (V_M), voltage gain (g), and noise margins (NM_L and NM_H) are affected.

3.1 Plot of Voltage Transfer Curves for Various PMOS Widths

To plot the Voltage Transfer Curves for various PMOS widths, we can use the same method described in Section 2.1 for one PMOS width. To perform a DC analysis with a different PMOS width, we modify the PMOS width in the netlist. For example, if we want to change the PMOS width to 100 nm and repeat the DC analysis, the following statement can be used:

```
.alter
X1 VIN VOUT VDD 0 INV WPI = 300n WNI = 100n
```

Figure 4 illustrates the voltage transfer curves (VTC) for different PMOS transistor widths, while the NMOS width is kept constant. From this figure, we can observe that the curves shift slightly to the left as the PMOS width decreases.

3.2 Data Analysis for Different PMOS Widths

Table 1 summarizes the switching voltage (V_M), voltage gain (g), V_{IL}, V_{IH}, and noise margins (NM_L and NM_H) for PMOS widths of 300 nm, 200 nm, and 100 nm.

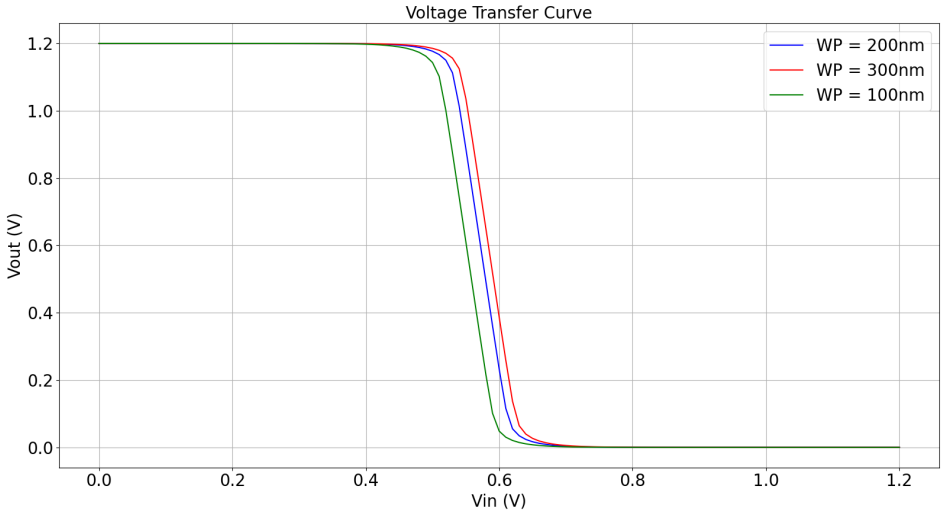

Fig. 4: Voltage Transfer Curves with Different PMOS width

From this table, we observe that key parameters, other than NM_H, increase with the PMOS-to-NMOS width ratio (PN ratio). Table 2 shows the region of unknown output logic, which remains largely unaffected by the PN ratio. Additionally, from Table 1, we see that the nNM_H is larger than the NM_L, indicating that the inverter is more prone to output high logic.

PMOS Width, nm	300	200	100
V_M, volts	0.5850	0.5739	0.5543
g	-13.1942	-13.2261	-13.2743
V_{IL}, volts	0.5384	0.5266	0.5057
V_{IH}, volts	0.6293	0.6173	0.5961
NM_L, volts	0.5384	0.5266	0.5057
NM_H, volts	0.5707	0.5827	0.6039

Table 1: Switching voltage, gain, V_{IL}, V_{IH} and noise margin of inverters with different width

PMOS Width, nm	300	200	100
V_{IH} - V_{IL}, volts	0.0909	0.9097	0.0904

Table 2: Difference between V_{IH} and V_{IL} indicating the region of unknown output logic for different PMOS widths

3.3 Comparison of Key Parameters for Different PMOS Width

In this section, we delve into key parameters such as the switching voltage (V_M), voltage gain (g), V_{IL}, V_{IH}, and noise margins (NM_L and NM_H) for varying

PMOS widths. We perform a sweep of the PMOS width from 50 nm to 600 nm while keeping the NMOS width constant, as shown in Figures 5, 6, 7, and 8. These figures analyze how these critical parameters change with the PMOS-to-NMOS width ratio.

From these figures, we observe that key parameters, except for NM_H, increase slightly as the PMOS-to-NMOS ratio increases, while NM_H decreases slightly as well. However, all of these parameters show weak dependence on transistor size, with smooth slopes. Table 3 summarizes the maximum and minimum values of each parameter, revealing that the maximum-to-minimum ratio for these parameters is close to 1, indicating that they are not highly sensitive to transistor sizing. This implies that manufacturing variations in transistor size have minimal impact on the inverter's performance.

	Max	Min	ratio (%)
V_M, volts	0.5328	0.6036	1.1329
$\|g\|$	13.1327	13.3165	1.0001
V_{IL}	0.4827	0.5582	1.1564
V_{IH}	0.5728	0.6496	1.1337
NM_L	0.4827	0.5582	1.1564
NM_H	0.5504	0.6272	1.1395

Table 3: Max Min Ratio of key parameters

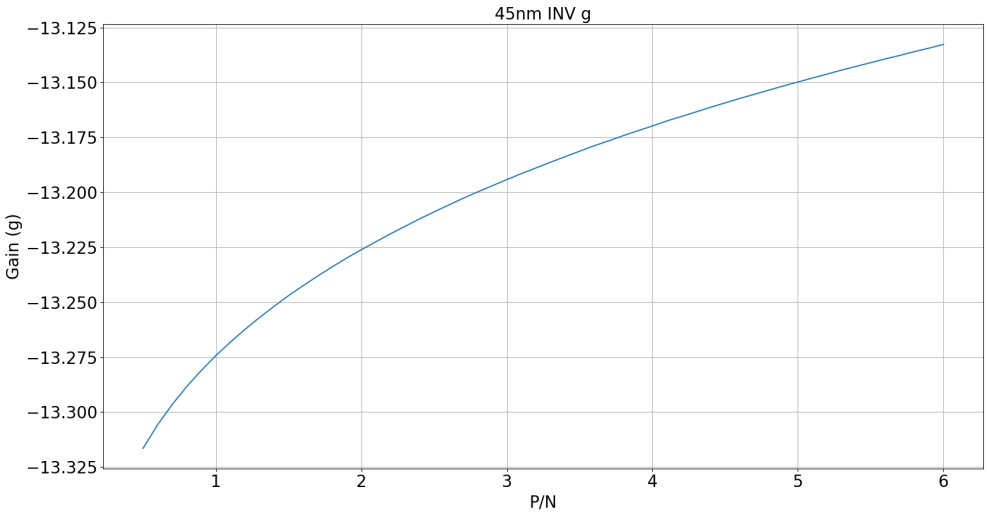

Fig. 5: gain vs PN ratio

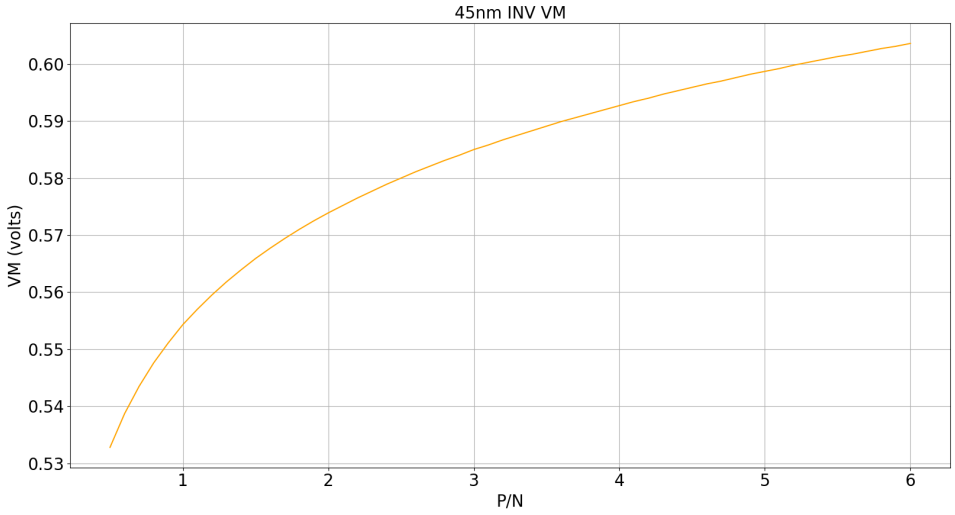

Fig. 6: V_M vs PN ratio

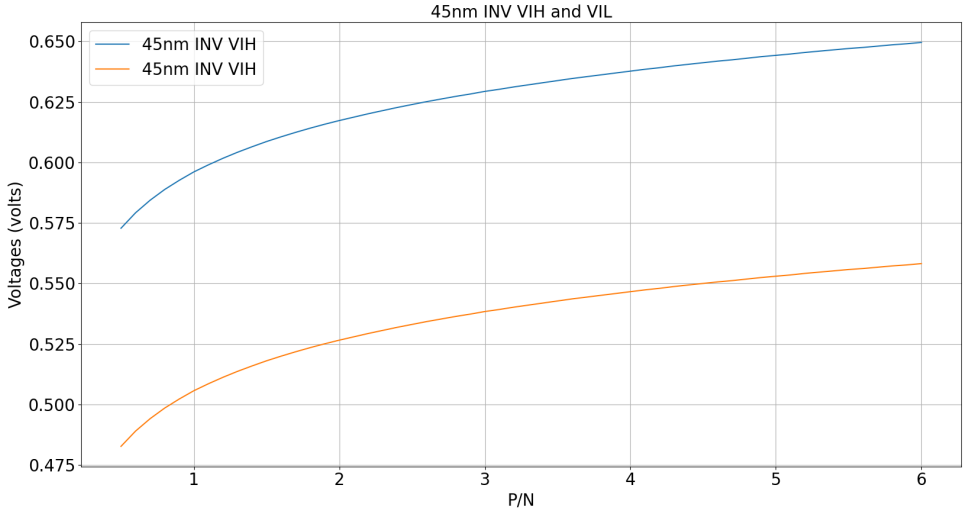

Fig. 7: V_{IH} and V_{IL} vs PN ratio

4 Impact of Different Supply Voltages (V_{DD}) on CMOS Inverter Performance

In this section, we explore the impact of varying the supply voltage (V_{DD}) on the performance of a CMOS inverter. By performing measurements at different V_{DD} values—$1.2V$, $0.9V$, $0.6V$, and $0.3V$—we analyze key DC characteristics such as the switching voltage (V_M), voltage gain (g), V_{IL}, V_{IH}, and noise margins (NM_L and NM_H). The analysis helps us understand how adjusting the supply voltage affects both power consumption and performance.

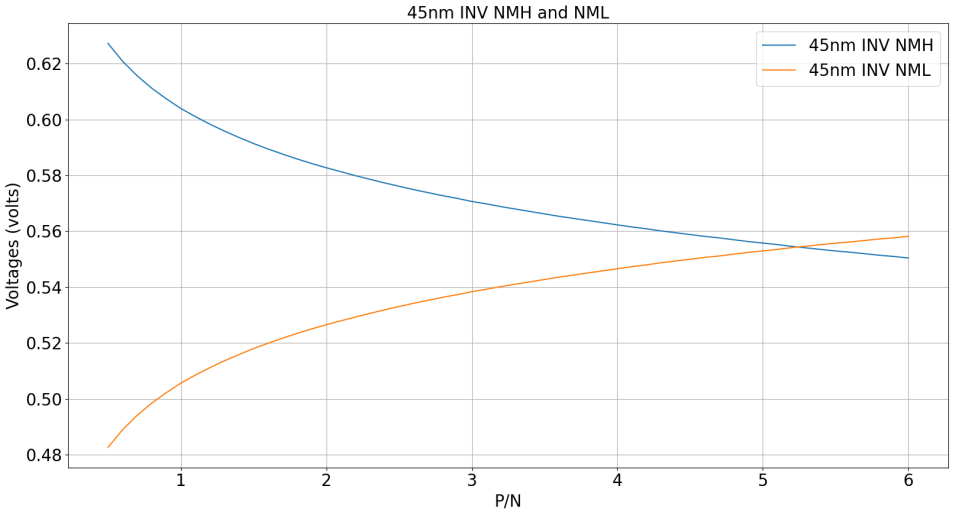

Fig. 8: NM_H and NM_L vs PN ratio

4.1 Voltage Transfer Curves and Key DC Characteristics for VDD = $1.2V$, $0.9V$, $0.6V$, and $0.3V$

Figure 9 shows the voltage transfer curves for different supply voltages (V_{DD}). To plot this figure, we use the same method described in Section 2.1. Table 4 summarizes the key parameters, including the switching voltage (V_M), voltage gain (g), V_{IL}, V_{IH}, and noise margins (NM_L and NM_H), for varying supply voltages (V_{DD}).

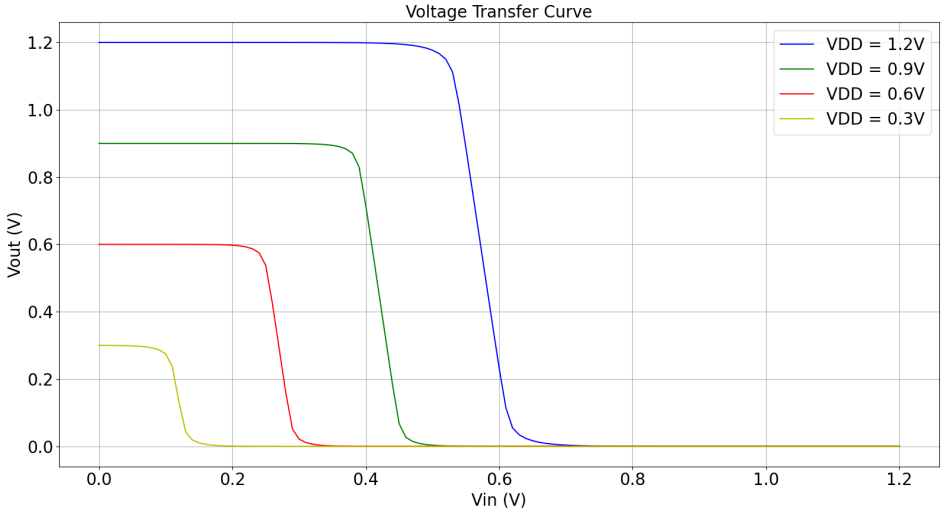

Fig. 9: Voltage Transfer Function with Different Supply Voltage

V_{DD}, volts	1.2	0.9	0.6	0.3
V_M, volts	0.5739	0.4221	0.2716	0.1208
g	-13.2261	-13.3632	-13.2939	-11.5097
V_{IL}, volts	0.5266	0.3863	0.2469	0.1052
V_{IH}, volts	0.6173	0.4537	0.2920	0.1313
NM_L, volts	0.5266	0.3863	0.2469	0.1052
NM_H, volts	0.5827	0.4463	0.3080	0.1687

Table 4: Switching voltage, gain, V_{IL}, V_{IH} and noise margin of inverters with different width

4.2 Observations

In order to better observe the voltage transfer curves (VTC) and key parameters, we normalize the values with respect to V_{DD}, as shown in Figure 10 and Table 4.

In Figure 10, we observe that the curve shifts to the left as V_{DD} decreases. The noise margin for $V_{DD} = 0.3V$ becomes significantly worse, while the other voltages show minimal differences. To analyze this further, we examine Table 5. It shows that V_M/V_{DD}, $|g|$, V_{IL}/V_{DD}, V_{IH}/V_{DD}, and NM_L/V_{DD} increase as the supply voltage increases, whereas NM_H/V_{DD} decreases.

Table 6 provides deeper insight into the noise margins for different V_{DD} values. The normalized output unknown region for $V_{DD} = 1.2V$, $0.9V$, and $0.6V$ are quite similar due to their close voltage gain values. However, for $V_{DD} = 0.3V$, the unknown region becomes larger due to its smaller voltage gain compared to the others.

Figures 11 and **??** provide an in-depth analysis of $|g|$ and V_M as V_{DD} varies. From the operational analysis of SPICE, we know that the threshold voltage for both NMOS and PMOS transistors is around 0.6V. When V_{DD} falls below 0.6V, both the PMOS and NMOS transistors in the inverter are no longer operating in the saturation region, resulting in a lower voltage gain and poorer noise margin performance, as seen for $V_{DD} = 0.3V$ in Figure 10. In Figure 12, we observe that V_M/V_{DD} remains almost constant when V_{DD} is above 0.6V, but it starts to decrease rapidly when V_{DD} falls below 0.6V. This behavior is similar to the reduction in voltage gain.

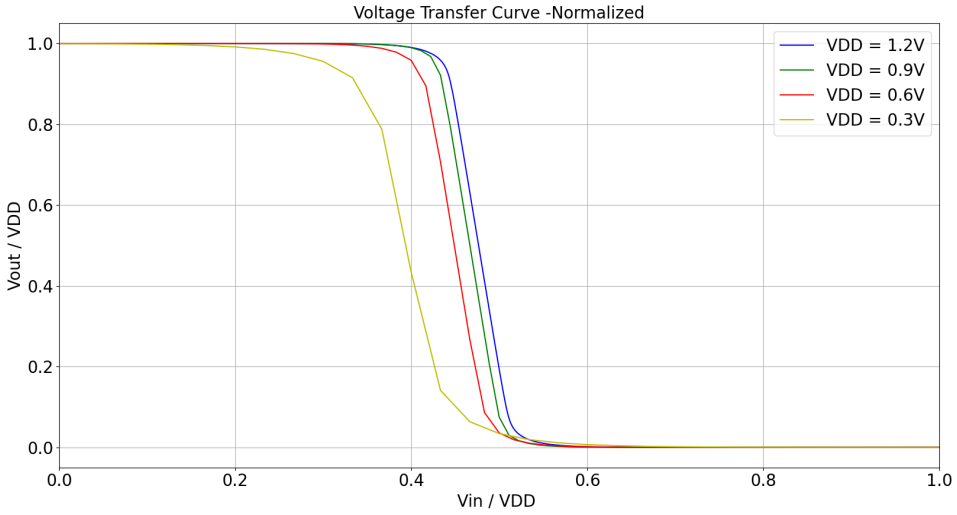

Fig. 10: Normalized Voltage Transfer Function with Different Supply Voltage

V_{DD}, volts	1.2	0.9	0.6	0.3
V_M, volts	0.4783	4690	0.4527	0.4027
$\|g\|$	13.2261	13.3632	13.2939	11.5097
V_{IL}, volts	0.4388	0.4292	0.4115	0.3507
V_{IH}, volts	0.5144	0.5041	0.4867	0.4377
NM_L, volts	0.4388	0.4292	0.4115	0.3507
NM_H, volts	0.4856	0.4959	0.5133	0.5683

Table 5: Switching voltage, gain, V_{IL}, V_{IH} and noise margin of inverters with different width-Normalized

5 Conclusion

In this analysis, we explored the behavior of a CMOS inverter under various PMOS-to-NMOS width ratios and different supply voltages (V_{DD}). We observed that key parameters such as switching voltage (V_M), voltage gain (g), and noise margins (NM_L and NM_H) are not highly sensitive to changes in transistor sizes. However, V_{DD} plays a significant role in inverter performance. As V_{DD} decreases, the noise margin and voltage gain deteriorate, particularly when V_{DD} falls below the threshold voltage of the NMOS and PMOS transistors. The inverter's ability to maintain strong logic levels is compromised at lower V_{DD} values, especially at $0.3V$, where both the voltage gain and noise margins are significantly reduced. Overall, the study provides valuable insights into the trade-offs between power consumption, performance, and robustness in CMOS inverter design.

V_{DD}, volts	1.2	0.9	0.6	0.3
$(V_{IH}$ - $V_{IL})/V_{DD}$, volts	0.7558	0.7489	0.7517	0.8700

Table 6: Normalized Difference between V_{IH} and V_{IL} indicating the region of unknown output logic for different supply Voltages

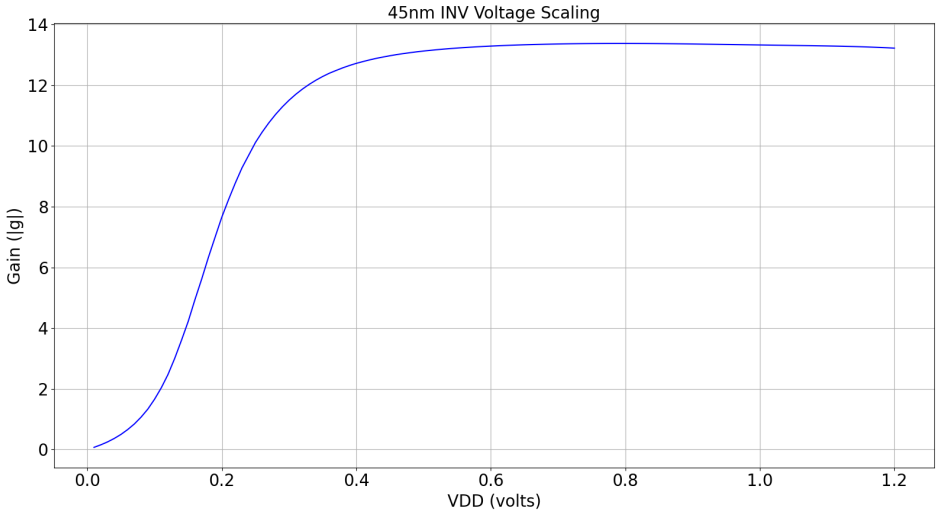

Fig. 11: $|g|$ vs. V_{DD}

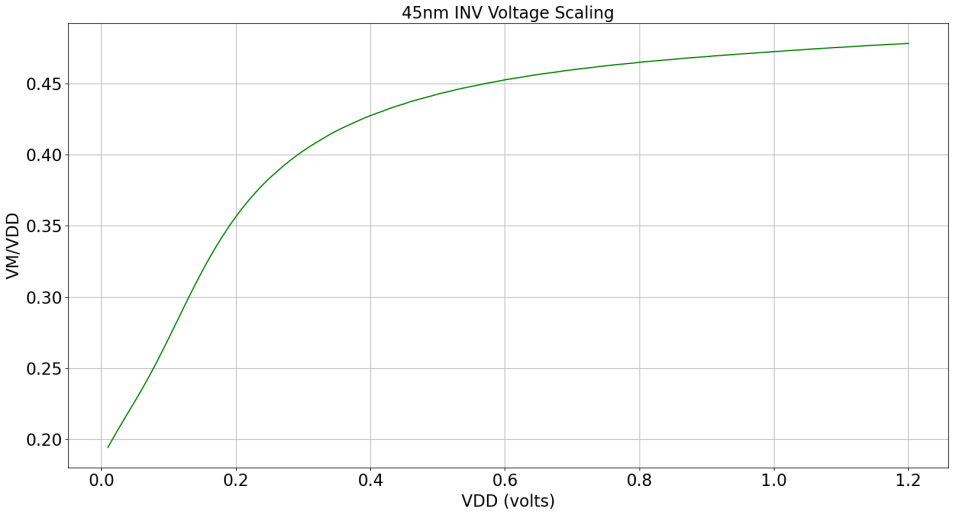

Fig. 12: V_M/V_{DD} vs. V_{DD}