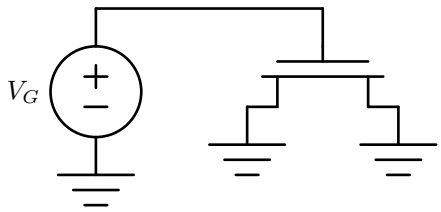
Digital Integrated Circuits

Homework 1. MOSFET Capacitance

Due: Sep. 18, 2024

A predictive SPICE model for 45nm technology is given in the file `asu_45nm`. Using the this model and an NMOS transistor with width of 100nm and length of 45nm, find the followings.

1. Bias the NMOS as shown in the figure below with bulk grounded, and vary V_G from 0 to 1.2V.



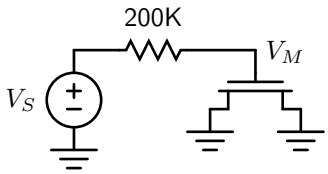
   1.1. Plot $|C_{gg}| = |C_{gs}| + |C_{gd}| + |C_{gb}|$, $|C_{gs}|$, $|C_{gd}|$, $|C_{gb}|$ versus V_G.

   1.2. Plot $|C_{bg}|$, $|C_{bd}|$, $|C_{bs}|$ versus V_G.

   1.3. Plot $|C_{dg}|$, $|C_{db}|$, $|C_{ds}|$ versus V_G.

   1.4. State your observations.

2. The NMOS transistor can be used as a MOS capacitor. Assuming it is connected as the circuit below. (NMOS bulk terminal is also grounded.)



   2.1. Plot NMOS $|C_{gg}|$ and Q_g from $V_S = 0$ to 1.2 Volts.

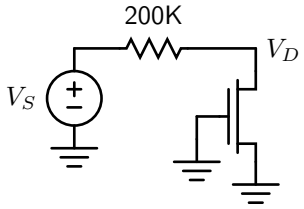
   2.2. If V_S varies between 0V and 1.2V and has the same rise and fall time of 1ps, pulse width of 999ps and period of 2ns, find the rise and fall delays for V_M.

   2.3. Using the large signal equivalent capacitance concept discussed in the class, find C_{eq} from the charges obtained in 2.1. (Voltage swing range is 0V to 1.2V.)

   2.4. Find the rise and fall delays if the NMOS is replaced by C_{eq}.

   2.5. Compare the rise, fall and the sum of rise and fall delays found in 2.2 and 2.4. What are your observations?

3. Connect the NMOS as the circuit below. The bulk is connected to ground.



3.1. The voltage source has the same waveform as specified in 2.2. Find the rise and fall delays for V_D.

3.2. Find the equivalent capacitance such that the sum of rise and fall delays equals to that found in 3.1.

3.3. State your observations.

Notes.

1. Please turn in your report in `pdf` format, and the SPICE input files.
2. For each question above, in addition to the resulting numbers or plots, you need to describe how do you do the simulations. The description should clear enough such that I can repeat the simulations to get the same results.
3. To use the SPICE model, simply include the model file in your SPICE file as following:

   ```
   .include "/home/course/ene5220/hw01/asu_45nm"
   ```

4. The NMOS model name is `nmos`. Thus, an NMOS can be defined as

   ```
   M1 VD VG VS VB NMOS W=100n L=45n AS=22.5f AD=22.5f PS=145n PD=145n
   ```

5. For question 1 you can use SPICE `.DC` analysis to find the capacitances. Since there is no need for capacitance in any DC analysis, you need to turn on the following option to force capacitance calculation:

   ```
   .option dccap=1 bypass=0
   ```

6. For questions 2 and 3, please use `.measure` statement to measure the delay times. A typical `.measure` statement is as following:

   ```
   .measure tran tdr trig v(vs) val=0.6 rise=1
   +                 targ v(vm) val=0.6 rise=1
   ```

7. Name you report `hw02a.pdf` and submit your report on EE workstation by following command:

   ```
   $ ~ene5220/bin/sbmtpdf hw01 hw01a.pdf
   $ ~ene5220/bin/sbmtspice hw01 q1.sp q2.sp q3.sp
   ```

   where `hw01` indicates homework 1.

8. Your report should be clearly written such that I can understand it. The writing, including English grammar, is part of the grading criteria.