Chapter 1

Walls and pitfalls

1.1 Introduction

1.2 Walls

HPC is facing several main problems to iterate to the next step and in general more performances. Those problems are called *walls* and can be grouped.

1.2.1 Memory Wall

THis problem is targeting for the first time in [WM95]. The author explains that:

> We all know that the rate of improvement in microprocessor speed exceeds the rate of improvement in DRAM memory speed, each is improving exponentially, but the exponent for microprocessors is substantially larger than that for DRAMs.

The new release of accelerators also have an impact on the memory wall, the memory of the host processors and devices accelerators cannot be accessed directly and copies from one to the other are requested.

1.2.2 Communication wall

The multiplicity of racks, nodes and

1.2.3 Power wall

The energy consumption of nowadays and future supercomputers is the main wall in HPC. Indeed, an exascale supercomputer could be construct using several petascale supercomputer but, with todays architectures, will require a nuclear plant to operate. In this objective low energy consumption architectures need to be find. Power wall can be of two kind: the energy to power the machine itself and the many nodes, processors and accelerators but also, and not the least, the energy requires to handle the heat generated by the machine. For the second part many new technologies arise with direct water cooling in the supercomputer racks.

1.2.4 Computational wall

The computational wall is a conjugation of all the wall cited before. By increasing the memory wall, the energy consumption and the communications we can increase the overall computation of the supercomputer.

1.3 Benchmark

1.3.1 Irregular behavior

1.3.2 Our choices

1.4 Conclusion

Bibliography

[WM95] Wm A Wulf and Sally A McKee. Hitting the memory wall: implications of the obvious. *ACM SIGARCH computer architecture news*, 23(1):20–24, 1995.