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Les Architectures Hybrides pour Atteindre l'Exascale

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Croyez ceux qui cherchent la vérité, doutez de ceux qui la trouvent; doutez de tout, mais ne doutez pas de vous-même.

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Introduction

In the aurora 2020-2021 for United States of America and Europe and maybe before, like 2019, for China, the world of High Performance Computing (HPC) will reach another milestone in the power of machines: the Exascale. These supercomputers will be 100 times faster than the estimated overfall operations performed by the human brain and its 10^{16} **F**loating point **O**perations **P**er **S**econd (FLOPS) [?, kurzweil2010singularity]nd achieve a computational power of a quintillion of (10^{18}) FLOPS. This odyssey started a long time ago with the first vacuum tubes computers and the need of ballistic computation for war. Nowadays the aim is very nearby and the power of a nation is represented by its army and money but also by the computational power of its supercomputers. HPC's applications also spread into all the area of science and technology.

Since 1962, considering the Cray CDC 6600 as the first supercomputer, the power of those machines have increased following an observation of the co-fonder of the Intel company, Gordon Moore. Better known under the name of "Moore's Law", it speculates in 1965 that: considering the constant evolution of technology the number of transistors on a dense integrated circuit will double approximately every two years. Thus, the computational power, that intrinsically depends on the number of transistors on the chip, will increase; more important, as "*money is the sinews of war*", the cost of the die for the same performances will decrease. This observation can be related to the supercomputers results through the years in the TOP500 list. As presented on figure 1, even if estimated in early 1965, the Moore's law seems to be accurate and sustainable.

This linear evolution is not only driven by the shrink in the semiconductor with smaller transistors. In fact the first one-core Central Processing Units (CPUs) were made using more transistors but also faster frequency. They later faced limitations to reach high frequencies, because of the power consumption and the inherent cooling of the heat generated by the chip. This is why, at some point in early twentieth century, IBM proposed the first multi-core processor on the same die, the Power4. The constructors started to create chips with more than one core to increase the computational power in conjunction with the shrink of semiconductors, answering the constant demand of more powerful devices and allowing the Moore's law to thrive. This increase of the overall power of the chip comes with some downside costs in synchronizations steps between the cores for memory access, work sharing and complexity. The general purpose CPU nowadays features from 2 to less than a hundred of cores on a single chip.

In order to reach even more computational power some researchers started to use many-core approaches. Using hundreds of cores these devices are using very "simple" computing units, with slow frequency and low power consumption but add more complexity and requirement for their efficient programming with even more synchronizations needed between the cores. Usually those many-core architectures are used coupled with a CPU that sends the data and drives them. Some accelerators like the Intel Xeon Phi can be driven or driver depending on their configuration. Usually called accelerators, those devices are used in addition to the host processor to provide their efficient computational power in the key part of execution. The most famous accelerators are the Xeon Phi, the General Purpose Graphics Processing Unit (GPGPU) initially used for graphic processing, Field Programmable Gates Array (FPGA) or dedicated Application-Specific Integrated Circuit (ASIC). The model using a host with additional device(s) appears and we will mention it as "Hybrid Architecture". In fact a cluster can be composed of CPUs, CPUs



Figure 1: Computational power evolution in the TOP500 list

with accelerator(s) of the same kind, CPUs with heterogeneous accelerators or even accelerators like Xeon Phi driving different kinds of accelerators.

Since 2013-2014 many companies, like the Gordon Moore's company *Intel* itself, stated that that the Moore's law is over. This can be seen on figure 1: on the right part of the graph, the evolution is not linear anymore and tends to decrease slowly in time. This can be imputed to two main factors: on one hand, we slowly reach the maximal shrink size of the transistors implying hard to handle side effects. On the other hand the power wall implied by the power consumption required by so many transistors and frequency speed on the chip.

Even with all these devices, nowadays supercomputers are facing several problems in their conception and utilization. The three main walls bounding the overall computational power of the machines are the power consumption wall, the communication wall and the memory wall. Some subproblems like the the interconnect wall, resilience wall or even the complexity wall also arise and make the task even harder.

In this context of doubts and questions about the future of HPC, this study propose several points of view. We think that the future of HPC is made with those hybrid architectures or acceleration devices adapted to the need, using well suited API, Framework and code. We consider that the classical benchmarks, like the TOP500, are not enough to target the main walls of those architectures and especially accelerators. Domain scientists applications like physcis/astrophysics/chemist/biologist require benchmarks based on more irregular cases with heavy computation, communications and memory accesses.

In this document we propose a metric that extracts the three main issues of HPC and apply them to accelerated architectures to figure out how to take advantage of those architectures and what the limitations are. The first step to this metrics is obtained when merging two characteristic problems and then a third one combining all our knowledge. The first two are targeting computation and communication wall over very irregular cases with high memory accesses, using an academic combinatorial problem and the Graph500 benchmark. The last is a computational scientific problem that covers both difficulties of the previous problems and appears to be hard to implement on supercomputers and even more on accelerated ones. The results obtain comfort our thesis and show hybrid architectures as the best solution to reach exascale.

This thesis is composed of three parts.

The first develop the state of the art in HPC from the main laws to the hardware. We go through the basic laws from Amdahl's to Gustafson's laws and the specification of speedup and efficiency. Classical CPUs, GPGPUs and other accelerators are described and discussed regarding the state of the art. The main methods of ranking and the issues regarding them are presented.

In the second part we propose our metric based on characteristic problems to target classical and hybrid architectures. The Langford problem is described as an irregular and computationally heavy problem. This shows how the accelerators, in this case GPUs, are able to support the memory and computation wall. This work leads to the publication of one journal paper [KLAJ16b] and many conferences/presentations/posters [DJK⁺14, LJAK16, JDK⁺14]. This allowed us to beat a world record with the last instances of this academic problem.

The Graph500 problem is then proposed as an irregular and communications heavy problem. We present our implementation, and more over the logic to take advantage of the GPUs computational power for characteristic applications. This work leads to the publication of a conference paper [KLAJ16a] and many presentations/posters [LAJK15, LJAK15].

In the third part we consider a problem that is heavy and irregular regarding computation and communications. We analyze it and show that it combines all the previous limitations.

Then we apply our methodology and show how nowadays supercomputers can overcome those issues. This computational science problem is based on the Smoothed Particle Hydrodynamics method. The former application we started with was developed on top of the FleCSI framework from the Los Alamos National Laboratory it allowed us to exchange directly with the LANL domain scientists on their need. Based on our global work to efficiently parallelize those kinds of production application, we intend to provide an efficient tool for physicists and astrophysicists called FleCSPH. This work leads to several presentation and posters [DBGH⁺16, LLMB17].

The last part will conclude on this work and results and show some of the main prospects of this study and my future researches.

Part I

HPC and Exascale

Introduction

This part of this thesis contains a state of the art presentation for theory and applications of High Performance Computing. It describes the tools we need for our study. High Performance Computing, HPC, does not have a strict definition. Its history starts with domain scientists in need of more complex and more reliable computation for models checking or simulations. They developed their own tools beginning with vacuum tubes computers which can be consider as a milestone in HPC history. Since this first machine the technology became more and more complex at every layer: the hardware conception, the software to handle it and even the models and topologies. HPC is now a scientific field on its own but always dedicated to the end purpose, domain scientist computations. HPC experts are interested in supercomputer construction, architecture and code optimization, interconnection behaviors and creating more software, framework or tools to facilitate access to these very complex machines.

In this part we give a non-exhaustive definition of HPC focusing on models, hardware and tools required for our study in three chapters.

We first focus on what are the theoretic models for the machines and the memory we base our work on. This first chapter also presents what is defined as performance for HPC and the main laws that define it.

The second chapter details the architecture base on these models. We present nowadays platforms with dominant constructors and architectures from multi-core to specific many-core machines. Representative members of today's supercomputers are described. We show that hybrid architectures seem to be the only plausible way to reach the exascale: they offer the best performance per watt ratio and nowadays API/tools allow to target them more easily and efficiently than ever.

In the third chapter we detail the main software to target those complex architectures. We present tools, frameworks and API for shared and distributed memory. We also introduce the main benchmarks used in the HPC world in order to rank the most powerful supercomputers. This chapter also shows that those benchmarks are not the best to give an accurate score or scale for "realistic" domain scientists' applications.

Chapter 1

Models for HPC

1.1 Introduction

High Performance Computing (HPC) takes its roots from the beginning of computer odyssey in the middle of 20th century. A lot of rules, observations and theories emerged from it and most of the Computer Science fields. In order to understand and characterize HPC and supercomputers, some knowledge on theory is required. This part describes the Von Neumann model, the generic model of sequential computer on which every nowadays machine is built. It is presented along with the Flynn taxonomy that is a classification of the different execution models. We also present the different memory models based on those elements.

Then we give more details on what parallelism is and how to reach performances though it. And thus we define what performance implies in HPC. The Amdahl's and Gustafson's laws are presented and detailed along with the strong and weak scaling used in our study.

1.2 Von Neumann Model

First computers, in early 20th century, were built using vacuum tubes making them high power consuming, hard to maintain and expensive to build. The most famous of first vacuum tubes supercomputers, the ENIAC, was based on a decimal system. It might be the most known of first supercomputers but the real revolution came from its successor. In 1944 the first binary system based computer was created, called the Electric Discrete Variable Automatic Computer (EDVAC). In the EDVAC team, a physicist described the logical model of this computer and provided a model on which every nowadays computing device is based.

John Von Neumann published its *First Draft of a Report on the EDVAC* [VN93] in 1945. Extracted from this work, the model is known as the Von Neumann model or more appears as generally Von Neumann Machine. The model is presented on figure 1.1.

On that figure we identify three parts: the input and output devices and, in the middle, the computational device itself.

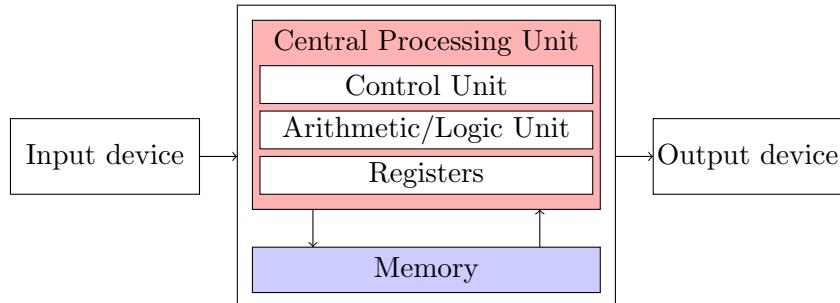


Figure 1.1: Von Neumann model

Input/Output devices The input and output devices are used to store data in a read/write way. They can be represented as hard drives, solid state drives, monitors, printers or even mouse and keyboard. The input and output devices can also be the same, reading and writing in the same area.

Memory Inside the computational device we have to mention the memory for data storage. For the most common nowadays architectures it can be considered as a Random Access Memory (RAM). Several kinds of memory exists and will be discussed later.

Central Processing Unit The Central Processing Unit, CPU, is composed of several elements in this model.

- On one hand, the *Arithmetic and Logic Unit*, ALU, which takes as input one or two values, the data, and applies an operation on them. The operation can be either logic with operations such as AND, OR, XOR, etc. or arithmetic with operations such as ADD, MUL, SUB, etc. Those operations may be more complex on modern CPUs.
- On the other hand, we find the *Control Unit*, CU, which controls the data carriage to the ALU from the memory and the operation to be performed on data. It is also the part that takes care of the Program Counter (PC): the address of the next instruction in the program.
- We can also identify the *Registers* section which represents data location used for both ALU and CU to store temporary results, the current instruction address, etc. Some representations may vary since the *Registers* can be represented directly inside the ALU or the CU.

Buses The links between those elements are called Buses and can be separated in data buses, control buses and addresses buses. These will have a huge importance for the first machines optimizations, growing the size of the buses from 2, 8, 16, 32, 64 and even more for vector machines with 128 and 256 bits.

The usual processing flow on such architectures can be summarized as a loop:

- Fetch instruction at current PC from memory;
- Decode instruction using the Instruction Set Architecture (ISA). The main ISA are Reduce Instruction Set Computer architecture (RISC) and Complex Instruction Set Computer architecture (CISC);
- Evaluate operand(s) address(es);
- Fetch operand(s) from memory;
- Execute operation(s).
- Store results, increase PC.

With some instructions sets and new architectures several similar operations can be processed in the same clock time. Every device or machine we describe in the next chapter has this architecture as a basis. One will consider execution models and architecture models to characterize HPC architectures.

1.3 Flynn taxonomy and execution models

The Von Neumann model gives us a generic idea of how a computational unit is fashioned. The constant demand in more powerful computers required the scientists to find more ways to provide this computational power. In 2001, IBM proposed the first multi-core processor on the same die: the Power4 with its 2 cores. This evolution required new paradigms. A right characterization

	Data Stream(s) →	
Instruction Stream(s) ↓	Single Data (SD)	Multiple Data (MD)
Single Instruction (SI)	SISD	SIMD <i>SIMT</i>
Multiple Instruction (MI)	MISD	MIMD <i>SPMD/MPMD</i>

Table 1.1: Flynn taxonomy for execution models completed with SPMD and SIMT models

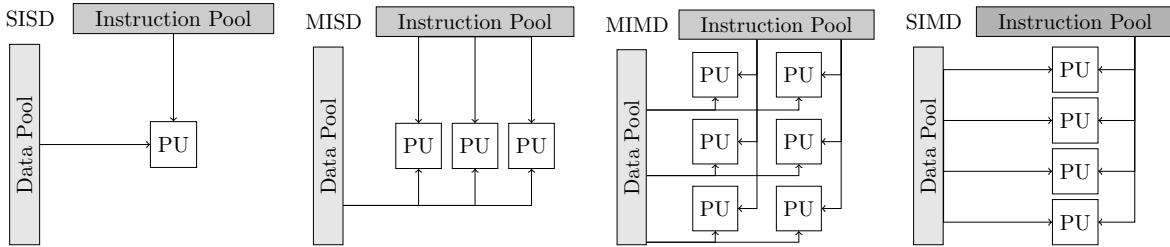


Figure 1.2: Flynn taxonomy schematic representation of execution models

is then essential to be able to target the right architecture for the right purpose. The Flynn taxonomy presents a hierarchical organization of computation machines and executions models.

In this classification [Fly72b] from 1972, Michael J. Flynn presents the SISD, MISD, MIMD, and SIMD models. Each of those execution models, presented on table 1.1 and figure 1.2, corresponds to a specific machine and function.

1.3.1 Single Instruction, Single Data: SISD

This is the model corresponding to a single core CPU like in the Von Neumann model. This sequential model takes one instruction, operates on one data and the result is then stored and the process continues over. SISD is important to consider for a reference computational time and will be taken into account in the next part for Amdahl's and Gustafson's laws.

1.3.2 Multiple Instructions, Single Data: MISD

This model can correspond to a pipelined computer. Different operations flows are applied to the datum, which is transferred to the next computational unit and so on. This is the least common execution model.

1.3.3 Multiple Instructions, Multiple Data: MIMD

In MIMD every element executes its own instructions flow on its own data set. This can represent the behavior of a processor using several cores, threads or even the different nodes of a supercomputer cluster. Two subcategories are identified in this model: SPMD and MPMD.

SPMD

The Single Program Multiple Data model, SPMD, is the most famous parallelism way for HPC purpose: each process executes the same program. The programs are the same but does not share the same instruction counter. This model was proposed for the first time in [DGNP88] in 1988 using Fortran. This is the common approach working with runtime like MPI. The programs

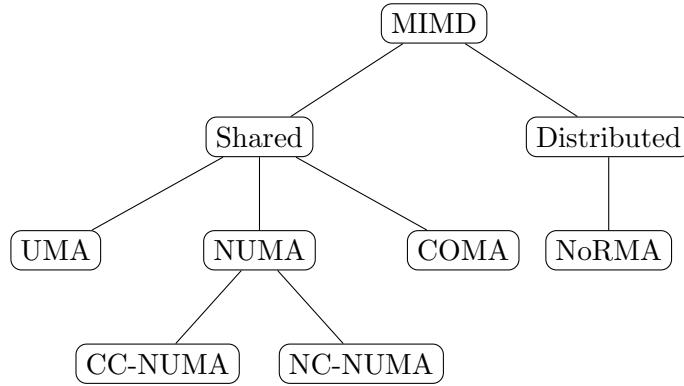


Figure 1.3: MIMD memory models

are the same and the executions are independent but based on their ID the processes will target different data.

MPMD

The Multiple Program Multiple Data model is also known for HPC: Some of the processes may execute programs for different purposes. Generally with a separation between a main program generating data for sub-programs. This is the model on which we work in part II, regarding the Langford problem resolution using a master program generating tasks for the slaves CPUs/GPGPUs programs.

1.3.4 Single Instruction, Multiple Data: SIMD

This execution model corresponds to many-core architectures like a GPU. SIMD can be extended from 2 to 16 elements for classical CPUs to hundreds and even thousands of core for GPGPUs. In the same clock cycle, the same operation is executed on every process on different data. A good example is the work on matrices with stencils: same instruction executed on every element of the matrix in a synchronous way: the processing elements share one instruction unit and program counter.

1.3.5 SIMT

We find another characterization to describe the new GPUs architecture: Single Instruction, Multiple Threads. This first appears in one of NVIDIA's company paper [LNOM08]. This model describes a combination of MIMD and SIMD architectures, every block of threads is working with the same control processor on different data and in such a way that every block has its own instruction counter. This is the model we describe in part 3.3.3, used for the *warps* model in NVIDIA CUDA.

1.4 Memory

In addition to the execution model and parallelism, the memory access patterns have a main role in performances in SIMD and MIMD. In this classification we identify three categories: UMA, NUMA and NoRMA for shared and distributed cases. This classification has been pointed out in the Johnson's taxonomy[Joh88].

Those different types of memory for SIMD/MIMD model are summarized in figure 1.3, and presented below.

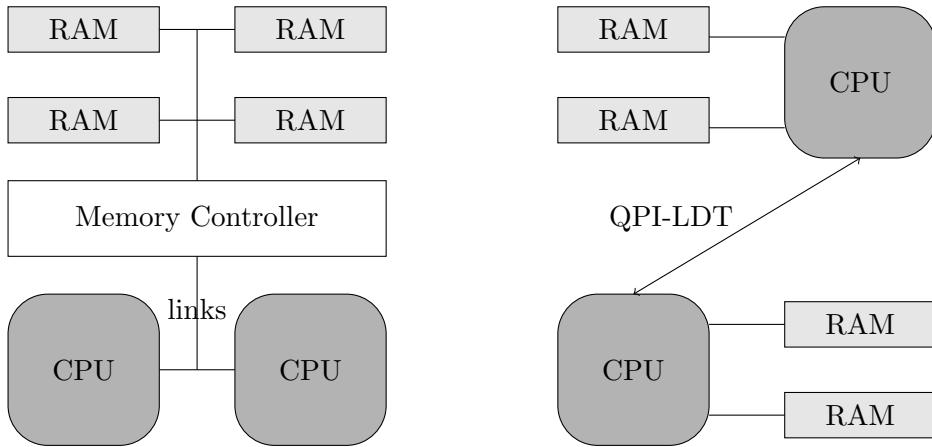


Figure 1.4: UMA vs NUMA memory models

1.4.1 Shared memory

Several kinds of memory models are possible when it comes to multi-threaded and multi-cores execution models like MIMD or SIMD models. We give a description of the most common shared memories architectures. Those shared memory models are the key stone for the next parts of our study. We find them in multi-core but also many-core architectures and the performances are completely dependent of their usage.

UMA

The Uniform Memory Access architecture have a global memory shared by every threads or cores. In UMA every processor uses its own cache as local private memory and the accesses consume the same amount of time: the addresses can be accessed directly by each processor which makes the access time ideal. The downside is that more processors require more buses and thus UMA is hardly scalable. The cache consistency problem also appears in this context and will be discussed in next part: indeed, if a data is loaded in one processor cache and modified, this information has to be spread to the memory and maybe other processes cache.

With the arising of accelerators like GPUs and their own memory, some constructors found ways to create UMA with heterogeneous memory: AMD created the heterogeneous UMA, hUMA [RF13] in 2013, allowing CPU and GPU to target the same memory area, but the performances still need to be checked in an HPC context.

NUMA

In Non Uniform Memory Access every processor has access to its own private memory but allows other processors to access it though Lightning Data Transport, LDT, or Quick Path Interconnect, QPI, for Intel architectures.

As mentioned for the UMA memory, even if the processors do not directly access to the memory cache, coherency is important. Two methods are possible: on one hand, the most used is Cache-Coherent NUMA (CC-NUMA) where protocols are used to keep data coherency through the memory. On the other hand No Cache NUMA (NC-NUMA) forces the processes to avoid cache utilization and write results to main memory, losing all the benefits of caching data.

COMA

In Cache-Only Memory Accesses, the whole memory is see as a cache shared by all the processes processes. An *Attraction memory* pattern is used to *attract* the data near the process that will

use them. This model is less commonly used and, in best cases, lead to same results as NUMA.

1.4.2 Distributed memory

The previous models are dedicated on shared memory, if the processes can access memory of their neighbors processes. In some cases, like supercomputers, it would be too heavy for processors to handle the requests of all the others through the network. Each process or node will then possess its own local memory, that can be shared only between local processes. Then, in order to access to other nodes memory, communications through the network have to be done and copied into local memory. This distributed memory model is called No Remote Memory Access (NoRMA). This requires transfer schemes, that have to be added to local read-write accesses.

1.5 Performances characterization in HPC

In the previous parts we described the different execution models and memory models for HPC. Based on those aspects we need to be able to emphasize the performances of a computer and a cluster.

The performance can be of several kinds. It can first be defined by the speed of the processors themselves with the frequency defined in GHz. We define the notion of *cycle* to be the number that determine the speed of a processor. This is the amount of time between two pulses of the oscillator at the best frequency. Higher cycles per seconds is better. It can be used to estimate the highest computational power of a machine. This information is not perfect because the ALU is not busy all the time due to memory accesses, communications or side effects. Then we have to go through more accurate ways to characterize performance.

1.5.1 FLOPS

The Floating point Operations Per Second value considers the number of floating-point operation that the system will execute in a second. Higher FLOPS is better and this is the most common scale used to consider supercomputers computational power. For a cluster we can compute the theoretical FLOPS (peak) based on the processor frequency in GHz with:

$$FLOPS_{cluster} = \#nodes \times \frac{\#sockets}{\#node} \times \frac{\#cores}{\#socket} \times \frac{\#GHz}{\#core} \times \frac{FLOPS}{cycle} \quad (1.1)$$

With $\#nodes$ the number of computational node of the system, $\frac{\#sockets}{\#node}$ the number of sockets (=processors) per node, $\frac{\#cores}{\#socket}$ the number of cores in the processor, $\frac{\#GHz}{\#core}$ the frequency of each core and finally $\frac{\#FLOP}{\#cycle}$ the number of floating-point operations per cycles for this architecture.

Table 1.2 presents the scale of FLOPS and the year of the first world machine reached this step. The next milestone, the exascale, is expected to be reached near 2020.

Even though, many ways exist to measure computer's performance: Instructions Per Seconds (IPS), Instructions per Cycle (IPC) or Operations Per Seconds (OPS) but none of these consider what an instruction or operation is. Thus, floating point can be considered as a basis, and a comparison can be provided.

1.5.2 Power consumption

Another way to consider machine performance is to estimate the number of operations regarding the power consumption. It considers all the previous metrics like FLOPS, IPS, IPC or OPS. Benchmarks like the Green500 consider the FLOPS delivered over the watts consumed. For nowadays architectures the many-cores accelerated architectures with GPUs seems to deliver the best FLOPS per watt ratio.

This subject is the underlying goal of our study. Without the power consumption limit we should just build supercomputer made of an addition of supercomputers. This is indeed not

Name	FLOPS	Year	Name	FLOPS	Year
kiloFLOPS	10^3		petaFLOPS	10^{15}	2005
megaFLOPS	10^6		exaFLOPS	10^{18}	2020 ?
gigaFLOPS	10^9	≈ 1980	zettaFLOPS	10^{21}	
teraFLOPS	10^{12}	1996	yottaFLOPS	10^{24}	

Table 1.2: Floating-point Operation per Second and years of reach in HPC.

doable due to processors power consumption and cooling cost. This question have been studied in our laboratory with the development of tools like *Powmon* (Power Monitor). It allows to instantaneously query the power consumption with CPU and GPU on a running node of a cluster.

1.5.3 Scalability

After considering architectures evaluation, one have to measure the applications performances. The scalability expresses the way a program reacts to parallelism. When an algorithm is implemented on a serial machine and is ideal to solve a problem, one may consider to use it on more than one core, socket, node or even cluster. Indeed, while using more resources one may expect less computation time or access larger instances, or a combination of both. This is completely dependent of the algorithm's parallelization and is expressed through scalability. A scalable program will scale on as many processors as provided, whereas a poorly scalable one will give same of even worst results than the serial code. Scalability can be approached using speedup and efficiency.

1.5.4 Speedup and efficiency

The latency is the time required to complete a task in a program. Lower latency is better.

The speedup compares the latency of both sequential and parallel algorithm. In order to get relevant results, one may consider the given best serial program against the best parallel implementation.

Considering n , the number of processes, and $n = 1$ the sequential case. T_n is the execution time working on n processes and T_1 the sequential execution time. The speedup can be defined using the latency by the formula:

$$\text{speedup} = S_n = \frac{T_1}{T_n} \quad (1.2)$$

In addition to speedup, the efficiency is defined by the speedup divided by the number of workers:

$$\text{efficiency} = E_n = \frac{S_n}{n} = \frac{T_1}{nT_n} \quad (1.3)$$

The efficiency, usually expressed in percent, represents the evolution of the code stability to growing number of processors. As the number of processes grows, a scalable application will keep an efficiency near 100%.

As shown on figure 1.5 several kinds of speedup can be observed.

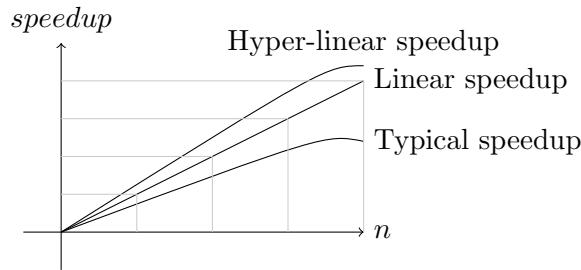


Figure 1.5: Observed speedup: linear, typical and hyper-linear speedups

Linear, reference speedup: The linear speedup usually represents the target for every program in HPC. Indeed, having a constant efficiency, which means that the speedup grows linearly as the number of processors grows is the ideal case. Codes fall typical into two cases, typical and hyper-linear speedup.

Typical speedup: This represents the most common observed speedup. As the number of processors grows, the program faces several of the HPC walls like communications wall or memory wall. The increasing number of computational power may be lost in parallel overhead, and efficiency reduced.

Hyper-linear speedup: In some cases we observe an hyper-linear speedup, meaning that the results in parallel are even better than the ideal case. This increasing efficiency can occur if the program fits exactly in memory for less data on each processor or even fit perfectly for the cache utilization. The parallel algorithm can also be more efficient than the sequential one, for example with optimizations application: if the search space is divided over processing units, one can find good solutions more quickly.

1.5.5 Amdahl's and Gustafson's law

The Amdahl's and Gustafson's laws are ways to evaluate the maximal possible speedup for an application taking into account different characteristics.

Amdahl's law

The Amdahl's law[Amd67] is used to find the theoretical speedup in latency of a program. We can separate a program into two parts, the one that can be executed in parallel with optimal speedup and the one that is intrinsically sequential. The law states that even if we reduce the parallel part using an infinity of processes the sequential part will reach 100% of the total computation time.

Extracted from the Amdahl paper the law can be written as:

$$S_n = \frac{1}{Seq + \frac{Par}{n}} \quad (1.4)$$

Where Seq and Par respectively the sequential and parallel ratio of a program ($Seq + Par = 1$). Here if we use up to $n = \inf$ processes, $S_n \leq \frac{1}{Seq}$ the sequential part of the code become the most time consuming.

And the efficiency become:

$$E_n = \frac{1}{n \times Seq + Par} \quad (1.5)$$

A representation of Amdahl's speedup is presented on Fig. 1.6 with varying percentage of serial part.

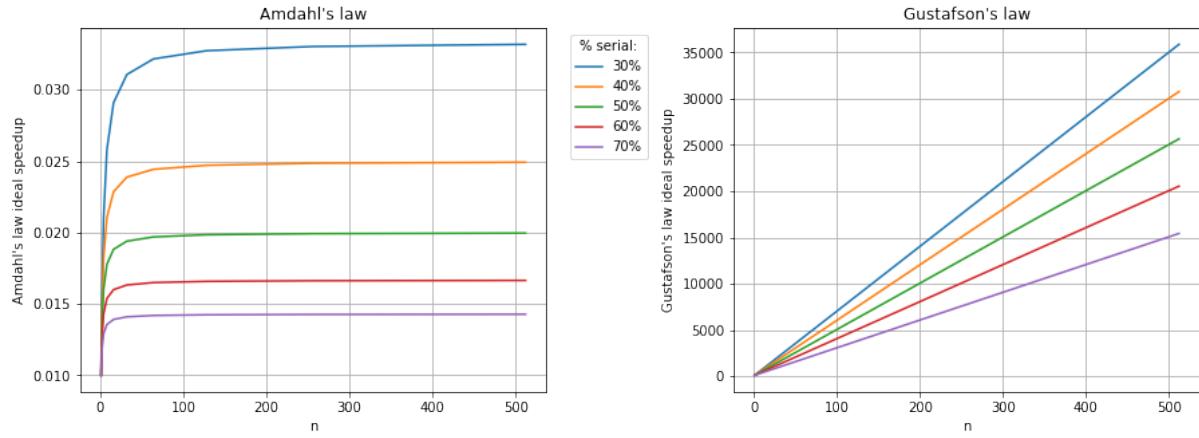


Figure 1.6: Theoretical speedup for Amdahl's (left) and Gustafson's (right) law

Gustafson's law

The Amdahl's law focuses on time with problem of the same size. John L. Gustafson's idea is that using more computational units and the same amount of time, the problem size can grow accordingly. He considered a constant computation time with evolving problem, growing the size accordingly to the number of processes. Indeed the parallel part grows as the problem size does, reducing the percentage of the serial part for the overall resolution.

The speedup can now be estimated by:

$$S_n = Seq + Par \times n \quad (1.6)$$

And the efficiency:

$$E_n = \frac{Seq}{n} + Par \quad (1.7)$$

Both Amdahl's and Gustafson's law are applicable and they represent two solutions to check the speedup of our applications. **The strong scaling**, looking at how the computation time vary evolving only the number of processes, not the problem size. **The weak scaling**, at the opposite to strong scaling, regards to how the computation time evolves varying the problem size but keeping the same amount of work per processes.

1.6 Conclusions

In this chapter we presented the different basic considerations to be able to understand HPC: the Von Neumann model that is implemented in every nowadays architecture; the Flynn taxonomy that is in constant evolution with new paradigms like recent SIMT from NVIDIA. We also presented the memory types that will be used at different layers in our clusters, from node memory, CPU-GPGPU shared memory space to global fast shared memory. We finished by presenting the most important laws with Amdahl's and Gustafson's laws. We introduced the concept of strong and weak scaling that will lead our tests through all the examples in Part II and Part III.

Those models have now to be confronted to the reality with hardware implementation and market reality, the vendors. The next chapter introduces chronologically hardware enhancements and their optimization and always keeps a link with the models presented in this part.

As there is always a gap between models and implementation we will have to find ways to rank and characterize those architectures. This will be discussed in the last chapter.

Chapter 2

Hardware in HPC

2.1 Introduction

Although parallel models address most of the key points to discuss application performance it also depends on architectures hardware, which may influence the way to consider problems resolution. Thus the knowledge of hardware architecture is essential to reach performances through optimizations. Even if the nowadays software, API, framework or runtime already handle most of the optimizations, the last percents of gain are architecture's dependent. In this chapter we describe the most important devices architectures from classical processors, General Purpose Graphics Processing Units (GPGPUs), Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). This study keeps a focus on multi-core processors and GPUs as we based our tests on those devices.

This chapter also details the architecture of some remarkable supercomputers. This has to go with the description of interconnection network for the most used interconnection topologies.

We choose to present the architectures in a chronological order following the models presented in the previous chapter - SISD, MIMD and SIMD/SIMT - and presenting the last released technologies. We also present the optimizations of current technologies with the arising of parallelism and new types of memories.

2.2 Early improvements of Von Neumann machine

In this section we present the different hardware evolution from 1970s single core processors to nowadays multi-core and many-core architectures that are the milestones, the basic units, to build supercomputers. We can see the most important optimizations that are always implemented in the most recent machines: in/out of order processors, pre-fetching strategies, vectorization and the memory technologies breakthroughs.

2.2.1 Single core processors

The first processors, around the 1970s, were built using a single computation core as described in the Von Neumann model. Many evolutions were made on those single core processors for the memory, the order of the instructions and the frequency increase.

Transistor shrink and frequency

A lot of new ways to produce smaller transistors have been discovered. Their size was about $10\mu m$ in 1971 and reach $10nm$ in nowadays machines. This allowed the constructors to add more transistors on the same die and build more complex ISA and features for the CPUs.

In parallel of the shrink of transistors, the main feature for better performances with the single core architectures came from the frequency augmentation, the clock rate. Indeed, as the clock rate get higher, more operations can be performed on the core in the same amount of

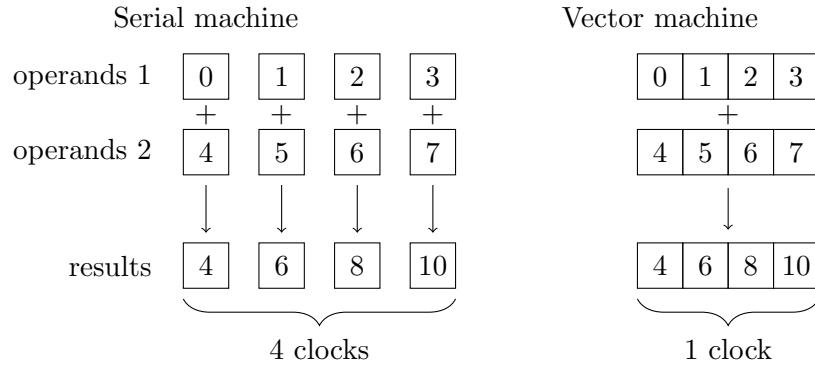


Figure 2.1: Vectorized processeur example on 4 integer addition: 128 bits wide bus

time. In 1970s the frequency was about 4 MHz allowing a maximum of 4 millions of cycles per seconds. Nowadays single cores can work at a frequency of 4GHz and even 5GHz performing billions of operations per cycles, but the next sections will show that due to power consumption and coding considerations, frequency is no more used to improve performances.

In/Out-Of-Order execution

In-order-process is the one described in previous chapter. The control unit fetches instructions and the operands from memory. Then the ALU computes the operation, and finally the result is stored to memory.

In this model the time to perform an instruction is the cumulation of: instruction fetching + operand(s) fetching + *computation* + result storage. This time may be high regarding the use of the ALU for *computation*, technically just one clock cycle. The idea of *out-of-order* execution is to compute the instructions without following the Program Counter order. Indeed, for independent tasks (pointed out with dependency graphs) while the process fetches the next instruction data, the ALU can perform another operation with already available operands. This leads to better usage of computational resources in the CPU and thus better overall performances.

Vectorization

Vector processors allow the instructions to be executed at the same time in a SIMD manner. If the same instruction is executed on coalescent data they can be executed in the same clock cycle. As an example we can execute operations simultaneously on 4 to 8 floats with a bus size of 128 or 256 bits. This requires specific care for coding with *unrolling* and *loop tiling* that will be addressed later in this study, and to avoid bad behavior leading to bad performances. But latest architectures vectorization imposes to slightly lower the frequency of processors.

The Cray-1 supercomputer[Rus78], installed in 1975 in the Los Alamos National Laboratory, is a perfect example of vector processor supercomputer. This supercomputer was designed by Seymour Cray, the founder of Cray Research. Based on vector processor it was able to deliver up to 160 MFLOPS. It was the fastest supercomputer in 1978 and due to its shape and price it was humorously called *the world's most expansive love-seat*.

The behavior of vector machine is presented on figure 2.1 for a 16 bytes vector machine (4 integer of 4 bytes = 128 bits bus). We see on the left that performing the 4 operations requests 4 cycle and, at the opposite, 1 cycle on the right with the vectorized machine.

Linked with the CPU optimizations, the memory optimizations also have to be considered. Indeed, even if the ALU can perform billions of operations per second it needs to be fed with data by fast transfers.

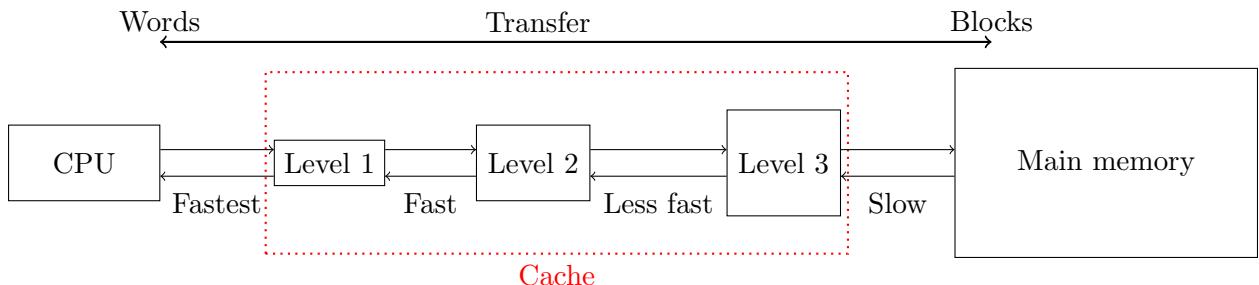


Figure 2.2: Cache memory technology on three levels L1, L2 and L3

Memory technology evolution

The memories technologies optimizations address several aspects. The early 1980s saw the augmentation of bus size from 4 bits to nowadays 32 bits for single precision and 64 bits for double precision. 128 bits or 256 bits buses can also be used to allow vectorization presented just before.

Different kind of technologies are considered: the SRAM and DRAM.

SRAM: The Static Random Access Memory is built using so called "flip-flop" circuits that can store data at anytime time with no time lost in "refresh operations". This kind of memory is very expensive to produce due to the number of transistors by memory cell. Therefore it is usually limited for small amounts of storage. The SRAM is mainly used for cache memory.

DRAM: The Dynamic Random Access Memory is based on transistors and capacitors to store binary information. This memory is less expensive to produce but needs to be refreshed at a determined frequency otherwise the data are lost. This refresh step is in fact a read-write operation on the whole memory at a specific frequency. There are several sub categories of DRAM used in different device depending on the way the bus are used with Single Data Rate (SDR), Double Data Rate (DDR) and Quad Data Rates (QDR). The number of data carried can vary from 1x to 4x but the limitation of those products is the price, constantly rising.

Cache memory:

Cache is a memory mechanism that is useful to consider when targeting performance. The main idea of cache technology is presented on figure 2.2. This memory is built hierarchically over several levels. The closer to the CPU is L1, then L2 and generally no more than L3 except on specific architectures. When looking for a data the CPU first checks if it is present in the L1 cache, otherwise L2 and L3 to get the data to higher level. From the main memory to the L3 cache *blocks* are exchanged, by chunks. With levels L2 and L1, lines of informations are exchanged usually called *words*. This is based on the idea that if a data is used, it shall be used again in the near future. Many cache architectures exist: direct, associative, fully associative, etc. Cache-hits occur when the data required is present in cache, and cache-miss when it has to be retrieved from lower levels or main memory. In a program the ratio of cache-miss has to be kept low in order to reach performance, and the impact may be very high.

Pre-fetching

Pre-fectching was developed Based on memory optimization and especially the cache. When a data is not available in L1 cache, it has to be moved from either L2 to L1 or L3 to L2 to L1 or in the worst case from RAM to L3 to L2 to L1. Pre-fectching technology is a way to, knowing the next instructions operands, pre-fetch the data in closer cache before the instruction is decoded.

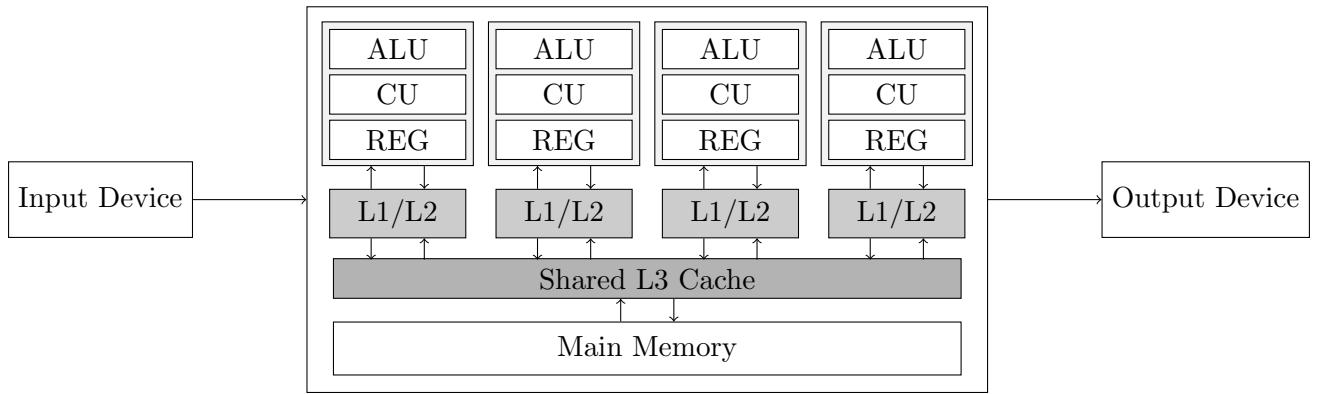


Figure 2.3: Multi-core CPU with 4 cores based on Von Neumann Model

The pre-fetch can either be hardware or software implemented and can concern data and even instructions.

2.2.2 Multi-CPU servers and multi-core processors

Around the beginning of 2000s the limitations of single core processors were too important. The frequency was already high and requested more power consumption and caused more heat dissipation. The first idea was to provide multi-CPU devices, embedding several CPU on the same motherboard and allowing them to share memory. The evolution of that is multi-core, having several processing units on the same die allowed more optimization inside the die and combining all the advantages of single core processors. But CPUs each embedding the function and units required consume n times more energy and cumulate heat effects. Thus, unable to answer the constant augmentation of computational power needed for research and HPC, IBM was the first company to create a multi-core CPU in 2001, the Power4.

Compared to the core inside multi-CPU, multi-core CPU shared one of the material (L3 caches, buses, ...) and are implemented on the same die; this allows to reach the same CPU performances with less transistors and less power consumption, avoiding most of the heat issues.

This architecture is presented on figure 2.3. The main memory is now shared between the cores. The registers and L1/L2 cache are the same but a L3 layer is added to the cache, and consistency has to be maintained over all the cores: if a process modifies a data in the memory this information has to be spread over all the other users of this data, even in their local cache.

We note here that in nowadays language the CPU, as describe in the Von Neumann model, is also the name of the die containing several cores. This is the architecture of most of nowadays processors. These multi-cores provide 2 to 32 cores in most cases. Thus the multi-core CPU are called "Host" and the attached accelerators are called "Devices".

2.3 21th century architectures

After years of development and research on hardware for Computer Science and specifically HPC, we present here the latest and best technologies to product efficient and general purpose supercomputers.

We present the latest architectures with multi-core, many-core and specific processors, and the most famous vendors.

2.3.1 Multi-core implementations

The most world spread architecture in public and hight performance computing is the multi-core processors. Most of nowadays accelerators require a classical processor to offload tasks and data

The Tick-Tock model through the years

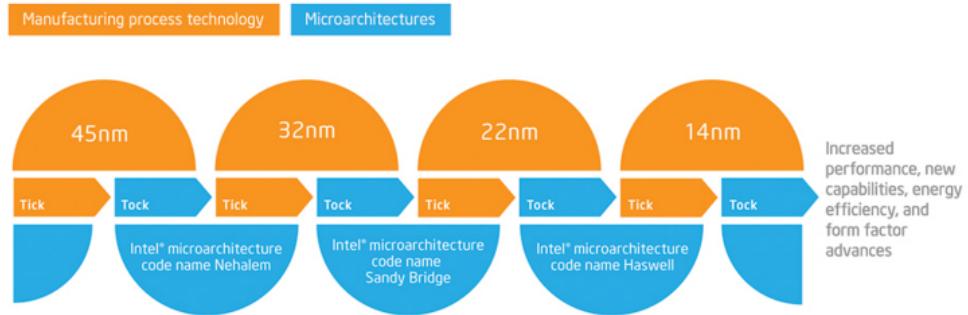


Figure 2.4: Intel Tick-Tock model

on it.

We start this presentation from the most popular processors in HPC world, the Intel company ones. We also present ARM which is another multi-core architecture based on RISC instructions set.

Intel

Intel was created in 1968 by a chemist and a physicist, Gordon E. Moore and Robert Noyce, in Mountain View, California. Nowadays processors are mostly Intel ones, this world leader equips around 90% of the supercomputers (November 2017 TOP500 list).

In 2007 Intel adopted a production model called the "Tick Tock", presented on figure 2.4. Since its creation this model followed the same fashion: a new manufacturing technology like shrink of the chip with better engraving on a "Tick" followed by a "Tock" by the delivery of a new micro-architecture. The Intel processors for HPC are called Xeon and feature ECC memory, higher number of cores, large RAM support, large cache-memory, Hyper-threading, etc. Compared to desktop processors, their performances are of a different magnitude. Every new processor has a code name. The last generations are chronologically called Westemere (2011), Sandy Bridge (2012), Ivy Bridge(2013), Haswell (2014), Broadwell (2015), Skylake (2015) and Kaby lake (2016).

Kaby Lake, the last architecture provided, does not exactly fit the usual "Tick-Tock" process because it is just based on optimizations of the Skylake architecture. It is produced like Skylake in 14nm. The tick-tock model seems to be hard to maintain due to the difficulties to engrave in less than 10nm with quantum tunneling. This leads to using larger many-cores architecture and base next supercomputer evolutions road-map on hybrid models.

Hyper-threading Another specificity of Intel Xeon processors is Hyper-threading (HT). This technology makes a single physical processing unit (core) appearing as two logical ones for user's level. In fact a processor embedding 8 cores appears as a 16 cores for user. Adding more computation per node can technically allow the cores to switch context when data are fetched from the memory using the processor 100% during all the computation. A lot of studies have been released on HT from Intel itself [Mar02] to other studies [BBDD06, LAH⁺02]. This optimization does not fit to all the cases of applications and can be disabled for normal use of the processors in the context of general purpose HPC architectures.

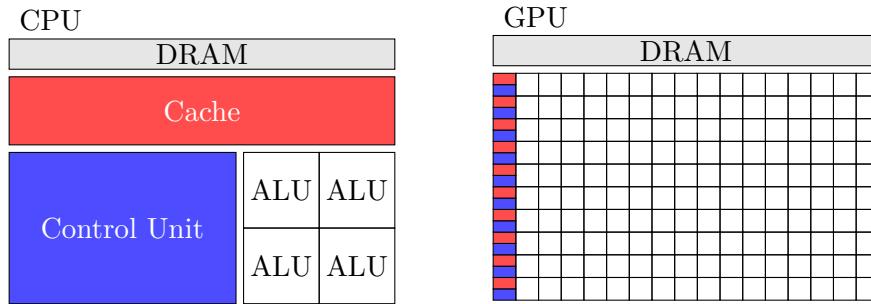


Figure 2.5: Multi-core versus Many-core architecture, case of GPUs

ARM

Back in 1980s, ARM stood for Acorn RISC Machine in reference to the first company implementing this kind of architecture, Acorn Computers. This company later changed the name to Advanced RISC Machine (ARM). ARM is a specific kind of processors based on RISC architecture as its ISA, despite usual processors using CISC. The downside of CISC machines makes them hard to create and they require way more transistor and thus energy to work. The ISA from the RISC is simpler and requires many transistors to operate and thus a smaller silicon area on the die. Therefore, the energy required and the heat dissipated is less important. It would then be easier to create massively parallel processors based on ARM. On the other hand, simple ISA imposes more work on the source code compilation to fit the simple architecture. That makes the instructions sources longer and therefore more single instructions to execute.

The ARM company provides several versions of ARM processors named Cortex-A7X (2015), Cortex-A5X (2014) and Cortex-A3X (2015), respectively featured for highest-performances, for balancing performances and efficiency or for less power consumption.

The new ARMv8 architecture starts to provide the tools to target HPC context [RJAJVH17]. The European approach towards energy efficient HPC, Mont-Blanc project¹, already constructs ARM based supercomputers. For the exascale project in Horizon 2020 this project focuses on using ARM-based systems for HPC with many famous contributors with Atos/Bull as a project coordinator, ARM, French Alternative Energies and Atomic Energy Commission (CEA), Barcelona Supercomputing Center (BSC), etc. The project is decomposed into several steps to finally reach exascale near 2020. The third step, Mont-Blanc 3, is about to work on a pre-exascale prototype powered by Cavium's ThunderX2 ARM chip based on 64-bits ARMv8.

2.3.2 Many-core architecture, SIMT execution model

Several architectures can be defined as many-cores. Those devices integrate thousands of cores that are usually controlled by less control units. We can consider those cores as "simpler" since they have to work synchronously and under the coordination of a control unit. They are based on SIMD Flynn taxonomy. Some devices are specific like the Xeon Phi of Intel integrating a hundred of regular processor cores which can work independently.

GPU

When a CPU can usually have 2 to 32 computation cores that can operate on different instruction streams, the SIMT architecture of the GPU is slightly different. The cores are grouped and have to share the same instruction at the same clock time but all the groups can have their own instruction.

¹<http://montblanc-project.eu/>



Figure 2.6: NVIDIA Tesla Kepler architecture. Single-precision in green and double-precision in yellow

Figure 2.5 present the vision between CPU and GPU processors. We see on that figure the usual topology with the ALU lined up in front of their control unit and shared cache memory. Every ALU also have its own memory and registers to operate local computations.

Those devices are called General Purpose Graphics Processing Units (GPGPUs). They are derivative from classical GPUs used for graphics purpose. Pioneer shows that they can be use efficiently for classical scientific computations. The vendor provides then specific GPU for general purpose computing. We present here the two main companies providing GPGPUs for HPC world: NVIDIA and AMD.

NVIDIA GPU architecture The NVIDIA company was founded in April 1993 in Santa Clara, Carolina, by three persons in which Jensen Huang, the actual CEO. The company name seems to come from *invidia* the Latin word for Envy and vision for graphics rendering.

Known as the pioneer in graphics, cryptocurrency, portable devices and now Artificial Intelligence (IA), it seems to be even the creator of the name "GPU". NVIDIA's GPUs, inspired from visualization and gaming at a first glance, are available as a dedicated device for HPC purpose since the company released the brand named *Tesla*. The public GPUs can also be use for dedicated computation but does not feature ECC memory, double precision or special functions/FFT cores. The different versions of the architecture are named following famous physicists, chronologically: Tesla, Fermi, Kepler, Maxwell, Pascal and Volta.

We describe here the Kepler brand GPU and more specifically the K20Xm GPU on which we based our study. This NVIDIA Tesla Kepler GPU is based on the GK110 graphics processor describes in the white-paper[Nvi12] on 28nm process. The figure 2.6 is a representation of the physical elements of this graphics processor. The K20X comes in active and passive cooling mode with respectively K20Xc and K20Xm. This GPU embeds 2688 CUDA cores distributed in 14 SMX (we note that GK110 normally provides 15 SMX but only 14 are present on the K20X). In this model each SMX contains 192 single precisions cores, 64 double precision cores, 32 special function units and 32 load/store units. In a SMX the memory provides 65536 32-bits registers, 64KB of shared memory L1 cache, 48KB of read-only cache The L2 cache is 1546KB shared

by the SMX for a total of 6GB of memory adding the DRAM. The whole memory is protected using Single-Error Correct Double-Error Detect (SECDED) ECC code. The power consumption is estimated to 225W. This GPGPU is expected to produce 1.31 TFLOPS for double-precision and 3.95 TFLOPS of single-precision.

AMD Another company is providing GPUs for HPC, Advanced Micro Devices (AMD). In front of the huge success of NVIDIA GPU that leads from far the HPC market, it is hard for AMD to find a place for its GPGPUs in HPC. Their HPC GPUs are called FirePro. They are targeted using a language near CUDA but not hold by a single company called OpenCL. An interesting creation of AMD is the Accelerated Processing Units (APUs) which embedded the processor and the GPU on the same die since 2011. This solution allows them to target the same memory.

In the race to market and performances, AMD found a accord with Intel to provide dies featuring Intel processor, AMD GPU and common HBM memory. The project is call Kaby Lake-G and announce for first semester of 2018 but for public, not HPC itself.

Intel Xeon Phi

Another specific HPC product from Intel is the Xeon Phi. This device can be considered as a Host or Device/Accelerator machine. Intel describes it as "a bootable host processor that delivers massive parallelism and vectorization". This architecture embedded multiple multi-cores processors interconnected. This is call Intel's Many Integrated Core (MIC). The architectures names are Knights Ferry, Knights Corner and Knight Landing [SGC⁺16]. The last architecture, Knight Hill, was recently canceled by Intel due to low performances and to focus the Xeon Phi for Exascale. The main advantage of this architecture compared to GPGPUs is the x86 compatibility of the embedded cores and the fact this device can boot and use to drive other accelerators. They also feature more complex operations and handle double precision natively. We considered the Xeon Phi in the many-cores architecture despite the fact that it is composed of completely independent processors. This is due to the number of cores that is very high and the fact it can be use as an accelerator instead of the host.

PEZY

Another many-core architecture just appears in the last benchmarks. The PEZY Super Computer 2, PEZY-SC2, is the third many-core microprocessor developed by the company PEZY. The three first machine ranked in the GREEN500 list are accelerator using this many-core die. We also note that in the November 2017 list the 4th supercomputer, Gyukou, is also powered by PEZY-SC2 cards.

2.3.3 Other architectures

Numerous architecture have not been presented because out of scope in this study. We present here two technologies we have been confronted in our researches and that can be tomorrow solution for exascale in HPC.

FPGA

Field Programmable Gates Array are device that can be reprogram to fit the needs of the user after their construction. The leader was historically Altera with the Stratix, Arria and Cyclone FPGAs and is now part of Intel. With the FPGAs the user have access to the hardware itself and can design its own circuit. Nowadays FPGA can be targeted with OpenCL programming language. The arrival of Intel in this market promises the best hopes for HPC version of FPGAs. The main gap for users is the circuit building itself, perfect to respond to specific needs but hard to setup.

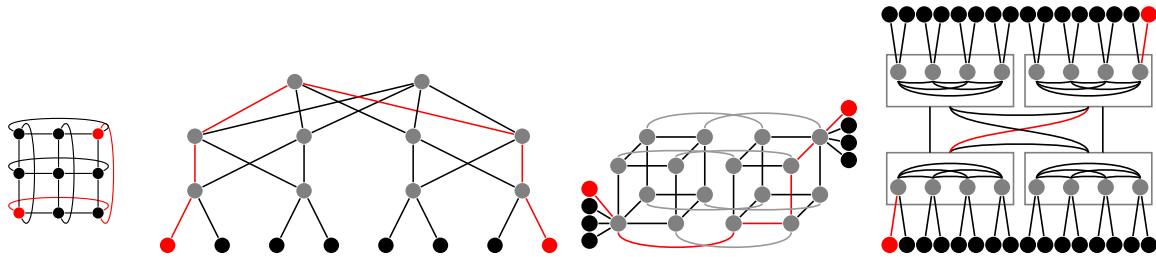


Figure 2.7: Torus, Fat-Tree, HyperX, DragonFly

ASIC

Application Specified Integrated Circuits are dedicated device construct for on purpose. An example of ASIC can be the Gravity Pipe (GRAPE) which is dedicated to compute gravitation given mass/positions. Google leads the way for ASIC and just created its dedicated devices to boost AI bots. We also find ASIC in some optimized communication devices like in fast interconnection network in HPC.

2.4 Distributed architectures

The technologies presented in previous part is the milestone of supercomputers. They are used together in a whole system to create machine delivering incredible computational power.

2.4.1 Architecture of a supercomputer

From the hardware described before we can create the architecture of a cluster from the smallest unit, cores, nodes, to the whole system:

Core: A core is the smallest unit in our devices. It can refer to the Von Neumann model in case of core with ALU and CU. We can separate core from CPU to GPU, the first one able to be independent whereas the second ones working together and sharing the same program counter.

Socket/Host: A socket is mistakenly called a CPU in nowadays language. It is, for multi-cores sockets, composed of several cores. The name Host comes from the Host-Device architecture using accelerators.

Accelerators/Devices: Accelerators are devices that, when attached to the Host, provide additional computational power. We can identify them as GPUs, FPGAs, ASICs, etc. A socket can have access to one or more accelerators. They can also share the accelerator usage.

Computation node: The next layer of our HPC system if the computation node. Grouping together several socket and accelerators sharing memory;

Rack: A rack is a set of computation nodes, generally a vertical stack. It can also include specific nodes dedicated to the network or the Input/Output.

Interconnection: The nodes are grouped together with hard wire connection following a specific interconnection topology with very high bandwidth.

System/Cluster/Supercomputer The cluster group several racks though an interconnection network.

In order to connect node together and allow distributed programming an interconnect technology is required. Interconnection network is the way the nodes of a cluster are connected together.

2.4.2 Interconnection topologies

Several topologies exists from point to point to multi dimensional torus. The figure 2.7 is a rep-

Name	Gbs	Year	Name	Gbs	Year
Single DR	2.5	2003	Enhanced DR	25	2014
Double DR	5	2005	Highg DR	50	2017
Quad DR	10	2007	Next DR	100	2020
Fourth DR	14	2011			

Table 2.1: InfiniBand technologies name, year and bandwidth

resentation of famous topologies. Each interconnect technology has its own specificity. These networks takes in account the number of nodes to interconnect and the targeted bandwidth/budget. Several declination of each network are not detailed here. The Mesh and the Torus are use as a basis in lower layers of others more complex interconnection networks. A perfect example is the supercomputer called K-Computer describe in the next section. The Fat Tree presented here is a k-ary Fat Tree, higher the position in the tree more connection are found and the bandwidth is important. The nodes are available as the leafs, on the middle level we find the switches and on top the routers. This is the topology of the ROMEO supercomputer we used for our tests. Another topology, HyperX[ABD⁺09], is base on Hyper-Cube. The DragonFly[KDSA08] interconnect is recent, 2008, and use in nowadays supercomputers.

InfiniBand (IB) is the most spread technology used for interconnect with different kind of bandwidth presented in figure 2.1. It provides high bandwidth and small latency and companies like Intel, Mellanox, etc provide directly adapters and switches specifically for IB.

Unfortunately this augmentation of clock rate is not sustainable due to the energy required and the heat generated by the running component. Another idea came in 19th century with the first multi-core processors.

2.4.3 Remarkable supercomputers

The TOP500² is the reference benchmarks for the world size supercomputers. This benchmark is based the LINPACK and aim to solve a dense system of linear equations. Most of the TOP10 machines have specific architectures and, of course, the most efficient ones. In this section we give details on several supercomputers about their interconnect, processors and specific accelerators.

Sunway Taihulight

Sunway Taihulight is the third Chinese supercomputer to be ranked in the first position of the TOP500 list, November 2017. A recent report from Jack J. Dongarra, a figure in HPC, decrypt the architecture of this supercomputer[Don16]. The most interesting point is the conception of this machine, completely done in China. The Sunway CPUs were designed and built in China. The Vendor is the Shanghai High Performance IC Design Center.

The SW26010, a many core architecture processor, features 260 cores based on RISC architecture and a specific conception depicted on figure 2.8. The processor is composed of the master core, a Memory Controller (MC), a Management Processing Element (MPE) that manages the Computing Processing Elements (CPE) which are the slaves cores.

The interconnect network is called Sunway Network and connected using Mellanox Host Channel Adapter (HCA) and switches. This is a five level interconnect going through computing nodes, computing board, super-nodes and cabinets to the complete system. For the latest TOP500 list, November 2017: the total memory is 1.31 PB and the number of cores available

²<https://www.top500.org>

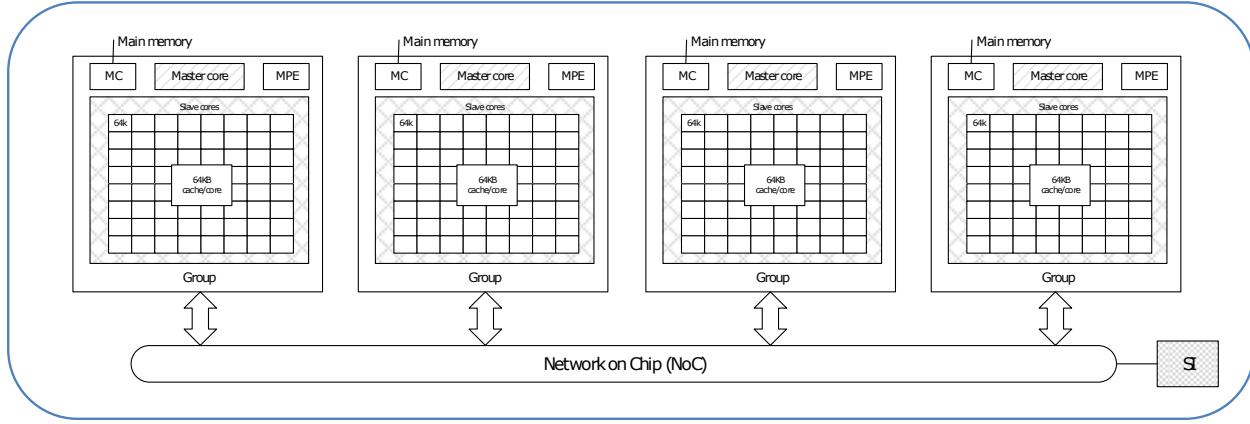


Figure 2.8: Sunway Taihulight node architecture from *Report on the Sunway TaihuLight System*, Jack Dongarra, June 24, 2016.

is 10,649,600. The peak performance is 125.4 PFLOPS and the Linpack is 93 PFLOPS which induce 74.16% of efficiency.

Piz Daint

The supercomputer of the CSCS, Swiss National Supercomputing Center, is currently ranked 2nd of the November 2017 TOP500 list. This GPUs accelerated supercomputer is a most powerful representative of GPU hybrid acceleration. This is also the most powerful European supercomputer. He is composed of 4761 hybrids and 1210 multi-core nodes. The hybrids nodes embedded an Intel Xeon E5-2690v3 and an NVIDIA Tesla Pascal P100 GPGPU. The interconnect is based on a Dragonfly network topology and Cray Aries routing and communications ASICs. The peak performance is 25.326 TFLOPS using only the hybrid nodes and the Linpack gives 19.590 TFLOPS. The low power consumption rank Piz Daint as 10th in the GREEN500 list of November 2017.

K-Computer

K-Computer was the top 1 supercomputer of TOP500 2011 list. The TOFU interconnect network makes the K-Computer unique [ASS09] and stands for TOrus FUision. This interconnect presented in figure 2.9 mixes a 6D Mesh/Torus interconnect. The basic units are based on a mesh and are interconnected together in a 3 dimensional torus. In this configuration each node can access to its 12 neighbors directly. It also provide a fault tolerant network with many routes to reach distant node.

Sequoia/Mira

Sequoia supercomputer was top 1 of the TOP500 2012 list. It is based on BlueGene from IBM. The BlueGene project made up to three main architectures with BlueGene/L, BlueGene/P and BlueGene/Q. It is very interesting to notice the BlueGene architecture because even in the last GRAPH500 list, November 2017, there is 15 of these machines in the TOP20. The algorithm used on these supercomputers will be our basis in the part II regarding our implementation of the GRAPH500 benchmark.

2.5 ROMEO Supercomputer

The ROMEO supercomputer center is the computation center of the Champagne-Ardenne region in France. Hosted since 2002 by the University of Reims Champagne-Ardenne, this so called

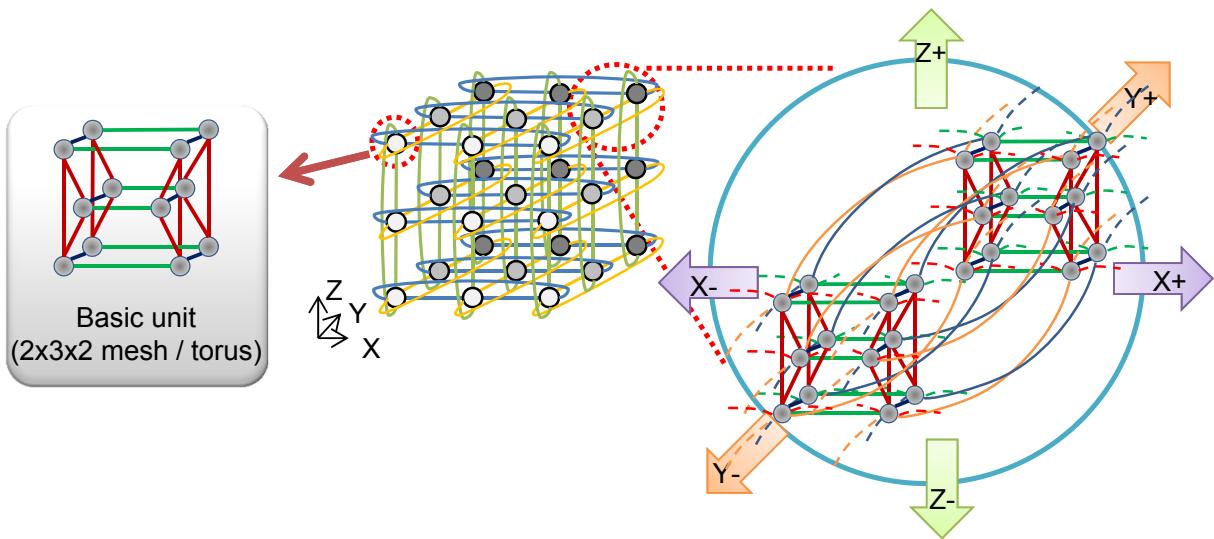


Figure 2.9: TOFU Interconnect schematic from *The K-Computer: System Overview*, Atsuya Uno, SC11

meso-center (Medium size HPC center) is used for HPC for theoretic research and domain science like applied mathematics, physics, biophysics and chemistry.

This project is supported by Europe, National fundings, Grand-Est region and Reims Metropole. It aims to host research and production codes of the region for industrial, research and academics purposes.

We are currently working on the fourth version of ROMEO, installed in 2013. As many of our tests in this study have been done on this machine, we will carefully describe its architecture.

This supercomputer was ranked 151st in the TOP500 and 5th in the GREEN500 list.

2.5.1 ROMEO hardware architecture

ROMEO is a Bull/Atos supercomputer composed of 130 BullX R421 computing nodes.

Each node is composed of two processors Intel Ivy Bridge 8 cores @ 2,6 GHz. Each processor have access to 16GB of memory for a total of 32GB per node, the total memory if 4.160TB. Each processor if linked, using PCIe-v3, to an NVIDIA Tesla K20Xm GPGPU. This cluster provide then 260 processors for a total of 2080 CPU cores and 260 GPGPU providing 698880 GPU cores. The computation nodes are interconnected with an Infiniband QDR non-blocking network structured as a FatTree. The Infiniband is a QDR providing 10GB/s.

The storage for users is 57 TB and the cluster also provide 195 GB of Lustre and 88TB of parallel scratch file-system.

In addition to the 130 computations nodes, the cluster provides a visualization node NVIDIA GRID with two K2 cards and 250GB of DDR3 RAM. The old machine, renamed Clovis, is always available but does not features GPUs.

The supercomputer supports MPI with GPU Aware and GPUDirect.

ROMEO is based on the Slurm³ workload manager for node distribution among the users. This manager allows different usage of the cluster with classical reservation-submission or more asynchronous computation with best-effort. We developed advantages of both submissions systems in part II.

2.5.2 New ROMEO supercomputer, June 2018

Avoir les info et decrire le nouveau ROMEO

³<https://slurm.schedmd.com/>

2.6 Conclusion

In this chapter we reviewed the most important nowadays hardware architectures and technologies. In order to use the driver or API in the most efficient way we need to keep in mind the way the data and instructions are proceed by the machine.

As efficiency is based on computation power but also communications we showed different interconnection topologies and their specificities. We presented perfect use cases of the technologies in nowadays top ranked systems. They also show that every architecture is unique in its construction and justify the optimization work dedicated to reach performance.

We can see through the new technologies presented here that every one is moving toward hybrids architectures featuring multi-core processors accelerated by one or more devices, many-core architectures. The exascale supercomputer of 2020 will be shape with hybrid architectures and they represent the best of nowadays technology for purpose of HPC. Combining CPU and GPUs or FPGA on the same die, sharing the same memory space can also be the solution.

Chapter 3

Software in HPC

3.1 Introduction

After presenting the rules of HPC and the hardware that compose the cluster, we introduce the most famous ways to target those architectures and supercomputers with programming models. Then, fitting those models, we present the possible options in the language, the API, the distribution and the accelerators code.

This chapter details the most important programming models and the software options for HPC programming and include the choices we made for our applications. Then it presents the software used to benchmark the supercomputers. We present here the most famous, the TOP500, GRAPH500, HPGC and GREEN500 to give their advantages and weaknesses.

3.2 Parallel and distributed programming Models

The Flynn taxonomy developed in chapter 1 was a characterization of the executions models. This model can be extended to programming models which are an extension of MIMD. We consider here a *Random Access Machine* (RAM). The memory of this machine consists of an unbounded sequence of registers each of which may hold an integer value. In this model the applications can access to every memory words directly in write or read manner. There are three main operations: load from memory to register; compute operation between data; store from register to memory. This model is used to estimate the complexity of sequential algorithms. If we consider the unit of time of each operation (like in cycle) we can have an idea of the overall time of the application. We identify two types of RAM, the Parallel-RAM using shared memory and the Distributed-RAM using distributed memory.

3.2.1 Parallel Random Access Machine

The Parallel Random Access Machine [FW78], PRAM, is a model in which the global memory is shared between the processes and each process has its own local memory/registers. The execution is synchronous, processes execute the same instructions at the same time. In this model each process is identified with its own index enabling to target different data. The problem in this model will be the concurrency in reading (R) and writing (W) data as the memory is shared between the processes. Indeed, mutual exclusion have to be set with exclusive (E) or concurrent (C) behaviors and we find 4 combinations: EREW, ERCW, CREW and CRCW. As the reading is not critical for data concurrency the standard model will be Concurrent Reading and Exclusive Writing: CREW.

An example of PRAM model applied on a reduction is given on figure 3.1. In this example the computation of minimum, maximum or a reduction can be performed on an array of n values in $\log(n)$ steps and $n - 1$ operations. This kind of reduction or scan are used to reach performances

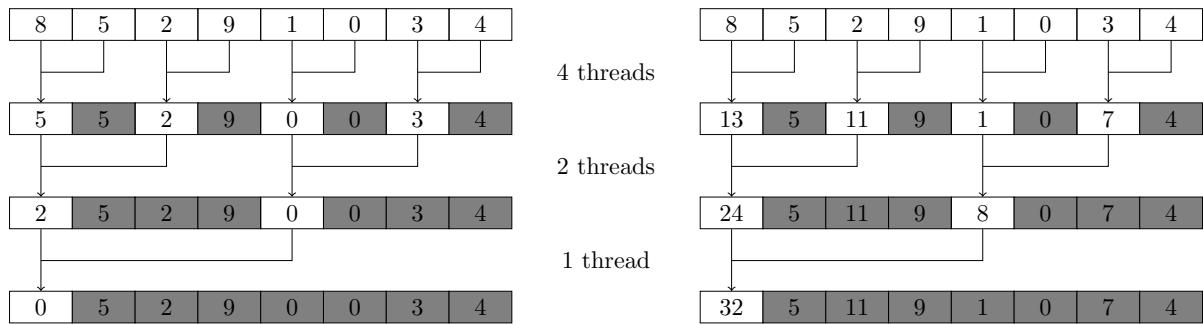


Figure 3.1: PRAM model example on minimum and reduction computation

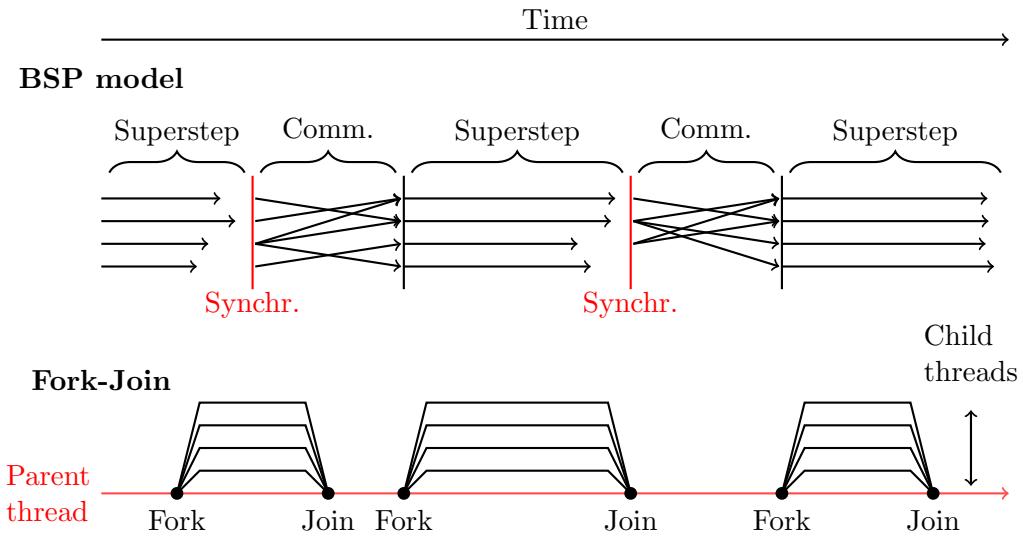


Figure 3.2: Bulk Synchronous Parallel model and Fork-Join model

on multi-core and many-core code in this study. We will give example of those reductions in different languages and API.

3.2.2 Distributed Random Access Machine

For machine that base their memory model on NoRMA the execution model can be qualify of Distributed Random Access Machine, DRAM. It is based on NoRMA memories detailed in part 1.4. This model is in opposition to PRAM because the synchronization between processes is made by communications and messages. Those communications can be of several kind and depend of physical architecture, interconnection network and software used.

3.2.3 H-PRAM

A DRAM can be composed of an ensemble of PRAM system interconnected. Each of them working on their own data and instructions. This is an intermediate model between PRAM and DRAM having a set of shared memory and synchronous execution, the overall execution being asynchronous and having distributed memory.

3.2.4 Bulk Synchronous Parallelism

This model was presented in 1990 in [Val90]. Being the link of HRAM and PRAM The Bulk Synchronous Parallelism model is based on three elements:

- a set of processor and their local memory;

- a network for point-to-point communications between processors;
- a unit allowing global synchronization and barriers.

This model is the most common on HPC clusters. It can be present even on node themselves: a process can be assigned on a core or set of cores and the shared memory is separated between the processes. The synchronization can be hardware but in most cases it is handled by the runtime used. A perfect example of runtime, presented later, is MPI.

In this model the applications apply a succession of *supersteps* separated by *synchronizations* steps and data exchanges.

At opposite to H-PRAM which represent the execution as a succession of independent blocks working synchronously, BSP propose independent blocks of asynchronous applications synchronized by synchronization steps.

In a communication/synchronization step we can consider the number of received messages h_r and the number of send ones h_s .

The time lost in communication in one synchronization step is:

$$T_{comm} = hg + I \quad (3.1)$$

With $h = \max(h_s, h_r)$, g the time to transfer data and I the start-up latency of the algorithm. Indeed, the entry points and exit points of communications super-step can be a bottleneck considered in I .

The time for computing a super-step is:

$$T_{comp} = \frac{w}{r} + I \quad (3.2)$$

With w the maximum number of flops in the computation of this super-step, r the speed of the CPU expressed in FLOPS and I the start-up latency of the algorithm. Indeed, the entry points and exit points of communications super-step can be a bottleneck considered in I .

The BSP model estimates the cost of one super-step with:

$$T_{comm} + T_{comp} = w + gh + 2l \quad (3.3)$$

With T a measure of time, a wall clock that measures elapsed time. We also note that usually g and I are function of the number of processes involved.

It can then be used to compute the overall cost in BSP model summing all super-steps s :

$$T = \sum_s \frac{\max(w_s)}{r} + h_s g + I \quad (3.4)$$

The problem of performances in this model can come from unequal repartitions of work, the load balancing. The processes with less than w of work will be idle.

3.2.5 Fork-Join model

The Fork-Join model or pattern is presented in figure 3.2. A main thread pilot the overall execution. When requested by the application, typically following the idea of *divide-and-conquer* approach, the main thread will fork and then join other threads. The *Fork* operation, called by a logical thread parent, creates new logical threads children working in concurrency. There is no limitations in the model and we find nested fork-join where a child can also call fork to generate sub-child and so on. The *Join* can be called by both parents and child. Children call join when done and the parent join by wait until children completion. The Fork operation increase concurrency and join decrease concurrency.

3.3 Software/API

In this section we present the main runtime, API and frameworks used in HPC and in this study in particular. The considered language will be C/C++, the most present in HPC world along with Fortran.

```

...
int min_val = MAX;
#pragma omp parallel for reduction(min:min_val)
for(int i = 0 ; i < X ; ++i){
    min_val = arr[i] < min_val ? arr[i] : min_val;
}
...

```

Figure 3.3: OpenMP reduction code for minimum

3.3.1 Shared memory programming

On the supercomputers nodes we find one or several processors that access to UMA or NUMA memory. Several API and language provide tools to target and handle concurrency and data sharing in this context. The two main ones are PThreads and OpenMP for multi-core processors. We can also cite Cilk++ or TBB from Intel.

PThreads

The Portable Operating System Interface (POSIX) threads API is an execution model based on threading interfaces. It is developed by the IEEE Computer Society. It allows the user to define threads that will execute concurrently on the processor resources using shared/private memory. PThreads is the low level handling of threads and the user need to handle concurrency with semaphores, conditions variables and synchronization "by hand". This makes the PThreads hard to use in complex applications and used only for very fine-grained control over the threads management.

OpenMP

Open Multi-Processing, OpenMP¹ [Cha08, Sup17], is an API for multi-processing shared memory like UMA and CC-NUMA. It is available in C/C++ and Fortran. The user is provided with pragmas and functions to declare parallel loop and regions in the code. In this model the main thread, the first one before forks, command the fork-join operations.

The last versions of OpenMP 4.0 also allow the user to target accelerators. During compilation the user specify on which processor or accelerator the code will be executed in parallel.

We use OpenMP as a basis for the implementation of our CPU algorithms. Perfect for loop parallelization and parallel sections, we show that we can have the best results for CPU algorithms in most of the case. In our case, OpenMP is always use on the node to target all the processors cores in the shared memory.

We note that the new versions of OpenMP also allows to target directly accelerators like NVIDIA ones.

The code corresponding to a reduction using OpenMP API is presented on figure 3.3. This is linked with the PRAM model reduction presented at the beginning of this part.

3.3.2 Distributed programming

In the cluster once the code have been developed locally and using the multiple cores available, the new step is to distribute it all over the nodes of the cluster. This step requires the processes to access NoRMA memory from a node to another. Several runtime are possible for this purpose and concerning our study. We should also cite HPX, the c++ standard distribution library, or AMPI for Adaptive MPI, Multi-Processor Computing (MPC) from CEA, etc.

¹<http://www.openmp.org>

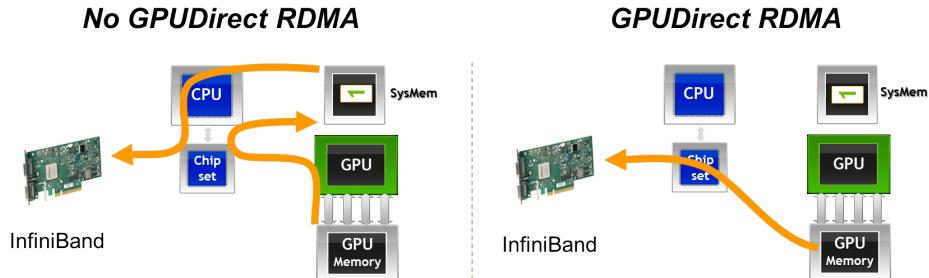


Figure 3.4: GPUDirect RDMA from NVIDIA Developer Blog, *An Introduction to CUDA-Aware MPI*

MPI

The Message Passing Interface, MPI, is the most famous runtime for distributed computing [Gro14, Gro15]. Several implementations exists from Intel MPI² (IMPI), MVAPICH³ by the Ohio State University and OpenMPI⁴ combining several MPI work like Los Alamos MPI (LA-MPI). Those implementation follow the MPI standards 1.0, 2.0 or the latest, 3.0.

This runtime provides directs, collectives and asynchronous functions for process(es) to process(es) communication. A process can be a whole node or one or several cores on a processor.

Some MPI implementations offer a support for accelerators targeting directly their memory through the network without multiple copies on host memory. The data go through one GPU to the other through network and PCIe. This feature is used in our code in part 2 and 3.

Most of our code presented here are based on MPI for the distribution on the cluster. The advantage is its presence on all the cluster and the control over the data transfers.

For NVIDIA this technology is called GPUDirect RDMA and presented on figure 3.4.

In term of development MPI can be very efficient if use carefully. Indeed, the collectives communications such as *MPI_Alltoall*, *MPI_Allgather*, etc. can be a bottleneck when scaling up to thousands of processes. A specific care have to be taken in those implementation with privilege to asynchronous communications to hide computation than synchronous idle CPU time.

Charm++

Charm++⁵ is an API for distributed programming developed by the University of Illinois Urbana-Champaign. It is asynchronous messages paradigm driven. In contrary of runtime like MPI that are synchronous but can handle asynchronous, charm++ is natively asynchronous. It is based on *chare object* that can be activated in response to messages from other *chare objects* with triggered actions and callbacks. The repartition of data to processors is completely done by the API, the user just have to define correctly the partition and functions of the program. Charm++ also provides a GPU manager implementing data movement, asynchronous kernel launch, callbacks, etc.

A perfect example can be the hydrodynamics N-body simulation code Charm++ N-body Gravity Solver, ChaNGa [JWG⁺10], implemented with charm++ and GPU support.

Legion

Legion⁶ is a distributed runtime support by Stanford University, Los Alamos National Laboratory (LANL) and NVIDIA. This runtime is data-centered targeting distributed heterogeneous

²<https://software.intel.com/en-us/intel-mpi-library>

³<http://mvapich.cse.ohio-state.edu/>

⁴<http://www.open-mpi.org>

⁵<http://charmplusplus.org/>

⁶<http://legion.stanford.edu/>

```
--inline__ __device__ void warpReduceMin(int& val, int& idx)
{
    for (int offset = warpSize / 2; offset > 0; offset /= 2) {
        int tmpVal = __shfl_down(val, offset);
        int tmpIdx = __shfl_down(idx, offset);
        if (tmpVal < val) {
            val = tmpVal;
            idx = tmpIdx;
        }
    }
}
```

Figure 3.5: CUDA kernel for reduction of minimum

architectures. Data-centered runtime focuses to keep the data dependency and locality moving the tasks to the data and moving data only if requested. In this runtime the user defines data organization, partitions, privileges and coherency. Many aspect of the distribution and parallelization are then handle by the runtime itself.

The FleCSI runtime develops at LANL provide a template framework for multi-physics applications and is built on top of Legion. We give more details on this project and Legion on part 3.

3.3.3 Accelerators

In order to target accelerators like GPU, several specific API have been developed. At first they were targeted for matrix computation with OpenGL or DirectX through specific devices languages to change the first purpose of the graphic pipeline. The GPGPUs arriving forced an evolution and new dedicated language to appear.

CUDA

The Compute Device Unified Architecture is the API develop in C/C++ Fortran by NVIDIA to target its GPGPUs. The API provide high and low level functions. The driver API allows a fine grain control over the executions.

The CUDA compiler is called NVidia C Compiler, NVCC. It converts the device code into Parallel Thread eXecution, PTX, and rely to the C++ host compiler for host code. PTX is a pseudo assembly language translated by the GPU in binary code that is then execute. As the ISA is simpler than CPU ones and able the user to work directly in assembly for very fine grain optimizations.

As presented in figure 3.6, NVIDIA GPUs include many *Streaming Multiprocessors* (SM), each of which is composed of many *Streaming Processors* (SP). In the Kepler architecture, the SM new generation is called SMX. Grouped into *blocks*, *threads* execute *kernels* functions synchronously. Threads within a block can cooperate by sharing data on an SMX and synchronizing their execution to coordinate memory accesses; inside a block, the scheduler organizes *warps* of 32 threads which execute the instructions simultaneously. The blocks are distributed over the GPU SMXs to be executed independently.

In order to use data in a device kernel, it has to be first created on the CPU, allocated on the GPU and then transferred from the CPU to the GPU; after the kernel execution, the results have to be transferred back from the GPU to the CPU. GPUs consist of several memory categories, organized hierarchically and differing by size, bandwidth and latency. On the one hand, the device's main memory is relatively large but has a slow access time due to a huge latency. On the other hand, each SMX has a small amount of shared memory and L1 cache, accessible by

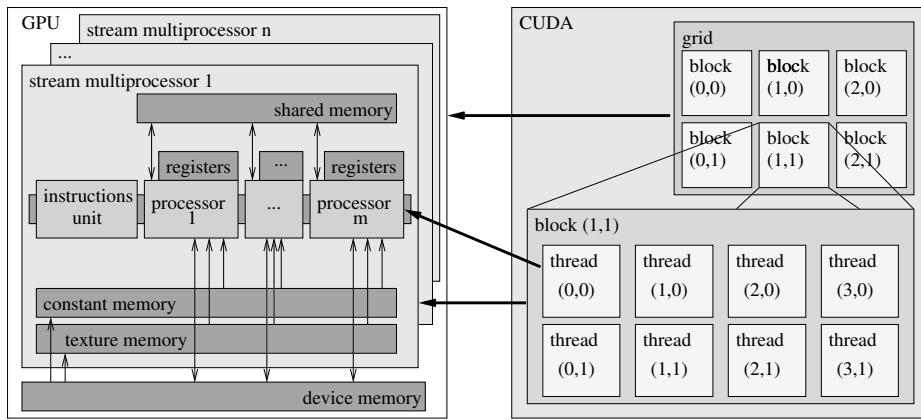


Figure 3.6: NVIDIA GPU and CUDA architecture overview

its SPs, with faster access, and registers organized as an SP-local memory. SMXs also have a constant memory cache and a texture memory cache. Reaching optimal computing efficiency requires considerable effort while programming. Most of the global memory latency can then be hidden by the threads scheduler if there is enough computational effort to be executed while waiting for the global memory access to complete. Another way to hide this latency is to use streams to overlap kernel computation and memory load.

It is also important to note that branching instructions may break the threads synchronous execution inside a warp and thus affect the program efficiency. This is the reason why test-based applications, like combinatorial problems that are inherently irregular, are considered as bad candidates for GPU implementation.

Specific tools have been made for HPC in the NVIDIA GPGPUs.

Dynamic Parallelism This feature allow the GPU kernels to run other kernels themselves.

When more sub-tasks have to be generated this can be done directly on the GPU using dynamic parallelism.

Hyper-Q This technology enable several CPU threads to execute kernels on the same GPU simultaneously. This can help to reduce the synchronization time and idle time of CPU cores for specific applications.

NVIDIA GPU-Direct GPUs' memory and CPU ones are different and the Host much push the data on GPU before allowing it to compute. GPU-Direct allows direct transfers from GPU devices through the network. Usually implemented using MPI.

Indeed, working with a very low level API like CUDA can lead to better performances. This can be very costly in development time. Regarding the time involved in coding compared to the performances gain, one may consider to use higher levels API like OpenACC.

The reduction using the CUDA API is presented on figure 3.5. It shows, compared to OpenMP, the complexity of CUDA code.

OpenCL

OpenCL is a multi-platform framework targeting a large part of nowadays architectures from processors to GPUs, FPGAs, etc. A large group of company already provided conform version of the OpenCL standard: IBM, Intel, NVIDIA, AMD, ARM, etc. This framework allows to produce a single code that can run in all the host or device architectures. It is quite similar to NVIDIA CUDA Driver API and based on kernels that are written and can be used in On-line/Off-line compilation meaning Just In Time (JIT) or not. The idea of OpenCL is great by rely on the vendors wrapper. Indeed, one may wonder, what is the level of work done by NVIDIA on its own CUDA framework compare to the one done to implement OpenCL standards? What is the advantage for NVIDIA GPU to be able to be replace by another component and compare

```

...
int min_val = MAX;
#pragma acc parallel loop copyin(arr[0:n]) reduction(min:min_val)
for (int i=0; i<n; i++) {
    min_val = arr[i]<min_val?arr[i]:min_val;
}
...

```

Figure 3.7: OpenACC code for reduction of minimum

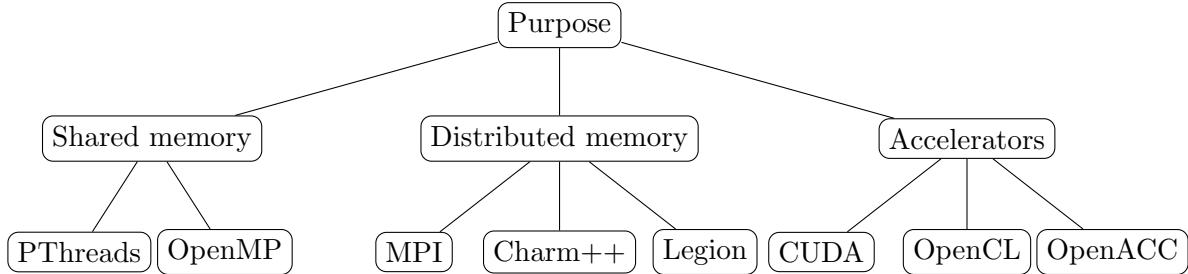


Figure 3.8: Runtimes, libraries, frameworks or APIs

on the same level? Those questions are still empty but many tests prove that OpenCL can be as comparable as CUDA but rarely better[KDH10, FVS11].

In this study most of the code had been developed using CUDA to have the best benefit of the NVIDIA GPUs present in the ROMEO Supercomputer. Also the long time partnership of the University of Reims Champagne-Ardenne and NVIDIA since 2003 allows us to exchange directly with the support and NVIDIA developers.

OpenACC

Open ACCelerators is a "user-driven directive-based performance-portable parallel programming model"⁷ developed with Cray, AMD, NVIDIA, etc. This programming model propose, in a similar way to OpenMP, pragmas to define the loop parallelism and the device behavior. As the device memory is separated specific pragmas are used to define the memory movements. Research works[WStAM12] tend to show that OpenACC performances are good regarding the time spent in the implementation itself compare to fine grain CUDA or OpenCL approaches. The little lack of performances can also be explained by the current contribution to companies in the wrapper for their architectures and devices.

The reduction example is given on figure 3.7. This shows the simplicity of writing accelerator code using high level API like OpenACC compared to the complex CUDA code. Indeed, this approach works in most of the case but for specific ones CUDA might outperform OpenACC.

The runtime, libraries, frameworks and APIs are summarized in figure 3.8. They are used in combination. The usual one is MPI for distribution, OpenMP and CUDA to target processors and GPUs.

3.4 Benchmarks

All those models, theory, hardware and software leads to better understanding and characterization of machines to produce better algorithm and solve bigger and harder problems. The question that arise is: how to know if a machine is better than another? We answer that ques-

⁷<https://www.openacc.org/>

tion with FLOPS, IPC, OPS or just the frequency of the machine. The models like BSP or law's like Amdahl and Gustafson ones propose to find the best/worst case during the execution.

In real application the only way to really know what will be the behavior of a supercomputer is to try, test real code on it. This is call benchmarking. Several kind of benchmarks exists and target a specific application of supercomputers. We present here the most famous benchmarks of HPC and their specificities.

3.4.1 TOP500

The most famous benchmark is certainly the TOP500⁸. It gives the ranking of the 500 most powerful, known, supercomputers of the world as its name indicates. Since 1993 the organization assembles and maintains this list updated twice a year in June and November.

This benchmark is based on the LINPACK[DMS⁺94] a benchmark introduced by Jack J. Dongarra. This benchmark rely on solving dense system of linear equations. As specified in this document this benchmark is just one of the tools to define the performance of a supercomputer. It reflects "the performance of a dedicated system for solving a dense system of linear equations". This kind of benchmark is very regular in computation giving high results for FLOPS.

In 1965 the Intel co-fonder Gordon Moore made an observation[Pre00] on the evolution of devices. He pointed the fact that the number of transistors in a dense integrated circuit doubles approximately every eighteen months. This is know as the Moore's law. Looking at the last TOP500 figure presented on figure 1, in the introduction of this document, we saw that nowadays machines does not fit in the law anymore. This is due to the size of transistor and the energy needed to reach more powerful machines. The Moore's law have been sustains by the arrival of many-cores architectures such as GPU or Xeon Phi. Tomorrow machines architectures will have to be based on hybrid with more paradigms and tools to take part of massive parallelism.

3.4.2 Green500

In conjunction of the TOP500, the Green500⁹ focus on the energy consumption of supercomputers. The scale is based on FLOPS per watts [FC07]. Indeed the energy wall is the main limitation for next generation and exascale supercomputers. In the last list, November 2017, the TOP3 machines are accelerated with PEZY-SC many-core devices. The TOP20 supercomputers are all equipped with many-cores architectures: 5 with PEZY-SC, 14 with NVIDIA P100 and 1 with the Sunway many-core devices. This show clearly that the nowadays energy efficient solutions resides in many-core architecture and more than that, hybrid supercomputers.

3.4.3 GRAPH500

The GRAPH500¹⁰ benchmark[MWBA10] focus on irregular memory accesses, and communications. The authors try to find ways to face the futures large-scale large-data problems and data-driven analysis. This can be see as a complement of the TOP500 for data intensive applications. The aim is to generate a huge graph to fill all the maximum memory on the machine and then operate either:

BFS: A Breadth-First Search which is an algorithm starting from a root and exploring recursively all the neighbors. This requires a lot of irregular communications and memory accesses.

SSSP: A Single Source Shortest Path which is an algorithm searching the shortest path from one node to the others. Like the BFS it has an irregular behavior but also requires to keep more data during the computation.

⁸<http://www.top500.org>

⁹<https://www.top500.org/green500/>

¹⁰<https://www.graph500.org/>

This benchmark will be detailed in Part II Chapter II in our benchmark suite.

3.4.4 HPCG

The High Performance Conjugate Gradient benchmark¹¹ is a new benchmark created in 2015 and presented for the first time at SuperComputing 2015. The last list, November 2017 contains 115 supercomputers ranked. The list also offer to compare the results of Linpack compared to Conjugate Gradient. This benchmark is a first implementation of having both computation and communications aspects of HPC in the same test.

This benchmark is presented and features:

- Sparse matrix-vector multiplication;
- Vector updates;
- Global dot products;
- Local symmetric Gauss-Seidel smoother;
- Sparse triangular solve (as part of the Gauss-Seidel smoother);
- Driven by multigrid preconditioned conjugate gradient algorithm that exercises the key kernels on a nested set of coarse grids;
- Reference implementation is written in C++ with MPI and OpenMP support.

The benchmarks presented in this section are the most famous of HPC world. Indeed, they are not the perfect representative of the nowadays application. The upcoming of big data and artificial intelligence in addition to classical "real life" applications impose HPC to evolute and find new ways to target new architectures. The TOP500 target the computational problem but does not handle a lot of irregularity. Indeed, solving dense linear equation is straight forward and also use the memory in a regular way. The Graph500 is very interesting to focus on communication and does handle irregular behavior for communications and memory. The Green500 does target energy wall but can also be applied to any benchmark. The most interesting one may be the HPCG benchmark. It does create irregularity during computation and communication along to memory traversal.

3.5 Conclusion

In this chapter we presented the most used software tools for HPC. From inside node with shared memory paradigms, accelerators and distributed memory using message passing runtime with asynchronous or synchronous behavior.

The tools to target accelerators architectures tend to be less architecture dependent with API like OpenMP, OpenCL or OpenACC targeting all the machines architectures. Unfortunately the vendor themselves have to be involve to provide the best wrapper for their architecture. In the mean time vendor dependent API like CUDA for NVIDIA seems to deliver the best performances.

We show through the different benchmark that hybrid architecture start to have their place even in computation heavy and communication heavy context. They are the opportunity to reach exascale supercomputers in horizon 2020.

¹¹<http://www.hpcg-benchmark.org/>

Conclusion

This part detailed the state of the art theory, hardware and software in High Performance Computing and the tools we need to detail our experiences.

In the first chapter we introduced the models for computation and memory. We also detailed the main laws of HPC.

The second chapter was an overview of hardware architectures in HPC. The one that seems to be the most promising regarding computational power and energy consumption seems to be hybrid architectures. Supercomputers equipped with classical processors accelerated by devices like GPGPUs, Xeon Phi or, for tomorrow supercomputers, FPGAs.

In the third section we showed that the tools to target such complex architecture are ready. They provide the developer a two or three layer development model with MPI for distribution over processes, OpenMP/PThreads for tasks between the processor's cores and CUDA/OpenCL/OpenMP/OpenACC to target the accelerator.

We also showed in the last part that the benchmarks proposed to rank those architectures are based on regular computation. They are node facing realistic domain scientists code behavior. The question that arise is: How the hybrid architecture will handle irregularity in term of computation and communication? This question will be developed in the next part through one example for irregular computation and another for irregular communication using accelerators.

Part II

Complex problems metric

Introduction

The tools described in the previous part for comprehension of High Performance Computing from theory, hardware and software give us the basic elements to go toward optimizations and benchmarking. We showed through examples that hybrid architectures seem to be the way to reach exascale in few years. In the same time many optimizations need to be done. On one hand, the exascale supercomputer will need to fit the energy envelope imposed, to be able to sustain the computational power and the price of the hardware itself for economical reasons. This is made by vendors and is a specific area of optimization. On the other hand, we focus on the performances we have using a specific architecture/accelerator to fit the targeted application with the best resources usage. The need of regular memory accesses, synchronization and the host-device memory separation put some constraint on their usage. As many-cores architectures presented nowadays come with several downsides we need to confront them to classical processor in a specific set of problems, a metric, a dedicated benchmark suite.

In benchmarks like the TOP500 the target is to solve a problem with regular computation and communication behavior. We think that this behavior does not fit realistic and production applications. In many domains like meteorology, oceanography, astrophysics, big data, ... the underlying issue are the irregular input and behavior. The irregularity in an application can have several definitions. This is defined by [JTB] as a problem which: can not be characterized a priori, is input data dependent and evolves with the computation itself. In [SL06] the author specifies that the work involves subcomputations which cannot be determined before and implies work distribution during runtime. The irregularity can then spread on all the layers of the resolution: the communications, the computation and the memory searches.

In order to target more representative applications of nowadays realistic problems, we identify several bottlenecks and limitations in HPC. Those limitations are called *walls* against which nowadays architectures are confronted to reach exascale.

Memory Wall: This problem is targeted for the first time in [WM95]. The author explains that:

We all know that the rate of improvement in microprocessor speed exceeds the rate of improvement in DRAM memory speed, each is improving exponentially, but the exponent for microprocessors is substantially larger than that for DRAMs.

In the case of accelerator another layer of memory is added. The memory of the host processors and devices accelerators cannot be accessed directly and copies from one to the other are requested. The problems of coalescent accesses are also addressed in this study. Some companies try to find ways using shared memory between host and device but this technology is always under development and tests for HPC purpose.

The two problems we propose for our metric implement heavy memory utilization. The first one dynamically uses the memory in an irregular way. The tree traversal of the first method generates temporary data and binary tests. The algebraic method uses a dedicated big integers library and carries propagation are applied just when necessary. In the second benchmark the memory is saturated and prepared at the startup. It is then accessed in an irregular way during all the computation.

Communication wall: We showed that the supercomputer architecture is based on a set of racks, composed of nodes composed of computation units. The network topology can never be perfect for all the kind of problems and even the fastest technologies are limited to the software handling. Limiting the big synchronizations steps, like in the BSP model, allows the system to be asynchronous and hide computation by communications. Unfortunately this is not applicable to all the applications and a huge care have to be taken to approach perfect scaling.

We decided to target this problem in two main ways. In the first benchmark the model corresponds to FIIT: Finite number of Independent and Irregular Tasks, introduced in [FKF03]. The tasks can be solved independently and then merged at the end. We show that the accelerators can also take advantage of specific distribution methods like Best-Effort. In the second problem communications are central because the data are too big to be represented on a single machine and cannot be computed independently. The irregularity in communication is very high. In this benchmark the number of data shared is never known before reaching the end of a superstep.

Power wall: The energy consumption of nowadays and future supercomputers is the main wall in HPC. Indeed, an exascale supercomputer could be constructed using several petascale supercomputers but, with today's architectures, will require a full nuclear plant to operate. In this objective low energy consumption and innovative architectures need to be found. The energy considered is required to power the machine itself but also handle the heat generated.

This wall is the underlying goal of this study. The hybrid architectures seem to deliver better performances for less watts. This thesis shows through different benchmarks what is the real benefit of accelerators on realistic problems and that the performances can be even better for less watts of consumption.

Computational wall: The computational wall is a combination of the walls presented before. By increasing the memory wall, the energy consumption and the communications we can increase the overall computation power of the supercomputer. The limitation in computational power also comes from the fact that the Moore's law seems to be over. Vendors have more difficulties to shrink transistors due to physical side effects. The frequency itself seems to reach its highest values due to the energy required to operate, the heat dissipated and synchronization issues.

This is targeted in the first benchmark we propose. The algebraic method is heavy in computation with irregular memory accesses. The second one does focus on irregular communication and memory usage with test base operations.

This is why we propose in this part a new metric for the main HPC walls to confront many-core architectures to multi-core architectures. The two applications we targeted cover all the walls we specify.

The first academic problem is a perfect candidate for our benchmark since it characterizes the behavior of accelerators and more specifically GPUs focusing on irregular computations and memory accesses. It is the problem of Langford and it shows how we can take advantage of accelerators for this kind of problem.

The second problem is focused on irregular memory accesses and communications. It is based on a benchmark we presented in the previous part, the Graph500 benchmark.

The combination of those two problems creates a metric covering all the walls and limitations we are facing in HPC. This allows us to emphasize on the behavior of hybrid architecture on several types of problems.

Chapter 4

Computational Wall: Langford Problem

4.1 Introduction

Our goal is to determine the behavior of accelerators compared to classical processor in case of irregular-computationally heavy problems. For this purpose we choose the Langford problem which is an academic problem of combinatorial counting.

We present the problem and expose the two possible methods to solve it:

- The tree traversal, call Miller's method, providing us benchmark targeting irregular memory and computation.
- The algebraic version, calls Godfrey's method, showing the performances of many-core vs multi-core architectures in respect to computationally heavy and memory irregular behaviors.

We show the optimizations made to the regular processor algorithm to efficiently implement this application on GPU. We compare the two approaches with classical processor and GPU implementation. The results are then presented to show the acceleration using the whole ROMEO supercomputer.

4.1.1 The Langford problem

C. Dudley Langford gave his name to a classic permutation problem [Gar56, Sim83]. While observing his son manipulating blocks of different colors, he noticed that it was possible to arrange three pairs of different colored blocks (yellow, red and blue) in such a way that only one block separates the red pair - noted as pair 1 -, two blocks separate the blue pair - noted as pair 2 - and finally three blocks separate the yellow one - noted as pair 3 -, see figure 4.1.

This problem has been generalized to any number n of colors and any number s of blocks having the same color. $L(s, n)$ consists in searching for the number of solutions to the Langford problem, up to a symmetry. In November 1967, Martin Gardner presented $L(2, 4)$ (two cubes and four colors) as being part of a collection of small mathematical games and he stated that

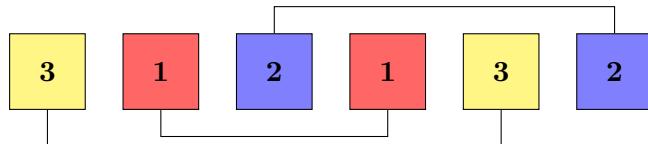


Figure 4.1: $L(2,3)$ arrangement

Instance	Solutions	Method	Computation time
L(2,3)	1	Miller algorithm	-
L(2,4)	1		-
...
L(2,16)	326,721,800		120 hours
L(2,19)	256,814,891,280		2.5 years (1999) DEC Alpha
L(2,20)	2,636,337,861,200	Godfrey algorithm	1 week
L(2,23)	3,799,455,942,515,488		4 days with CONFIIT
L(2,24)	46,845,158,056,515,936		3 months with CONFIIT
L(2,27)	111,683,611,098,764,903,232		2 days on ROMEO
L(2,28)	1,607,383,260,609,382,393,152		23 days on ROMEO

Table 4.1: Solutions and time for Langford problem using different methods

$L(2, n)$ has solutions for all n such that:

$$\text{solutions for: } \begin{cases} n = 4k \\ n = 4k - 1 \end{cases} \quad k \in \mathbb{N}^+ \quad (4.1)$$

The central resolution method consists in placing the pairs of cubes, one after the other, on the free places and backtracking if no place is available (see figure 4.3 for detailed algorithm).

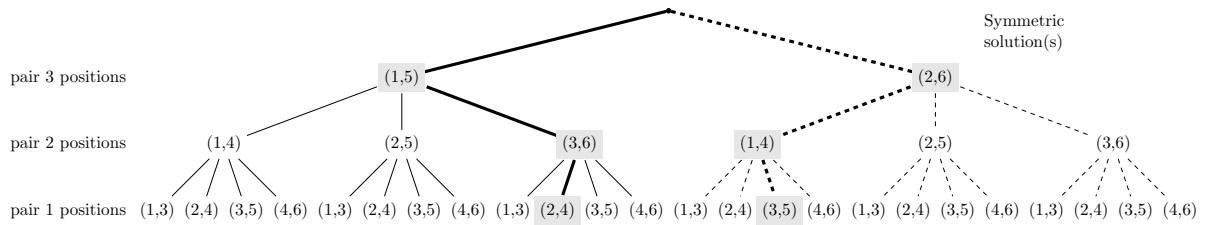
The Langford problem has been approached in different ways: discrete mathematics results, specific algorithms, specific encoding, constraint satisfaction problem (CSP), inclusion-exclusion ... [Mil99, Wal01, Smi00, Lar09]. In 2004, the last solved instance, $L(2, 24)$, was computed by our team [JK04a] using a specific algorithm. Table 4.1 presents the latest results and number of solutions. $L(2, 27)$ and $L(2, 28)$ have just been computed but no details were given.

The most efficient known algorithms are: the Miller backtrack method, the Godfrey algebraic method and the Larsen inclusion-exclusion method. The Miller one is based on backtracking and can be modeled as a CSP; it allowed us to move the limit of explicits solutions building up to $L(2, 21)$ but combinatorial explosion did not allow us to go further. Then, we use the Godfrey method to achieve $L(2, 24)$ more quickly and then recompute $L(2, 27)$ and $L(2, 28)$, presently known as the last instances. The Larsen method is based on inclusion-exclusion [Lar09]; although this method is effective, practically the Godfrey one is better. The latest known work on the Langford Problem is a GPU implementation proposed in [ABL15] in 2015. Unfortunately this study does not provide any performance considerations but just gives the number of solution of $L(2, 27)$ and $L(2, 28)$.

4.2 Miller algorithm

The Miller's method is based on a tree traversal to be able to check all the cubes positions. This method finds its limits because even using branch cutting algorithm to traverse the tree, the number of branches to explore stay very high. We implemented a multi-core and many-core version of it for the purpose of our benchmark. Indeed, this huge tree traversal requires irregular computation and memory accesses: two elements fitting the wall we want to confront to our architectures.

In this section we present our multi-GPU cluster implementation of the Miller's algorithm. First, we introduce the backtrack method itself and the elements allowing us to consider it as a good candidate for our metric. Then we present our implementation in order to fit the GPUs architecture. The last section presents our results.

Figure 4.2: Search tree for $L(2, 3)$

4.2.1 CSP

Combinatorial problems are NP-complete [GJ79] and can be described as satisfiability problems (SAT) using a polynomial transformation. They can be transformed into CSP formalism. A *Constraint Satisfaction Problem* (CSP), first introduced by Montanari [Mon74], is defined as a triple $\langle X, D, C \rangle$ where:

$$\begin{cases} X = \{X_1, \dots, X_n\}: \text{a finite set of variables} \\ D = \{D_1, \dots, D_n\}: \text{their finite domains of values} \\ C = \{C_1, \dots, C_p\}: \text{a finite set of constraints} \end{cases} \quad (4.2)$$

The goal in this formalism is to assign values in D to n -uple X respecting all the C p -uple constraints. This approach is a large field of research. [AC14] developed *local search* and compares GPU to CPU. This first work brings to light that GPU is a real contributor to the global computation speed. [CDPD⁺14] proposes a solver using *propagator* on a GPU architecture to solve CSP problems. [JAO⁺11] cares about GPU weak points, loading bandwidth and global memory latency.

Considering a basic approach, combinatorial problems formed into CSP can be represented as a tree search. Each level corresponds to a given variable, with values in its domain. Leaves of the tree correspond to a complete assignment (all variables are set). If it meets all the constraints this assignment is called an acceptor state. Depending on the constraints set, the satisfiability evaluation can be made either on complete or partial assignment.

4.2.2 Backtrack resolution

As presented above the Langford problem is known to be a highly irregular combinatorial problem. We first present here the general tree representation and the ways we regularize the computation for GPUs. Then we show how to parallelize the resolution over a multi-GPU cluster.

Langford's problem tree representation

As explained, CSP formalized problems can be transformed into tree evaluations. In order to solve $L(2, n)$, we consider a tree of height n : see example of $L(2, 3)$ in figure 7.6.

- Every level of the tree corresponds to a cube color.
- Each node of the tree corresponds to the placement of a pair of cubes without worrying about the other colors. Color p is represented at depth $n - p + 1$, where the first node corresponds to the first possible placement (positions 1 and $p+2$) and i^{th} node corresponds to the placement of the first cube of color p in position i , $i \in [1, 2n - 1 - p]$.
- Solutions are leaves generated without any placement conflict.

```

while not done do
  test pair           <- test
  if successful then
    if max depth then
      count solution
      higher pair
    else
      lower pair       <- remove
    else
      higher pair     <- add
  for pair 1 positions
    assignment
    for pair 2 positions
      assignment
      for ...
    for pair n positions
      assignment
      if final test ok then
        count solution
      <- add
    <- add
  <- add

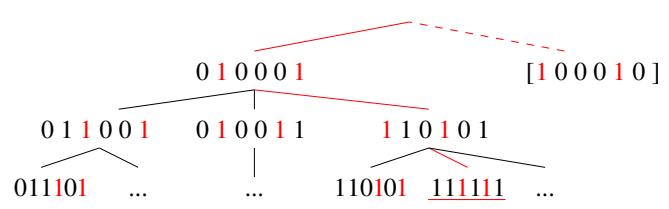
```

Figure 4.3: Backtrack algorithm

	pair 1	pair 2	pair 3
1	0 0 0 1 0 1	0 0 1 0 0 1	0 1 0 0 0 1
2	0 0 1 0 1 0	0 1 0 0 1 0	1 0 0 0 1 0
3	0 1 0 1 0 0	1 0 0 1 0 0	
4	1 0 1 0 0 0		

Figure 4.5: Bitwise representation of pairs positions in $L(2, 3)$

Figure 4.4: Regularized algorithm

Figure 4.6: Bitwise representation of the Langford $L(2, 3)$ placement tree

- As we consider the solution up to a symmetry, the left part is represented dashed and is in fact not traversed.

There are many ways to browse the tree and find the solutions: *backtracking*, *forward-checking*, *backjumping*, etc [Pro93]. We limit our study to the naive *backtrack* resolution and choose to evaluate the variables and their values in a static order; in a depth-first manner, the solutions are built incrementally and if a partial assignment can be aborted, the branch is cut. A solution is found each time a leaf is reached.

The recommendation for performance on GPU accelerators is to use non test-based programs. Due to its irregularity, the basic *backtracking* algorithm, presented on figure 4.3, is not supposed to suit the GPU architecture. Thus a vectorized version is given when evaluating the assignments at the leaves' level, with one of the two following ways: assignments can be prepared on each tree node or totally set on final leaves before testing the satisfiability of the built solution (figure 4.4).

Data representation

In order to count every Langford problem solution, we first identify all possible combinations for one color without worrying about the other ones. Each possible combination is coded within an integer, a bit to 1 corresponding to a cube presence, a 0 to its absence. This is what we called a *mask*. This way figure 4.5 presents the possible combinations to place the one, two and three weight cubes for the $L(2, 3)$ Langford instance.

Furthermore the masks can be used to evaluate the partial placements of a chosen set of colors: all the 1 correspond to occupied positions; the assignment is consistent *iff* there are as many 1 as the number of cubes set for the assignment.

With the aim to find solutions, we just have to go all over the tree and *sum* one combination of each of the colors: a solution is found *iff* all the bits of the sum are set to 1.

Each route on the tree can be evaluated individually and independently; then it can be evaluated as a thread on the GPU. This way the problem is massively parallel and can be, indeed, computed on GPU. figure 4.6 represents the tree masks' representation.

a) adding a pair

mask	or	$\begin{array}{r} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{array}$	or	$\begin{array}{r} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{array}$
pair		$\underline{\begin{array}{r} 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 0 \end{array}}$		$\underline{\begin{array}{r} 0 \\ 0 \\ 0 \\ 1 \\ 0 \\ 1 \end{array}}$
		$\begin{array}{r} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$		$\begin{array}{r} 1 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$

b) testing a pair

mask	and	$\begin{array}{r} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{array}$	and	$\begin{array}{r} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{array}$
pair		$\underline{\begin{array}{r} 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 0 \end{array}}$		$\underline{\begin{array}{r} 0 \\ 0 \\ 0 \\ 1 \\ 0 \\ 1 \end{array}}$
		$= 0$		$= 1$

Figure 4.7: Testing and adding position

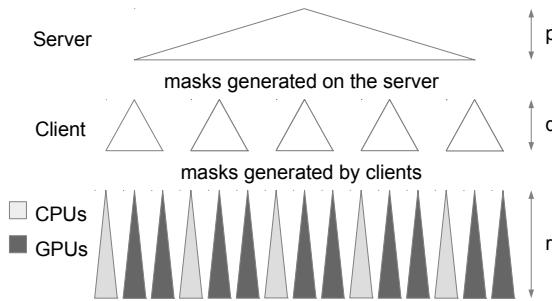


Figure 4.8: Server client distribution

Specific operations and algorithms

Three main operations are required in order to perform the tree search. The first one, used for both backtrack and regularized methods, aims to add a pair to a given assignment. The second one, allowing to check if a pair can be added to a given partial assignment, is only necessary for the original backtrack scheme. The last one is used for testing if a global assignment is an available solution: it is involved in the regularized version of the Miller algorithm.

Add a pair: Top of figure 4.7 presents the way to add a pair to a given assignment. With a *binary OR*, the new mask contains the combination of the original mask and of the added pair. This operation can be performed even if the position is not available for the pair (however the resulting mask is inconsistent).

Test a pair position: On the bottom part of the same figure, we test the positioning of a pair on a given mask. For this, it is necessary to perform a *binary AND* between the mask and the pair.

$= 0$: *success*, the pair can be placed here

$\neq 0$: *error*, try another position

Final validity test: The last operation is for *a posteriori* checking. For example the mask 101111, corresponding to a leaf of the tree, is inconsistent and should not be counted among the solutions. The final placement mask corresponds to a solution *iff* all the places are occupied, which can be tested as $\neg \text{mask} = 0$.

Using this data representation, we implemented both *backtrack* and *regularized* versions of the Miller algorithm, as presented in figure 4.3 and 4.4.

The next section presents the way we hybridize these two schemes in order to get an efficient parallel implementation of the Miller algorithm.

4.2.3 Hybrid parallel implementation

Section 4.2.2 presents the Miller algorithm and the tools needed for the resolution. The irregularity is present in the tree traversal and specific data representation has been chosen for efficient use of the memory. This section presents our methodology to implement Miller's method on a multi-GPU cluster.

Tasks generation: In order to parallelize the resolution we have to generate tasks. Considering the tree representation, we construct tasks by fixing the different values of a first set of variables [pairs] up to a given level. Choosing the development level allows to generate as many tasks as necessary. This leads to a *Finite number of Irregular and Independent Tasks* (*FIIT*) applications [Kra99].

Cluster parallelization: The generated tasks are independent and we spread them in a client-server manner: a server generates them and makes them available for clients. As we consider the cluster as a set of CPU-GPU(s) machines, the clients are these machines. At the machines level, the role of the CPU is, first, to generate work for the GPU(s): it has to generate sub-tasks, by continuing the tree development as if it were a second-level server, and the GPU(s) can be considered as second-level client(s).

The sub-tasks generation, at the CPU level, can be made in parallel by the CPU cores. Depending on the GPUs number and their computation power the sub-tasks generation rhythm may be adapted, to maintain a regular workload both for the CPU cores and GPU threads: some CPU cores, not involved in the sub-tasks generation, could be made available for sub-tasks computing.

This leads to the 3-level parallelism scheme presented in figure 4.8, where p , q and r respectively correspond to: (p) the server-level tasks generation depth, (q) the client-level sub-tasks generation one, (r) the remaining depth in the tree evaluation, *i.e.* the number of remaining variables to be set before reaching the leaves.

Backtrack and regularized methods hybridization: The Backtrack version of the Miller algorithm suits CPU execution and allows to cut branches during the tree evaluation, reducing the search space and limiting the combinatorial explosion effects. A regularized version had to be developed, since GPUs execution requires synchronous execution of the threads, with as few branching divergence as possible; however this method imposes to browse the entire search space and is too time-consuming.

We propose to hybridize the two methods in order to take advantage of both of them for the multiGPU parallel execution: for tasks and sub-tasks generated at sever and client levels, the tree development by the CPU cores is made using the backtrack method, cutting branches as soon as possible [and generating only possible tasks]; when computing the sub-tasks generated at client-level, the CPU cores involved in the sub-tasks resolution use the backtrack method and the GPU threads the regularized one.

4.2.4 Experiments tuning

In order to take advantage of all the computing power of the GPU we have to refine the way we use them: this section presents the experimental study required to choose optimal settings. This tuning allowed us to prove our proposal on significant instances of the Langford problem.

Registers, blocks and grid: In order to use all GPUs capabilities, the first way was to fill the blocks and grid. To maximize occupancy (ratio between active warps and the total number of warps) NVIDIA suggests to use 1024 threads per block to improve GPU performances and proposes a CUDA occupancy calculator¹. But, confirmed by the Volkov's results[Vol10], we experimented that better performances may be obtained using lower occupancy. Indeed, another critical criterion is the inner GPU registers occupation. The optimal number of registers (57 registers) is obtained by setting 9 pairs placed on the client for $L(2, 15)$, thus 6 pairs are remaining for GPU computation.

In order to tune the blocks and grid sizes, we performed tests on the ROMEO architecture. Figure 4.9 represents the time in relation with the number of blocks per grid and the number of threads per block. The most relevant result, observed as a local minimum on the 3D surface, is obtained near 64 or 96 threads per block; for the grid size, the limitation is relative to the GPU global memory size. It can be noted that we do not need shared memory because their are no data exchanges between threads. This allows us to use the total available memory for the L1 cache for each thread.

¹http://developer.download.nvidia.com/compute/cuda/CUDA_Occupancy_calculator.xls

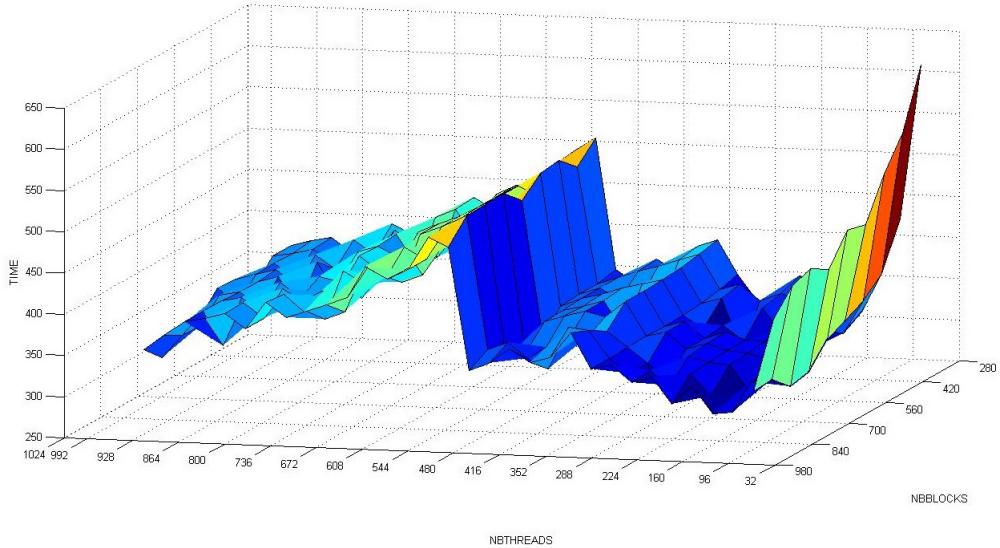
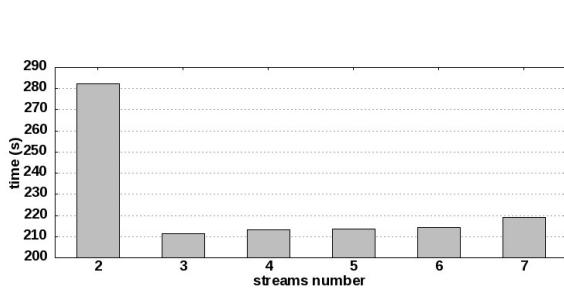
Figure 4.9: Time depending on grid and block size on $n = 15$ 

Figure 4.10: Computing time depending on streams number

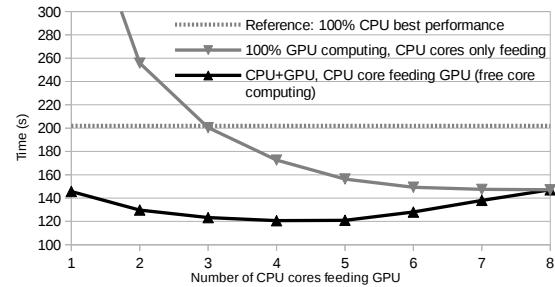


Figure 4.11: CPU cores optimal distribution for GPU feeding

Streams: A client has to prepare work for GPU. There are four main steps: generate the tasks, load them into the device memory, process the task on the GPU and then get the results.

CPU-GPU memory transfers cause huge time penalties (about 400 cycles latency for transfers between CPU memory and GPU *device memory*). At first, we had no overlapping between memory transfer and kernel computation because the tasks generation on CPU was too long compared to the kernel computation. To reduce the tasks generation time we used OpenMP in order to use the eight available CPU cores. Thus CPU computation was totally hidden by memory transfers and GPU kernel computation. We tried using up to 7 streams; as shown by figure 4.10, using only two simultaneous streams did not improve efficiency because the four steps did not overlap completely; the best performances were obtained with three streams; the slow increase in the next values is caused by synchronization overhead and CUDA streams management.

Setting up the server, client and GPU depths: We now have to set the depths of each actor, server (p), client (q) and GPU (r) (see figure 4.8).

First we set the $r = 5$ for large instances because of the GPU limitation in terms of registers by threads, exacerbated by the use of numerous 64bits integers. For $r \geq 6$, we get too many registers (64) and for $r \leq 4$ the GPU computation is too fast compared to the memory load overhead.

Clients are the buffers between the server and the GPUs: $q = n - p - r$. So we have conducted tests by varying the server depth, p . The best result is obtained for $p = 3$ and

n	CPU (8c)	GPU (4c) + CPU (4c)	n	CPU (8c)	GPU (4c) + CPU (4c)
15	2.5	1.5	17	29.8	7.3
16	21.2	14.3	18	290.0	73.6
17	200.3	120.5	19	3197.5	803.5
18	1971.0	1178.2	20	—	9436.9
19	22594.2	13960.8	21	—	118512.4

(a) Regularized method (seconds)

(b) Backtrack (seconds)

Table 4.2: Comparison between multi-core processors and GPUs for regularized and backtrack method

performance decreases quickly for higher values. This can be explained since more levels on the server generates smaller tasks; thus GPU use is not long enough to overlap memory exchanges.

CPU: Feed the GPUs and compute The first work of CPU cores is to prepare tasks for GPU so that we can generate overlapping between memory load and kernel computation. In this configuration using eight cores to generate GPU tasks under-uses CPU computation power. It is the reason why we propose to use some of the CPU cores to take part of the sub-problems treatment. Figure 4.11 represents computation time in relation with different task distributions between CPU and GPU. We experimentally demonstrated that only 4 or 5 CPU cores are enough to feed GPU, the other ones can be used to perform backtrack resolution in competition with GPUs.

4.2.5 Results

Regularized method results We now show the results obtained for our massively parallel scheme using the previous optimizations, comparing the computation times of successive instances of the Langford problem. These tests were performed on 20 nodes of the ROMEO supercomputer, hence 40 CPU/GPU machines.

The previous limit with Miller’s algorithm was $L(2, 19)$, obtained in 1999 after 2.5 years of sequential effort and at the same time after 2 months with a distributed approach[Mil99]. Our computation scheme allowed us to obtain it in less than 4 hours (Table 4.2a), this being not only due to Moore law progress.

Note that the computation is 1.6 faster with CPU+GPU together than using 8 CPU cores. In addition, the GPUs compute 200,000× more nodes of the search tree than the CPUs, with a faster time.

The computation time between two different consecutive instances being multiplied by 10 approximately, this could allow us to obtain $L(2, 20)$ in a reasonable time.

Backtracking on GPUs It appears at first sight that using backtracking on GPUs without any regularization is a bad idea due to threads synchronization issues. But in order to compare CPU and GPU computation power in the same conditions we decided to implement the original backtrack method on GPU (see figure 4.3) with only minor modifications. In these conditions we observe very efficient work of the NVIDIA scheduler, which perfectly handles threads desynchronization. Thus we use the same server-client distribution as in 4.2.3, each client generates masks for both CPU and GPU cores. The workload is then statically distributed on GPU and CPU cores. Executing the backtrack algorithm on a randomly chosen set of sub-problems allowed us to set the GPU/CPU distribution ratio experimentally to 80/20%.

The experiments were performed on 129 nodes of the ROMEO supercomputer, hence 258 CPU/GPU machines and one node for the server. Table 4.2b shows the results with this configuration. This method first allowed us to perform the computation of $L(2, 19)$ in less than 15 minutes, 15× faster than with the regularized method; then, we pushed the limitations of the

Miller algorithm up to $L(2, 20)$ in less than 3 hours and even $L(2, 21)$ in about 33 hours².

This first benchmark application provides a perfect example for the behavior of many-core accelerators confronted to irregular application. Even if the application does not seem to fit with the direct tree traversal, the results prove that if used in the right way performance can be achieved in this case.

4.3 Godfrey's algebraic method

The previous part presents the Miller algorithm for the Langford problem, this method cannot achieve bigger instances than the $L(2, 21)$. It allows us the target specific walls with memory and computation irregularities.

An algebraic representation of the Langford problem has been proposed by M. Godfrey in 2002. This example is perfect in our study to target computationally heavy context with irregular memory behavior. In this part we describe this algorithm and optimizations, and then our implementation on multiGPU clusters. As a side note, this implementation also allowed us to break a new world record on the computation time needed to solve the last instances, $L(2, 27)$ and $L(2, 28)$.

4.3.1 Method description

Consider $L(2, 3)$ and $X = (X_1, X_2, X_3, X_4, X_5, X_6)$. It proposes to modelize $L(2, 3)$ by:

$$\begin{aligned} F(X, 3) = & (X_1 X_3 + X_2 X_4 + X_3 X_5 + X_4 X_6) \times \\ & (X_1 X_4 + X_2 X_5 + X_3 X_6) \times \\ & (X_1 X_5 + X_2 X_6) \end{aligned} \quad (4.3)$$

In this approach each term represents a position of both cubes of a given color and a solution to the problem corresponds to a term developed as $(X_1 X_2 X_3 X_4 X_5 X_6)$; thus the number of solutions is equal to the coefficient of this monomial in the development. More generally, the solutions to $L(2, n)$ can be deduced from $(X_1 X_2 X_3 X_4 X_5 \dots X_{2n})$ terms in the development of $F(X, n)$.

If $G(X, n) = X_1 \dots X_{2n} F(X, n)$ then it has been shown that:

$$\sum_{(x_1, \dots, x_{2n}) \in \{-1, 1\}^{2n}} G(X, n)_{(x_1, \dots, x_{2n})} = 2^{2n+1} L(2, n) \quad (4.4)$$

So

$$\sum_{(x_1, \dots, x_{2n}) \in \{-1, 1\}^{2n}} \left(\prod_{i=1}^{2n} x_i \right) \prod_{i=1}^n \sum_{k=1}^{2n-i-1} x_k x_{k+i+1} = 2^{2n+1} L(2, n) \quad (4.5)$$

That allows to get $L(2, n)$ from polynomial evaluations. The computational complexity of $L(2, n)$ is of $O(4^n \times n^2)$ and an efficient big integer arithmetic is necessary. This principle can be optimized by taking into account the symmetries of the problem and using the Gray code: these optimizations are described below.

4.3.2 Method optimizations

Some works focused on finding optimizations for this arithmetic method[Jai05]. Here we explain the symmetric and computation optimizations used in our algorithm.

²Even if this instance has no interest since it is known to have no solution

Evaluation parity:

As $[F(-X, n) = F(X, n)]$, G is not affected by a global sign change. In the same way the global sign does not change if we change the sign of each pair or impair variable.

Using these optimizations we can set the value of two variables and accordingly divide the computation time and result size by four.

Symmetry summing:

In this problem we have to count each solution up to a symmetry; thus for the first pair of cubes we can stop the computation at half of the available positions considering

$$S'_1(x) = \sum_{k=1}^{n-1} x_k x_{k+2} \text{ instead of } S_1(x) = \sum_{k=1}^{2n-2} x_k x_{k+2}. \text{ The result is divided by 2.}$$

Sums order:

Each evaluation of $S_i(x) = \sum_{k=1}^{2n-i-1} x_k x_{k+i+1}$, before multiplying might be very important regarding to the computation time for this sum. Changing only one value of x_i at a time, we can recompute the sum using the previous one without global re-computation. Indeed, we order the evaluations of the outer sum using Gray code sequence. Then the computation time is considerably reduced.

Based on all these improvements and optimizations we can use the Godfrey method in order to solve huge instances of the Langford problem. The next section develops the main issues of our multiGPU architecture implementation.

4.3.3 Implementation details

In this part we present the specific adaptations required to implement the Godfrey method on a multiGPU architecture.

Optimized big integer arithmetic:

In each step of computation, the value of each S_i can reach $2n - i - 1$ in absolute value, and their product can reach $\frac{(2n-2)!}{(n-2)!}$. As we have to sum the S_i product on 2^{2n} values, in the worst case we have to store a value up to $2^{2n} \frac{(2n-2)!}{(n-2)!}$, which corresponds to 10^{61} for $n = 28$, with about 200 bits.

So we need few big integer arithmetic functions. After testing existing libraries like GMP for CPU or CUMP for GPU, we came to the conclusion that they implement a huge number of functionalities and are not really optimized for our specific problem implementation: product of "small" values and sum of "huge" values.

Finally, we developed a light CPU and GPU library adapted to our needs. In the summation, for example, as maintaining carries has an important time penalty, we have chosen to delay the spread of carries by using buffers: carries are accumulated and spread only when useful (for example when the buffer is full). Figure 4.12 represents this big integer handling.

This big integer library imposes many constraint on the accelerator memory. We conduct tests using simple and double precision for the basic unit. The carries propagation is also triggered when necessary only. This strategy implies random memory accesses to the words and irregular behavior between the threads.

Gray sequence in memory:

The Gray sequence cannot be stored in an array because it would be too large (it would contain 2^{2n} byte values). This is the reason why only one part of the Gray code sequence is stored in memory and the missing terms are directly computed from the known ones using arithmetic

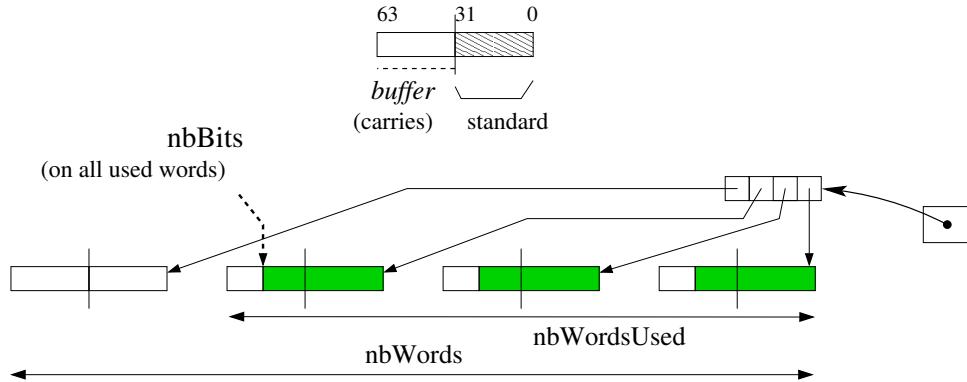


Figure 4.12: Big integer representation, 64 bits words

considerations. The size of the stored part of the Gray code sequence is chosen to be as large as possible to be contained in the processor's cache memory, the L1 cache for the GPUs threads: so the accesses are fastened and the computation of the Gray code is optimized. For an efficient use of the E5-2650 v2 ROMEO's CPUs, which disposes of 20 MB of level-3 cache, the CPU Gray code sequence is developed recursively up to depth 25. For the K20Xm ROMEO's GPUs, which dispose of 8 KB of constant memory, the sequence is developed up to depth 15. The rest of the memory is used for the computation itself.

Tasks generation and computation:

In order to perform the computation of the polynomial, two variables can be set among the $2n$ available. For the tasks generation we choose a number p of variables to generate 2^p tasks by developing the evaluation tree to depth p .

The tasks are spread over the cluster, either synchronously or asynchronously.

Synchronous computation: A first experiment was carried out with an MPI distribution of the tasks of the previous model. Each MPI process finds its tasks list based on its process id ; then converting each task number into binary gives the task's initialization. The processes work independently; finally the root process ($id = 0$) gathers all the computed numbers of solutions and sums them.

Asynchronous computation: In this case the tasks can be computed independently. As with the synchronous computation, the tasks' initializations are retrieved from their number. Each machine can get a task, compute it, and then store its result; then when all the tasks have been computed, the partial sums are added together and the total result is provided.

4.3.4 Experimental settings

This part presents the experimental context and methodology, and the way the experiments were carried out. This study has similar goals as for the Miller's resolution experiments.

Methodology:

We present here the way the experimental settings were chosen. Firstly we define the tasks distribution, secondly we set the number of threads per GPU block; finally, we set the CPU/GPU distribution.

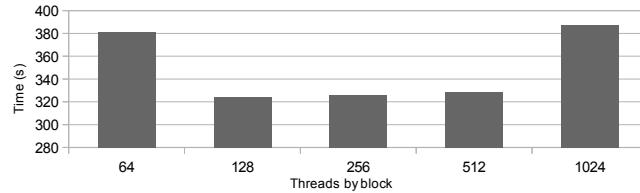
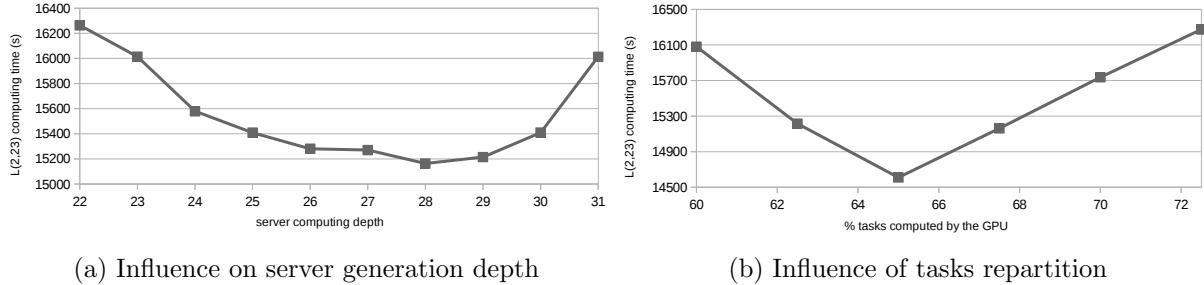
Figure 4.13: $L(2, 20)$, number of threads per block

Figure 4.14: Influences of repartitions of depths and CPU-GPU tasks

Tasks distribution depth: This value being set it is important to get a high number of blocks to maintain sufficient GPU load. Thus we have to determine the best number of tasks for the distribution. As presented in part 4.3.3 the number p of bits determines 2^p tasks. On the one hand, too many tasks are a limitation for the GPU that cannot store all the tasks in its 6GB memory. On the other hand, not enough tasks means longer tasks and too few blocks to fill the GPU grid. figure 4.14a shows that for the $L(2, 23)$ instance the best task number is with generation depth 28.

Number of threads per block: In order to take advantage of the GPU computation power, we have to determine the threads/block distribution. Inspired by our experiments with Miller's algorithm we know that the best value may appear at lower occupancy. We perform tests on a given tasks set varying the threads/block number and grid size associated. Figure 4.13 presents the tests performed on the $n = 20$ problem: the best distribution is around 128 threads per block.

CPU vs GPU distribution:

The GPU and CPU computation algorithm will approximately be the same. In order to take advantage of all the computational power of both components we have to balance tasks between CPU and GPU. We performed tests by changing the CPU/GPU distribution based on simulations on a chosen set of tasks. Figure 4.14b shows that the best distribution is obtained when the GPU handles 65% of the tasks. This optimal load repartition directly results from the intrinsics computational power of each component; this repartition should be adapted if using a more powerful GPU like Tesla K40 or K80.

Computing context:

As presented in part 2.5.1, we used the ROMEO supercomputer to perform our tests and computations. On this supercomputer SLURM[JG03] is used as a reservation and job queue manager. This software allows two reservation modes: a static one-job limited reservation or the opportunity to dynamically submit several jobs in a Best-Effort manner.

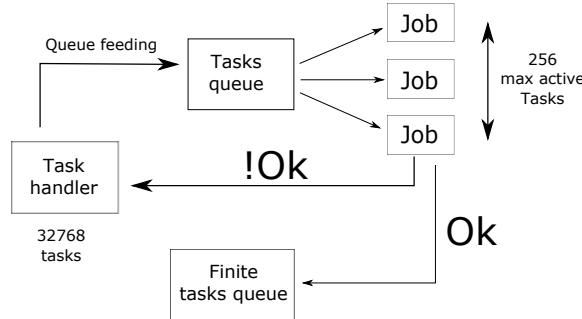


Figure 4.15: Best-effort distribution

Static distribution: In this case we used the synchronous distribution presented in 4.3.3. We submitted a reservation with the number of MPI processes and the number of cores per process. This method is useful to get the results quickly if we can get at once a large amount of computation resources. It was used to perform the computation of small problems, and even for $L(2, 23)$ and $L(2, 24)$.

As an issue, it has to be noted that it is difficult to quickly obtain a very large reservation on such a shared cluster, since many projects are currently running.

Best effort: SLURM allows to submit tasks in the specific Best-Effort queue, which does not count in the user *fair-share*. In this queue, if a node is free and nobody is using it, the reservation is set for a job in the best effort queue for a minimum time reservation. If another user asks for a reservation and requests this node, the best effort job is killed (with, for example, a SIGTERM signal). This method, based on asynchronous computation, enables a maximal use of the computational resources without blocking for a long time the entire cluster.

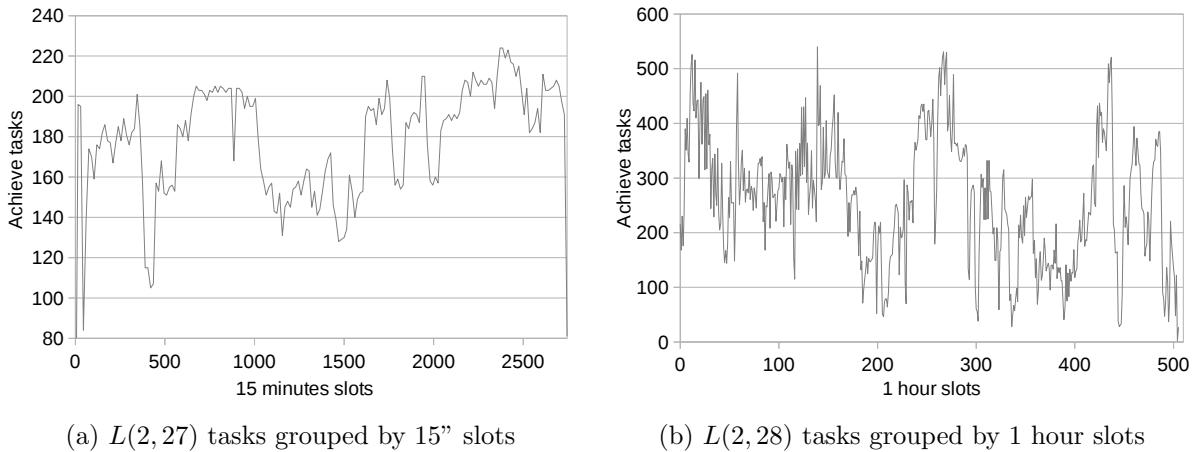
For $L(2, 27)$ and even more for $L(2, 28)$ the total time required is too important to use the whole machine off a challenge period, thus we chose to compute in a Best-Effort manner. In order to fit with this submission method we chose a reasonable time-per-task, sufficient to optimize the treatments with low loading overhead, but not too long so that killed tasks are not too penalizing for the global computation time. We empirically chose to run 15-20 minute tasks and thus we considered $p = 15$ for $n = 27$ and $p = 17$ for $n = 28$.

The best effort based algorithm is presented on figure 4.15. The task handler maintains a maximum of 256 tasks in the queue; in addition the entire process is designed to be fault-tolerant since killed tasks have to be launched again. When finished, the tasks generate an output containing the number of solutions and computation time, that is stored as a file or database entry. At the end the outputs of the different tasks are merged and the global result can be provided.

4.3.5 Results

After these optimizations and implementation tuning steps, we conducted tests on the ROMEO supercomputer using best-effort queue to solve $L(2, 27)$ and $L(2, 28)$. We started the experiment after an update of the supercomputer, that implied a cluster shutdown. Then the machine was restarted and was about 50% idle for the duration of our challenge. The computation lasted less than 2 days for $L(2, 27)$ and 23 days for $L(2, 28)$. The following describes performances considerations.

Computing effort - For $L(2, 27)$, the effective computation time of the 32,768 tasks was about 30 million seconds (345.4 days), and 165,000" elapsed time (1.9 days); the average time of the tasks was 911", with a standard deviation of 20%. For the $L(2, 28)$ 131,072 tasks the total computation time was about 1365 days (117 million seconds), as 23 day elapsed time; the tasks lasted 1321" on average with a 12% standard deviation.

Figure 4.16: Task repartition for $L(2, 27)$ and $L(2, 28)$

Best-effort overhead - With $L(2, 27)$ we used a specific database to maintain information concerning the tasks: 617 tasks were aborted [by regular user jobs] before finishing (1.9%), with an average computing time of 766" (43% of the maximum requested time for a task). This consumed 472873", which overhead represents 1.6% of the effective computing effort.

Cluster occupancy - Figure 4.16a presents the tasks resolution over the two computation days for $L(2, 27)$. The experiment elapse time was 164700" (1.9 days). Compared to the effective computation time, we used an average of 181.2 machines (CPU-GPU couples): this represents 69.7% of the entire cluster.

Figure 4.16b presents the tasks resolution flow during the 23 days computation for $L(2, 28)$. We used about 99 machines, which represents 38% of the 230 available nodes.

For $L(2, 27)$, these results confirm that the computation took great advantage of the low occupancy of the cluster during the experiment. This allowed us to obtain a weak best-effort overhead, and an important cluster occupancy. Unfortunately for $L(2, 28)$ on such a long period we got a lower part of the supercomputer dedicated to our computational project. Thus we are confident in good perspectives for the $L(2, 31)$ instance if computed on an even larger cluster or several distributed clusters.

4.4 Conclusion

This first benchmark presents two methods to solve the Langford pairing problem on multi-GPU clusters. Those methods are presented as the Miller's and Godfrey's algorithms.

4.4.1 Miller's method: irregular memory + computation

In this first implementation we showed that the accelerator can target irregularity in memory and computation. The tree traversal, even with branch cutting, gives us excellent results on many-core architecture. They GPUs handle 80% of the computation effort. Also as any combinatorial problem can be represented as a CSP, the Miller algorithm can be seen as general resolution scheme based on the backtrack tree browsing. A three-level tasks generation allows to fit the multiGPU architecture. MPI or Best-Effort are used to spread tasks over the cluster, OpenMP for the CPU cores distribution and then CUDA to take advantage of the GPU computation power. We were able to compute $L(2, 20)$ with this regularized method and to get an even better time with the basic backtrack. This proves the proposed approach and also exhibits that the GPU scheduler is very efficient at managing highly divergent threads.

4.4.2 Godfrey's method: irregular memory + heavy computation

We also presented the Godfrey's method which target irregular memory accesses but also heavy computational behavior. The results shows that the many-core version completely exceed the classical processor best performances. The GPU handle 65% of the computation effort. In addition we beat the Langford limits using multi-GPUs. In order to use the supercomputer ROMEO, which is shared by a large scientific community, we have implemented a distribution that does not affect the machine load, using a best-effort queue. The computation is fault-tolerant and totally asynchronous. The utilization of this technology also show the reliability of nowadays accelerators technologies. Indeed, they can be used at demand on specific tasks without specific warm-up.

Langford problem results: This work also enabled us to compute $L(2, 27)$ and $L(2, 28)$ in respectively less than 2 days and 23 days on the University of Reims ROMEO supercomputer. This is the fastest time on those problems nowadays. The total number of solutions is:

$$\begin{aligned} L(2,27) &= 111,683,611,098,764,903,232 \\ L(2,28) &= 1,607,383,260,609,382,393,152 \end{aligned}$$

This first benchmark implementation is clearly in favor of hybrid architecture. The many-core architecture shows a perfect handling of irregularity and heavy computations.

Chapter 5

Communication Wall: Graph500

5.1 Introduction

In order to face the communication wall in our metric for accelerators, we choose the Graph500 problem. This benchmark is based on huge tree traversal through a randomly generated graph. We already work on this kind of example with the first implementation of the Langford algorithm. The Graph500 push this example to its limits using terabyte to petabytes of data to represent the graph on which the traversal is executed. In this case the computation is absent or just reduce to tests on datum. This metric targets directly the memory and communication wall in irregular case.

In this part we present the benchmark itself, from the graph generation to the traversal. We focus on the BFS part, we do not work on the latest Graph500 using SSSP. We explain why this benchmark is perfect to target communication wall and memory wall. We present our implementation on GPUs and the results compared to the multi-core processor version.

5.1.1 Breadth First Search

The most commonly used search algorithms for graphs are Breadth First Search (BFS) and Depth First Search (DFS). Many graph analysis methods, such as the finding of shortest path for unweighted graphs and centrality, are based on BFS.

As it is a standard approach method in graph theory, its implementation and optimization require extensive work. This algorithm can be seen as frontier expansion and exploration. At each step the frontier is expanded with the unvisited neighbors.

The sequential and basic algorithm is well known and is presented on Algorithm 1.

This algorithm is presented on figure 5.1. At each step from the current queue we search through the neighbors of nodes. All the new nodes, not yet traversed, are added in the queue

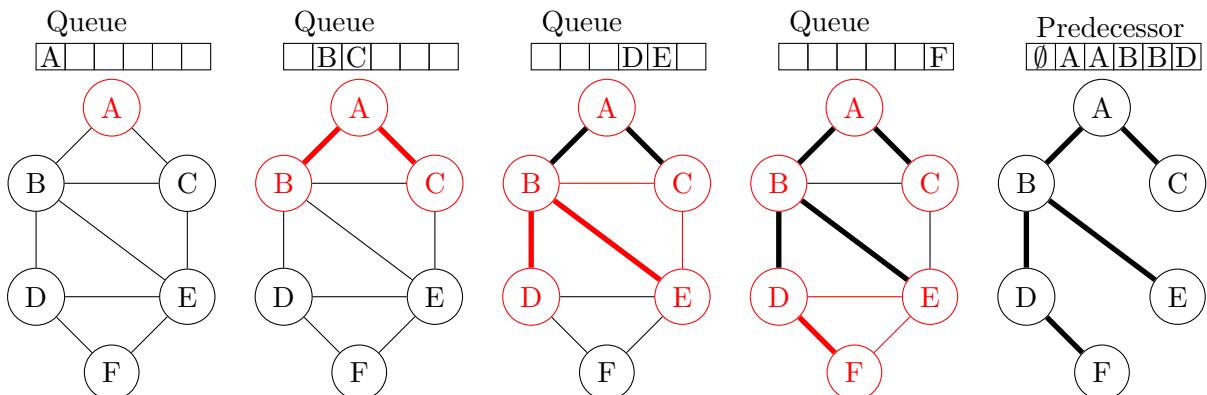


Figure 5.1: Example of Breadth First Search in an undirected graph

Algorithm 1 Sequential Breadth First Search algorithm

```

1: function COMPUTE_BFS( $G = (V, E)$ : graph representation,  $v_s$ : source vertex,  $In$ : current
   level input,  $Out$ : current level output,  $Vis$ : already visited vertices)
2:    $In \leftarrow \{v_s\}$ ;
3:    $Vis \leftarrow \{v_s\}$ ;
4:    $P(v) \leftarrow \perp \forall v \in V$ ;
5:   while  $In \neq \emptyset$  do
6:      $Out \leftarrow \emptyset$ 
7:     for  $u \in In$  do
8:       for  $v|(u, v) \in E$  do
9:         if  $v \notin Vis$  then
10:           $Out \leftarrow Out \cup \{v\}$ ;
11:           $Vis \leftarrow Vis \cup \{v\}$ ;
12:           $P(v) \leftarrow u$ ;
13:        end if
14:      end for
15:    end for
16:     $In \leftarrow Out$ 
17:  end while
18: end function

```

for the next step. We keep the information of neighbors exploration in order to recreate the predecessor array.

This algorithm is very famous thanks to its use in many applications but also thanks to the world supercomputer ranking called Graph500¹. This benchmark is designed to measure the performance on very irregular problems like BFS on a large scale randomized generated graph. The first Graph500 list was released in November 2010. The last list, issued in November 2017, is composed of 235 machines ranked using a specific metric: Traversed Edges Per Second, denoted as TEPS. The aim is to perform a succession of 64 BFS on a large scale graph in the fastest possible way. Then the ratio of edges traversed per the time of computation is used to rank the machines.

This benchmark is more representative of communication and memory accesses than computation itself. Other benchmarks can be used to rank computational power such as LINPACK for the TOP500 list. Indeed the best supercomputers (K-Computer, Sequoia, Mira, ...) on the ladder have a very specific communication topology and sufficient memory, and are large enough to quickly visit all the nodes of the graph.

This benchmark is conduct using GPUs as accelerators. There are many CPU algorithms available, which are listed on the Graph500 website. In order to rank the ROMEO supercomputer we had to create a dedicated version of the Graph500 benchmark in order to fit the supercomputer architecture. As this supercomputer is accelerated by GPUs, three successive approaches had to be applied: first create an optimized CPU algorithm; second provide a GPU specific version and third take advantage of both CPU and GPU computation power.

The first section performs a survey of graph representation and analysis; it also describes some specific implementations. The second section describes the Graph500 protocol and focuses on the Kronecker graph generation method and the BFS validation. The third section presents the chosen methods to implement graph representation and work distribution over the supercomputer nodes. It particularly focuses on the interest of a hybrid CSR and CSC representation. We compare the results for different graph scales and load distributions.

¹<http://www.graph500.org>

5.2 Existing methods

The most efficient algorithm to compute BFS traversal is used and detailed in [CPW⁺12]. It uses a 2D partition of the graph which will be detailed later. This algorithm is used on the BlueGene/P and BlueGene/Q architectures but can be easily adapted to any parallel cluster.

We use another key study in order to build our Graph500 CPU/GPU implementation. [MGG15] proposes various effective methods on GPU for BFS. Merrill & al. explain and test a few efficient methods to optimize memory access and work sharing between threads on a large set of graphs. It focuses on Kronecker graphs in particular. First they propose several methods for neighbor-gathering with a serial code versus a warp-based and a CTA-based approach. They also use hybridization of these methods to reach the performance level. In a second part they describe the way to perform label-lookup, to check if a vertex is already visited or not. They propose to use a bitmap representation of the graph with texture memory on the GPU for fast random accesses. In the last phase, they propose methods to suppress duplicated vertices generated during the neighbor exploration phase. Then based on these operations they propose *expand-contract*, *contract-expand*, *two-phase* and finally *hybrid* algorithms to adapt the method with all the studied graph classes. The last part they propose a multi-GPU implementation. They use a 1D partition of the graph and each GPU works on its subset of vertices and edges.

In [FDB⁺14], a first work is proposed to implement a multi-GPU cluster version of the Graph500 benchmark. The scheme used in their approach is quite similar to the one in our study but with a more powerful communication network, namely FDR InfiniBand.

In our work we focus on the GPUDirect usage on the ROMEO supercomputer.

5.3 Environment

As previously mentioned, a CPU implementation is available on the official Graph500 website. A large range of software technology is covered with MPI, OpenMP, etc. All these versions use the same generator and the same validation pattern which is described in this part below.

The Graph500 benchmark is based on the following stages:

- *Graph generation.* The first step is to generate the Kronecker graph and mix the edges and vertices. The graph size is chosen by the user (represented as a base-2 number of vertices). The *EDGEFACTOR*, average ratio of edges by vertex, is always 16. Self-loop and multiple edges are possible with Kronecker graphs. Then 64 vertices for the BFS are randomly chosen. The only rule is that a chosen vertex must have at least one link with another vertex in the graph. *This stage is not timed*;
- *Structure generation.* The specific code part begins here. Based on the edge list and its structure the user is free to distribute the graph over the machines. In a following section we describe our choices for the graph representation. *This stage is timed*;
- *BFS iterations.* This is the key part of the ranking. Based on the graph representation, the user implements a specific optimized BFS. Starting with a root vertex the aim is to build the correct BFS tree (up to a race condition at every level), storing the result in a predecessor list for each vertex;
- *BFS verification.* The user-computed BFS is validated. The number of traversed edges is determined during this stage.

The process is fairly simple and sources can be found at <http://www.graph500.org>. The real problem is to find an optimized way to use parallelism at several levels: node distribution, CPU and GPU distribution and then massive parallelism on accelerators.

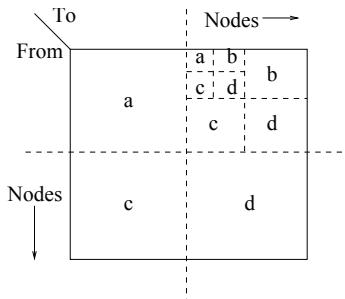


Figure 5.2: Kronecker generation scheme based on edge probability

5.3.1 Generator

The *Kronecker graphs*, based on Kronecker products, represent a specific graph class imposed by the Graph500 benchmark. These graphs represent realistic networks and are very useful in our case due to their irregular aspect [LCK⁺10]. The main generation method uses the Kronecker matrix product. Based on an initiator adjacency matrix K_1 , we can generate a Kronecker graph of order $K_1^{[k]}$ by multiplying K_1 by itself k times. The Graph500 generator uses Stochastic Kronecker graphs, avoiding large scale matrix multiplying, to generate an edge list which is utterly mixed (vertex number and edge position) to avoid locality.

As presented on figure 5.2, the generation is based on edge presence probability on a part of the adjacency matrix. For the Graph500 the probabilities are $a = 0.57$, $b = c = 0.19$ and $d = 0.05$. The generator handle can be stored in a file or directly split in the RAM memory of each process. The first option is not very efficient and imposes a lot of I/O for the generation and verification stage but can be very useful for large scale problems. The second option is faster but uses a part of the RAM thus less ressources are available for the current BFS execution.

5.3.2 Validation

The validation stage is completed after the end of each BFS. The aim is to check if the tree is valid and if the edges are in the original graph. This is why we must keep a copy of the original graph in memory, file or RAM. This validation is based on the following stages, presented on the official Graph500 website. First, the BFS tree is a tree and does not contain cycles. Second, each tree edge connects vertices whose BFS levels differ by exactly one. Third, every edge in the input list has vertices with levels that differ by at most one or that both are not in the BFS tree. Finally, the BFS tree spans an entire connected component's vertices, and a node and its parent are joined by an edge of the original graph.

In order to meet the Graph500 requirements we use the proposed verification function provided in the official code.

5.4 BFS traversal

In this section we present the actual algorithm we used to perform the BFS on a multi-GPU cluster. In a first part we introduce the data structure; then we present the algorithm and the optimizations used.

5.4.1 Data structure

We performed tests of several data structures. In a first work we tried to work with bitmap. Indeed the regularity of computation can fit very well with the GPU architecture. But this representation imposes a significant limitation on the graph size. This representation is used on the BlueGene/Q architecture. Indeed they have some specific hardware bit-wise operations

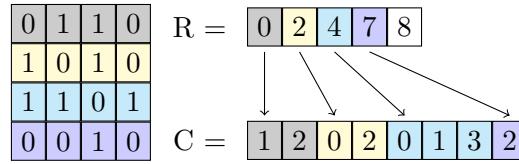


Figure 5.3: Compressed Sparse Row example

implemented in their processors and have a large amount of memory, allowing them to perform very large scale graph analysis.

In a second time we used common graph representations, Compressed Sparse Row (CSR) and Compressed Sparse Column (CSC) representation, which fit very well with sparse graphs such as the Graph500 ones.

Figure 5.3 is an example illustrating the CSR compression. The M adjacency matrix represents the graph. R vector contains the cumulative number of neighbors for each vertex, of size ($\#vertices + 1$). C , of size ($\#edges$), is, for each index of R , the edges of a vertex. This representation is very compact and very efficient to work with sparse graphs.

5.4.2 General algorithm

When looking at the latest Graph500 list we see that the best machines are the BlueGene ones. We count about 26 BlueGene/Q and BlueGene/P machines in the first 50 machines. This is due to a quite specific version of the BFS algorithm proposed in [CPW⁺12]. It proposes a very specific 2D distribution for parallelism and massive use of the 5D torus interconnect.

In the BFS algorithm, like other graph algorithms, parallelism can take several shapes. We can split the vertices into partitions using 1D partition. Each thread/machine can then work on a subset of vertices. The main issue with this method is that the partitions are not equal since the number of edges per vertex can be very different; moreover in graphs like Kronecker ones where some vertices have a very high degree compared to other ones. Thus we are confronted with a major load balancing problem.

In [CPW⁺12] they propose a new vision of graph traversal, here BFS, on distributed-memory machines. Instead of using standard 1D distribution their BFS is based on a 2D distribution. The adjacency matrix is split into blocks of same number of vertices. If we consider $l \times l$ blocks $A_{i,j}$ we can split the matrix as follows:

$$M = \begin{bmatrix} A_{0,0} & A_{0,1} & \cdots & A_{0,l-1} \\ A_{1,0} & A_{1,1} & \cdots & A_{1,l-1} \\ \vdots & \vdots & \ddots & \vdots \\ A_{l-1,0} & A_{l-1,1} & \cdots & A_{l-1,l-1} \end{bmatrix}$$

Each bloc $A_{x,y}$ is a subset of edges. We notice that blocks $A_{0,l-1}$ and $A_{l-1,0}$ have the same edges but in a reverse direction for undirected graphs. Based on this distribution they use *virtual processors*, which are either machines or nodes, each associated with a block. This has several advantages. First we reduce the load balancing overhead and a communication pattern can be set up. Indeed each column shares the same *in_queue* and each row will generate an *out_queue* in the same range. Thus for all the exploration stages, communications are only on line and we just need a column communication phase to exchange the queues for the next BFS iteration. Algorithm 2 presents the BlueGene/Q and BlueGene/P parallel BFS.

This algorithm is presented in algorithm 3 and is based on the exploration phase, denoted by *ExploreFrontier()*. It performs the exploration phase independently on all the machines. Then several communication phases follow. The first two phases are performed on the same processes line. The last one is performed on a processes column.

Algorithm 3 Algorithm for tree traversal presented for BlueGene

```

1:  $Vis_{i,j} \leftarrow In_{i,j}$ 
2:  $P(N_{i,j}, v) \leftarrow \perp$  for all  $v \in R_{i,j}^{1D}$ 
3: if  $v_s \in R_{i,j}^{1D}$  then
4:    $P(N_{i,j}, v_s) \leftarrow v_s$ 
5: end if
6: while true do
7:    $(Out_{i,j}, Marks_{i,j}) \leftarrow \text{ExploreFrontier}();$ 
8:    $done \leftarrow \bigwedge_{0 \leq k, l \leq n} (Out_{k,l} = \emptyset)$ 
9:   if  $done$  then
10:    exit loop
11:   end if
12:   if  $j = 0$  then
13:      $prefix_{i,j} = \emptyset$ 
14:   else
15:     receive  $prefix_{i,j}$  from  $N_{i,j-1}$ 
16:   end if
17:    $assigned_{i,j} \leftarrow Out_{i,j} \setminus prefix_{i,j}$ 
18:   if  $j \neq n - 1$  then
19:     send  $prefix_{i,j} \cup Out_{i,j}$  to  $N_{i,j+1}$ 
20:   end if
21:    $Out_{i,j} \leftarrow \bigcup_{0 \leq k \leq n} Out_{i,k}$ 
22:   WritePred()
23:    $Vis_{i,j} \leftarrow Vis_{i,j} \cup Out_{i,j}$ 
24:    $In_{i,j} \leftarrow Out_{j,i}$ 
25: end while

```

Iteration	Top-down	Bottom-up	Hybridization
0	27	22 090 111	27
1	8 156	1 568 798	8 156
2	3 695 684	587 893	587 893
3	19 565 465	12 586	12 586
4	214 578	8 256	8 256
5	5 865	1 201	1 201
6	12	156	12
Total	23,489,787	24,269,001	618,131

Table 5.1: BFS directions change from top-down to bottom-up

- On line 15, an exclusive scan is performed for each process on the same line, all the $A_{i,x}$ with $i \in [0, l - 1]$. This operation allows us to know which vertices have been discovered in this iteration.
- On line 19, a broadcast of the current *out_queue* is sent to the processes on the same line. With this information they would be able to update the predecessor list only if they are the first parent of a vertex.
- On line 24, a global communication on each column is needed to prepare the next iteration. The aim is to replace the previous *in_queue* by the newly computed *out_queue*.

Two functions are not specified: *ExploreFrontier()* converts the *in_queue* into *out_queue* taking account of the previously visited vertices; *WritePred()* aims to generate the BFS tree and therefore store the predecessor list. In this algorithm the predecessor distribution is still in 1D to avoid vertex duplication. This part can be done using RDMA communication to update predecessor value or with traditional MPI all-to-all exchanges. It can be done during each iteration stage or at the end of the BFS but this requires using a part of the memory to store this data.

This algorithm, which is the basis of many implementations, is the main structure of our distribution.

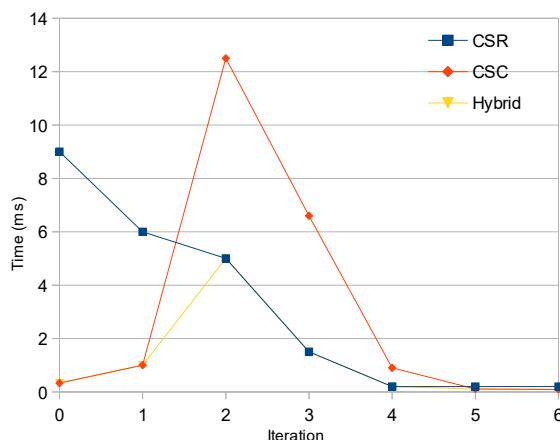
5.4.3 Direction optimization

In order to get an optimized computation in terms of TEPS we decided to sacrifice a small part of the memory for storing both the CSC and CSR representations. Indeed during the different BFS iterations the *in_queue* size varies a lot and, taking this into account, it is wiser to perform exploration from *top-down* or *bottom-up*. So, as proposed in [BAP13], we perform a direction-optimized BFS.

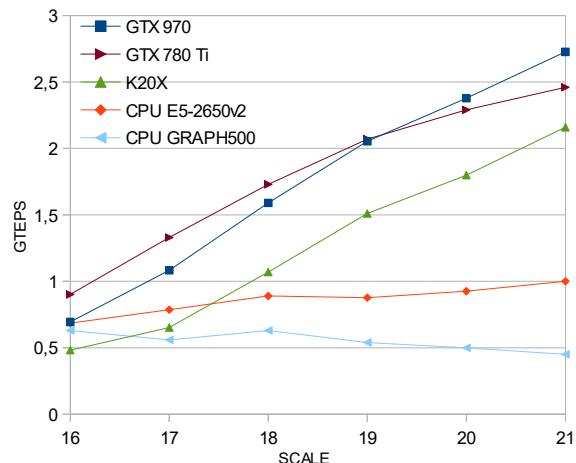
In the first case, *top-down*, we start from the vertices in the *in_queue* and check all the neighbors verifying each time if this neighbor has ever been visited. Then if not, it is added to the *out_queue*. When the *in_queue* is sparse, like for the first and latest iterations, this method is very efficient. In the second case, *bottom-up*, we start the exploration by the not-yet-visited vertices and verify if there is a link between those vertices and the *in_queue* ones. If yes, the not-yet-visited vertex is added to the *out_queue*. Table 5.1 shows the advantages of switching from top-down to bottom-up regarding the number of edges traversed. Figure 5.4a presents the two approaches, which the time visiting all the edges, and the benefits of their hybridization.

5.4.4 GPU optimization

In algorithm 2, two parts are not developed. namely *ExploreFrontier()* and *WritePred()*. Indeed these phases are optimized using the GPU. Based on the Merill et al. implementation, the algorithm is optimized to use the shared memory and the texture memory of the GPU. For our



(a) CSR and CSC approach comparison. On a 6 iterations BFS, the time with the two method is compared. The hybridization just takes the best time of each method



(b) Single CPU and accelerators comparison. CPU Graph500 represent the best implementation proposed by the Graph500 website.

version we decided to keep the bitmap implementation for the communications and the queues. So we have to fit the CSR and CSC implementations. On algorithm 4 we present the CSR algorithm; CSC is based on the same approach but starting from the *visited* queue.

In the CSR version each warp is attached to a 32 bit word of the *in_queue* bitmap. Then if this word is empty the whole warp is released; if it contains some vertices, the threads collaborate to load the entire neighbor list. Then they access the coalescent area in the main memory to load the neighbor list. A texture memory is used to accelerate the verification concerning this vertex. Indeed this memory is optimized to be randomly accessed. Then the vertex is added in the bitmap *out_queue*.

5.4.5 Communications

Based on the algorithm 2 communications pattern, we first used MPI with the CPU transferring the data. But the host-device transfer time between the CPU and the GPU was too time-consuming. In order to accelerate the transfers between the GPUs, we used a specific GPU MPI-aware library. This library allows direct MPI operations from the memory of one GPU to another and also implements direct GPU collective operations. GPUDirect can be used coupled with this library. In the last version we used this optimization with GDRCopy.

5.5 Results

5.5.1 CPU and GPU comparison

On figure 5.4b we present the single node implementation. Here we compare the best CPU implementation proposed by the Graph500 benchmark with our GPU implementation. On our cluster we worked with K20Xm GPUs. The GPU result is twice times better than the CPU one. We also carried out tests on some "general public" GPUs like GTX980 and GTX780Ti. The result is better on these GPUs because they do not implement the ECC memory and do not provide double precision CUDA cores. Indeed all the cores can be used for the Exploration phase.

5.5.2 Strong and weak scaling

On figure 5.5b and figure 5.5a we see the result of strong and weak scaling. In the strong scaling we used a *SCALE* of 21 for different numbers of GPUs. The application scales up to

Algorithm 4 Exploration kernel based on CSR

```

1: Constants:
2:  $NWARP$ : number of WARPS per block
3:
4: Variables:
5:  $pos\_word$ : position of the word in  $in\_queue$ 
6:  $word$ : value of the word in  $in\_queue$ 
7:  $lane\_id$ : thread ID in the WARP
8:  $warp\_id$ : WARP number if this block
9:  $comm[NWARP][3]$ : shared memory array
10:  $shared\_vertex[NWARP]$ : vertex in shared memory
11:
12: Begin
13: if  $word = 0$  then
14:   free this WARP
15: end if
16: if  $word \& 1 << lane\_id$  then
17:    $id\_sommet \leftarrow pos\_word * 32 + lane\_id$ 
18:    $range[0] \leftarrow C[id\_sommet]$ 
19:    $range[1] \leftarrow C[id\_sommet + 1]$ 
20:    $range[2] \leftarrow range[1] - range[0]$ 
21: end if
22: while  $_any(range[2])$  do
23:   if  $range[2]$  then
24:      $comm[warp\_id][0] \leftarrow lane\_id$ 
25:   end if
26:   if  $comm[warp\_id][0] \leftarrow lane\_id$  then
27:      $comm[warp\_id][0] \leftarrow range[0]$ 
28:      $comm[warp\_id][0] \leftarrow range[1]$ 
29:      $range[2] \leftarrow 0$ 
30:      $share\_vertex[warp\_id] = id\_sommet$ 
31:   end if
32:    $r\_gather \leftarrow comm[warp\_id][0] + lane\_id$ 
33:    $r\_gather\_end \leftarrow comm[warp\_id][2]$ 
34:   while  $r\_gather < r\_gather\_end$  do
35:      $voisin \leftarrow R[r\_gather]$ 
36:     if  $not \in tex\_visited$  then
37:       Adding in  $tex\_visited$ 
38:        $AtomicOr(out\_queue,voisin)$ 
39:     end if
40:      $r\_gather \leftarrow r\_gather + 32$ 
41:   end while
42: end while

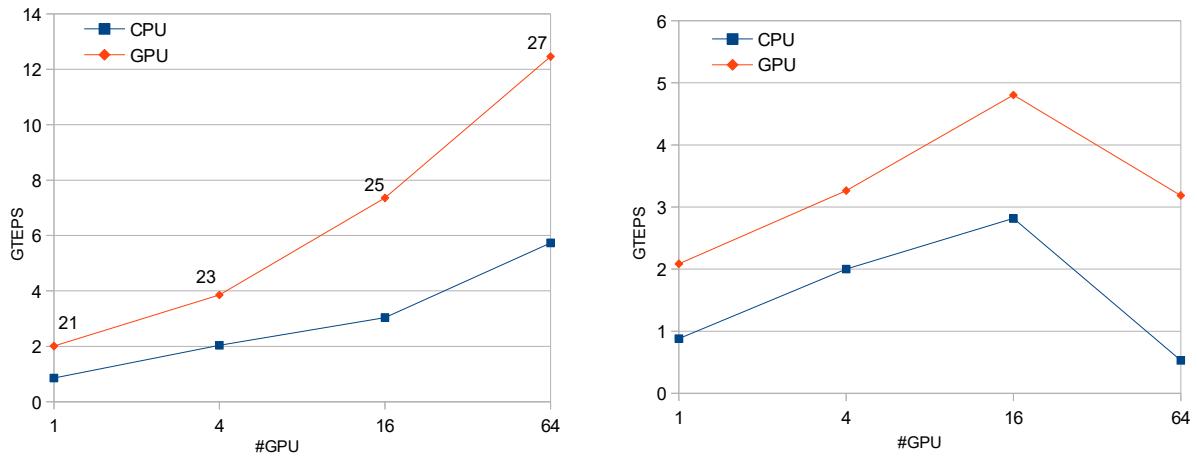
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16 GPUs but then the data exchanges are too penalizing; performance for 64 GPUs is lower. Indeed as the problem scale does not change, the computational part is reduced compared to the communication one. Using 16 GPUs we were able to perform up to 4.80 GTEPS.

For the weak scaling, the *SCALE* evolves with the number of GPUs. So the computation part grows and the limitation of communications is reduced. On figure 5.5a, the problem *SCALE* is presented on each point. With our method we were able to reach up to 12 GTEPS using this scaling.

5.5.3 Communications and GPUDirect

Each node of the ROMEO supercomputer is composed of two CPU sockets and two GPUs, named GPU 0 and GPU 1. Yet the node just has one HCA (Host Channel Adapters), linked with CPU 0 and GPU 0. In order to use this link GPU 1 has to pass through a Quick Path Interconnect link (QPI) between the two CPU sockets. This link considerably reduces the bandwidth available for node-to-node communication. Another problem is that the two GPUs have to share the same HCA for their communication.



(a) CPU *vs* GPU weak scaling. The number of CPUs is the same as the number of GPUs.

(b) CPU *vs* GPU strong scaling. The *SCALE* is showed on the GPU line. The number of CPUs is the same as the number of GPUs.

Figure 5.5: Weak and Strong scaling between CPU and GPU

On figure 5.6, the tests are based on the GPU-only implementation. First we worked with the two GPUs of the nodes. We were able to perform up to to *SCALE* 29 with 12 GTEPS. The GPUDirect implementation does not allow the communication with a QPI link. So in order to compare the results, we used only the GPU 0 of each node of the supercomputer. Based on our algorithm implementation we need to use a number 2^{2n} of GPUs. Then the tests on figure 5.6 are for 256 GPUs (with GPU 0 and GPU 1) and with 64 GPUs (using just GPU 0 only). Thus we were able to reach a better value of GTEPS. As the major limitation is the communications stage, using only GPU 0 allowed us to obtain about 13.70 GTEPS on the ROMEO supercomputer.

5.6 Conclusions

The Graph500 is already a benchmark and focus on memory and communication wall in an irregular behavior. We presented an optimized implementation of the Graph500 benchmark for the ROMEO multi-GPU cluster for the purpose of our metric to emphasize behavior of hybrid architectures. It is based on the BlueGene/Q algorithm and GPU optimization for BFS traversal by Merrill et al. This work highlights different key points. First, we have chosen a hybrid memory

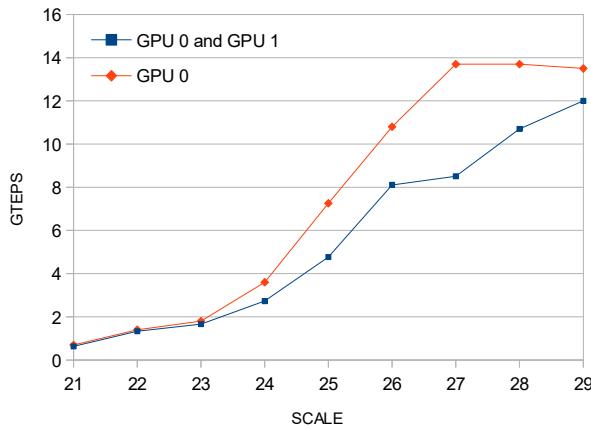


Figure 5.6: Full node GPUs *vs* GPU 0. The GPU 0 implementation not use the QPI link of the two CPU socket.

representation of graphs using both CSR and CSC. Although this representation requires more memory, it significantly reduces the computation workload and allows us to achieve outstanding performance. Second, the inter-node and intra-node communication is a critical bottleneck. Each compute node has two GPUs, however only one shares the same PCIe bridge with the Infiniband HCA that allows to take advantage of the GPUDirect technology. Third, due to the low compute power needed for BFS traversal, we get better performance by fully loading GPUs. Otherwise communication time cannot be overlapped with computation time. Thus to achieve the best performance we had to use only half of each node. Finally, using all these optimizations, we achieved satisfactory results. Indeed, by using GPUDirect on 64 GPUs, we are able to achieve 13,70 GTEPS. In this configuration CPUs are only used to synchronize GPUs kernels. All the communications are directly GPU to GPU using a CUDA-aware MPI library and GPUDirect.

These results have been published in the Graph500 list of November 2016 list. The ROMEO supercomputer was ranked 105th.

In addition to the previous benchmarks proposed in our thesis, the Graph500 complete the communication and memory irregular behavior. It shows the benefit of using many-core architectures in this context allowing twice better results using accelerators than CPUs.

Conclusion

In this part we showed the real advantage of accelerators, hybrid architectures, toward classical processors in HPC environment. In the two examples presented in this part we confronted both architectures to complex problems representing characteristic walls: irregular applications in computation and communications. In the first one, with the problem of Langford, we worked on an irregular and computationally heavy application that does not require much communications. The second one, the Graph500 BFS, was based on irregular communication over irregular memory usage. In both cases we showed better results using accelerator, in this case GPU, compared to classical multi-core processors systems.

5.6.1 Computational wall

We studied the Langford problem under two methods of resolution. In the first one, the Miller algorithm, the resolution was based on a tree traversal. We showed that even using the irregular algorithm directly on the GPU gave us way better results than on multi-core processors. We showed an acceleration of quad times using the GPUs with the backtrack method.

For the second method, the Godfrey algorithm, we were able to beat a new speed record for the last instances $L(2, 27)$ and $L(2, 28)$. We used the whole ROMEO supercomputer and were able to recompute them in 23 days using best-effort on the cluster: an average of 38% of the machine. This result can be theoretically reduced to a maximum of 10 days by using the whole cluster in the same time, using a linear scaling.

5.6.2 Communication wall

Several aspects of the Graph500 BFS makes it a good metric in our study. The graph generated is completely random and we cannot know in advance the exact number of edges and thus the perfect behavior for distribute the data. During the search of the BFS algorithm the memory is completely traversed with an irregular behavior due to the random generation of the graph.

In order to get performances we imposed regularization over our data. The Compressed Sparse Row and Compressed Sparse Column compression methods were used and the communications were based on bitmap transfers.

We showed that despite of the irregularity downside we were able to provide an efficient GPU algorithm, faster than the CPU algorithm and the reference code from Graph500 itself. We provided an acceleration of two times using our CPU algorithm and quad times using our GPU algorithm.

5.6.3 Reaching performances on accelerators

From those two metrics we extracted the main factors that leads us the performances on accelerators like GPU.

Regularization vs high number of tasks

We showed in both cases that the regularization of the tasks to fit the GPU execution model, based on synchronized execution, is not always the best way to reach performances. Indeed, if the number of tasks to solve on the GPU is high enough the SIMD models allows all the computational core to stay busy while fetching data. The number of blocks in the grid and threads per blocks have to be very high to allow the coordinator to switch from WARPS and cover the data fetching time.

Memory usage

All the kind of memory have to be consider and have their own interests. We used the constant memory to store the Gray code in the Langford problem. Despite its small amount of space it was a critical factor avoiding necessary re-computations. The texture memory, perfect for irregular data fetching, was a perfect area to store the neighbors informations for the Graph500 problem. Another very important part of the work is to focus on shared memory usage. Using the same data fetching instruction for all the threads of a WARP and provide shared memory informations like for the neighbor search will lead to performances. Another care have to be taken while considering the bank conflict during fetching data.

Communication/computation overlapping

For accelerator programming, and especially GPUs, the execution on the device is asynchronous regarding the host. That behavior allows the host to either prepare more data or compute part of the solutions itself. We studies both cases in our two studies. This repartition shows interest in the computationally heavy problem like Langford and both CPU and GPU were computing part of the result simultaneously. In the Graph500 the GPU itself had to be considered and using the CPU leads to lowest performances. Empiric tests have to be made for the work distribution regarding the targeted problem. Another critical factor for performance was the utilization of streams. This feature allows to hide communication between the host and device by dividing the communication in smaller chucks and starting the computation while the data are sent.

Distribution on multi-GPU clusters

We showed that the hybrid architecture handle multiple distributions strategies. The classical synchronous communications is perfectly handle and lead to good performances. We also used more complex start-stop systems like the best-effort used in the Langford problem. The GPU-Direct technology can be vital in data driven applications like the Graph500. This tool fits perfectly in the HPC environment and allows to reach even better performances.

From this first study, on both applications, we shows that the hybrid architecture gives really good results on different representative problems of HPC. The question that arise is now: what will be the behavior of GPUs confronted to both of those aspect ? In order to answer this question we present in the next part the Smoothed Particle Hydrodynamics problem on which we base the last part of this study. We show that GPUs can also be use in this context, targeting domain scientists codes.

Part III

Application

Introduction

The first part of the thesis presented the tools needed to understand and target performances in HPC. The second part exposed our metric showing the benefit of accelerators, in this case GPUs, over classical processors in two contexts: irregular computation and irregular communication/memory behaviors. We showed that the accelerators gave a real advantage on those two problems and even allows us to push the limits of performances. We are confident that hybrid architectures will be the way to reach exascale in 2020 horizon.

In order to validate our previous results and our metric we decided to target another irregular behavior problem embedding both computation and communication/memory wall over an irregular behavior. This problem can also be considered as a *realistic, production* code as it targets nowadays problems of domain scientists. In order to show how accelerators handle real world problems, we searched for an application fulfilling our needs. Our choose fell on the Smoothed Particle Hydrodynamics problem applied to fluid and astrophysics simulation.

We targeted this problem for several reasons. We show in the first chapter the computer science implementation issues and limitations. We present the elements making this application a perfect choice for our metric. This project is also part of an exchange with the Los Alamos National Laboratory in New Mexico, USA. This laboratory is part of the US Department of Energy, DoE, and groups thousands of researchers working on the most advanced nowadays problems. The Los Alamos National Laboratory, LANL, is also one of the three nuclear research facilities of the US National Nuclear Security Administration (NNSA). In summer 2016, I made a first internship of 3 months for a summer school called: *Co-Design Summer School*. This allowed us to discover a particular class of problems, Smoothed Particle Hydrodynamics and exchange with computer scientists and domain scientists. We extrapolate after the internship and saw what this problem really means in production context and its utility for our study. It makes a perfect example of realistic problem confronting computation and communication wall with irregular behavior. In order to characterize what physicists requested for this problem we also had another internship with the LANL in summer 2017 during three months.

In this part we first present the Smoothed Particle Hydrodynamics method from a physical point of view and drawing a parallel with the computer science problems involved. Indeed, a huge amount of time have been spend on the understanding of the physics side to be able to do realistic simulations and thus realistic behavior. The second chapter presents a distributed SPH code working for multi-CPU and multi-GPU. This program is called FleCSPH. Starting from the framework which is the base of FleCSPH, FleCSI, we introduce the algorithm and methods to solve efficiently this problem on classical processor and the acceleration generated adding GPUs.

Chapter 6

Complex system modelization

6.1 Introduction

In this chapter we give details on our choice for the generic application which is confronted to both computation and communication walls in irregular context. The problem we choose, the Smoothed Particle Hydrodynamics simulation method, is described on a physical aspect. We point out the difficulties involved in the implementation on supercomputers and especially hybrid architectures. A lot of work have been spent on the comprehension of the physical aspects to produce a code that meet the behavior of real astrophysics simulations.

The first section is a presentation of the SPH method itself and the overall limitation we face. Then we describe different kind of specific simulations we use as a benchmark of the application itself.

6.2 Physical modelization and downsides

We identified two main walls in our metrics: The computational wall and the communication/memory one. We conducted tests on both aspects keeping the irregularity behavior as a good representative of production codes. We show how these requirements are meet in the same problem with SPH and gravitation. In order to add another complexity layer in term of irregularity for both computation and communication we targeted astrophysical simulations. They require the computation of gravitation in addition to SPH on a very high number of particles. This part describes the SPH method itself and the gravitation computation based on fast multipole methods.

6.2.1 Smoothed Particles Hydrodynamics

Smoothed Particle Hydrodynamics (SPH) is an explicit numerical mesh-free Lagrangian method. It is used to solve hydrodynamical partial differential equations (PDEs) by discretized them into a set of fluid elements called particles. This computational method was invented for the purpose of astrophysics simulations by Monaghan, Gingold and Lucy in 1977 [Luc77, GM77]. This first SPH work conserved mass and they later proposed a method which also conserves linear and angular momenta [GM82]. The method was extended for general fluid simulations and many more fields from ballistics to oceanography. The development of new reliable, parallel and distributed tools for this method is a challenge for future HPC architectures with the upcoming exascale systems.

The method, as illustrated in figure 6.1, computes the evolution of a group of particles representing physical quantities. Those physical quantities are either invariant or computed for every particle at each step regarding its neighbors in the radius of its smoothing length h . The particles in this radius are then valued according to their distance using a smoothing function W , also called a kernel. The fundamental SPH formulation for any physical quantity A is then,

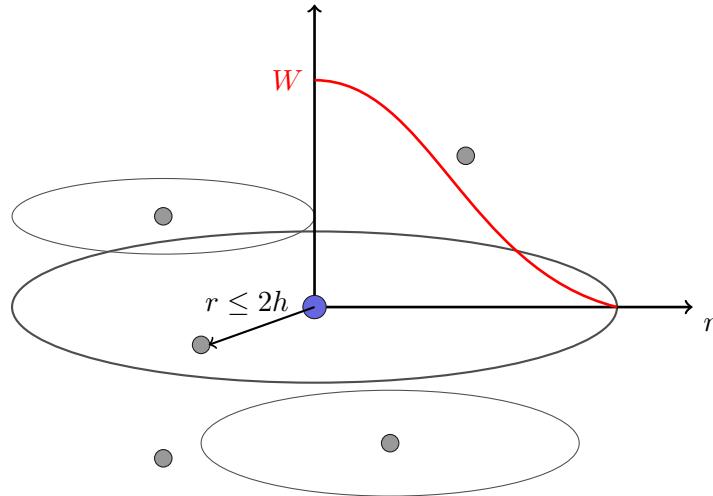


Figure 6.1: SPH kernel W and smoothing length h representation

with all the neighbors b of a particle a :

$$A(\vec{r})_a \simeq \sum_b \frac{m_b}{\rho_b} A(\vec{r}_b) W(|\vec{r} - \vec{r}_b|, h) \quad (6.1)$$

On a physics aspect, this method has several advantages: it can handle deformations, low densities, vacuum, and makes particle tracking easier. It also conserves mass, linear and angular momenta, and energy by its construction that implies independence of the numerical resolution. Another strong benefit of using SPH is its exact advection of fluid properties. Furthermore, the particle structure of SPH easily combines with tree methods for solving Newtonian gravity through N-body simulations. As a mesh-free method, it avoids the need of grid to calculate the spatial derivatives.

However, there are cons to consider using SPH: it cannot be extend to all PDE formulations; it requires careful setup of initial distribution of particles; further, it can be struggle to resolve turbulence-dominated flows and special care must be taken when handling high gradients such as shocks and surface structure of neutron stars. Many works are leading to handle more cases and to push the limitations of this method [DRZR17, LSR16, RDZR16].

In this work, we are solving Lagrangian conservation equations (Euler equations) for density, energy and momentum of an ideal fluid [LL59] such that:

$$\frac{d\rho}{dt} = -\rho(\nabla \cdot \vec{v}), \quad \frac{du}{dt} = -\frac{P}{\rho}(\nabla \cdot \vec{v}), \quad \frac{d\vec{v}}{dt} = -\frac{1}{\rho}(\nabla P) \quad (6.2)$$

with ρ the density, P the pressure, u the internal energy and v the velocity, ∇ the nabla operator and where $d/dt = \partial/\partial t + \vec{v} \cdot \nabla$ which is convective derivative.

By using the volume element $V_b = m_b/\rho_b$, we can formulate the Newtonian SPH scheme [Ros09] such that

$$\rho_a = \sum_b m_b W_{ab}(h_a) \quad (6.3)$$

$$\frac{du_a}{dt} = \frac{P_a}{\rho_a^2} \sum_b m_b \vec{v}_{ab} \cdot \nabla_a W_{ab} \quad (6.4)$$

$$\frac{d\vec{v}_a}{dt} = - \sum_b m_b \left(\frac{P_a}{\rho_a^2} + \frac{P_b}{\rho_b^2} \right) \nabla_a W_{ab} \quad (6.5)$$

where $W_{ab} = W(|\vec{r}_a - \vec{r}_b|, h)$ is the smoothing kernel. The equations we would like to solve allow for emergence of discontinuities from smooth initial data. At discontinuities, the entropy

increases in shocks. That dissipation occurs inside the shock-front. The SPH formulation here is inviscid so we need to handle this dissipation near shocks. There are a number of way to handle this problem, but the most widespread approach is to add artificial viscosity (or artificial dissipation) terms in SPH formulation such that:

$$\left(\frac{du_a}{dt} \right)_{art} = \frac{1}{2} \sum_b m_b \Pi_{ab} \vec{v}_{ab} \cdot \nabla_a W_{ab} \quad (6.6)$$

$$\left(\frac{d\vec{v}_a}{dt} \right)_{art} = - \sum_b m_b \Pi_{ab} \nabla_a W_{ab} \quad (6.7)$$

In general, we can express the equations for internal energy and acceleration with artificial viscosity

$$\frac{du_a}{dt} = \sum_b m_b \left(\frac{P_a}{\rho_a^2} + \frac{\Pi_{ab}}{2} \right) \vec{v}_{ab} \cdot \nabla_a W_{ab} \quad (6.8)$$

$$\frac{d\vec{v}_a}{dt} = - \sum_b m_b \left(\frac{P_a}{\rho_a^2} + \frac{P_b}{\rho_b^2} + \Pi_{ab} \right) \nabla_a W_{ab} \quad (6.9)$$

Π_{ab} is the artificial viscosity tensor. As long as Π_{ab} is symmetric, the conservation of energy, linear and angular momentum is assured by the form of the equation and antisymmetry of the gradient of kernel with respect to the exchange of indices a and b . Π_{ab} may define in different ways and here we use [MG83] such as:

$$\Pi_{ab} = \begin{cases} \frac{-\alpha \bar{c}_{ab} \mu_{ab} + \beta \mu_{ab}^2}{\bar{\rho}_{ab}} & \text{for } \vec{r}_{ab} \cdot \vec{v}_{ab} < 0 \\ 0 & \text{otherwise} \end{cases} \quad (6.10)$$

$$\mu_{ab} = \frac{\bar{h}_{ab} \vec{r}_{ab} \cdot \vec{v}_{ab}}{r_{ab}^2 + \epsilon \bar{h}_{ab}^2} \quad (6.11)$$

Using the usual form c_s as $c_s = \sqrt{\frac{\partial p}{\partial \rho}}$. The values of ϵ , α , and β have to be set regarding the problem targeted. As an example we used for the Sod shock tube problem: $\epsilon = 0.01h^2$, $\alpha = 1.0$, and $\beta = 2.0$.

There are many possibilities for the smoothing function, called the kernel. As an example the Monaghan's cubic spline kernel is given by:

$$W(\vec{r}_{ij}, h) = \frac{\sigma}{h^D} \begin{cases} 1 - \frac{3}{2}q^2 + \frac{3}{4}q^3 & \text{if } 0 \leq q \leq 1 \\ \frac{1}{4}(2-q)^3 & \text{if } 1 \leq q \leq 2 \\ 0 & \text{otherwise} \end{cases} \quad (6.12)$$

where $q = r/h$, r the distance between the two particles, D is the number of dimensions and σ is a normalization constant with the values:

$$\sigma = \begin{cases} \frac{2}{3} & \text{for 1D} \\ \frac{10}{7\pi} & \text{for 2D} \\ \frac{1}{\pi} & \text{for 3D} \end{cases} \quad (6.13)$$

In the computation of forces we also need to apply the gradient of the smoothing kernel. This is, in our example, for the cubic spline kernel:

$$\vec{\nabla}_i W(\vec{r}_{ij}, h) = \frac{\sigma}{h^{D+1}} \times \begin{cases} (-\frac{3}{h} + \frac{9}{4h}q)\vec{r}_{ij}, & \text{si } 0 \leq \frac{r}{h} < 1 \\ (\frac{-3}{r} + \frac{3}{h} - \frac{3}{4h}q)\vec{r}_{ij}, & \text{si } 1 \leq \frac{r}{h} < 2 \\ 0, & \text{si } \frac{r}{h} \geq 2 \end{cases} \quad (6.14)$$

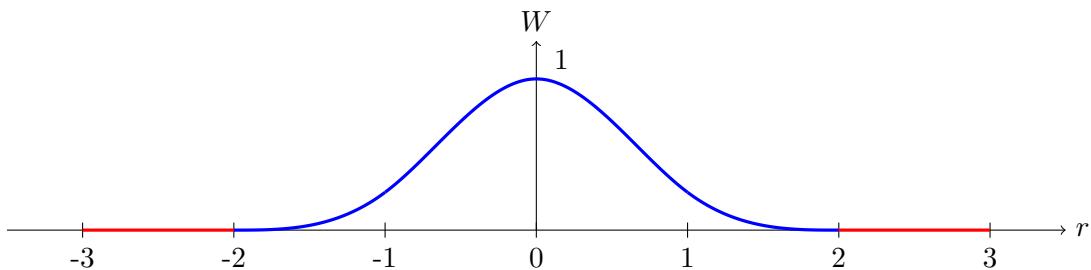


Figure 6.2: Cubic spline kernel example with $\sigma = 1$ and $h = 1$

Figure 6.2 is a representation of the cubic spline kernel with $\sigma = 1$ and $h = 1$. The abscissa axis represent r , distance between the particles and the ordinate the value of the smoothing kernel. When the support of the function, 2 is reached the particles are ignored $W = 0$, represented in red on the figure.

To sum up, the SPH resolution scheme and its routines are presented on algorithm 5. The Equation of State (EOS) and the integration are problem dependent and will be define for each test case in section 6.3.

Algorithm 5 SPH loop algorithm

- 1: **while** not last step **do**
 - 2: Compute density for each particle (6.3)
 - 3: Compute pressure using EOS
 - 4: Compute acceleration from pressure forces (6.9)
 - 5: Compute change of internal energy for acceleration (6.8)
 - 6: Advance particles after integration
 - 7: **end while**
-

The main downside for the implementation of this method is the requirement for local computation on every particle. The particles have to be grouped locally to perform the computation of (6.3), (6.8) and (6.9). A communication step is needed before and after (6.3) to get the local physical data to be able to compute (6.8) and (6.9). The tree data structure allows us to perform $O(N \log(N))$ neighbor search but also add a domain decomposition and distribution layer.

6.2.2 Gravitation

In order to target hard irregular simulation facing both the communication and computation wall in irregular behavior we decided to simulate astrophysical events. This choice is also accurate since our code, FleCSPH, will be used by the LANL astrophysicists in the near future. In order to perform those simulation the computation of gravitation/self-gravitation is required. This part present our implementation choice and expose the main problems for HPC implementation.

For classical problems like fluid flow the gravitation can directly be applied on the particles with the force:

$$\vec{a}_g = m \vec{g} \quad (6.15)$$

In order to consider astrophysics problems we need to introduce self-gravitation and gravitation. Each particle imply an action on the others based on its distance and mass. The equation of gravitation for a particle i with j other particles is:

$$\vec{f}_{ai} = \sum_j -G \frac{m_i m_j}{|\vec{r}_i - \vec{r}_j|^3} \vec{r}_{ij} \quad (6.16)$$

This computation involve an $O(N^2)$ complexity and thus is not applicable directly. We applied the method called Fast Multipole Method, FMM and discussed in [BG97]. This method is perfectly adapted to a tree representation of the domain and particles.

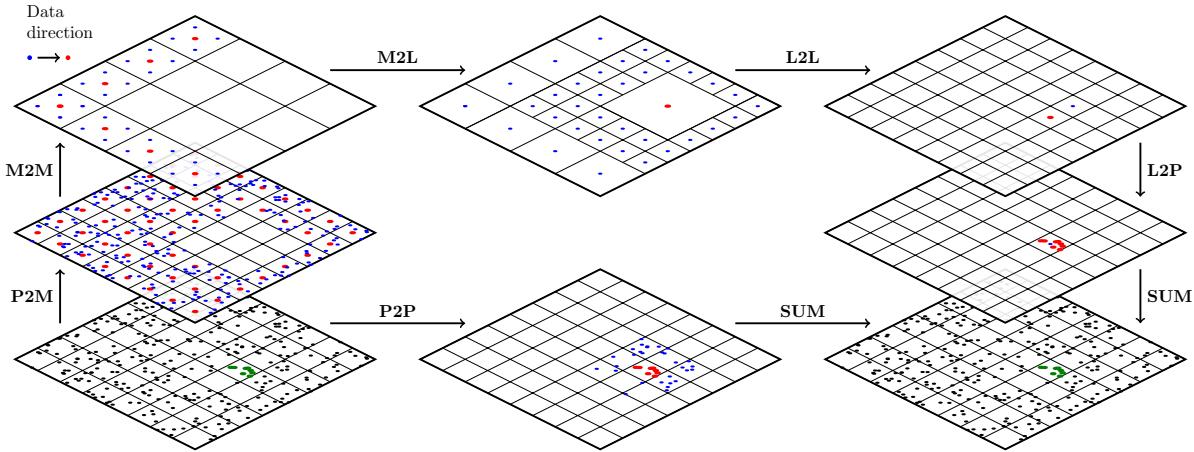


Figure 6.3: Fast Multipole Method schematics. Particles to Multipole (P2M), Multipole to Multipole (M2M), Multipole to Particles (M2P), Multipole to Local (M2L), Local to Local (L2L) and Particles to Particles (P2P). Schematic inspired from [YB11]

This method aim to compute the gravitation up to an approximation determined by the user. Details are given in figure 6.3, from left bottom to right bottom for a group of particles. We identify three main actors in this method:

Particles: the bodies on which we need to compute the gravitation regarding the other particles. In figure 6.3 we separate the green particles, on which we are computing the gravitation, from the other, blue, particles.

Multipoles: the center of mass for a group of particles. In our example they regroup the mass and barycenter of the sub-particles. There are several level of multipoles: particles' multipole and multipoles' multipole.

Locals: the center of mass for the reduction on the particles concerned in this walk. They have the same behavior as the multipoles but the information goes down to particles instead of up.

In order to compute the gravitation for a group of particles in the domain the steps are:

Particles to Particles (P2P): For the particles that are close, use the direct $O(N^2)$ algorithm. This is the part that grow if the user desires more accurate results.

Particles to Multipoles (P2M): Gather the data of all the sub-particles to the centers of mass, the multipoles. This is the first layer of the tree, the leaves.

Multipoles to Multipole (M2M): Gather the data of multipoles on higher level of the tree from the leaves to the root.

Multipoles to Local (M2L): Compute the gravitation part of all the distant multipole to the local.

Local to Local (L2L): Go down in the tree and spread the component to sub-locals.

Local to Particles (L2P): When a leaf of the tree is reached, compute the application of the local for all sub-particles.

Summation: At the end of the computation for both P2P and L2P the two interactions can be summed up to compute the gravitation applied to the particles.

This scheme have to be repeat for every group of particles. The P2M-M2M steps are done just once before the FMM method for all the groups of particles. For the choice between either P2P or M2L we use a criterion call MAC, Multipole Acceptance Criterion. In this study we used an angle between the local center of mass and the edge of distant multipole. If the angle fits

the criterion we use the current multipole, otherwise we go lower in the tree to consider smaller multipole. If the criterion never match, we are too close and consider P2P.

For the P2P step, the classical gravitation computation is used, like presented in equation 6.16. But for the interaction with distant multipoles, we use a Taylor series.

The gravitation function of equation 6.16 can be approximate on a particle at position \vec{r} by the gravitation computed at the centroid at position \vec{r}_c :

$$\vec{f}(\vec{r}) = \vec{f}(\vec{r}_c) + \left\| \frac{\partial \vec{f}}{\partial \vec{r}} \right\| \cdot (\vec{r} - \vec{r}_c) + \frac{1}{2} (\vec{r} - \vec{r}_c)^\top \cdot \left\| \frac{\partial^2 \vec{f}}{\partial \vec{r} \partial \vec{r}} \right\| \cdot (\vec{r} - \vec{r}_c) \quad (6.17)$$

From equation 6.16 we compute the term $\left\| \frac{\partial \vec{f}}{\partial \vec{r}} \right\|$:

$$\frac{\partial \vec{f}}{\partial \vec{r}} = - \sum_p \frac{m_p}{|\vec{r}_c - \vec{r}_p|^3} \begin{bmatrix} 1 - \frac{3(x_c - x_p)(x_c - x_p)}{|\vec{r}_c - \vec{r}_p|^2} & -\frac{3(y_c - y_p)(x_c - x_p)}{|\vec{r}_c - \vec{r}_p|^2} & -\frac{3(z_c - z_p)(x_c - x_p)}{|\vec{r}_c - \vec{r}_p|^2} \\ -\frac{3(x_c - x_p)(y_c - y_p)}{|\vec{r}_c - \vec{r}_p|^2} & 1 - \frac{3(y_c - y_p)(y_c - y_p)}{|\vec{r}_c - \vec{r}_p|^2} & -\frac{3(z_c - z_p)(y_c - y_p)}{|\vec{r}_c - \vec{r}_p|^2} \\ -\frac{3(x_c - x_p)(z_c - z_p)}{|\vec{r}_c - \vec{r}_p|^2} & -\frac{3(y_c - y_p)(z_c - z_p)}{|\vec{r}_c - \vec{r}_p|^2} & 1 - \frac{3(z_c - z_p)(z_c - z_p)}{|\vec{r}_c - \vec{r}_p|^2} \end{bmatrix} \quad (6.18)$$

And we propose a compact version of the matrix with:

$$\left\| \frac{\partial f^a}{\partial r^b} \right\| = - \sum_c \frac{m_c}{|\vec{r} - \vec{r}_c|^3} \left[\delta_{ab} - \frac{3 \cdot (r^a - r_c^a)(r^b - r_c^b)}{|\vec{r} - \vec{r}_c|^2} \right] \quad (6.19)$$

With δ_{ab} the Kronecker delta:

$$\delta_{ab} = \begin{cases} 1, & \text{if } a = b. \\ 0, & \text{if } a \neq b. \end{cases} \quad (6.20)$$

We note that a and b variate from 0 to 2 and $r^0 = x$, $r^1 = y$, and $r^2 = z$ as usual sense.

For the term $\left\| \frac{\partial^2 \vec{f}}{\partial \vec{r} \partial \vec{r}} \right\|$ we give the compact version by:

$$\left\| \frac{\partial^2 f^a}{\partial r^b \partial r^c} \right\| = - \sum_c \frac{3m_c}{|\vec{r} - \vec{r}_c|^5} \left[\frac{5(r^a - r_c^a)(r^b - r_c^b)(r^c - r_c^c)}{|\vec{r} - \vec{r}_c|^2} - \left(\delta_{ab}(r^c - r_c^c) + \delta_{bc}(r^a - r_c^a) + \delta_{ac}(r^b - r_c^b) \right) \right] \quad (6.21)$$

The equations 6.19 and 6.21 are use during the M2L step. Then to go down in the tree and apply the gravitation to locals and then particles in L2L and L2P we use equation 6.17.

This methods impose a lot of communications and exchanges between the processes. In our distributed version the particles are separate for each processes. Indeed, as each of them will hold part of the particles, the multipole in M2L computation imposes to share data. The P2P computation will face issues on the edge of each sub-domain. The irregular behavior is also present for the choice of the multipole to consider during the M2L step based on the MAC criterion.

6.3 Test cases with SPH

The generic SPH method and the gravitation computation, either simple or with FMM, allow us to run standard example to check the physical accuracy of our code. We choose four mains examples in this purpose: the Sod shock tube, the Sedov blast wave, fluid flow simulation and astrophysical examples like binary neutron stars coalescence. We present those problems in this section and their characteristics regarding the computer science difficulties involved.

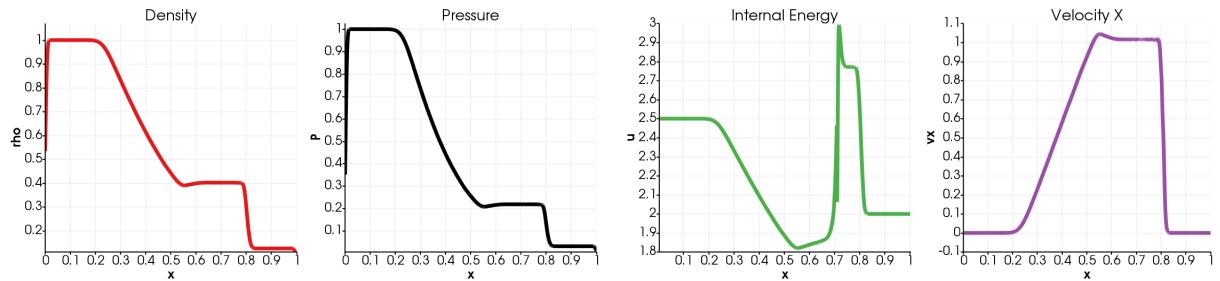
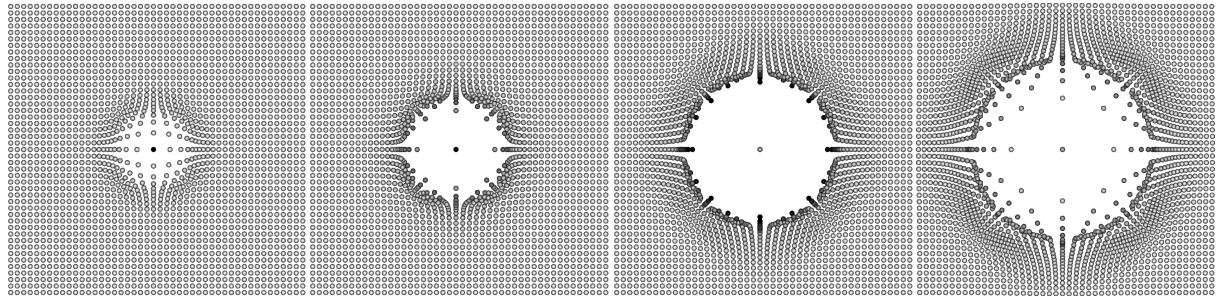


Figure 6.4: Sod shock tube with FleCSPH

Figure 6.5: Sedov Blast Wave with FleCSPH at respectively $t = 0.01$, $t = 0.03$, $t = 0.06$ and $t = 0.1$

6.3.1 Simple tests: tree and communications

Sod shock tube

The Sod shock tube is the test consisting of a one-dimensional Riemann problem with the following initial parameters [Sod78].

$$(\rho, v, p)_{t=0} = \begin{cases} (1.0, 0.0, 1.0) & \text{if } 0 < x \leq 0.5 \\ (0.125, 0.0, 0.1) & \text{if } 0.5 < x < 1.0 \end{cases} \quad (6.22)$$

In our code, we use the same initial data as in section 6.2.1 with ideal gas EOS such as:

$$P(\rho, u) = (\Gamma - 1)\rho u \quad (6.23)$$

where Γ is the adiabatic index of the gas, we set $\Gamma = 5/3$.

This test is used to check the physical accuracy of the code and thus the tree search itself. A simulation of our Sod shock experimentation is presented on figure 6.4 and shows physically correct results. The first difficulty of this problem is the tree repartition, the physics behind is not complicated and does not involve specific optimizations.

Sedov blast wave

A blast wave is the pressure and flow resulting from the deposition of a large amount of energy in a small very localized volume. There are different versions of blast wave test and we consider comparing it with the analytic solution for a point explosion as given by Sedov [Sed46], making the assumption that the atmospheric pressure relative to the pressure inside the explosion negligible. Here, we test 2D blast wave. In this simulation, we use ideal gas EOS with $\Gamma = 5/3$ and we are assuming that the undistributed area is at rest with a pressure $P_0 = 1.0^{-5}$. The density is constant ρ_0 , also in the pressurized region.

An example of our Sedov Blast wave experimentation is presented on figure 6.5 and shows physically correct results. This problem have the same conclusion as the Sod shock tube, his purpose is the test the tree behavior with 2 dimensions.

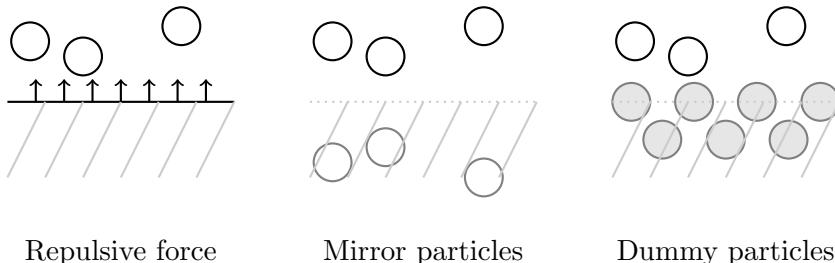


Figure 6.6: Different boundaries condition methods

6.3.2 High number of particles and specific formulation

After performing the tests regarding the physics reliability, we worked on fluid flow problem in 2D and 3D to reach high number of particles. The details can be found in [GGRC⁺12]. This test is based on an ideal EOS given by:

$$P = B \left[\left(\frac{\rho}{\rho_0} \right)^\gamma - 1 \right] \quad (6.24)$$

with $\gamma = 7$ and $B = c_0 \rho_0 / \gamma$ being $\rho_0 = 1000 \text{ kg.m}^{-3}$ the reference density.

Boundary conditions

For this experiment, realistic boundaries conditions were needed. Several methods are possible with SPH and we focused on the main ones: the repulsive wall, the mirror particles [LP91] and the dummies particles implementation [AHA12]. Those boundaries conditions implementation are presented in figure 6.6.

On our first implementation we used repulsive forces, but they imposed a lot of computation during the integration step and does not handle all the shape of boundaries easily.

For the current implementation we used the dummies particles method. This method is accurate and allows us to consider all the shape of boundaries. The wall particles are just considered as normal particles, with specific equations, and their quantities are evolved during the run. The main difference is that their position does not evolve at the end of the step. They are identified in the code with a specific type, provided during the data generation.

In this fluid flow example we were able to go up to a high number of particles with 2 or 3 dimensions. The handling of boundaries conditions added a pressure on the irregularity behavior.

6.3.3 SPH and gravitation

The final aim of our tests is to simulate astrophysical events. We are interested in one of the most important event recently discovered. Last year the Laser Interferometer Gravitational Wave, LIGO, detected the first gravitational wave generated by binary neutron stars merging [AAA⁺17b] and also more complexes event with Binary Black Holes coalescence in [AAA⁺17a]. We decided to conduct tests on Binary Neutron Star, BNS, coalescence. This problem represent all the aspect needed in our benchmark with the SPH method but also the self-gravitation and gravitation computation. In order to perform realistic simulations we consider two stars that are stable. We give details on the way to generate those data and the physics of the fusion itself. A lot of work have been involve in this understanding since it is quite out of the field of the primary researches.

The generation of initial data for binary neutron star merging is quite complicated. The first step is to generate the profile of mass regarding the radius of the star. This is made using the Lane-Emden equation. As those data are generated based on a grid with a fixed smoothing length in our case we need to add an extra step for relaxation. We used two relaxation methods

	NS ₁	NS ₂	NS ₃	NS ₄
Radius (cm)	$R = G = M = 1$	1500000	1400000	960000
K	0.636619	95598.00	83576.48	39156.94

Table 6.1: Examples of the proportionality constant K regarding the star stellar radius R

with the Roche Lobe and Darwin problems. The last step before the merging is to positioned the stars and add the rotation velocity.

Solving Lane-Emden Equation

In order to consider BNS we first consider two individual stars. The star is characterized by its radius and mass but also the density repartition inside. Indeed, we have to determine the density function based on the radius. For this purpose we used the so called Land-Emden equation.

REFERENCE As we consider the star as a polytropic fluid, we use the equation of Lane-Emden which is a form of the Poisson equation:

$$\frac{d^2\theta}{d\xi^2} + \frac{2}{\xi} \frac{d\theta}{d\xi} + \theta^n = 0 \quad (6.25)$$

With ξ and θ two dimensionless variables. There is only exact solutions for a polytropic index $n = 0.5, 1$ and 2 . In our work we use a polytropic index of 1 which can correspond to a NS simulation.

For $n = 1$ the solution of equation 6.25 is:

$$\theta(\xi) = \frac{\sin(\xi)}{\xi} \quad (6.26)$$

We note $\xi_1 = \pi$, the first value of ξ with $\theta(\xi) = 0$. $\theta(\xi)$ is also defined as:

$$\theta(\xi) = \left(\frac{\rho(\xi)}{\rho_c} \right)^{\frac{1}{n}} = \frac{\rho(\xi)}{\rho_c} \quad (6.27)$$

With ρ_c the internal density of the star and ρ the density at a determined radius. ξ is defined as:

$$\xi = \sqrt{\frac{4\pi G}{K(n+1)}} \rho_c^{(n-1)/n} \times r = \sqrt{\frac{2\pi G}{K}} \times r = Ar \quad (\text{for } n = 1 \text{ and } A = \sqrt{\frac{2\pi G}{K}})$$

With K a proportionality constant, r the radius and G the gravitational constant.

From the previous equations we can write the stellar radius R , the total radius of the star, as:

$$R = \sqrt{\frac{K(n+1)}{4\pi G}} \rho_c^{(1-n)/2} \xi_1 = \sqrt{\frac{K}{2\pi G}} \times \xi_1 \quad (\text{for } n = 1) \quad (6.28)$$

We note that for $n = 1$ the radius does not depend of the central density.

Here as an example we use dimensionless units as $G = R = M = 1$ (for the other results we use CGS with $G = 6.674 \times 10^{-8} \text{ cm}^3 \text{ g}^{-1} \text{ s}^{-2}$) We can compute K as:

$$K = \frac{R^2 2\pi G}{\xi_1^2} \quad (6.29)$$

Figure 6.1 give example of radius and the proportionality constant K .

Then we deduce the density function of r as :

$$\rho(\xi) = \frac{\sin(A \times r)}{A \times r} \times \rho_c \text{ with } A = \sqrt{\frac{2\pi G}{K}}$$

As we know the total Mass M , the radius R and the gravitational constant G we can compute the central density as:

$$\rho_c = \frac{MA^3}{4\pi(\sin(AR) - AR\cos(AR))}$$

Then we normalize the results to fit $R = M = G = 1$: $K' = K/(R^2G)$, $m'_i = m_i/M$, $h'_i = h_i/R$, $\vec{x}'_i = \vec{x}_i/R$

Generating Binary Neutron Stars initial data

The initial data are based on a cubic lattice within a sphere of radius R . The density function, based on radius, $\rho(\vec{r})$ is known using the result of the Lane-Emden equation (we use polytropic index $n = 1$ here). The mass associate to each particle i of the total N particles:

$$m_i = \frac{\rho(\vec{r}_i)}{n_r} \text{ with } n_r = \frac{3N}{4\pi R^3}$$

The smoothing length is define constant and the same for all particles for all the simulation:

$$h = \frac{1}{2} \sqrt{\frac{3N_N}{4\pi n}}$$

Here we choose N_N , the average number of neighbors, to be 100.

Relaxation

The last step is to perform a relaxation on the raw data. There is two methods we used: the Roche lobe and Darwin problems. In each of them we apply specific forces during a determined time for the particles to be stabilized.

Roche lobe problem: The Roche Lobe version is used to simulate the halo around the stars which is shaped like a tear-drop. For this Hydrostatic Equilibrium Models we use a different equation of motion:

$$\frac{d\vec{v}_i}{dt} = \frac{\vec{F}_i^{Grav}}{m_i} + \frac{\vec{F}_i^{Hydro}}{m_i} + \vec{F}_i^{Roche} - \frac{\vec{v}_i}{t_{relax}} \quad (6.30)$$

With $t_{relax} \leq t_{osc} \sim (G\rho)^{-1/2}$ and where \vec{F}_i^{Roche} is:

$$\vec{F}_i^{Roche} = \mu(3+q)x_i\hat{\vec{x}} + \mu q y_i\hat{\vec{y}} - \mu z_i\hat{\vec{z}}$$

With μ to be determined (for us $\mu = 0.069$) and $q = \frac{M'}{M} = 1$ as the two polytropes have the same total mass. This is apply to each star to get the equilibrium and the simulate the tidal effect.

Darwin problem: This is the way we use to generate the final simulation. The equation of motion for the relaxation is now:

$$\frac{d\vec{v}_i}{dt} = \frac{\vec{F}_i^{Grav}}{m_i} + \frac{\vec{F}_i^{Hydro}}{m_i} + \vec{F}_i^{Rot} - \frac{\vec{v}_i}{t_{relax}} \quad (6.31)$$

With t_{relax} same as before and \vec{F}_i^{Rot} defined by:

$$\vec{F}_i^{Rot} = \Omega^2(x_i\hat{\vec{x}} + y_i\hat{\vec{y}}) \quad (6.32)$$

With $\Omega = \sqrt{\frac{G(M+M')}{a^3}}$, $L_z = Q_{zz}\Omega$ and $Q_{zz} = \sum_i(x_i^2 + y_i^2)$. At $t = 0$ we compute the total angular moment L_z which stay constant. Using it during the relaxation we can compute Ω as: $\Omega = \frac{L_z}{Q_{zz}}$ just by recomputing Q_{zz} . Here the scheme is in N^2 but just for the relaxation step.

For this relaxation we use two stars generated as before, applying equation of motion 6.31. Using a as the distance between the two polytropes (Here $a = 2.9$ for $R = 1$) and \vec{x} going for the center of the first to the second star, and \vec{z} is like the rotation vector.

After the generation we are able to perform BNS coalescence. This provides us a code using SPH, self-gravity and gravitation.

6.4 Conclusion

The problem we presented in this part fulfill all the objectives for our metric. The computation wall is targeted via the physics and gravitation computation. The communication wall on the other hand is central regarding the exchanges needed for SPH and the fast multipole method. This problem is also very irregular for both cases. Indeed, the particles moves at every iteration without any prediction on their new position and data. In the same time the locality impose a very high level of irregularity to reach efficiently all the neighbors of a specific particle. This implies the usage of a tree data structure, the work of our two metrics can be apply in this context.

As the SPH method is used in a large panel of fields from astrophysics to fluid mechanic, there are numerous related works. We can cite a code developed in the LANL, 2HOT [War13] that introduced the Hashed Oct Tree structure used in our implementation. There is also GADGET-2 [Spr05], GIZMO [Hop14] and the most recent publication is GASOLINE [WKQ17] based on PKDGRAV, a specific tree+gravity implementation. Several implementations already implement GPU code and tree construction and traversal, one can cite GOTHIC [MU17], presenting gravitational tree code accelerated using the latest Fermi, Kepler and Maxwell architectures. But a lot of GPU accelerated work still focused on fluid problems and not on astrophysical problems [HKK07, CDB⁺11]. We also note that these implementations focus on SPH problems and does not provide a general purpose and multi-physics framework like we intent to provide through FleCSPH and FleCSI.

Our implementation have not to be considered as a revolution for the SPH method itself, neither the use of accelerators. This study provide a code easy to use by domain scientists moving the complexity of distribution, load balancing and accelerator use to the back-end framework. This tool will allows us to push forward and provide different type of accelerator in the future keeping a full transparency for the user.

Chapter 7

Complex simulations on hybrid architectures

7.1 Introduction

The previous part describes the method we want to implement. It also presents the wall faced with smoothed particle hydrodynamics and gravitation. We showed that this application meets the communication and computation wall in an irregular behavior context. We intent to target astrophysical simulation using hybrid architectures. This distributed SPH and gravitation implementation is called FleCSPH. This is a complex application that, beside of being interesting for our purpose, need to be accurate on the physics aspect to be used by the domain scientists from LANL.

This section gives details about the FleCSPH framework. We first present FleCSI, the base project in the Los Alamos National Laboratory on which FleCSPH is based. We then give details on the implementation itself and the tools we implemented to reach a working and efficient code. We give details on the domain decomposition strategy used with Morton Ordering. The tree traversal algorithm choices are then explained.

After this presentation of the native code using multi-CPU clusters we present our strategies for a multi-GPU implementation. The last section exposes the results for both implementation and the simulations.

A lot of code already exists for SPH simulation and some are already made using hybrid architectures. The contribution of FleCSPH is, like FleCSI, to provide a transparent tool for domain scientists. Those frameworks provides a bunch of topologies and functions and will handle the load balancing and distribution for the domain scientists. This allows the computer scientists to keep track of last hardware evolution and provide efficient algorithms for them while the physicists/astrophysicists/chemists can focus on the simulation itself. In this context FleCSPH is focused on tree topologies and will be integrated in FleCSI later on.

7.2 FleCSI

FleCSI¹ [BMC16] is a compile-time configurable framework designed to support multi-physics application development. It is developed at the Los Alamos National Laboratory as part of the Los Alamos Ristra project. As such, FleCSI provides a very general set of infrastructure design patterns that can be specialized and extended to suit the needs of a broad variety of solver and data requirements. FleCSI currently supports multi-dimensional mesh topology, geometry, and adjacency information, as well as n-dimensional hashed-tree data structures, graph partitioning interfaces, and dependency closures.

¹<http://github.com/laristra/flecsi>

FleCSI introduces a functional programming model with control, execution, and data abstractions that are consistent both with MPI and with state-of-the-art, task-based runtimes such as Legion[BTSA12] and Charm++[KK93]. The abstraction layer insulates developers from the underlying runtime, while allowing support for multiple runtime systems including conventional models like asynchronous MPI.

The intent is to provide developers with a concrete set of user-friendly programming tools that can be used now, while allowing flexibility in choosing runtime implementations and optimization that can be applied to future architectures and runtimes.

FleCSI's control and execution models provide formal nomenclature for describing poorly understood concepts such as kernels and tasks. FleCSI's data model provides a low-buy-in approach that makes it an attractive option for many application projects, as developers are not locked into particular layouts or data structure representations.

FleCSI currently provides a parallel but not distributed implementation of Binary, Quad and Oct-tree topology. This implementation is base on space filling curves domain decomposition, the Morton order. The current version allows the user to specify the code main loop and the data distribution requested. The data distribution feature is not available for the tree data structure needed in our SPH code and we provide it in the FleCSPH implementation. The next step will be to incorporate it directly from FleCSPH to FleCSI as we reach a decent level of performance. As FleCSI is an on-development code the structure may change in the future and we keep track of these updates in FleCSPH.

Based on FleCSI the intent is to provide a binary, quad and oct-tree data structure and the methods to create, search and share information for it. In FleCSPH this will be dedicated, apply and tested on the SPH method. In this part we first present the domain decomposition, based on space filling curves, and the tree data structure. We describe the HDF5 files structure used for the I/O. Then we describe the distributed algorithm for the data structure over the MPI processes.

7.3 Distributed SPH on multi-core architecture

Before going further in the SPH implementation and our development, we need to give details on the algorithm and the work involved. The general algorithm is presented on algorithm 6 and

Algorithm 6 SPH implementation

```

1: Read particles from file
2: while not last step do
3:   Generate keys for particles
4:   Load balance particles
5:   Generate local tree data structure
6:   while Physics not done do
7:     Physics: search and distributed search
8:     Update data
9:   end while
10:  Gravitation = FMM
11:  if Output step then
12:    Output data in H5part format
13:  end if
14: end while
```

present the features of SPH presented in the previous section. In this section we present the main features of our code and the problems involved: the domain decomposition, the tree data structure and traversal and our distribution strategy. This project, in collaboration with the LANL, is named FleCSPH.

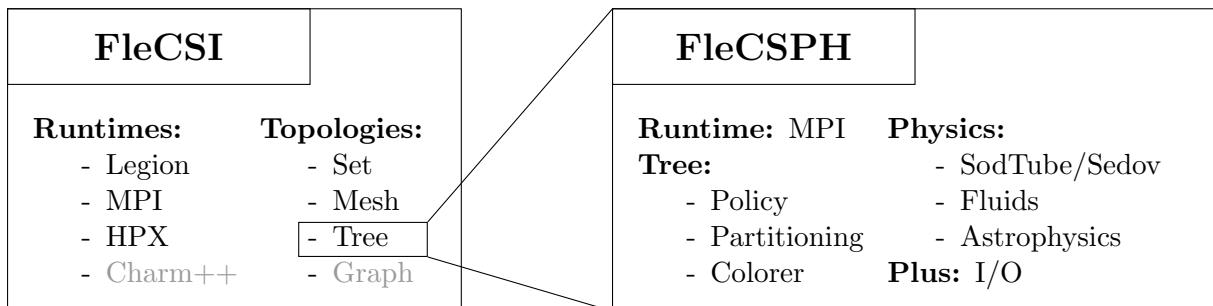


Figure 7.1: FleCSI and FleCSPH frameworks

FleCSPH² is a framework initially created as a part of FleCSI. The purpose of FleCSPH is to provide a data distribution and communications patterns to use the tree topology provided in FleCSI applied to SPH. The final purpose of FleCSPH is to complement the tree topology and provide the colorer to FleCSI. As presented in the previous sections, SPH is a very good candidate to benchmark the binary, quad and oct tree topology. The demand is high for astrophysics simulation regarding the recent discoveries of the LIGO and the SPH method allows us to generate those simulations. Figure 7.1 present how FleCSI and FleCSPH are integrated. FleCSPH is based on the tree topology of FleCSI and follows the same structure define in FleCI. The ideal runtime in FleCSI is Legion but this in-development code does not allows us to do more than static data distribution. This is why we decided to work with the MPI runtime in FleCSPH. Those MPI functions can then be integrated to FleCSI to generate group of particles and labeled them, the coloring.

Figure 7.2 present the file systems of the github repository. We use the tools from Cinch⁴ developed at LANL for the CMake and the makefile generation. It also provide the GoogleTests API for our unit tests. The FleCSPH code is currently public and available on github under the *laristra* (Los Alamos Ristra) project. The continuous integration is ensured by using Travis based on Docker and *Dockerfiles* provided in the Docker folder. In addition to Travis for the unit tests we use tools as CodeCov⁵ for the code coverage and SonarQube⁶ for the quality gates. In the current version we use external libraries: HDF5, H5hut and a specific library for I/O based on H5hut. Those elements are present and installed using scripts in *third-part-library* folder.

For the first implementation we present the code without considering accelerators. We intent to provide an efficient multi-CPU distributed code. The description starts with the domain decomposition strategy which is a basic element for the tree implementation. We explain the tree data structure for the construction and the search of particles along with the distribution strategy.

7.3.1 Domain decomposition

The number of particles can be high and represent a huge amount of data that does not fit in a single node memory. This implies the distribution of the particles over several computational nodes. As the particles moves during the simulation the static distribution is not possible and they have to be redistributed at some point in the execution. Furthermore, this distribution need to keep local particles in the same computation node to optimize the exchanges and computation itself.

A common approach is to distribute the particles over computational nodes using *space filling*

²<http://github.com/laristra/flecsph>

⁴<http://github.com/laristra/cinch>

⁵<http://codecov.io>

⁶<http://sonarqube.org/>

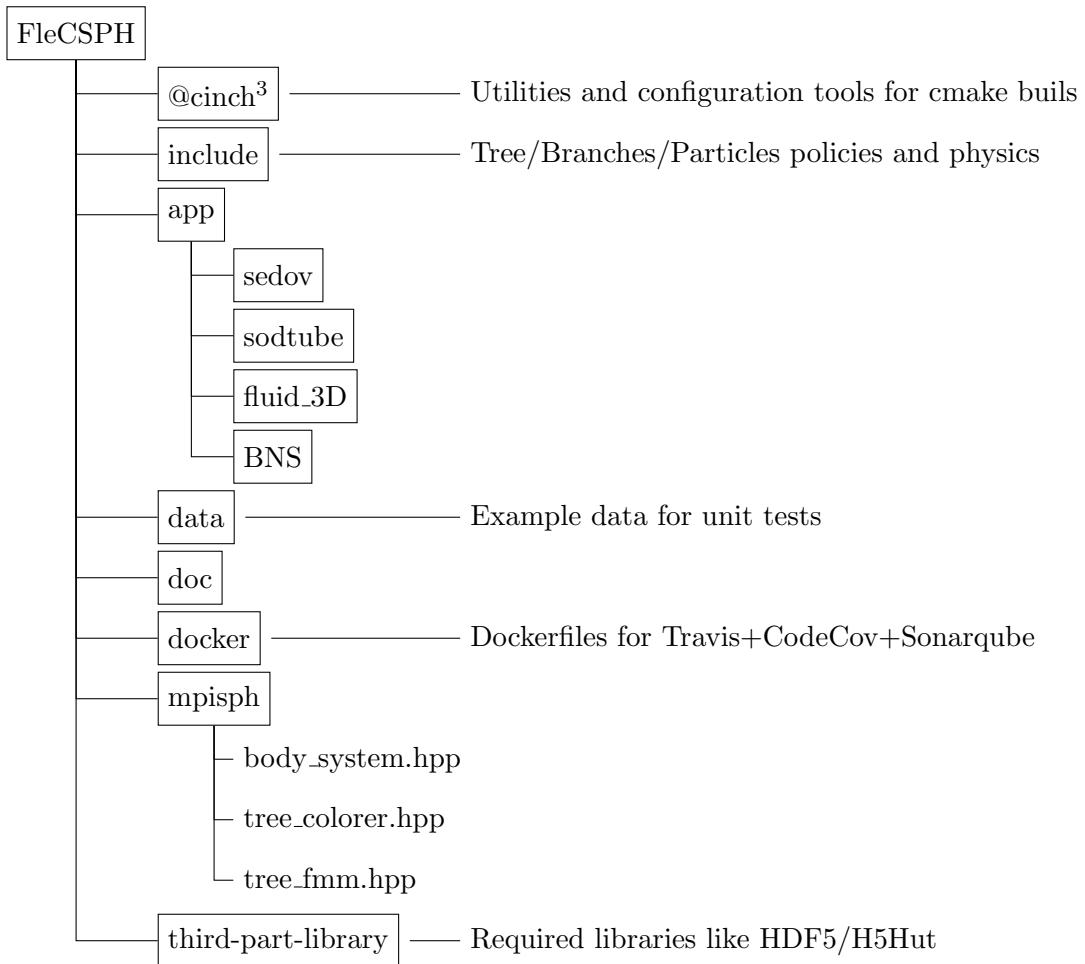


Figure 7.2: FleCSPH structures and files

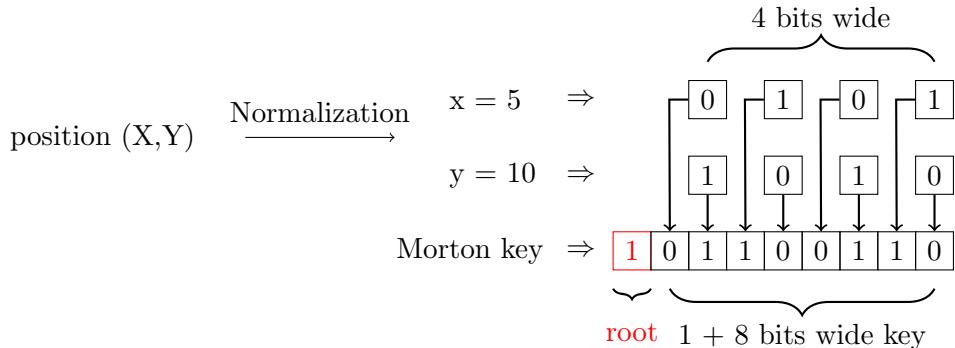


Figure 7.3: Morton order key generation

curves like in [War13, Spr05, BGF⁺14]. It intends to assign to each particle a key which is based on its spacial coordinates, then sorting particles based on those keys keeps particles grouped locally. Many space filling curves exists: Morton, Hilbert, Peano, Moore, Gosper, etc.

This domain decomposition is used in several layers for our implementation. On one hand, to spread the particles over all the MPI processes and provide a decent load balancing regarding the number of particles. On the other hand, it is also used locally to store efficiently the particles and provide a $O(N \log(N))$ neighbor search complexity, instead of $O(N^2)$, using a tree representation described in 7.3.2.

Several space filling curves can fit our purposes:

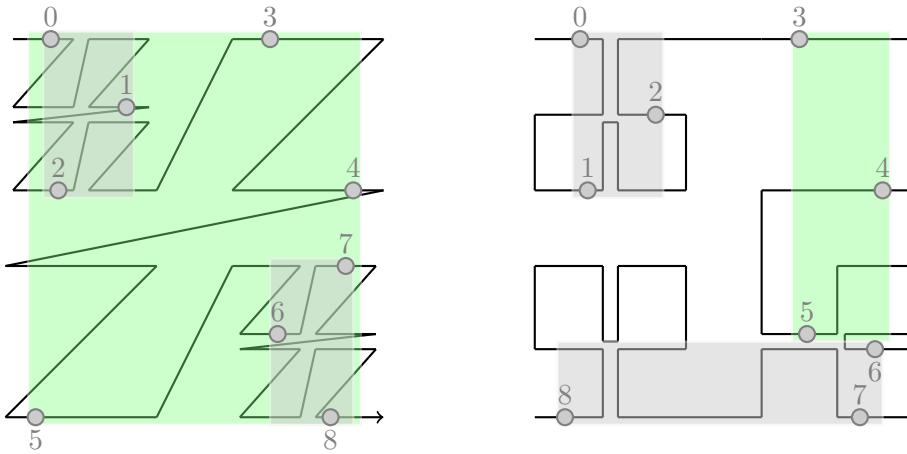


Figure 7.4: Morton and Hilbert space filling curves

The Morton curves

[Mor66], or Z-Order, is the most spread method. This method can produce irregular shape domain decomposition like shown in green on figure 7.4. The main advantage is to be fast to compute, the key is made by interlacing directly the X, Y and Z bits without rotations.

The Hilbert curves

[Sag12] are constructed by interlacing bits but also adding rotation based on the Gray code. This work is based on the Peano curves and also called Hilber-Peano. The construction is more complicated than Morton but allows a better distribution.

On figure 7.4, the Morton (left) and Hilbert (right) space-filling curves are represented in this example. The particles are distributed over 3 processes. The set of particles of the second process appears in green. As we can see there are discontinuities on the Morton case due to the Z-order "jump" over the space. This can lead to non-local particles and over-sharing of particles that will not be needed during the computation. In the Hilbert curve, the locality over the processes is conserved.

In this first implementation of FleCSPH we used the Morton ordering due to the computational cost. The next step of this work is to compare the computation time of different space filing curves.

Technically the keys are generated for each particle at each iteration because their position is expected to change over time. To be more efficient, the keys can stay the same during several steps and the final comparison can be made on the real particles positions. This increase the search time but allows less tree reconstructions.

We use 64 bits to represent the keys to avoid conflicts. The FleCSI code allows us to use a combination of memory words to reach the desired size of keys (possibly more than 64 bits) but this will cost in memory occupancy. The particle keys are generated by normalizing the space and then converting the floating-point representation to a 64 bits integer for each dimensions. Then the Morton interlacing is done and the keys are created. Unfortunately in some arrangements, like isolated particles, or scenarios with very close particles, the keys can be either badly distributed or duplicate keys can appear. Indeed, if the distance between two particles is less than $2^{-64} \approx 1e+20$, in a normalized space, the key generated through the algorithm will be the same. This problem is then handle during the particle sort and then the tree generation. In both case two particles can be differentiate based on their unique ID generated at the beginning execution.

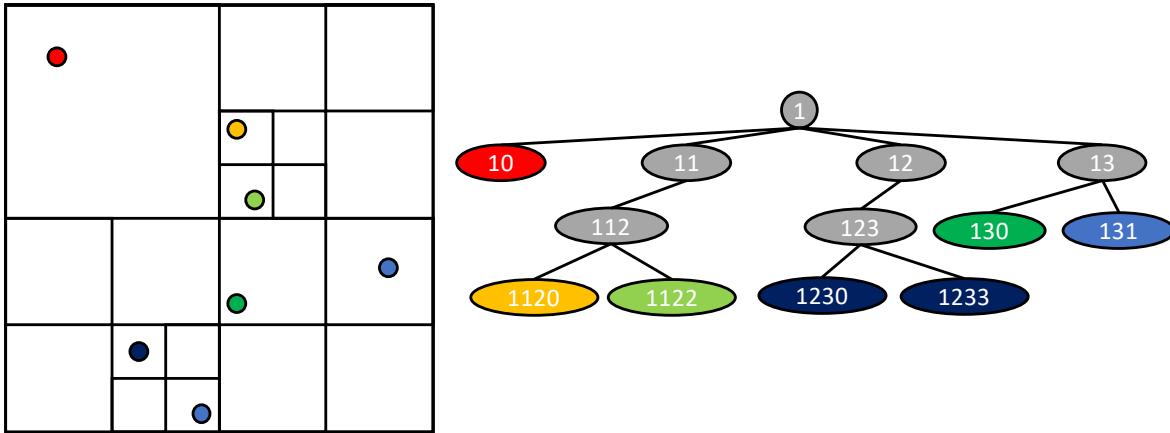


Figure 7.5: Quadtree, space and data representation

7.3.2 Hierarchical trees

The method we use for the tree data structure creation and research comes from Barnes-Hut trees presented in [BH86, Bar90]. By reducing the search complexity from $O(N^2)$ for direct summation to $O(N \log(N))$ it allows us to do very large simulations with billions of particles. It also allows the use of the tree data structure to compute gravitation using multipole methods.

We consider binary trees, for 1 dimension, quad-trees, for 2 dimensions, and oct-trees, for 3 dimensions. The construction of those trees is directly based on the domain decomposition using keys and space-filling curve presented in section 7.3.1.

As explained in the previous section, we use 64 bits keys. That gives us up to 63, 31 and 21 levels in the tree for respectively 1, 2 and 3 dimensions. As presented on figure 7.5 the first bit is used to represent the root of the tree, 1. This allows us to have up to 2^{63} different keys and unique particles.

Tree generation

After each particle gets distributed on its final process using its space-filling curve key, we can recursively construct the tree. Each particle is added and the branches are created recursively if there is an intersection between keys. Starting from the root of key "1" the branches are added at each levels until the particles are reached. An example of a final tree is shown on figure 7.5.

Tree search

When all the particles have been added, the data regarding the tree nodes are computed with a bottom up approach. Summing up the mass, position called Center of Mass (COM), and the boundary box of all sub-particles of this tree node.

For the search algorithm the basic idea would be to do a tree traversal for all the particles and once we reach a particle or a node that interact with the particle smoothing length, add it for computation or in a neighbor list. Beside of being easy to implement and to use in parallel this algorithm requires a full tree traversal for every particle and will not take advantage of the particles' locality.

Our search algorithm, presented on Algorithm 7, is a two step algorithm like in Barnes trees: First create the interaction lists and then using them on the sub-tree particles. In the first step we look down for nodes with a target sub-mass of particles $tmass$. Then for those branches we compute an interaction list and continue the recursive tree search. When a particle is reached, we compute the physics using the interaction list as the neighbors. The interaction list is computed using an opening-angle criterion comparing the boundary box and an user defined angle. This way we will not need a full tree traversal for each particle but a full tree

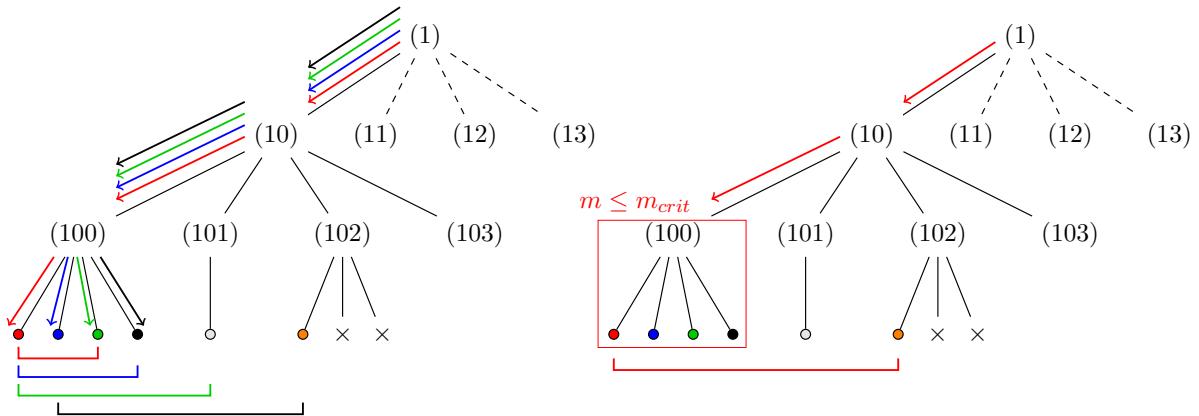


Figure 7.6: Neighbors search using a tree traversal per particle vs a group of particle and computing an interaction list

traversal for every group of particles. On figure 7.6 we present the classical and the two steps algorithm. We see that the first method, on left, force to do one walk per particle, compute the interaction list and then apply to particles. On the left, the two step method, only perform one tree traversal for the whole block of particles, compute the interaction list and then processed to the local computation. Indeed, this implies a check of particle distance during the computation since all the particles from the interaction list are not useful for every particle.

7.3.3 Distribution strategies

The previous section presented the tree data structure that can be use locally on every node. The distribution layer is added on top of it, keeping each sub-tree on the computation nodes. The current version of FleCSPH is still based on synchronous communications using the Message Passing Interface (MPI).

The main distributed algorithm is presented on algorithm 8:

Particle distribution

The sort step, line 5, is base on a distributed quick sort algorithm. The keys are generated using the Morton order described in part 7.3.1. As we associate a unique number to each particle we are able to sort them using the keys and, in case of collision keys, using their unique ID. This gives us a global order for the particles. Each process sends to a master node (or submaster for larger cases) a sample of its keys. We determined this size to be 256 KB of key data per process for our test cases but it can be refined for larger simulations. Then the master determines the general ordering for all the processes and shares the pivots. Then each process locally sort its local keys and, in a global communication step, the particles are distributed to the process on which they belong. This algorithm gives us a good partition in term of number of particles. But some downside can be identified:

- The ordering may not be balanced in term of number of particles per processes. But by optimizing the number of data exchanged to the master can lead to better affectation.
- The load balance also depend on the number of neighbors of each particle. If a particle get affected a poor area with large space between the particles, this can lead to bad load balancing too.

This is why we also provide another load balancing based on the particles neighbors. Depending on the user problem, the choice can be to distribute the particles on each processes regarding

Algorithm 7 Tree search algorithm

```

1: procedure FIND_NODES
2:   stack stk  $\leftarrow$  root
3:   while not_empty(stk) do
4:     branch b  $\leftarrow$  stk.pop()
5:     if b is leaf then
6:       for each particles p of b do
7:         apply_sub_tree(p,interaction.list(p))
8:       end for
9:     else
10:      for each child branch c of b do
11:        stk.push(c)
12:      end for
13:      end if
14:    end while
15:  end procedure
16:
17: procedure APPLY_SUB_TREE(node n, node-list nl)
18:   stack stk  $\leftarrow$  n
19:   while not_empty(stk) do
20:     branch b  $\leftarrow$  stk.pop()
21:     if b is leaf then
22:       for each particles p of b do
23:         apply_physics(p,nl)
24:       end for
25:     else
26:       for each child branch c of b do
27:         stk.push(c)
28:       end for
29:     end if
30:   end while
31: end procedure
32:
33: function INTERACTION_LIST(node n)
34:   stack stk  $\leftarrow$  root
35:   node-list nl  $\leftarrow$   $\emptyset$ 
36:   while not_empty(stk) do
37:     branch b  $\leftarrow$  stk.pop()
38:     if b is leaf then
39:       for each particles p of b do
40:         if within() then
41:           nl  $\leftarrow$  nl + p
42:         end if
43:       end for
44:     else
45:       for each child branch c of b do
46:         if mac(c,angle) then
47:           nl  $\leftarrow$  nl + c
48:         else
49:           stk.push(c)
50:         end if
51:       end for
52:     end if
53:   end while
54: end function

```

Algorithm 8 Main algorithm

```

1: procedure SPECIALIZATION_DRIVER(input data file f)
2:   Read f in parallel
3:   Set physics constant from f
4:   while iterations do
5:     Distribute the particles using distributed quick sort
6:     Compute total range
7:     Generate the local tree
8:     Share branches
9:     Compute the ghosts particles
10:    Update ghosts data
11:    PHYSICS
12:    Update ghosts data
13:    PHYSICS
14:    Distributed output to file
15:   end while
16: end procedure

```

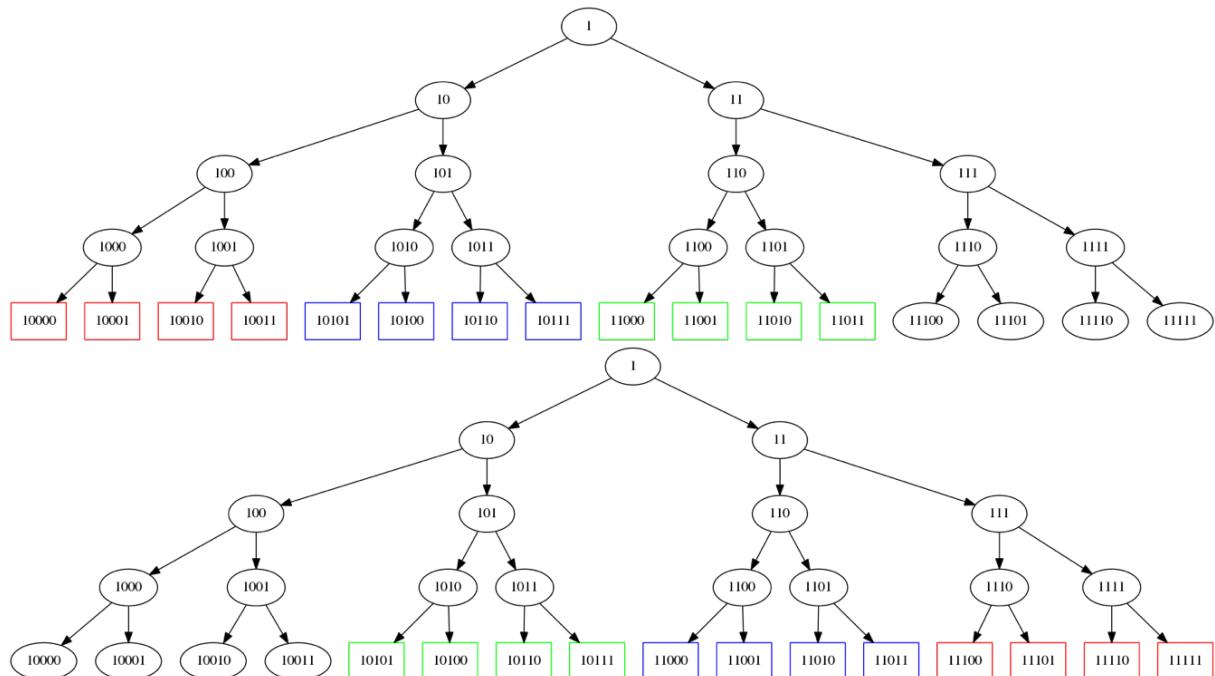


Figure 7.7: Binaries tree for a 2 processes system. Exclusive, Shared and Ghosts particles resp. red, blue, green.

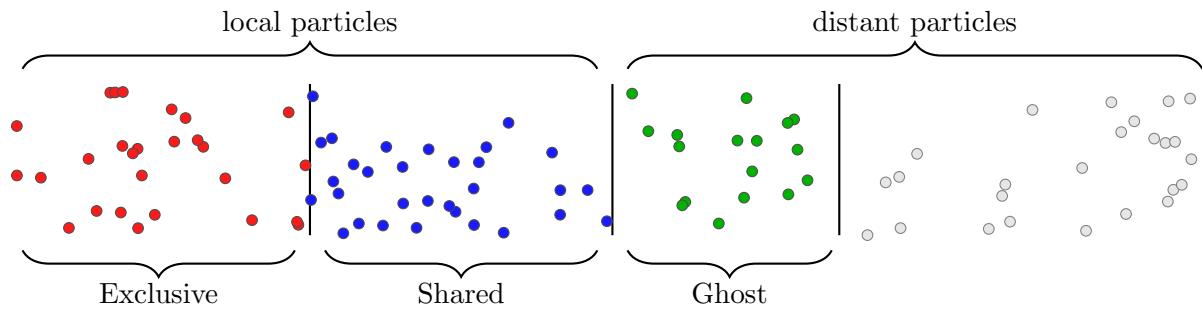


Figure 7.8: Particles "coloring" with local particles: exclusive, shared and distant particles useful during run: ghost particles

the number of neighbors, having the same amount of physical computation to perform on each processes.

After this first step, the branches are shared between the different processes, line 8. Every of them send to its neighbors several boundaries boxes, defined by the user. Then particles from the neighbors are computed, exchanged and added in the local tree. Those particles are labeled as NON_LOCAL particles. At this point a particle can be referenced as: EXCLUSIVE: will never be exchanged and will only be used on this process; SHARED: may be needed by another process during the computation; GHOSTS: particles information that the process need to retrieve from another process. An example is given for 2 processes on figure 7.8 and on a tree data structure on figure 7.7.

Exchange Shared and Ghosts particles

The previous distribution shares the particles and the general information about neighbors particles. Then each process is able to do synchronously or asynchronously communications to gather distant particles. In the current version of FleCSPH an extra step is required to synchronously share data of the particles needed during the next tree traversal and physics part. Then after this step, the ghosts data can be exchanged as wanted several times during the same time step.

7.3.4 I/O

Regarding the high number of particles, an efficient, parallel and distributed I/O implementation is required. Several choices were available but we wanted a solution that can be specific for our usage. The first requirement is to allow the user to work directly with the Paraview visualization tool and splash⁷ [Pri07].

We base this first implementation on HDF5 [FCY99] file structure with H5Part and H5Hut [HAB⁺10]. HDF5 support MPI runtime with distributed read and write in a single or multiple files. We added the library H5hut to add normalization in the code to represent global data, steps, steps data and the particles data for each steps. The I/O code was developed internally at LANL and provides a simple way to write and read the data in H5Part format. The usage of H5Hut to generate H5part data files allows us to directly read the output in Paraview without using a XDMF descriptor like requested in HDF5 format.

7.4 Distributed SPH on hybrid architectures

WORKING ON We constructed an efficient and reliable SPH code working on multi-CPU clusters. In this section we present our multi-GPU implementation and compare it with our multi-CPU code. We kept the same data structure, distribution strategy and code architecture

⁷<http://users.monash.edu.au/~dprice/splash/>

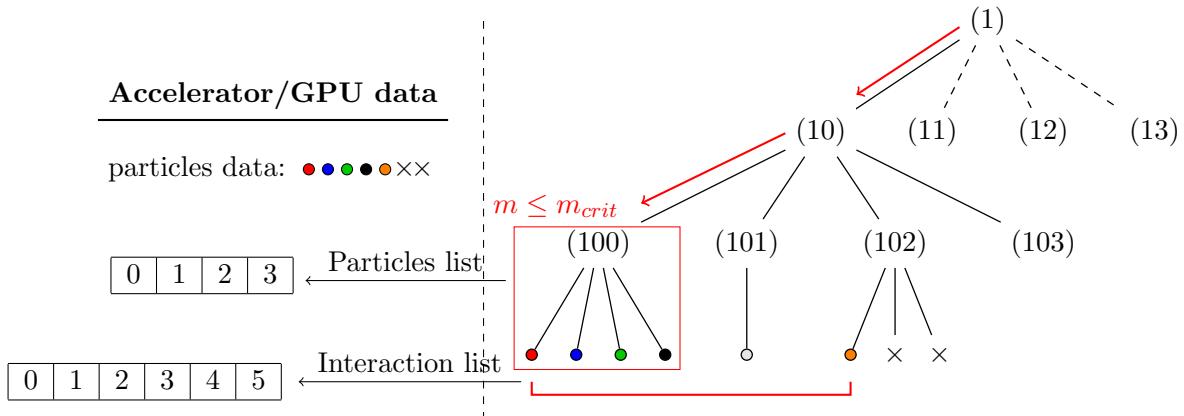


Figure 7.9: Task resolution using GPUs

in the accelerator code. Several options are possible for the accelerator implementation but we wanted to keep the code usable and working for the domain scientists to work on. As the current version of FleCSI does not allow utilization of accelerator like GPU for the data structure, we decided to embed the GPU code directly on FleCSPH. We provided the same approach we studies in the Langford problem offloading part of the tree computation on the accelerators.

7.4.1 Distribution strategies

WORKING ON During our study we The first one is to implement the whole tree traversal and data representation on GPU. This strategy imposes several downside especially for asynchronous communication. **add elements later** Figure 7.9 present the choose distribution of tasks with the accelerator. The tree traversal itself stay on the host processor and lower part of the tree are offloaded to the accelerators.

7.4.2 Physics on accelerators

WORKING ON

7.5 Results

WORKING ON In this part we compare the results of the multi-GPU version and the multi-CPU version of FleCSPH. We decided to conduct the tests on the 2D and 3D fluids.

7.5.1 Performances

7.5.2 Simulations

As explained in the previous part we simulated several physical and astrophysical event in order to check the code behavior and reliability. The first tests, done on Sod shock tube and Sedov blast wave were presented in the previous part, showed perfect results. The fluid simulations are presented on figure 7.10.

The final test of our study is a binary neutron stars merging simulation.

7.6 Conclusion

In this section we presented a tool completing our metric. This production application dedicated to smoothed particles hydrodynamics and gravitation simulation is called FleCSPH. It allows

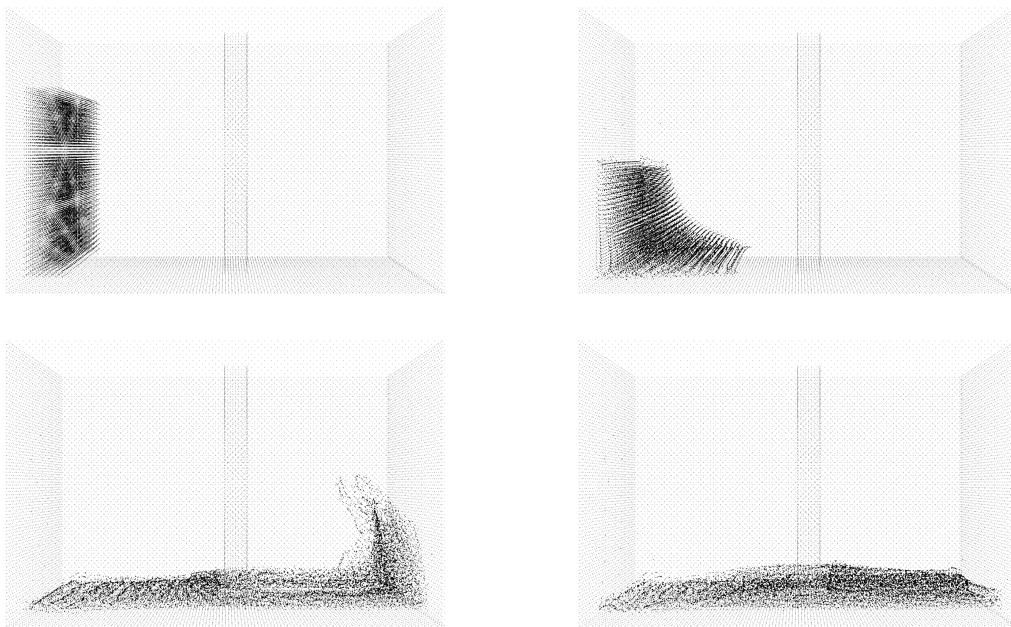


Figure 7.10: Fluid flow simulation, the dam break. For $t = 0$, $t = 0.4$, $t = 0.8$ and $t = 1$ seconds

us to target both computation and communication walls in a highly irregular context.

We showed the advantage of using hybrid architecture on this kind of application and this behavior can be find in many others.

This application is based on the FleCSI framework also developed at the Los Alamos National Laboratory. The experience and exchanges with this important laboratory of DoE and NNSA was a real opened my eyes on simulation and the complexity of such codes

Conclusion

This part highlights our study and shows the advantages of hybrid architectures compared to classical CPU centric architectures. We showed that the GPU can handle part of the computation even in the case of computation and communication walls with irregular behavior application. We took for this last metric a simulation problem. As simulation is intrinsically linked with HPC for a lot of field this application find perfectly its place in our metric.

A huge amount of time had been spend on the comprehension and implementation of the physics itself. This was required to provide realistic test cases and show the benefit of hybrid architecture even in the most complex case. We propose simulation for classical physics problems but also complex astrophysical phenomenons like binary neutron star merging. Based on this physics knowledge and the target of completing our metric we create a dedicated distributed application.

This application is called FleCSPH and is based on the FleCSI framework developed at LANL. The intent of this project is to provide a distributed and reliable framework for multi physics purpose to domain scientists. Indeed, with the fast evolution of technologies and the complexity of new supercomputers, new tools needed to be developed. FleCSPH is a first step to reach this goal and target tree topologies. It provides a domain decomposition, a tree data structure, I/O and efficient gravitation computation.

Our hybrid version of the code is based on GPU utilization. It follows the principles we described in the second part for Langford tree structure with GPUs. A subpart of the tree traversal is dedicated to the GPUs which handle all the physics computation.

This implementation is not the best and better results can be done using exclusively GPUs for the resolution. In this case we limited the code transformation to stay in a realistic usable code for the domain scientists. The overall transformation would have create a SPH dedicated program and this is not the aim of this work, targeting realistic production applications.

Conclusion

This study starts by introducing the tools and theory needed to understand and reach performances in HPC. We presented several architectures and their advantages and showed that the next objective for the world most powerful countries is to reach the computational power of one exaflop near 2020. Our believe is that those architectures will be hybrid powering accelerators like GPUs, specific many-cores or FPGAs.

From this observation regarding the power consumption and computation performances we defined a metric targeting the most important walls of HPC. The intent of this metric is to confront classical and hybrid architecture to show the real benefit that can be obtained using accelerators. This metric is decomposed in two parts.

In the fist part we target classical, academical and even benchmark problems as a metric. We confront the classical architecture to hybrid one on a problem featuring heavy computation and another one heavy communications. In two cases we wanted to fit production code and their worst behavior: irregularity.

The first problem is the Langford pairing counting problem. This problem is study with two different approaches based on respectively a tree traversal and a mathematic resolution. The tree resolution shows very good results and up to 80% of the overall work handle by the GPU with an efficient load balancing strategy. The mathematical solution is also very irregular due to the big integer arithmetic on GPUs. In this case we showed that the GPU is able to handle up to 65% of the computation effort. This hybrid architecture implementation allows us to beat a time record for the computation of the last instances using best-effort on the ROMEO supercomputer.

The second problem we choose is the Graph500. This is a perfect candidate in order to consider communication problem without heavy computation. Indeed, the only operations are memory checking for values and copy in queues. This problem stay very irregular in both memory and communication usage. We proposed an algorithm based on both NVIDIA and IBM BlueGene/Q state of the art algorithm. This allows us to rank the ROMEO supercomputer 105th in the Graph500 list of November 2016.

Those two first approaches give a lot of credit for the hybrid architecture on both walls separately. In order to complete our metric we needed to confront the classical and hybrid architecture to a production application issuing both walls. We targeted a complex simulation application. The problem fitting our needs in computational and communication over irregular context is the smoothed particle hydrodynamics and gravitation simulation of hard astrophysics events. We developed, in collaboration with the LANL, a framework named FleCSPH dedicated for tree topology and physics/astrophysics simulations. We showed with this metric the performances using hybrid architectures. Even keeping an approach of production code, not fully GPU, the performances on hybrid architectures can be way superior to classical CPU ones.

This study shows based three cases that the hybrid architecture can be the solution for exascale supercomputer. The main walls are solved using specific implementation and other ways of thinking the algorithm them-self. The problem of nowadays architectures resides in the framework and tools developed. On one hand the old softwares on which rely most of nowadays libraries need to be re-think and ported for massively parallel architectures. On the other hand,

frameworks like FleCSI can be developed to hide the complexity of clusters, nodes, accelerators offloading to domain scientists.

Parallelism is the way of the future, and always will be.

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