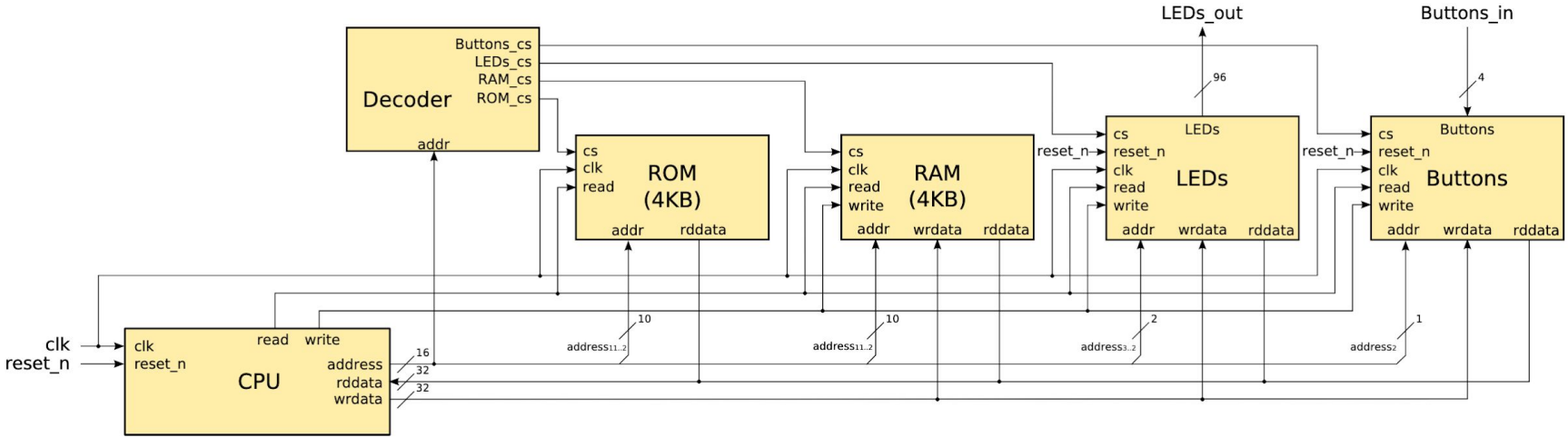
Projet de Sysnum

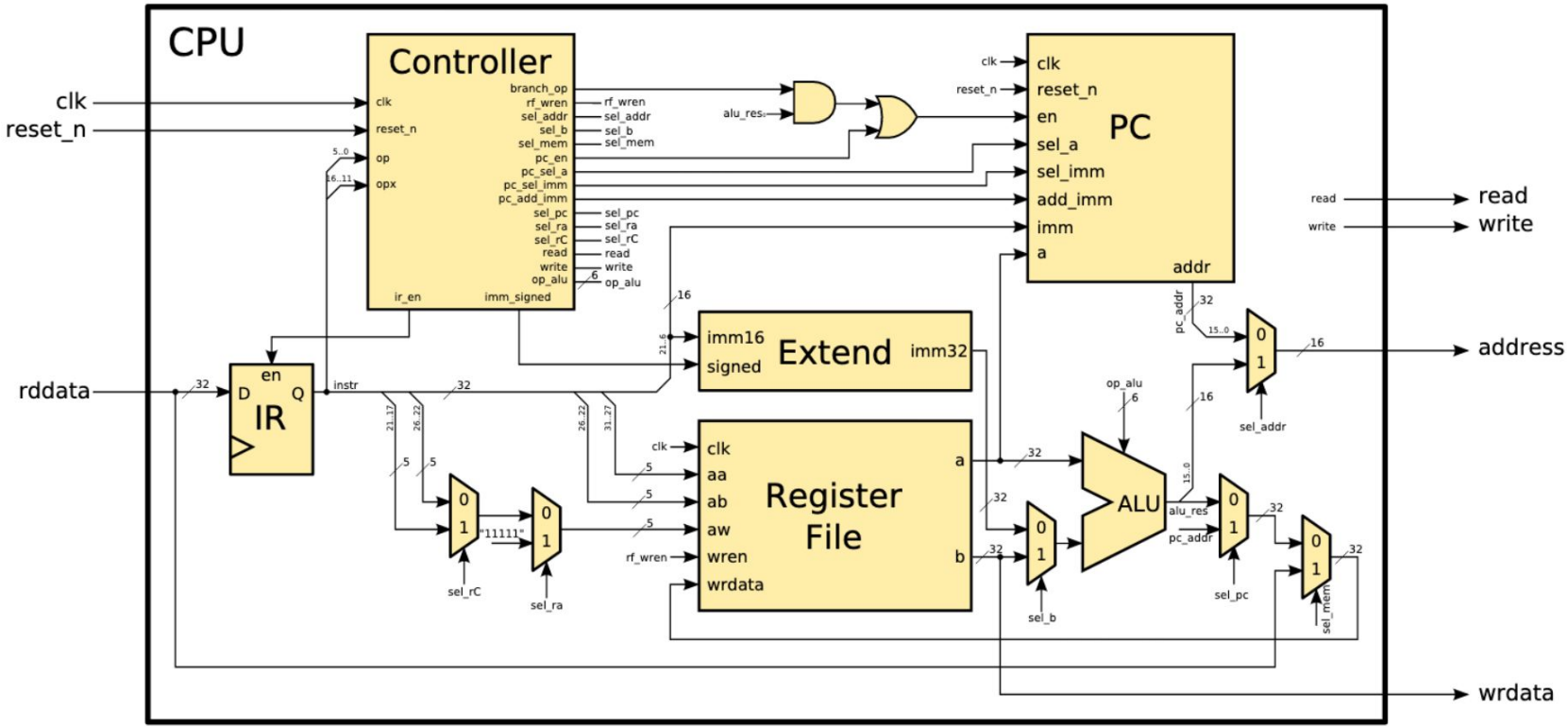
Objectif : Implémenter un processeur NiosII

- 32 bits
- 32 registers
- Un set d’instruction riche

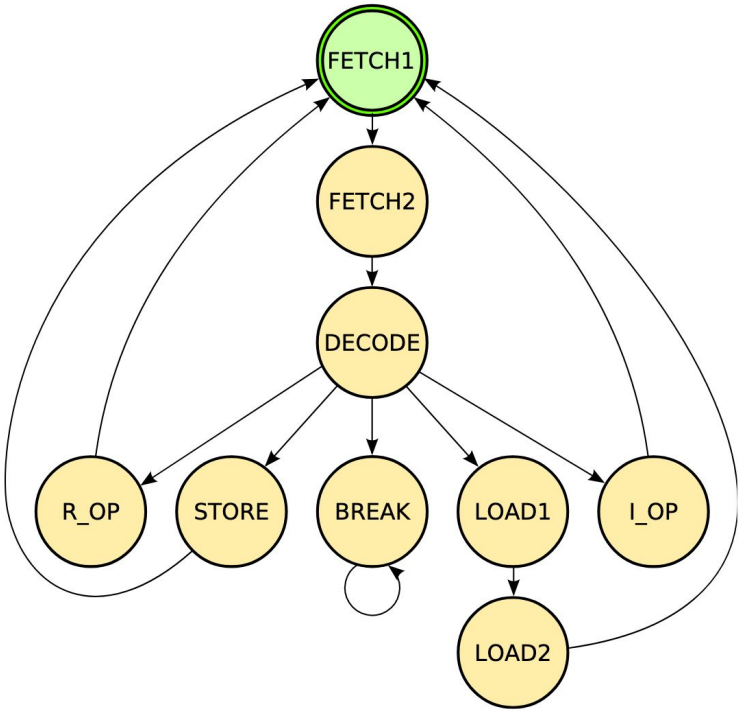
Architecture générale



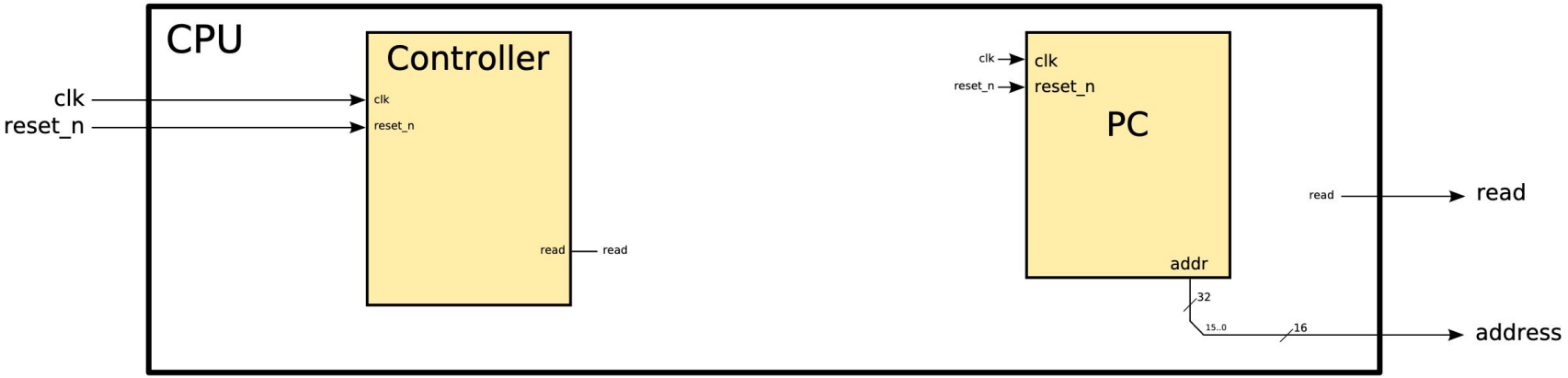
CPU


CPU
Controller
clk
reset_n
op
opx
branch_op
rf_wren
sel_addr
sel_b
sel_mem
pc_en
pc_sel_a
pc_sel_imm
pc_add_imm
sel_pc
sel_ra
sel_rC
read
write
op_alu
ir_en
imm_signed
PC
en
sel_a
sel_imm
add_imm
imm
a
addr
Extend
imm16
signed
imm32
IR
D
Q
instr
rddata
Register File
aa
ab
aw
wren
wrdata
a
b
ALU
op_alu
alu_res
pc_addr
"11111"
sel_rC
sel_ra
sel_b
sel_pc
sel_mem
read
write
address
wrdata

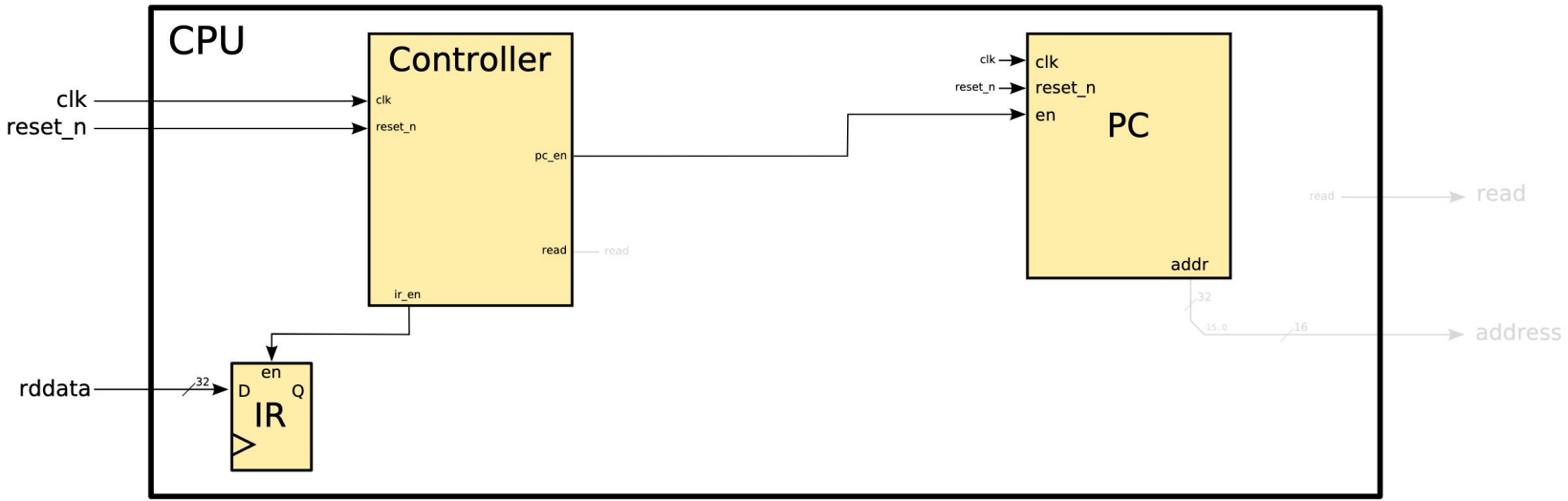
Fonctionnement du CPU



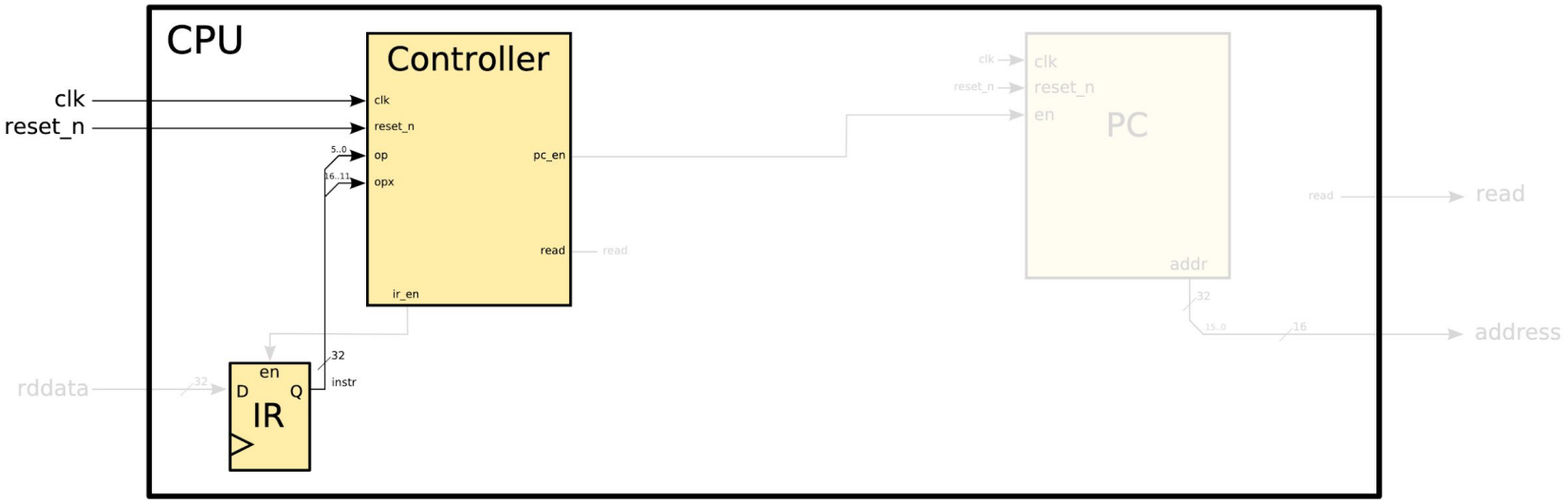
Fetch1


CPU
clk
reset_n
Controller
clk
reset_n
read
read
clk
reset_n
clk
reset_n
PC
addr
read
read
32
15..0
16
address

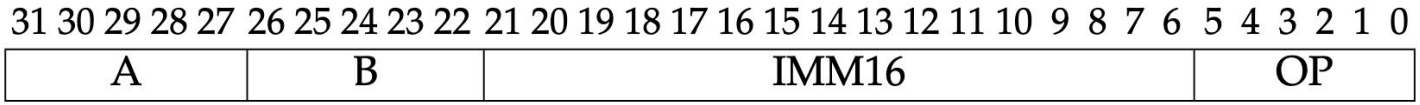
Fetch2


CPU
Controller
clk
reset_n
pc_en
read
ir_en
clk
reset_n
en
PC
addr
read
read
32
15..0
16
address
clk
reset_n
rddata
32
en
D
Q
IR

Decode


CPU
Controller
clk
reset_n
op
opx
pc_en
read
ir_en
5..0
16..11
clk
reset_n
en
PC
addr
read
read
32
15..0
16
address
rddata
32
en
D
Q
IR
32
instr

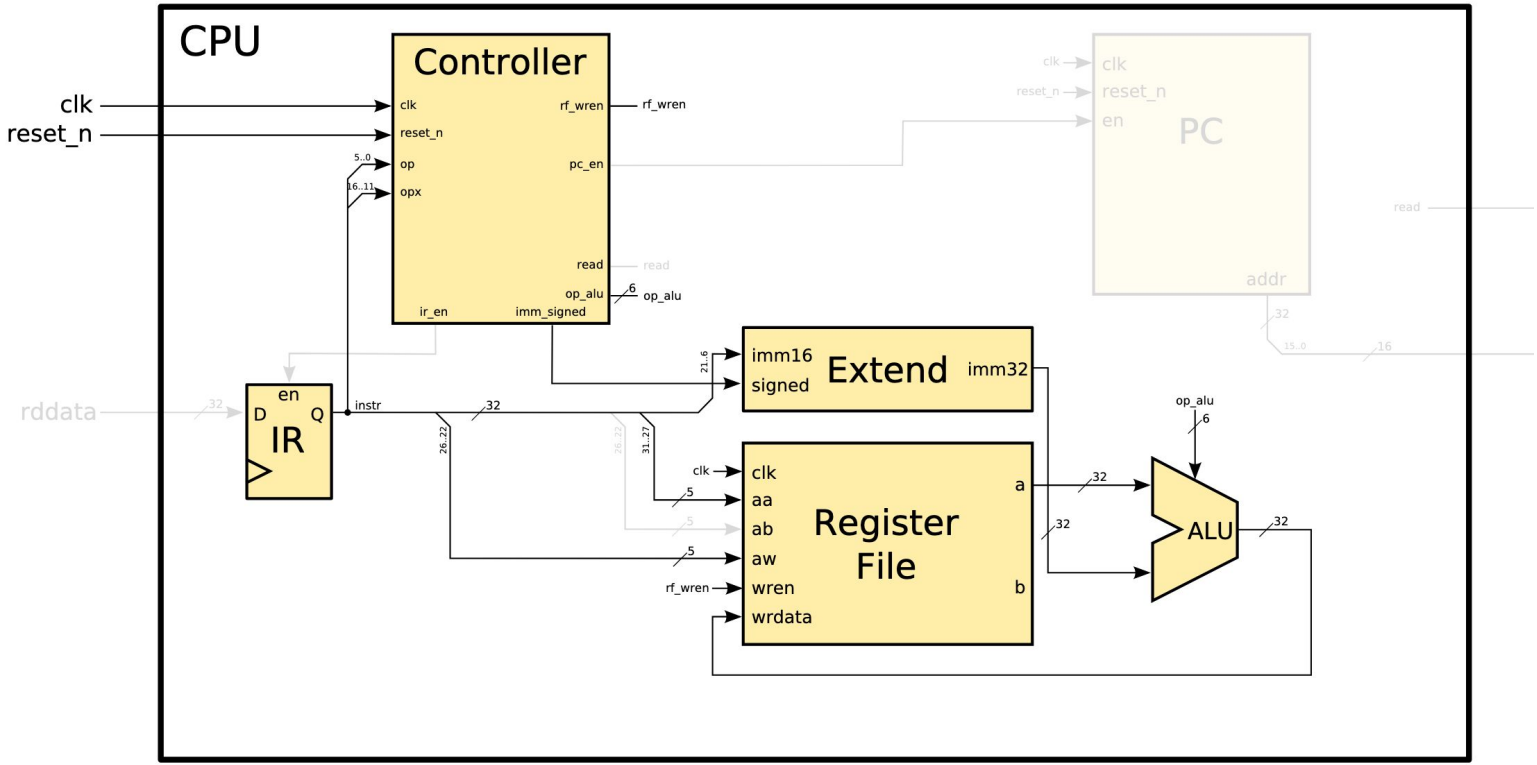
Execute state : I_OP



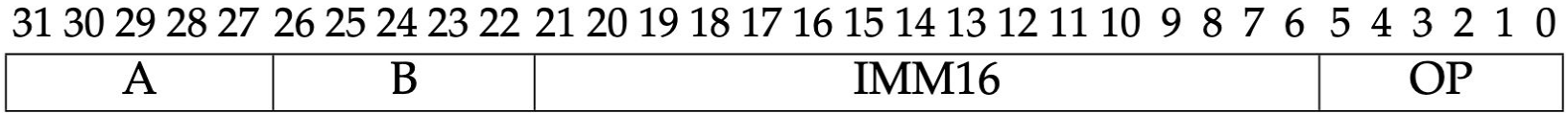
opérande destination

addi rB, rA, imm $rB \leftarrow rA + imm_s$

Execute state : I_OP

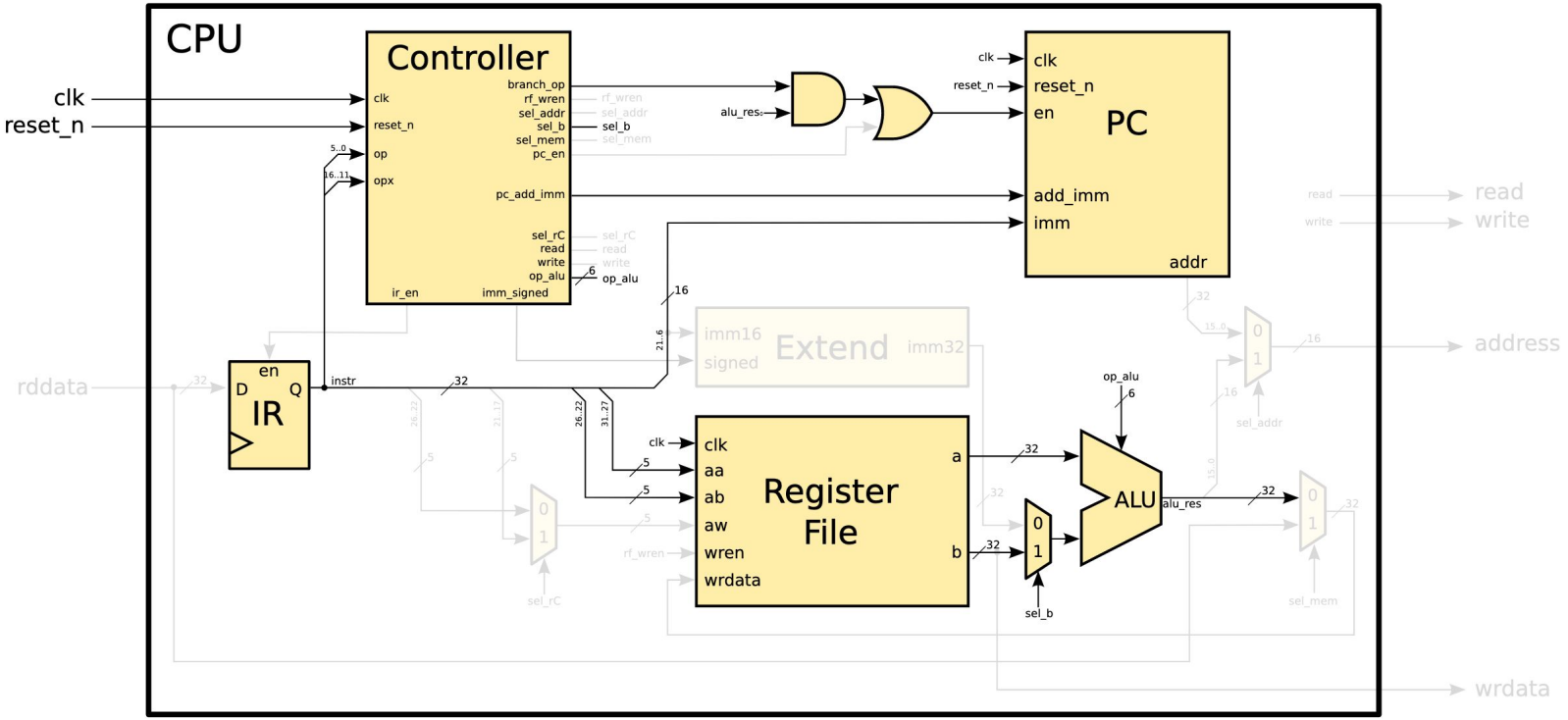


Execute state : Branch

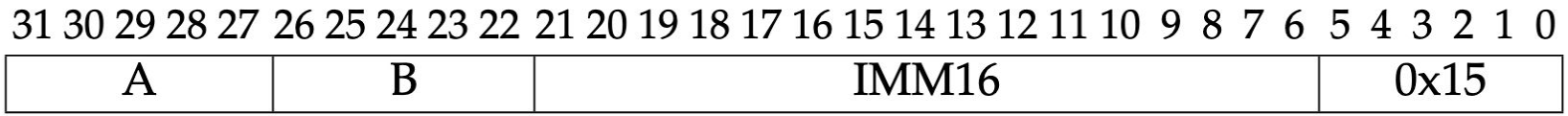


beq rA, rB, imm if (rA = rB) goto PC+4+imm_s

Execute state : Branch

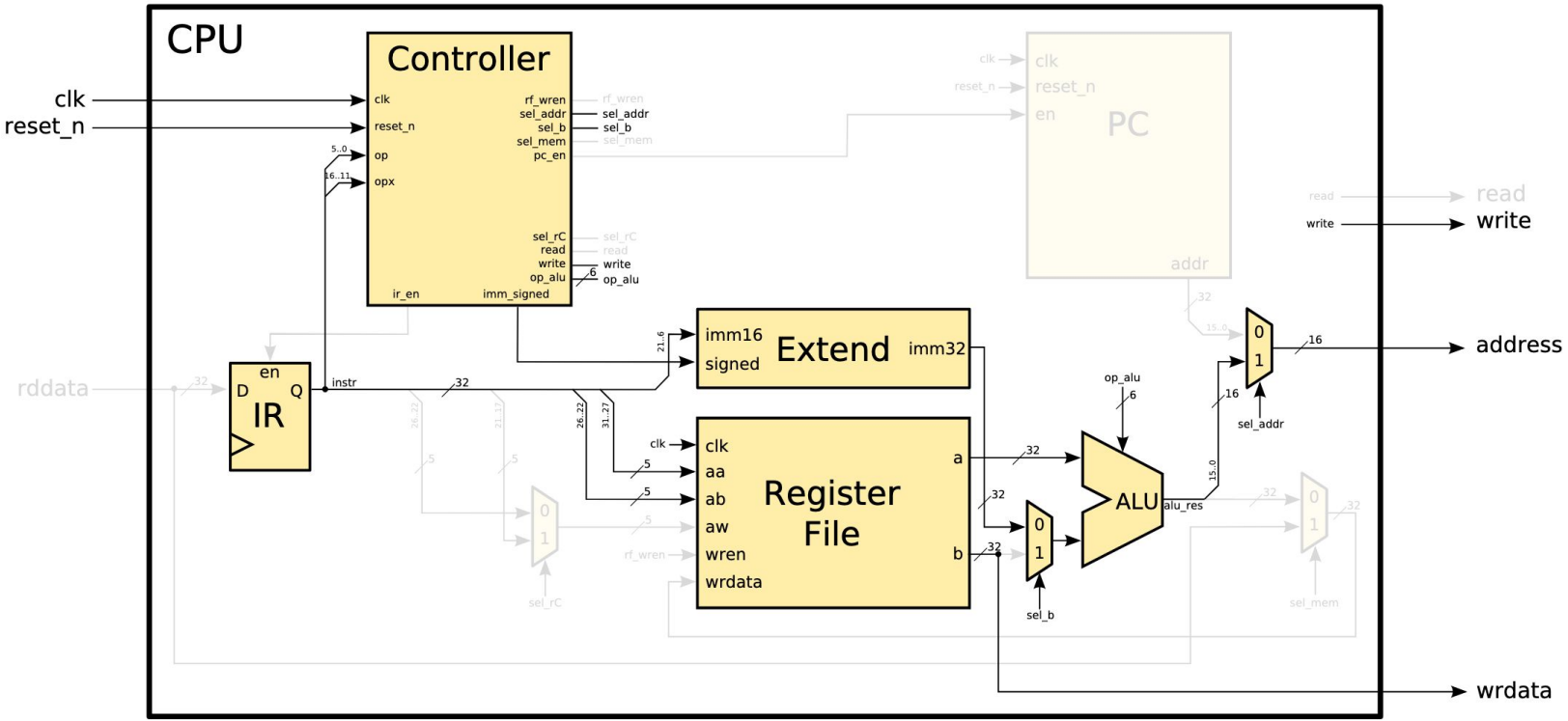


Execute state : Store



stw rB, imm (rA) $\text{MEM}[\text{imm}_s + \text{rA}] \leftarrow \text{rB}$

Execute State : Store



Difficultés rencontrés

- Minijazz : trop lent pour faire tout ce que j’avais envisagé
- La simulation permet de faire moins de chose que le hardware tel que le simulateur est concu

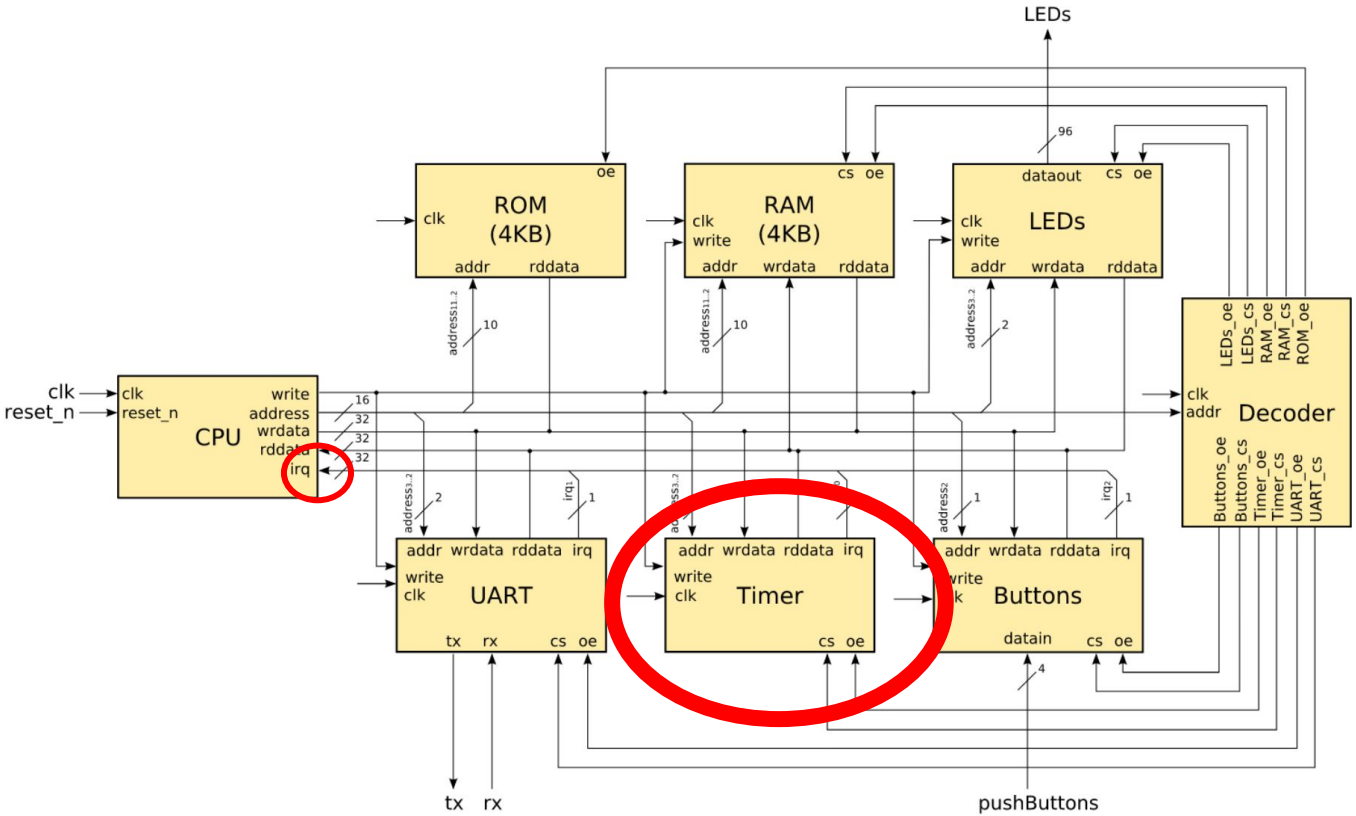
Bilan

- Une grande partie de l’instruction set a été implémentée et est fonctionnelle

Cela comporte :

- L’arithmétique
- La logique
- Les comparaisons
- Les branch
- L’accès mémoire

La clock : idée de base



Il faut donc rajouter à notre processeur

- La gestion des interruptions en modifiants le PC
- Une routine d’interruption

Problème

- La clock de mon processeur n’est pas assez rapide pour bénéficier des interruptions
- Il faut deux clocks différentes : une pour le timer, une pour le processeur. Ce n’est pas possible sans grosses modifications du simulateur

Solution

- Une boucle très moche

Démo time