

Sistemas Basados en Microprocesador

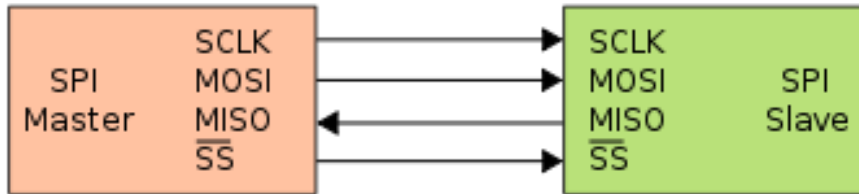
B2 SPI (Serial Peripheral Interface Bus)

SPI Características

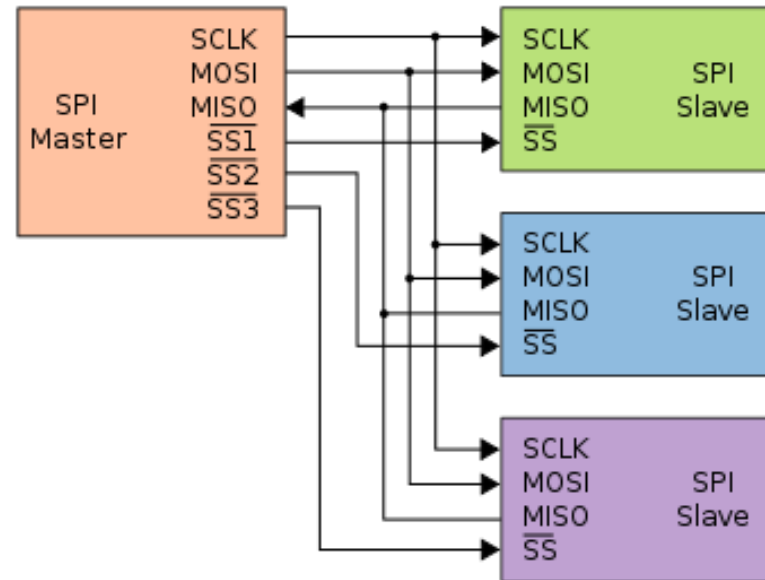
- Bus síncrono, serie, con comunicación bidireccional simultanea (Full Duplex)
- SPI maestro/esclavo
- Se envía un dato en cada pulso de reloj
- De 8 a 16 bits por transferencia

SPI – Ejemplo Arquitectura

Bus SPI: un maestro y un esclavo.



SPI bus: un maestro y tres esclavos.



Señales en el interfaz SPI

- MISO: Master In / Slave Out data. This pin can be used to transmit data in slave mode and receive data in master mode.
- MOSI: Master Out / Slave In data. This pin can be used to transmit data in master mode and receive data in slave mode.
- SCK: Serial Clock output for SPI masters and input for SPI slaves.
- NSS: Slave select. This is an optional pin to select a slave device. This pin acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave NSS inputs can be driven by standard IO ports on the master device. The NSS pin may also be used as an output if enabled (SSOE bit) and driven low if the SPI is in master configuration. In this manner, all NSS pins from devices connected to the Master NSS pin see a low level and become slaves when they are configured in NSS hardware mode. When configured in master mode with NSS configured as an input (MSTR=1 and SSOE=0) and if NSS is pulled low, the SPI enters the master mode fault state: the MSTR bit is automatically cleared and the device is configured in slave mode (refer to [Section 28.3.10](#)).

Señalización

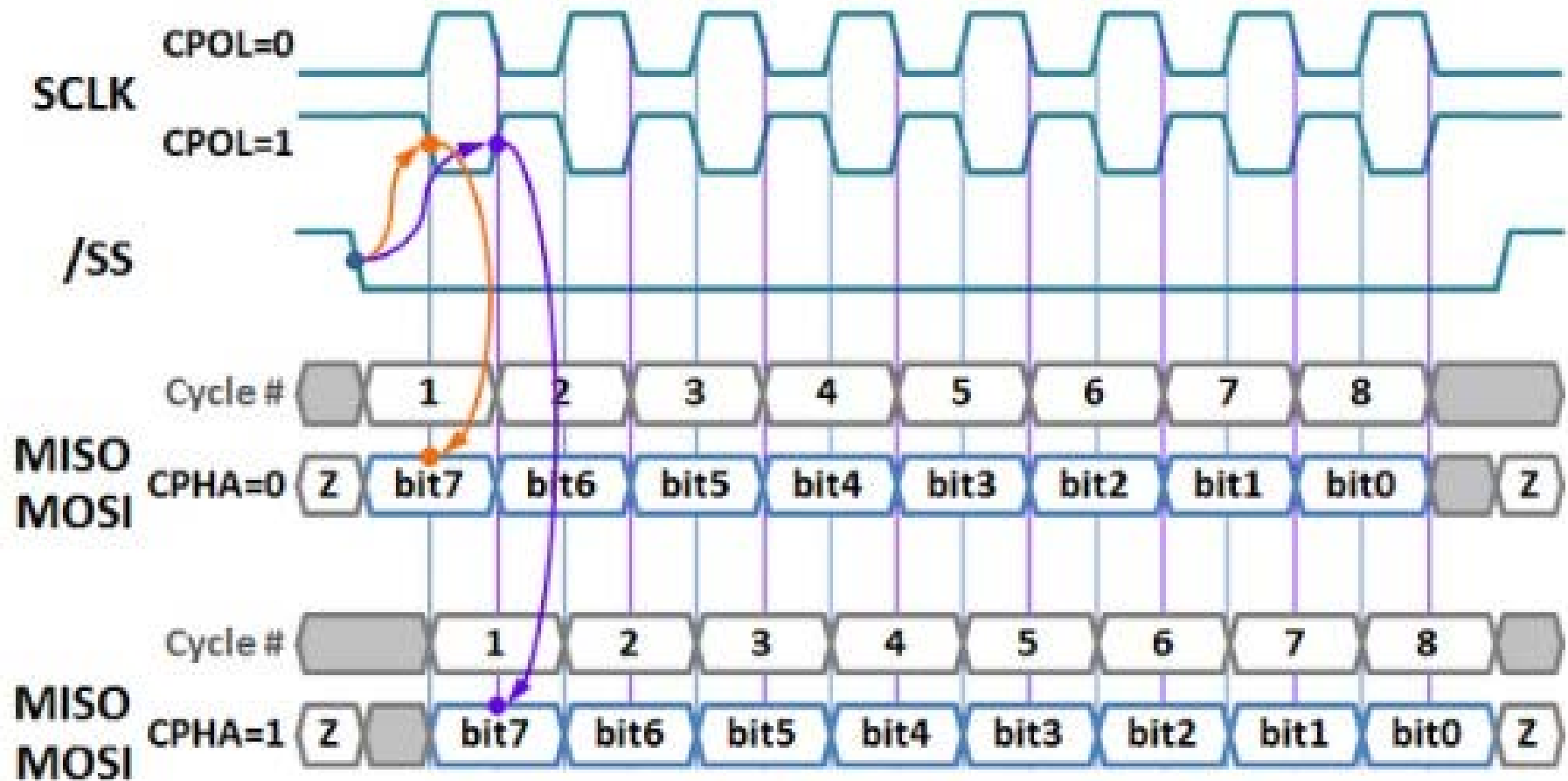
- La polaridad del reloj (flanco de subida o bajada) es configurable con el bit CPOL en el registro de control.
- Se puede programar cuándo comienza la transmisión del primer bit

Table 360. SPI Data To Clock Phase Relationship

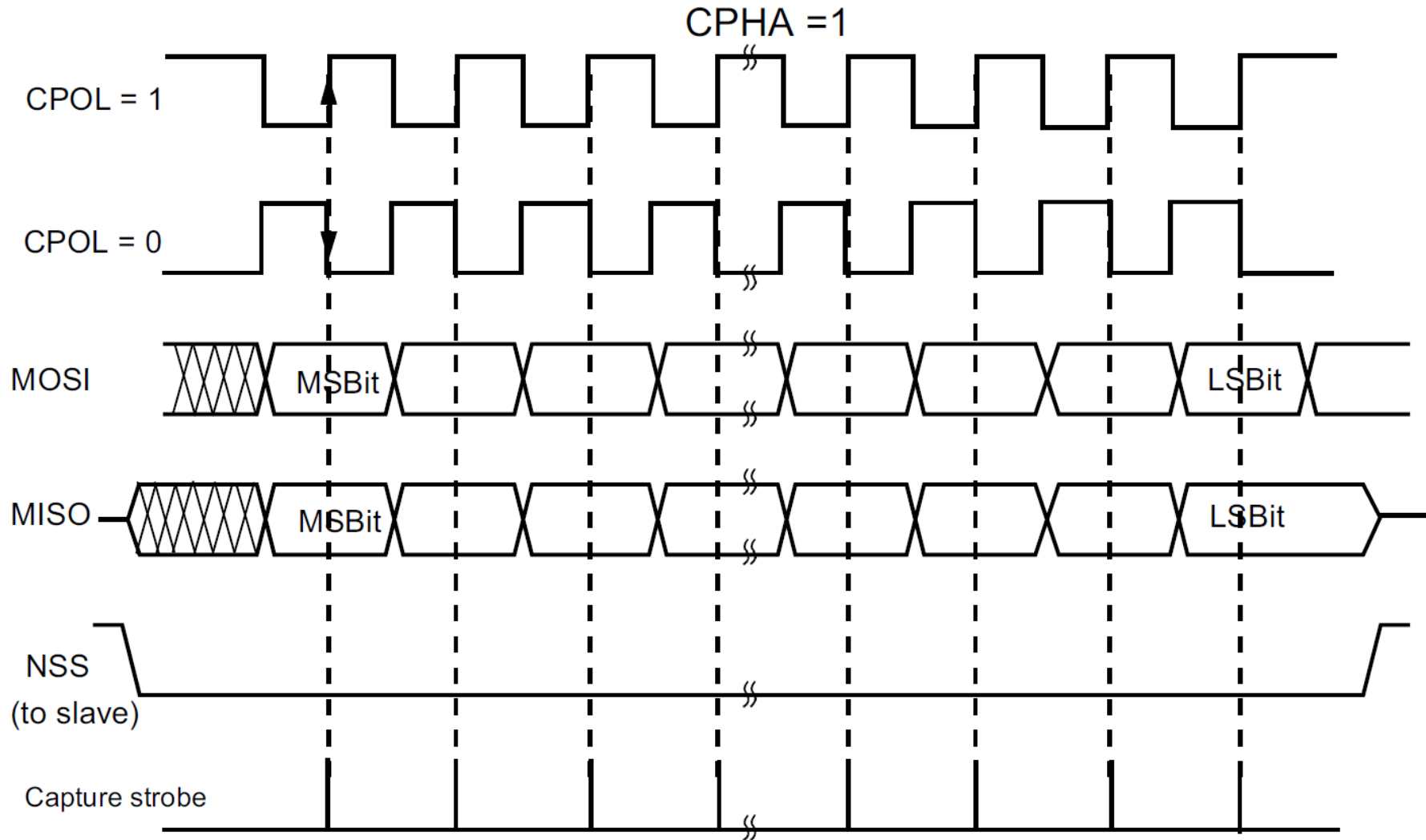
CPOL and CPHA settings	When the first data bit is driven	When all other data bits are driven	When data is sampled
CPOL = 0, CPHA = 0	Prior to first SCK rising edge	SCK falling edge	SCK rising edge
CPOL = 0, CPHA = 1	First SCK rising edge	SCK rising edge	SCK falling edge
CPOL = 1, CPHA = 0	Prior to first SCK falling edge	SCK rising edge	SCK falling edge
CPOL = 1, CPHA = 1	First SCK falling edge	SCK falling edge	SCK rising edge

Cronogramas

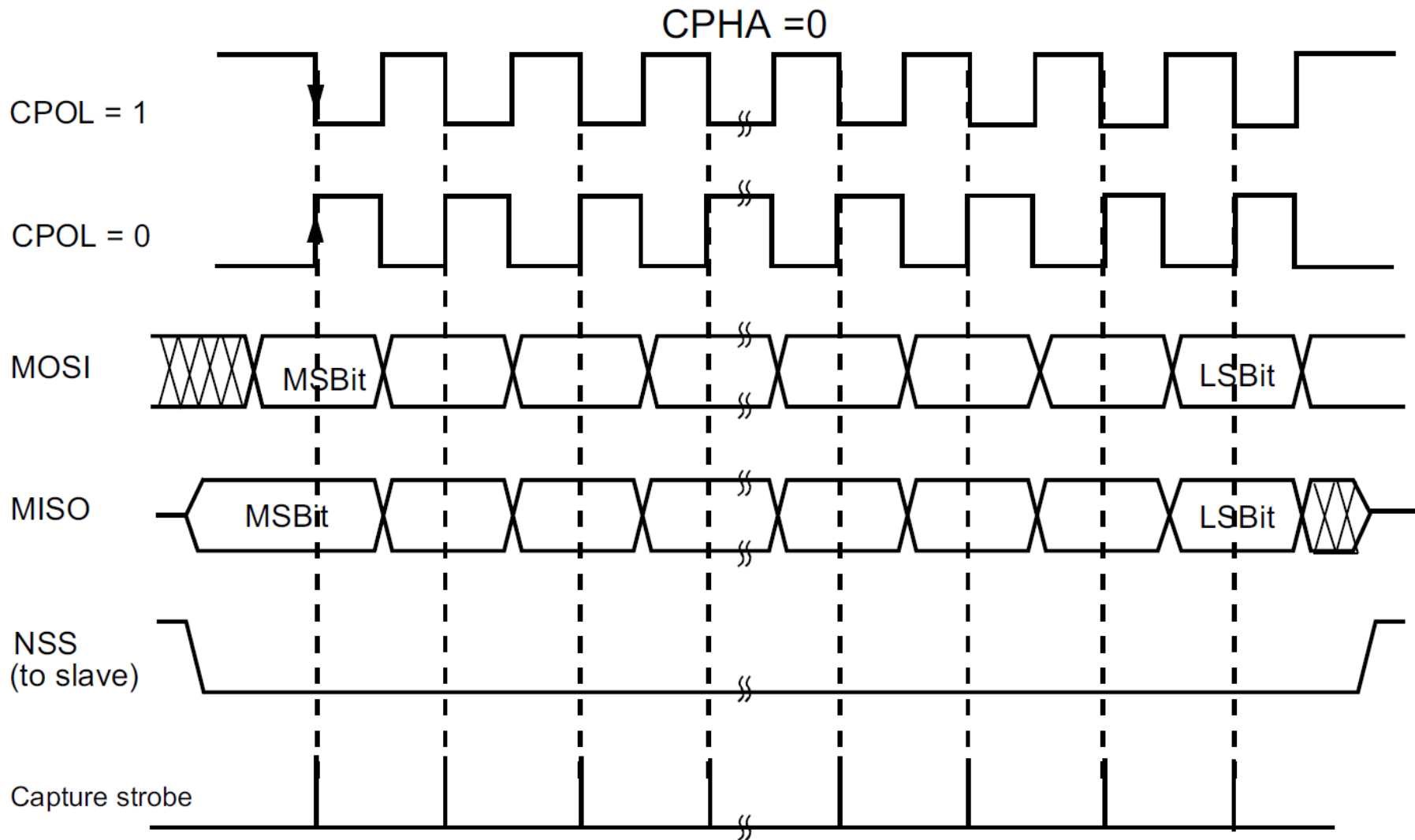
SPI Timing Chart



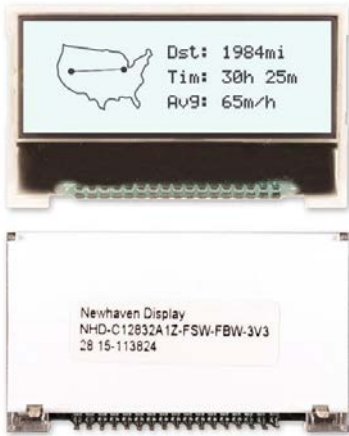
Cronogramas



Cronogramas



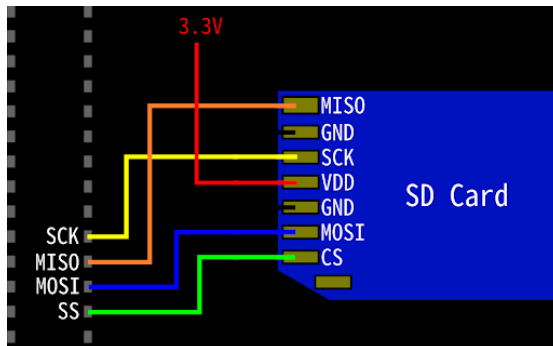
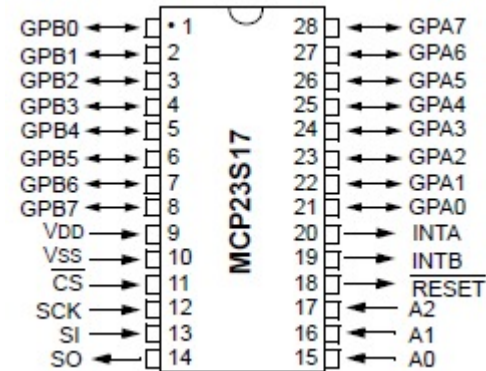
Periféricos SPI



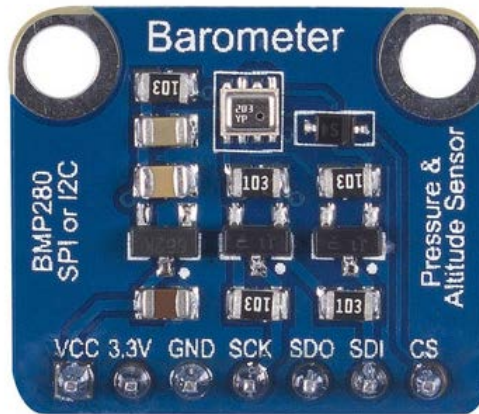
LCD Gráfico



Expansor GPIOs



Lector SD

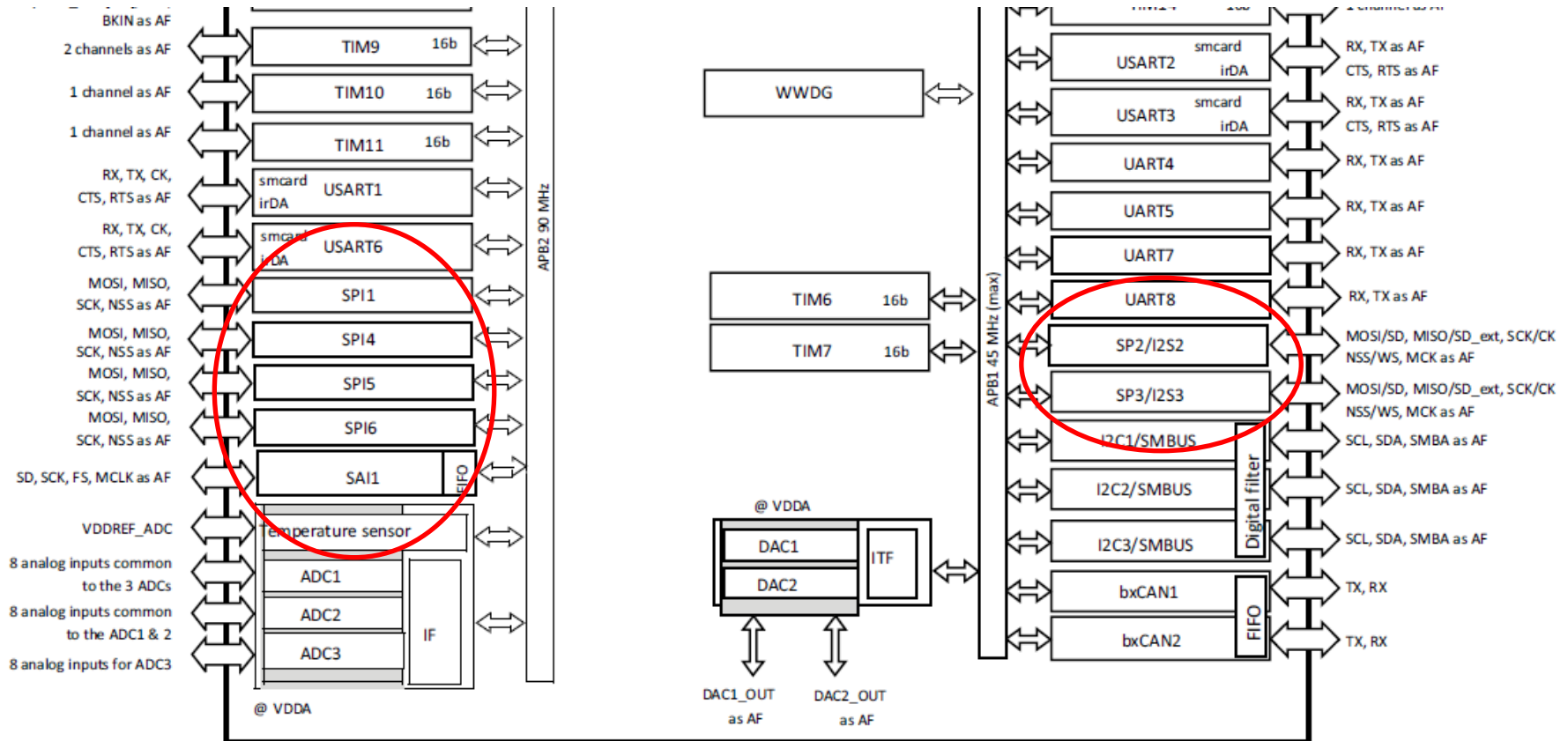


Sensor Tª/Presión



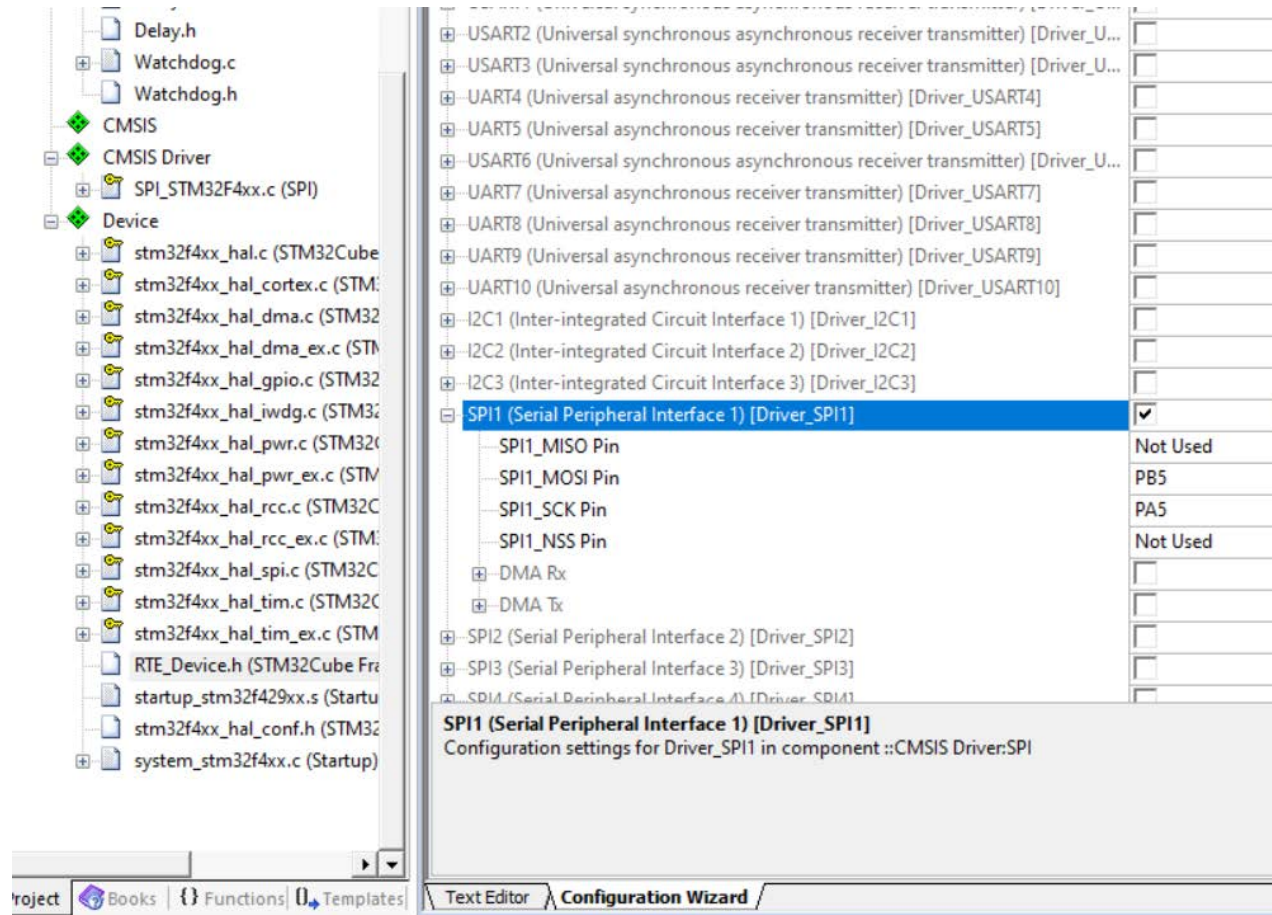
Emisor RF-433

SPI en el F429ZI



SPI en el F429ZI

Hasta 6 interfaces series síncronos (SP1-SPI6) que se pueden utilizar para dispositivos SPI y otros dispositivos serie síncronos.



Registros

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0x00	SPI_CR1	Reserved																BIDIMODE	BIDIOE	CRCEN	CRCNEXT	DFE	RXONLY	SSM	SSI	LSBFIRST	SPE	BR [2:0]			MSTR	CPOL	CPHA				
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0x04	SPI_CR2	Reserved																								TXEIE			RXNEIE	ERRIE	FRF	Reserved	SSOE	TXDMAEN	RXDMAEN		
	Reset value																									0			0	0	0	0	0	0	0	0	0
0x08	SPI_SR	Reserved																							FRE	BSY	OVR	MODF	CRCERR	UDR	CHSIDE	TXE	RXNE				
	Reset value																								0	0	0	0	0	0	0	0	1	0			
0x0C	SPI_DR	Reserved														DR[15:0]																					
	Reset value															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
0x10	SPI_CRCPR	Reserved														CRCPOLY[15:0]																					
	Reset value															0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1						
0x14	SPI_RXCRCR	Reserved														RxCRC[15:0]																					
	Reset value															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
0x18	SPI_TXCRCR	Reserved														TxCRC[15:0]																					
	Reset value															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						
0x1C	SPI_I2SCFGR	Reserved																				I2SMOD	I2SE	I2SCFG	PCMSYNC	Reserved	I2SSTD	CKPOL	DATLEN	CHLEN							
	Reset value																					0	0	0	0		0	0	0	0	0	0					
0x20	SPI_I2SPR	Reserved																							MCKOE	ODD	I2SDIV										
	Reset value																								0	0	0	0	0	0	0	0	0	1	0		

Registros

Denominación	Función
SPI_CR1/SPI_CR2	SPI Control Registers
SPI_DR	SPI Data Register
SPI_SR	SPI Status Register

Página 916 (STM32F429-REFERENCE-MANUAL.pdf)