1. Develop and simulate a synthesizable VHDL description of an 8 bit register with the following specifications:
    a. Parallel data input
    b. Parallel data output
    c. Asynchronous active low *reset*
    d. *enable* input (active high)
    e. *rl* (rotate left) input; when set to '1' makes a one position rotation to the left (shift left one position reentering the most significant bit as the less significant bit) with the active clock edge if enable is active; when set to '0' data input is loaded with the active clock edge if enable is active.

2. Develop and simulate a synthesizable VHDL description of a cyclic BCD decrementer with the following specifications:
    a. Asynchronous active low reset sets the counter to 9.
    b. *enable* input (active high). When set to '1' value is decreased by 1 at each active clock edge; when set to '0', value is stacked.
    c. Decreasing value 0 sets the counter to 9.