Computer Architecture

Caches 1

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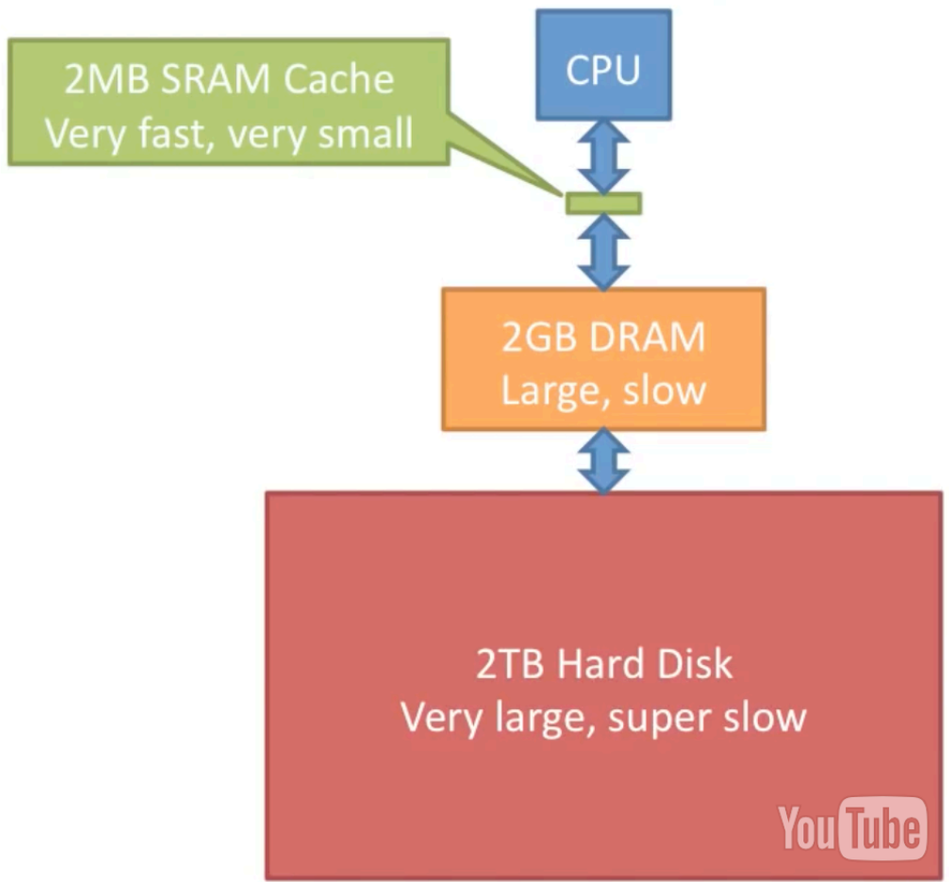

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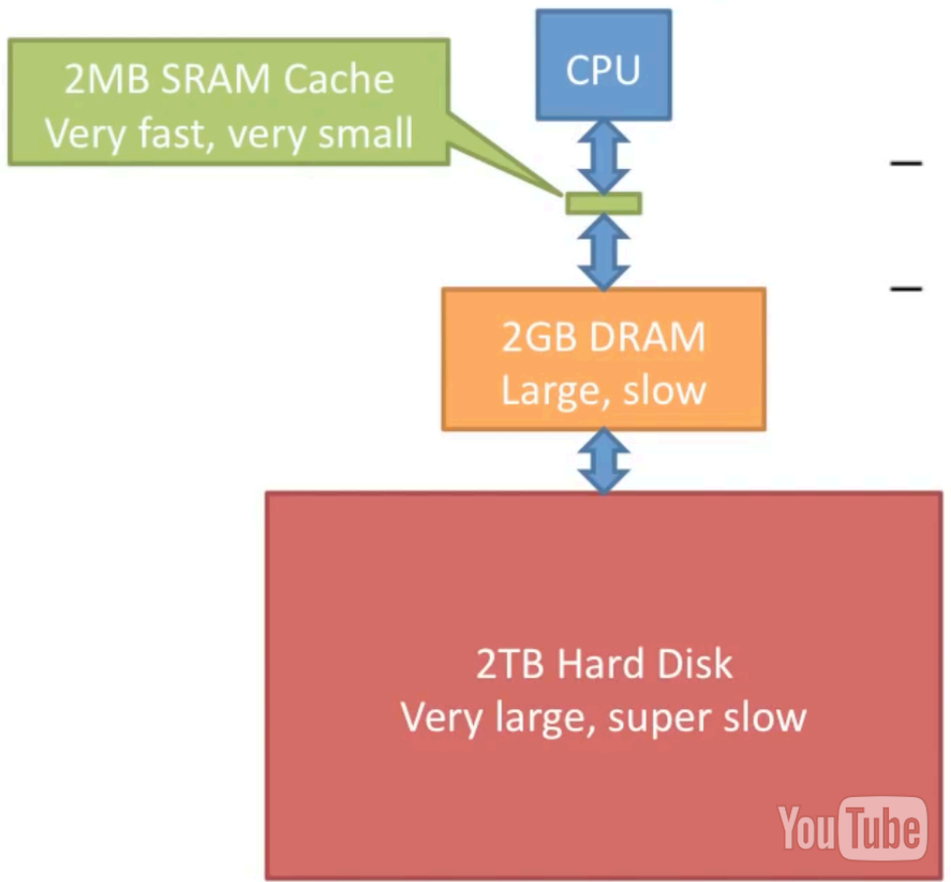
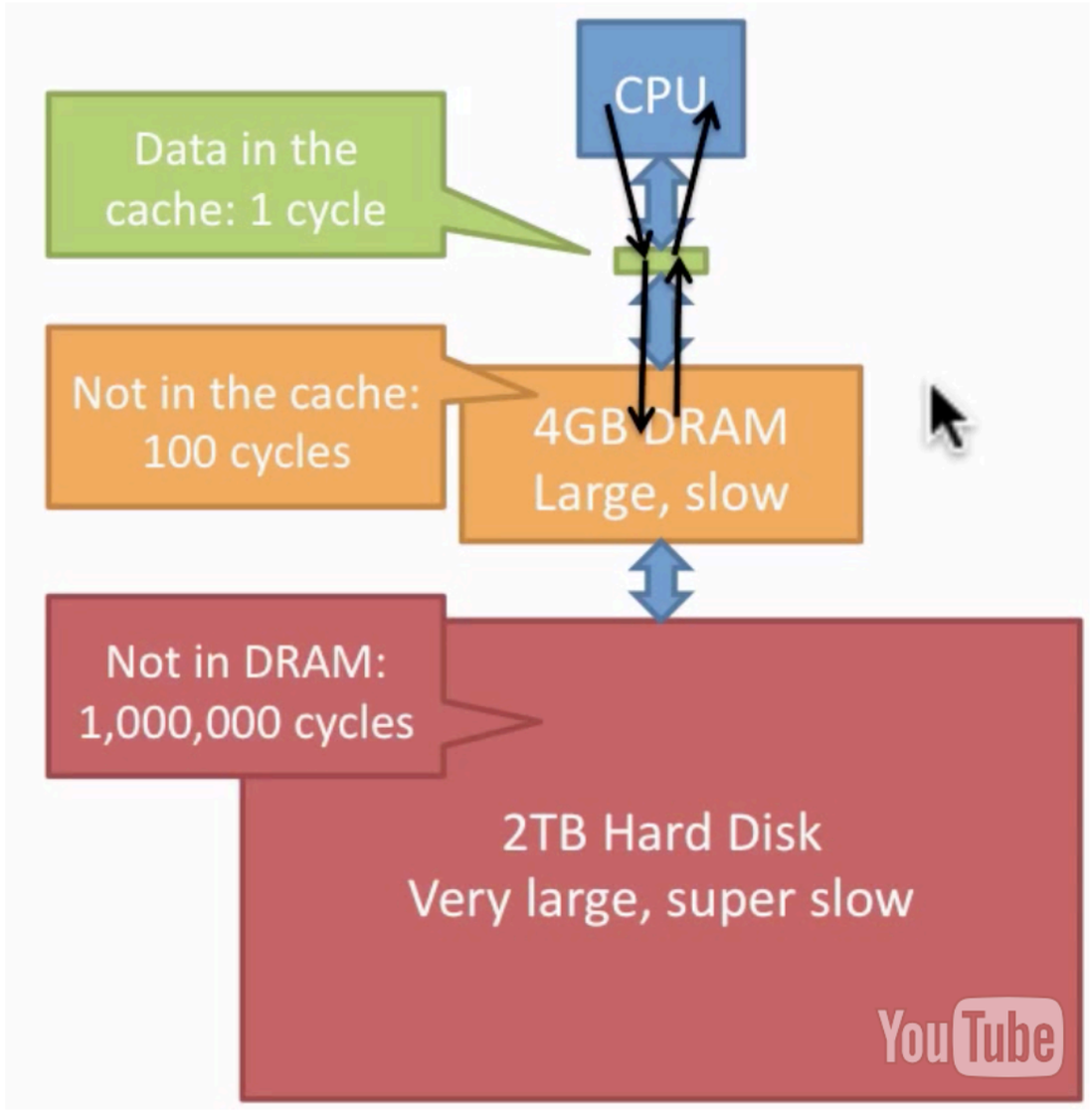
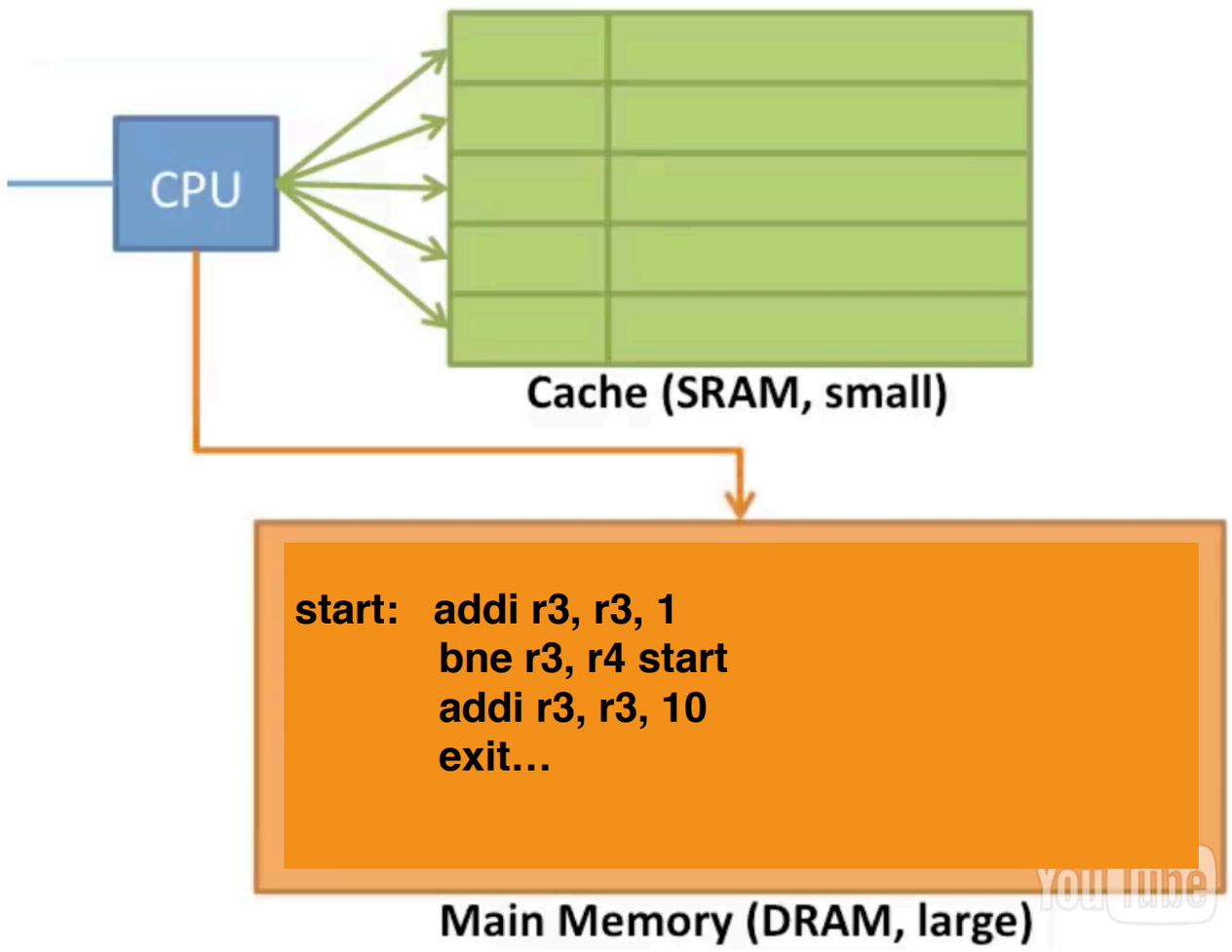
How to do this???

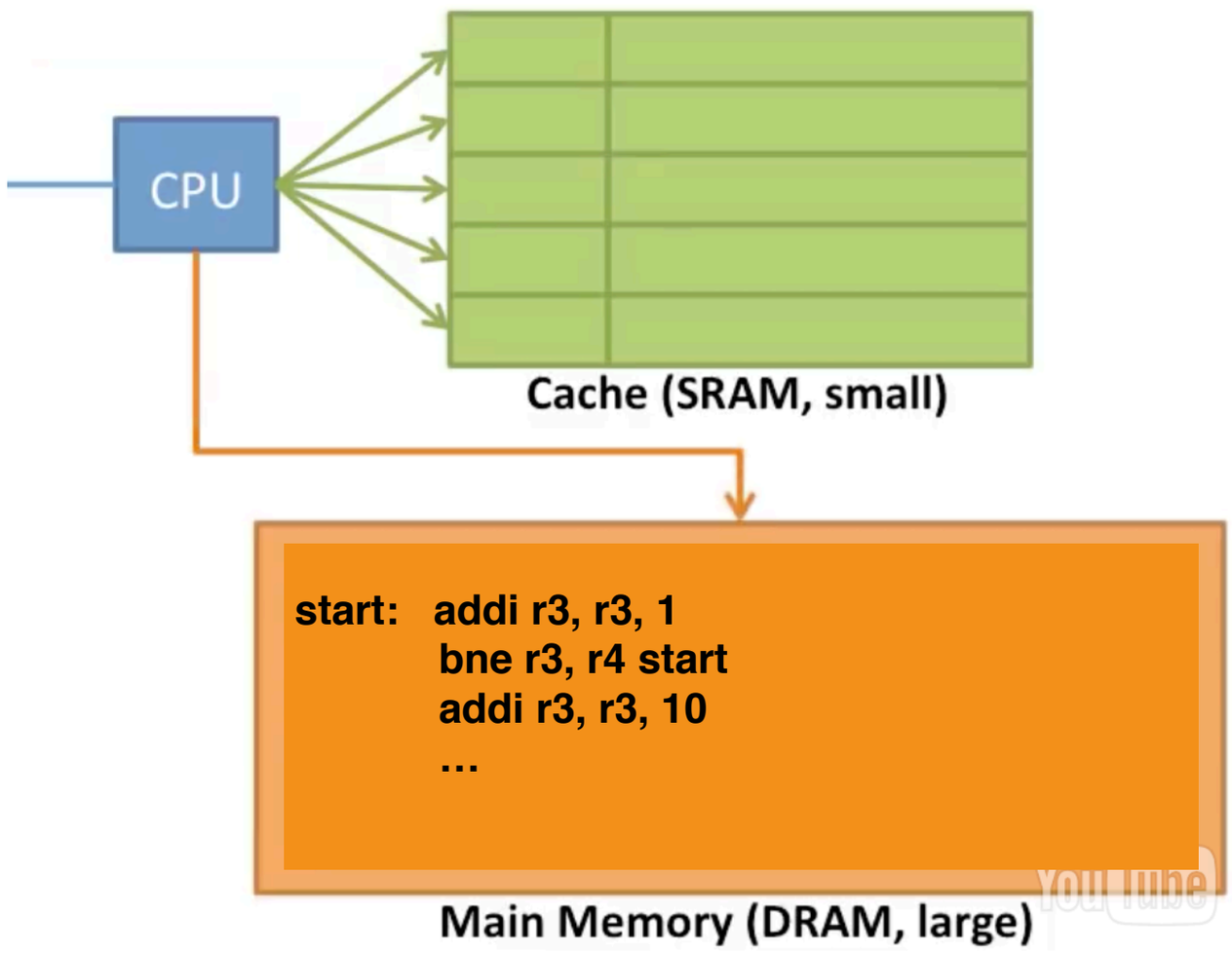
We define the memory hierarchy…



- Try to keep the **important data** in the **fast memory**
- Move the **unimportant data** to the **slow memory**


CPU
Data in the cache: 1 cycle
Not in the cache: 100 cycles
4GB DRAM
Large, slow
Not in DRAM: 1,000,000 cycles
2TB Hard Disk
Very large, super slow
YouTube


CPU
Cache (SRAM, small)
start: addi r3, r3, 1
bne r3, r4 start
addi r3, r3, 10
exit…
Main Memory (DRAM, large)

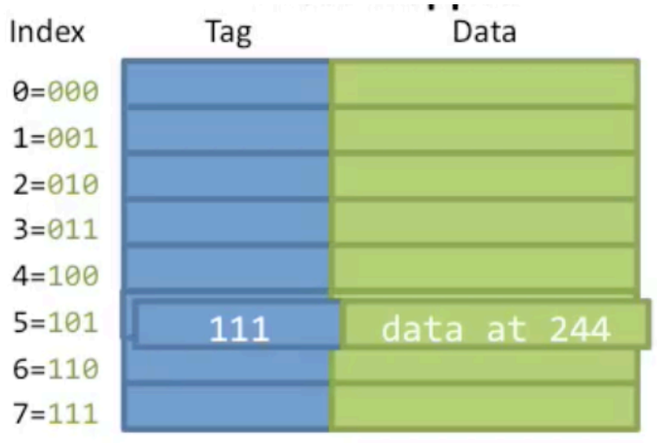


How many hits in the cache there will be when this set of instructions is executed? Assume that initial values of r3 and r4 are 0 and 10 respectively.

Question: Identify what type of caching is demonstrated in the following illustrations.

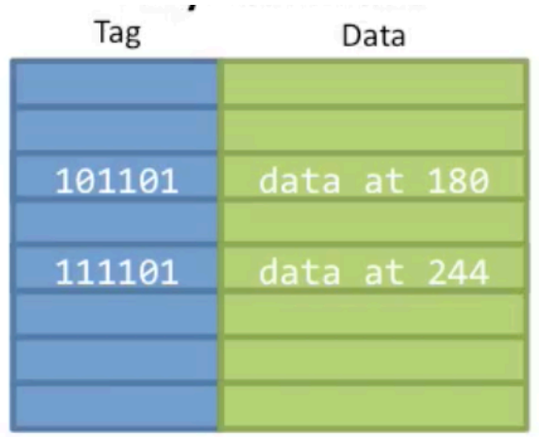
180=10110100
244=11110100

A



180=10110100
244=11110100

B



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C

Question: Identify what type of caching is demonstrated in the following illustrations.

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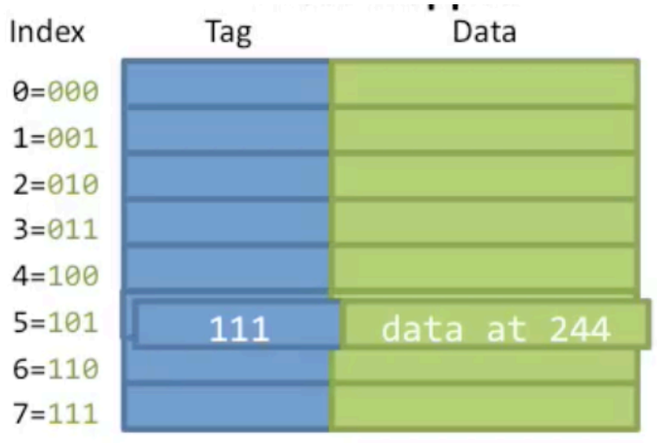
Set-Associative



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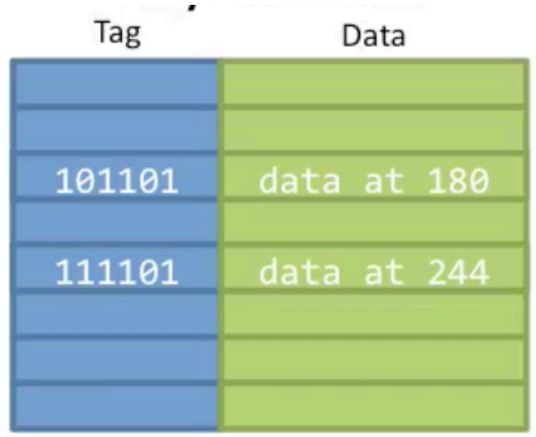
Direct-Mapped



180=10110100
244=11110100

Full Associative

Note:

- Last topic to watch: **Caches 1 (lecture/quiz Monday 5/15)**

- Final Exam Schedule:

- Thursday, 5/25 (1-3PM) Block A

- Thursday 5/25 (3:30-5:30PM) Block B