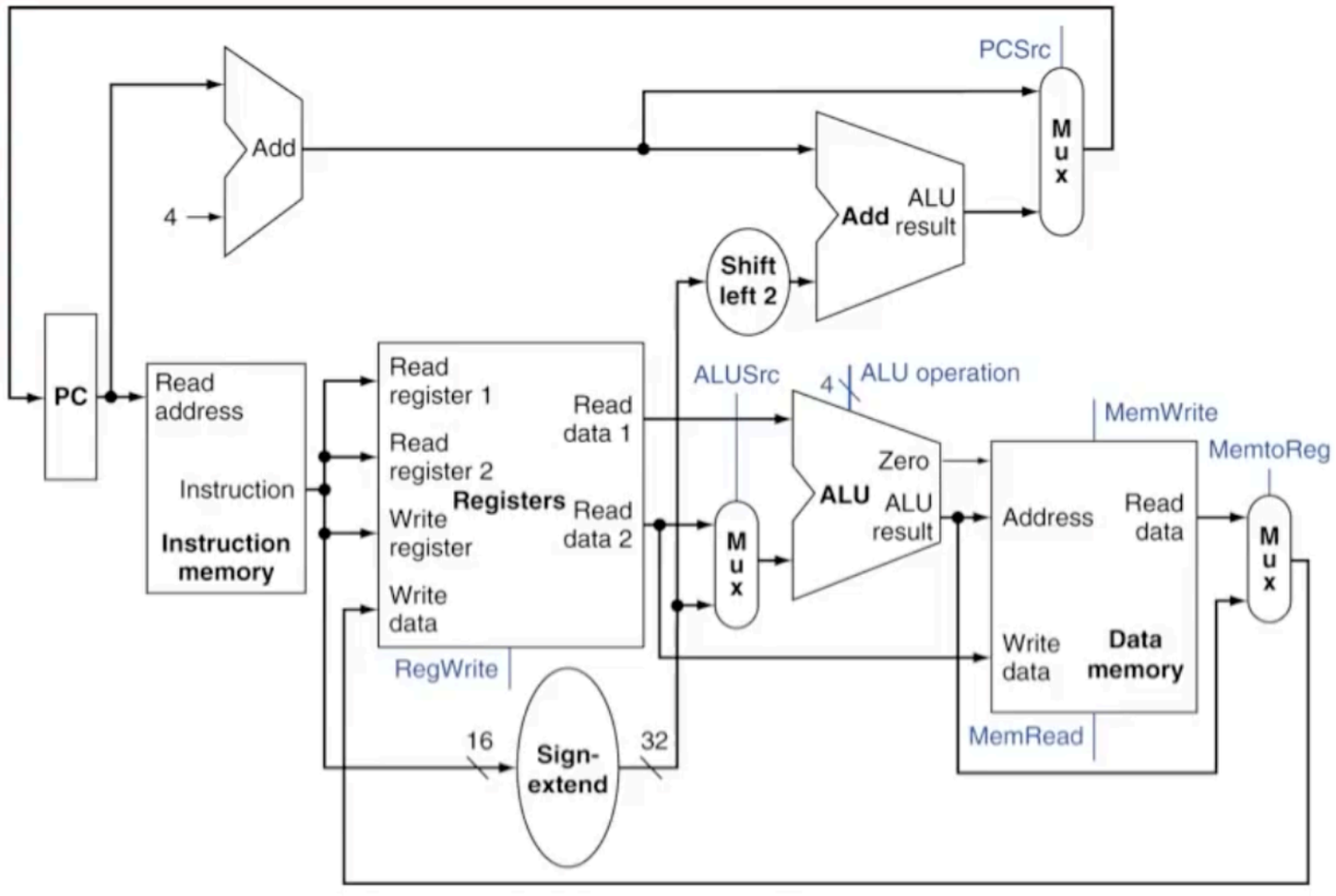
Computer Architecture

Processor Pipelining

Single-cycle datapath



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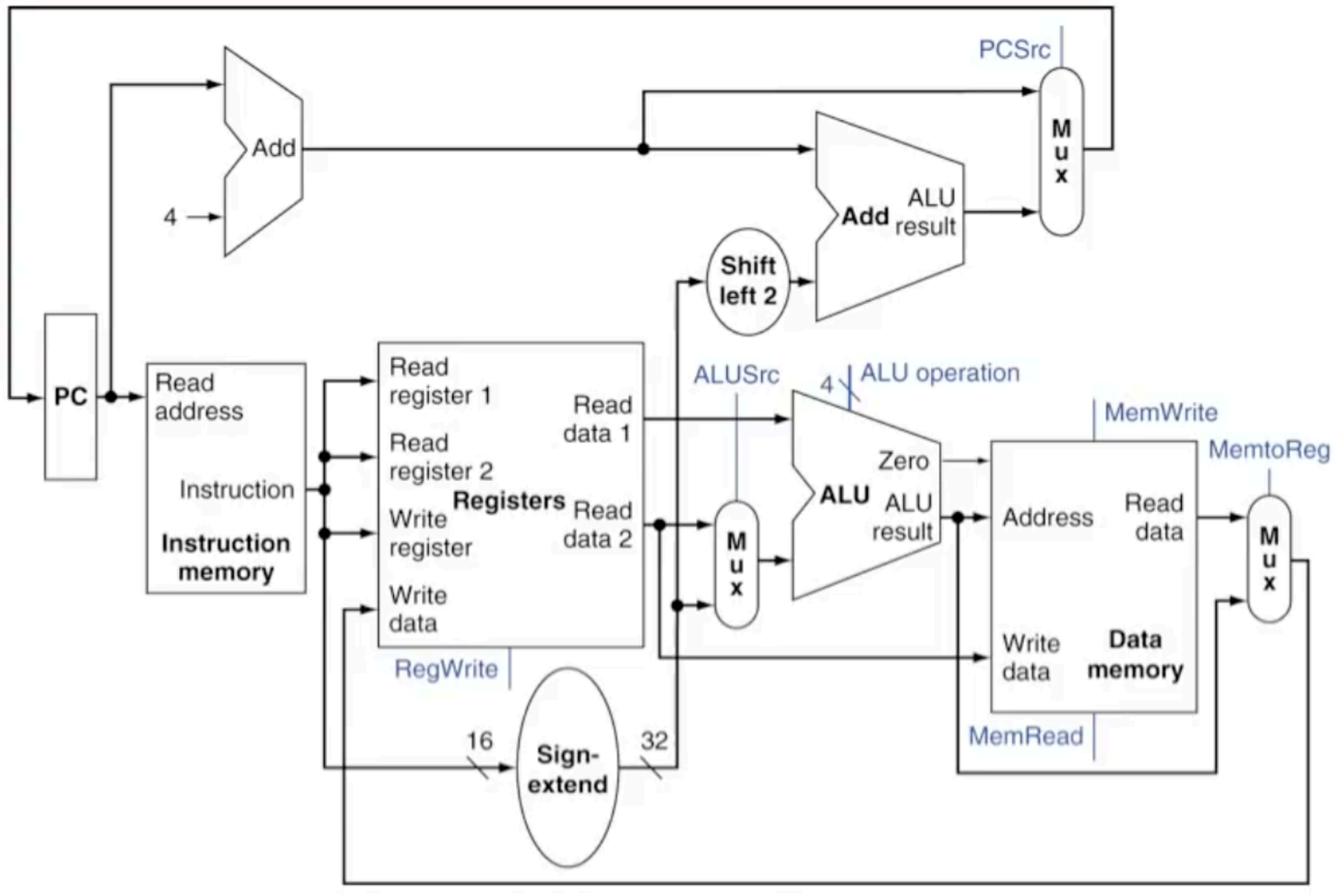

The speed of a processor is determined by what?

A. slower instruction

B. faster instruction

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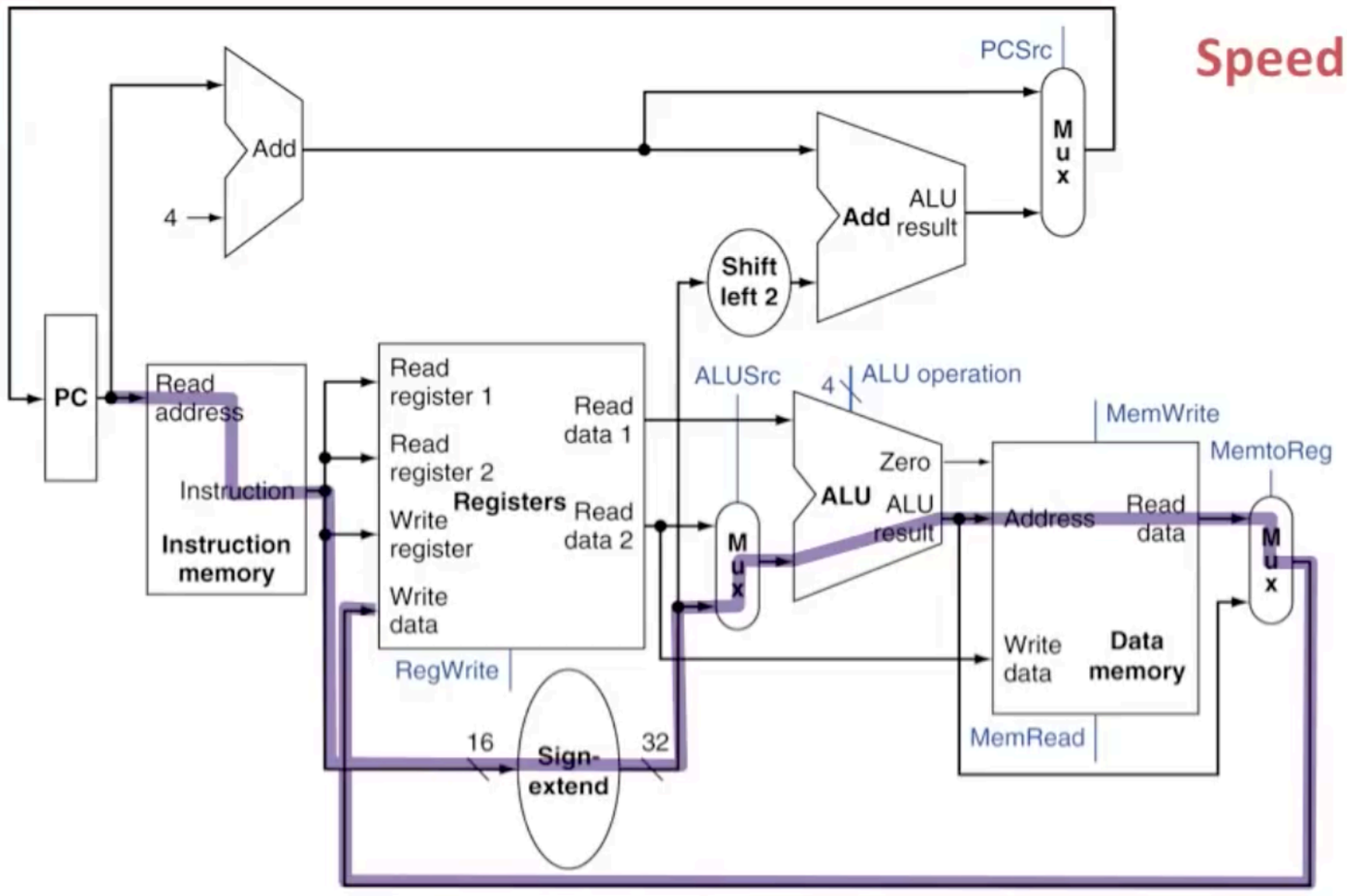
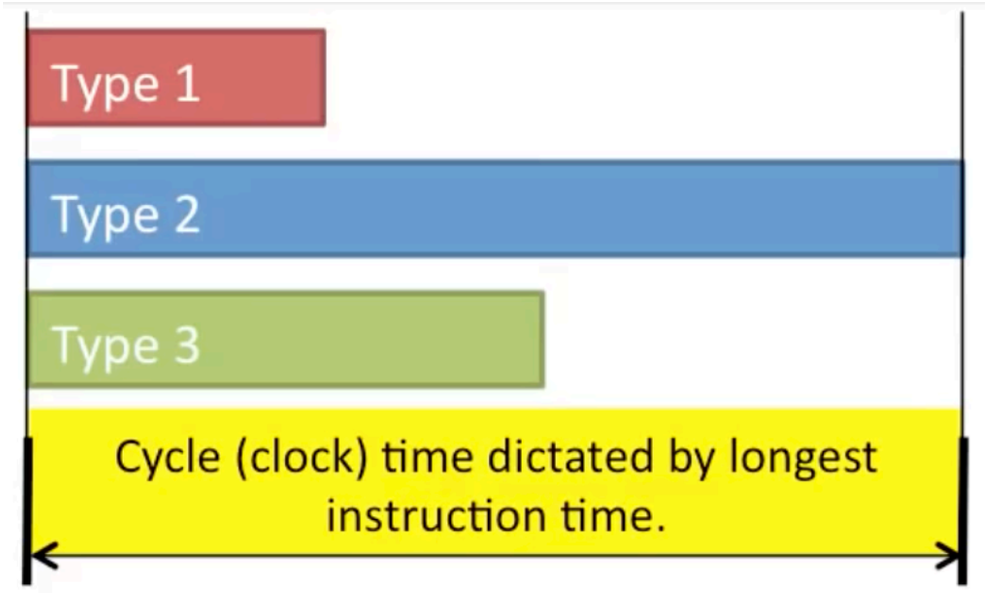
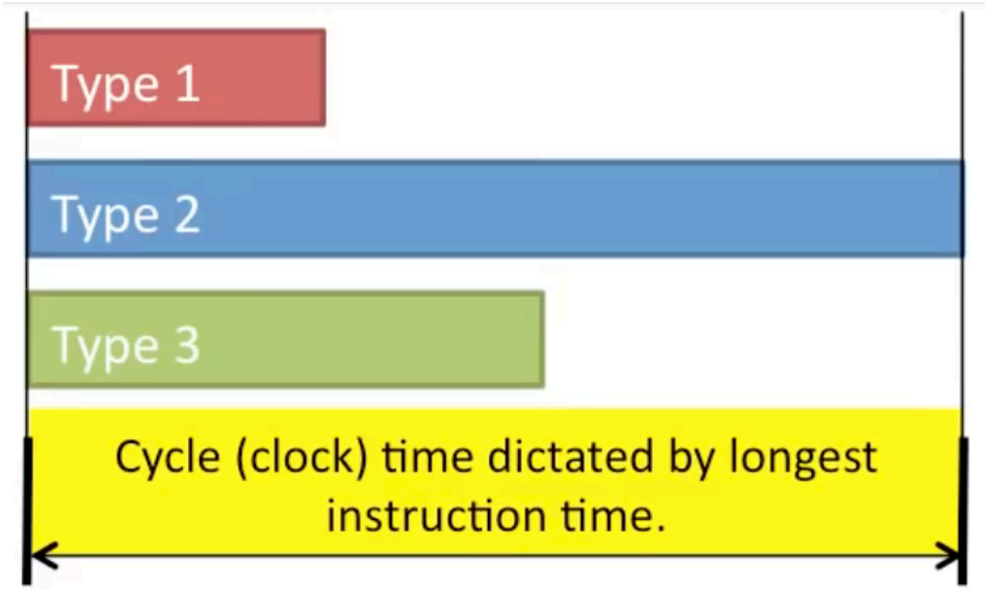


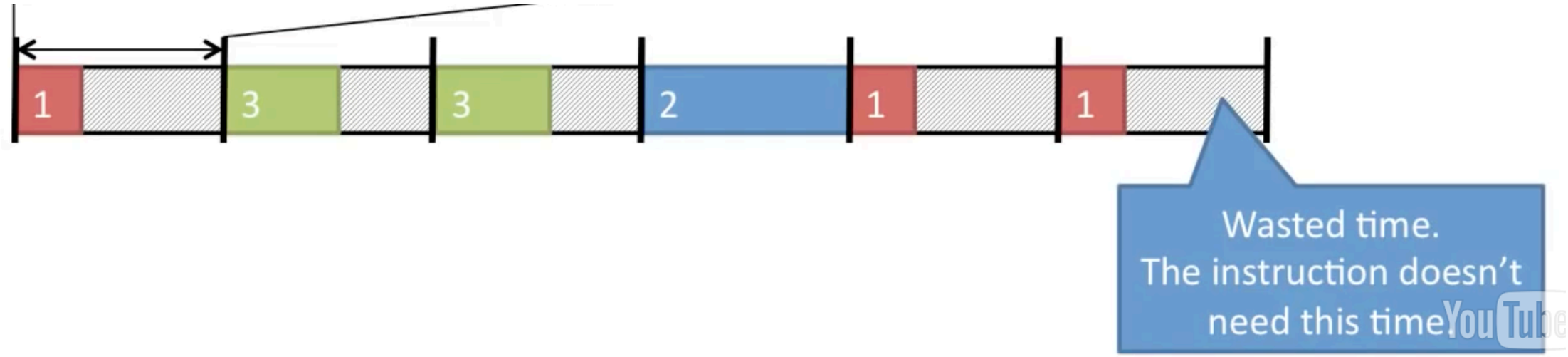
Speed limited by the slowest path

Single-cycle execution times



Single-cycle execution times





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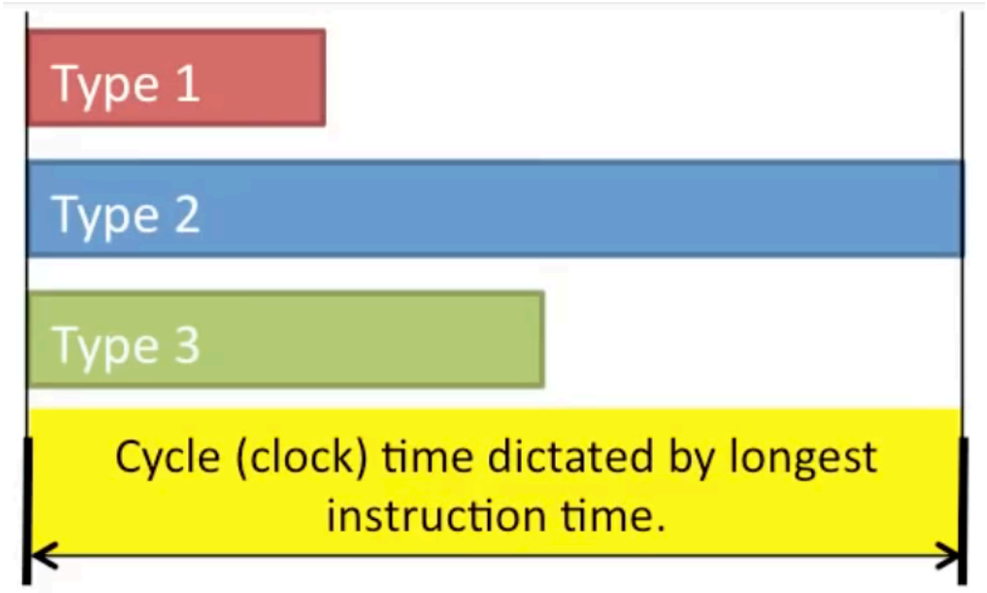

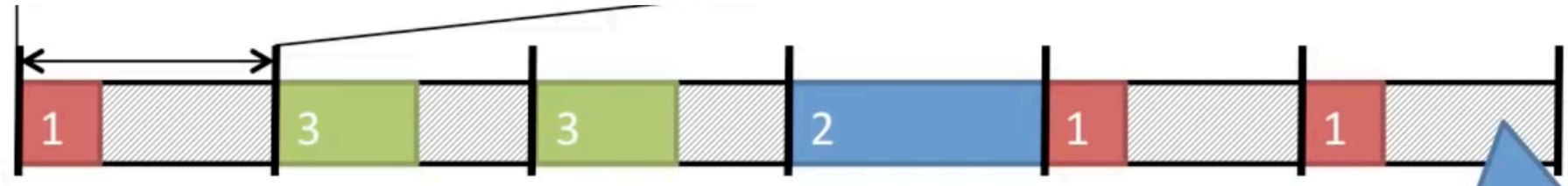

- Slowest instruction determines cycle time
- Much of the time is wasted

Wasted time.
The instruction doesn't need this time.

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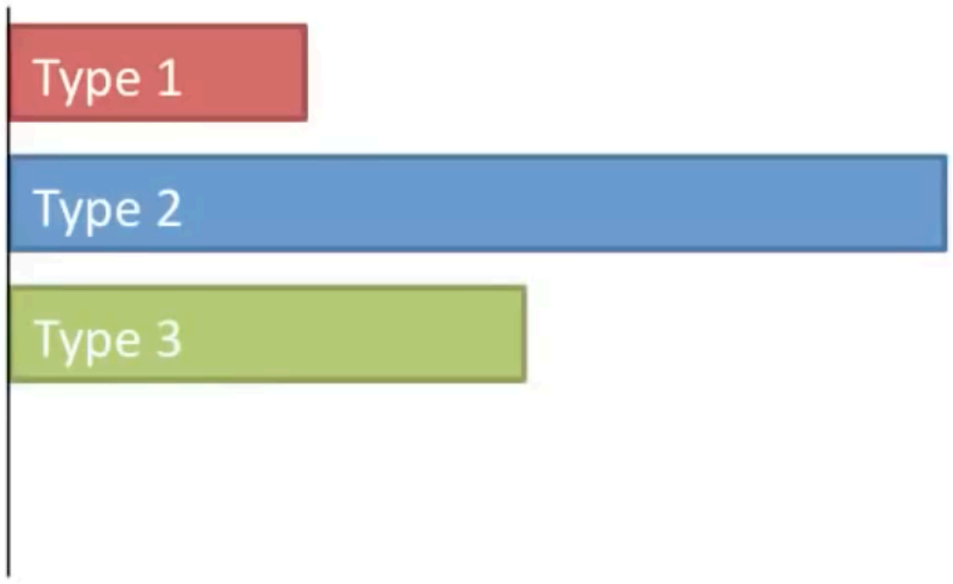

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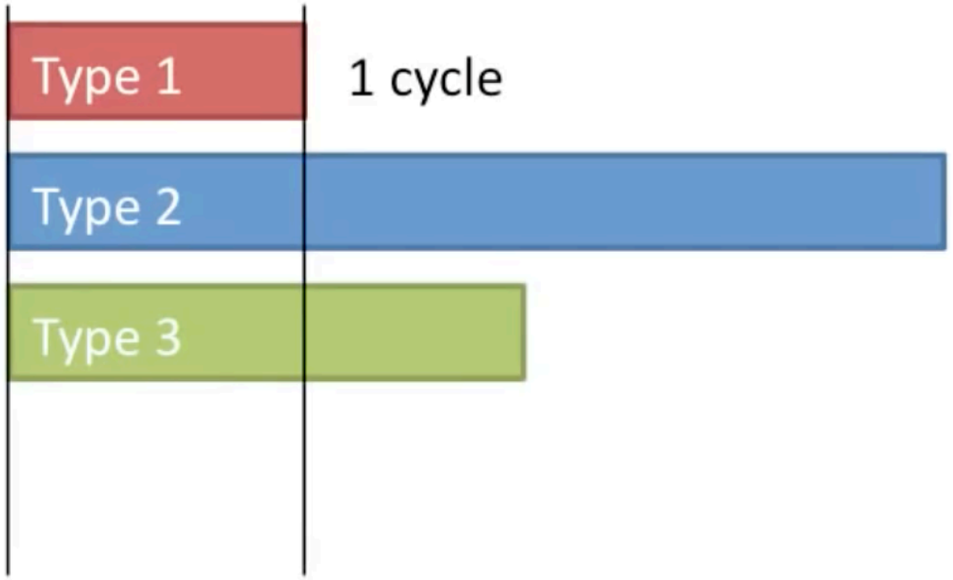

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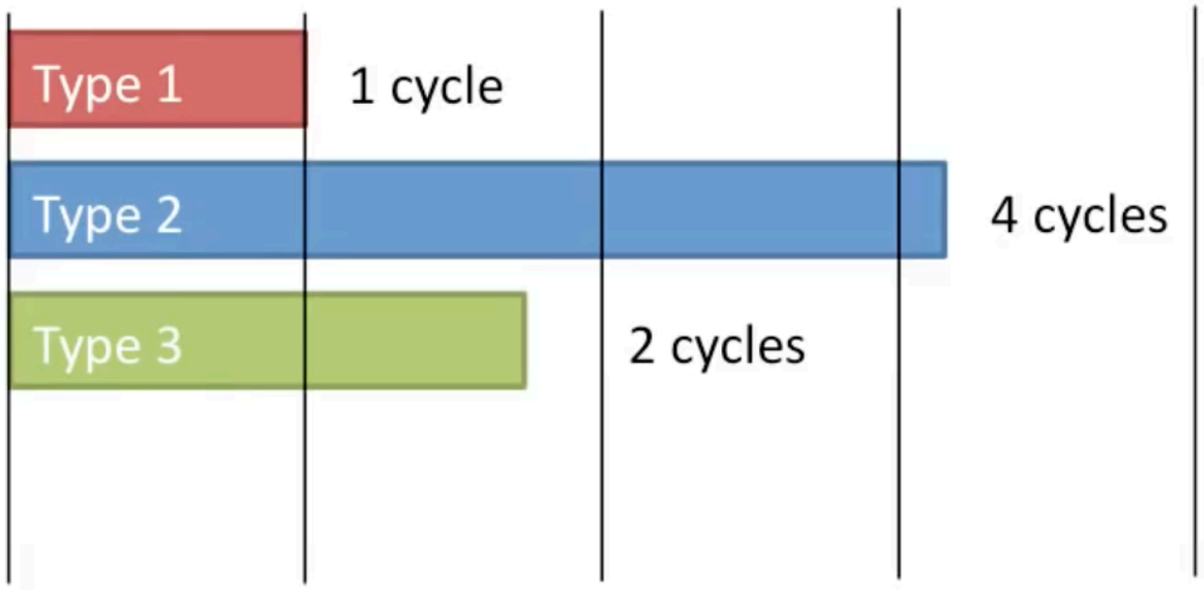

But very complicated to keep track of how long each instruction runs.

Much less wasted time

Which of the following statement is NOT necessarily TRUE?

A. In a single-cycle processor, the longest instruction determines the speed of the processor.

B. In a multi-cycle processor, the clock cycle is determined by the fastest instruction.

C. In a pipelined processor, the slowest instruction determines the speed of the processor.

D. None of the above

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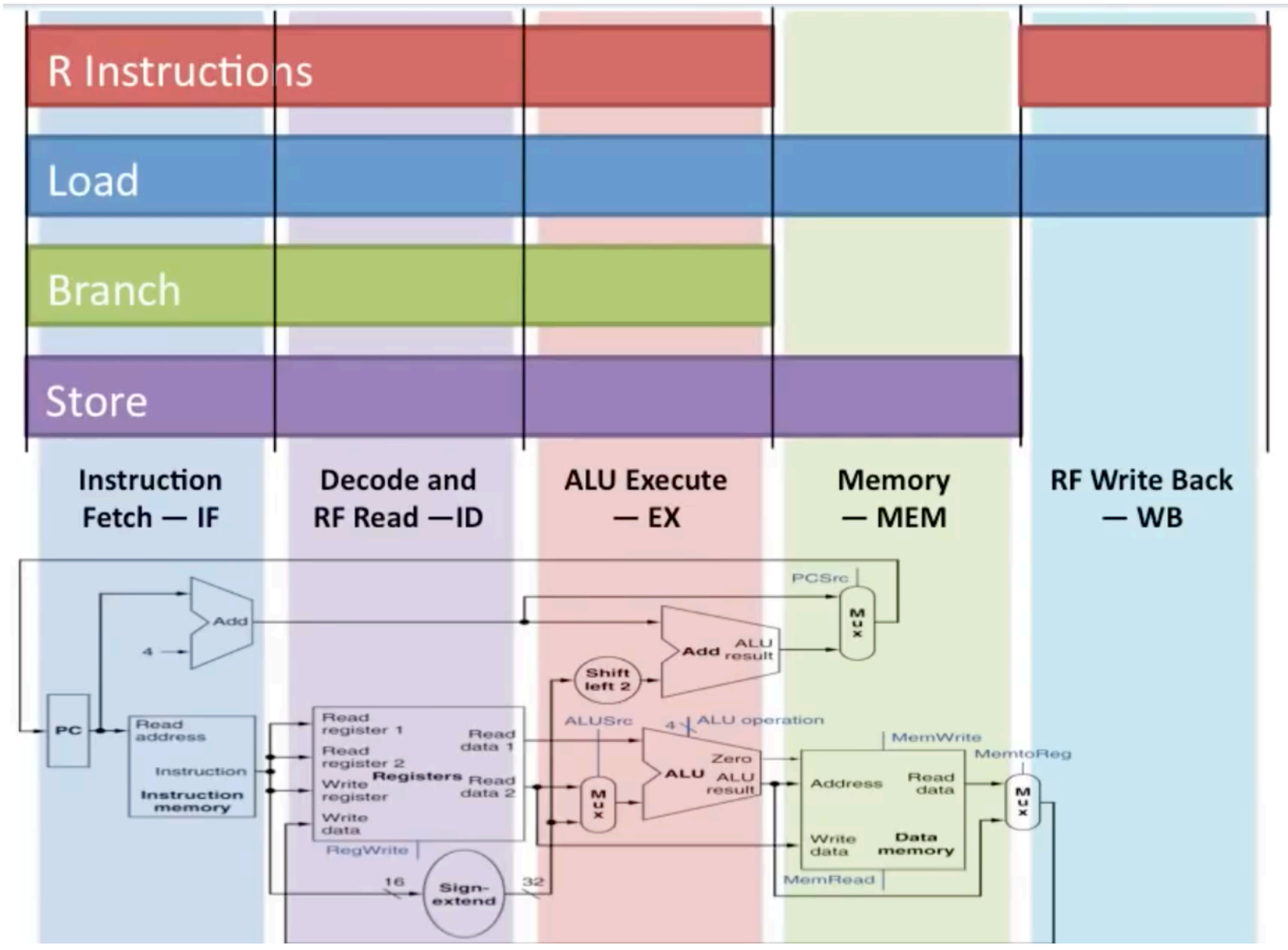
MIPS 5 stage pipeline



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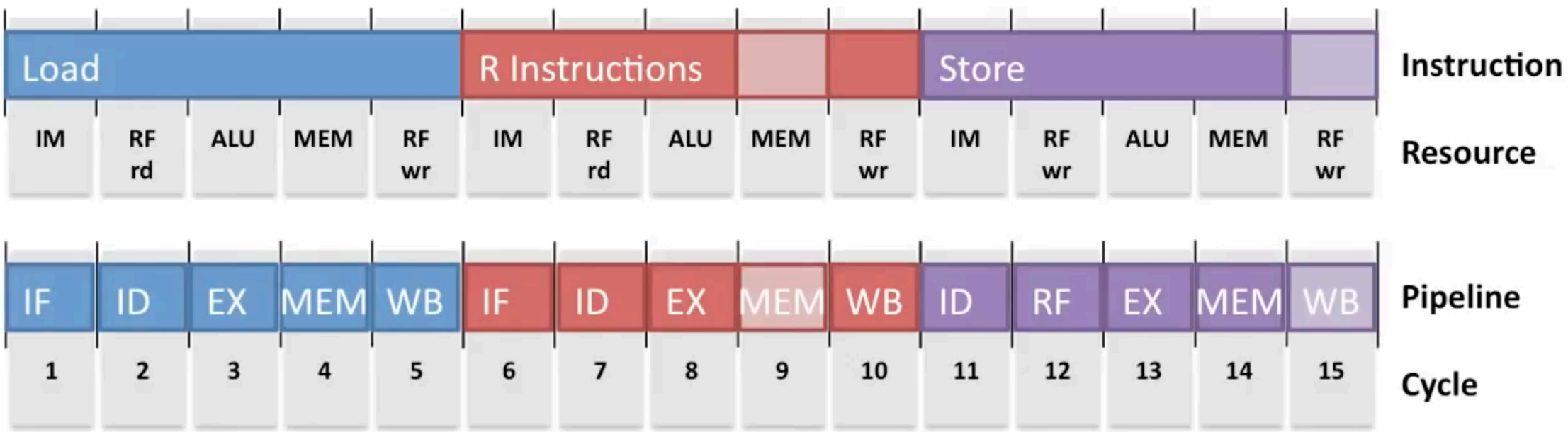
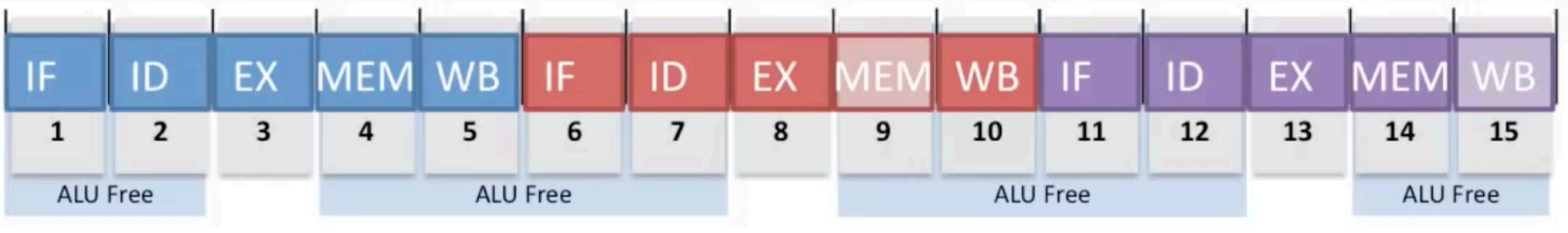


What is the ALU doing in cycle 7?

Pipelining to do work in parallel…

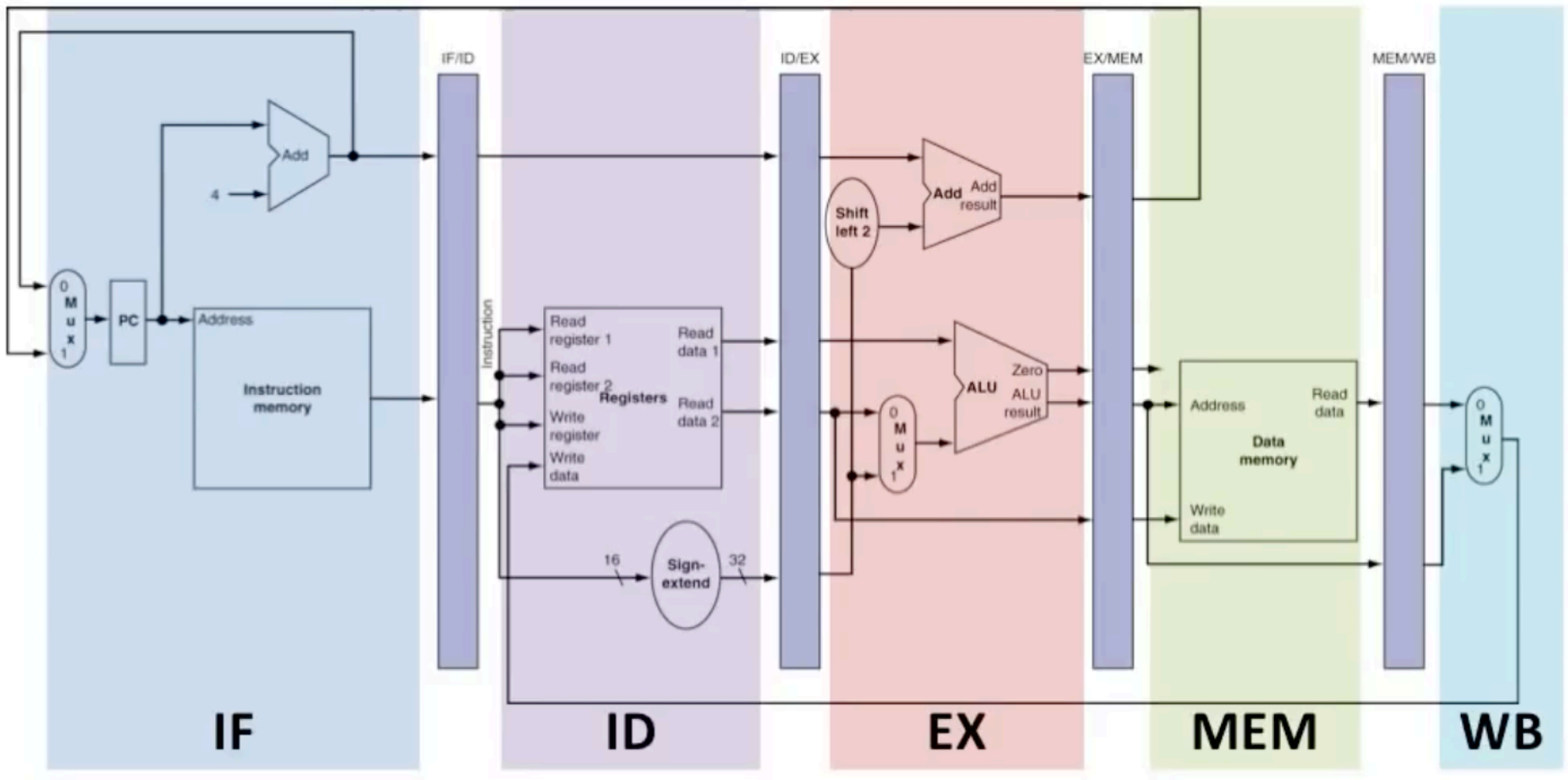


This is what we want from pipelining:
Use all parts of the processor for different instructions at the same time.

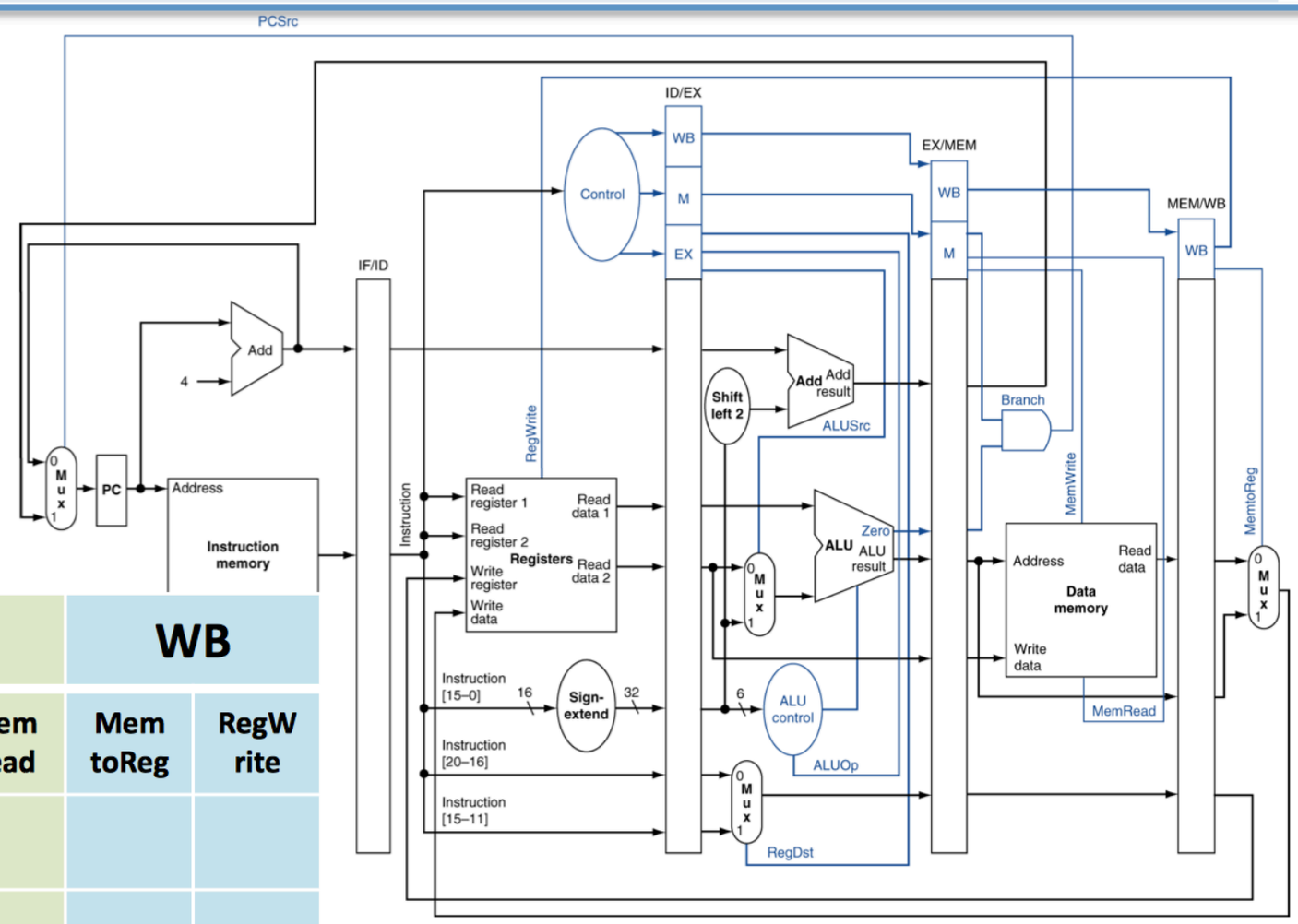
(This is why dividing up instructions into 5 phases was helpful.)

Differentiate throughput and latency.

Why is there a need to put pipeline registers?



- What are the control signals for add, load, and bne?
- What do they do?
- Fill in the table below specifying the value and meaning. (For ALUOp you can write the name of the op such as “Add”.)



		EX			MEM			WB	
	Inst. Type	ALU Src	Reg Dst	ALU Op	Branch	Mem Write	Mem Read	Mem toReg	RegW rite
add									
load									
bne									