Computer Architecture

Processor Control and Datapath

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1. Instruction access/fetch
2. ALU operations
3. Memory access/operations

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    - *figure out which instruction and load it*
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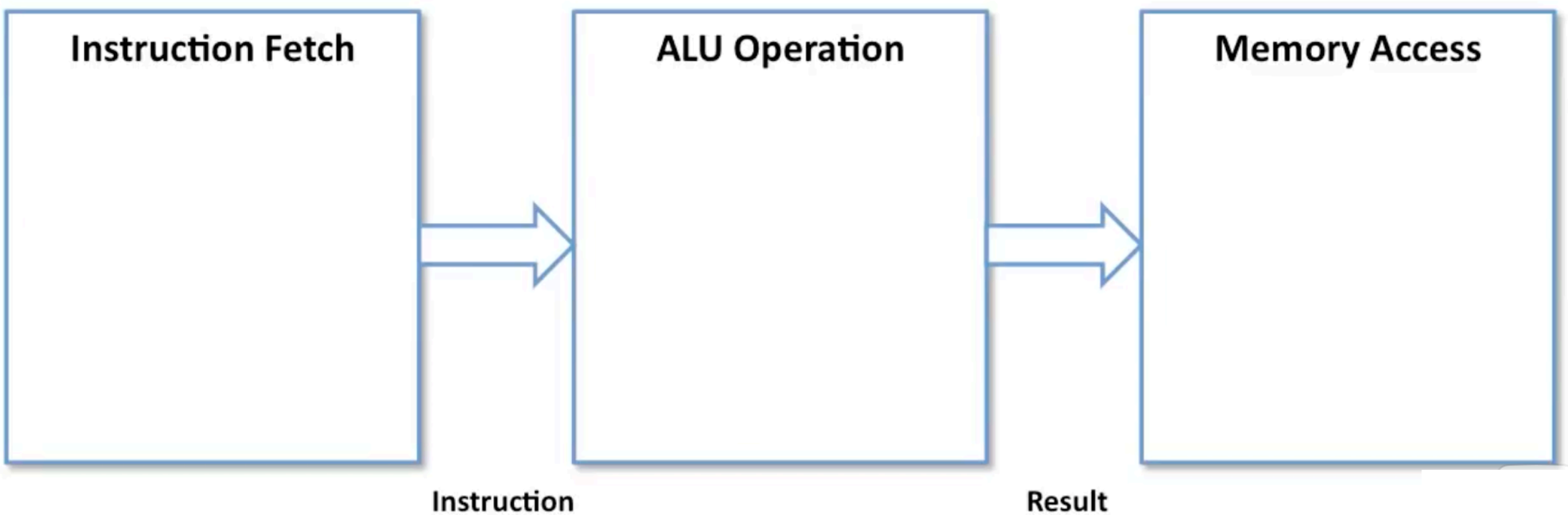

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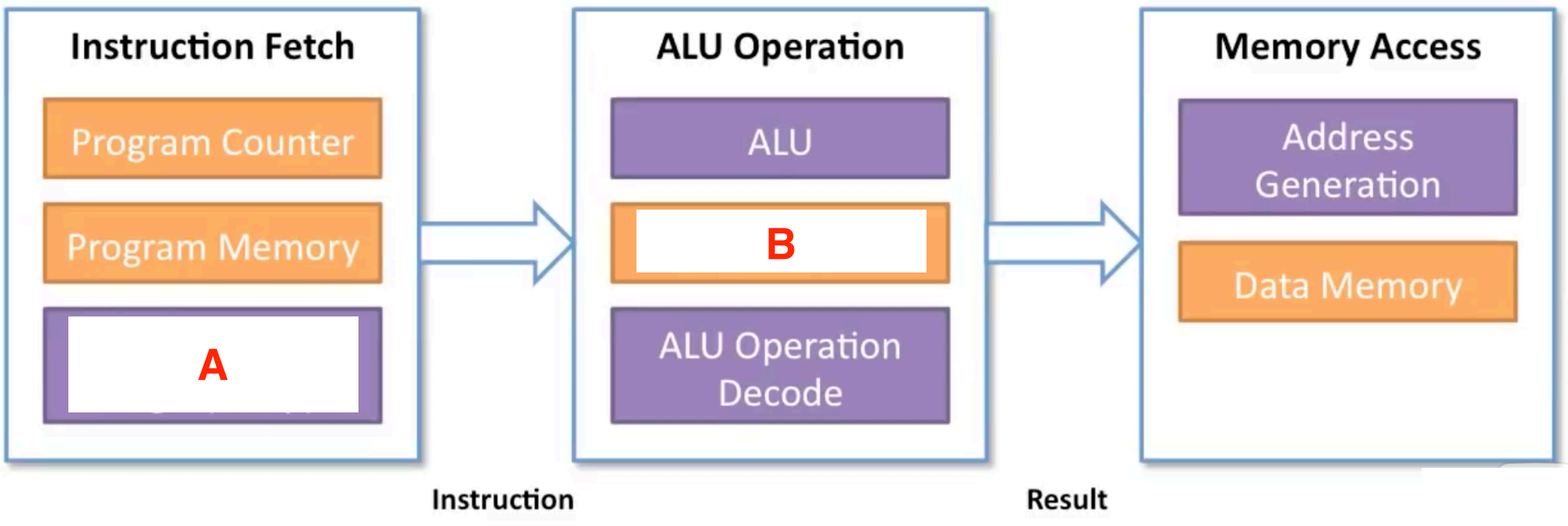

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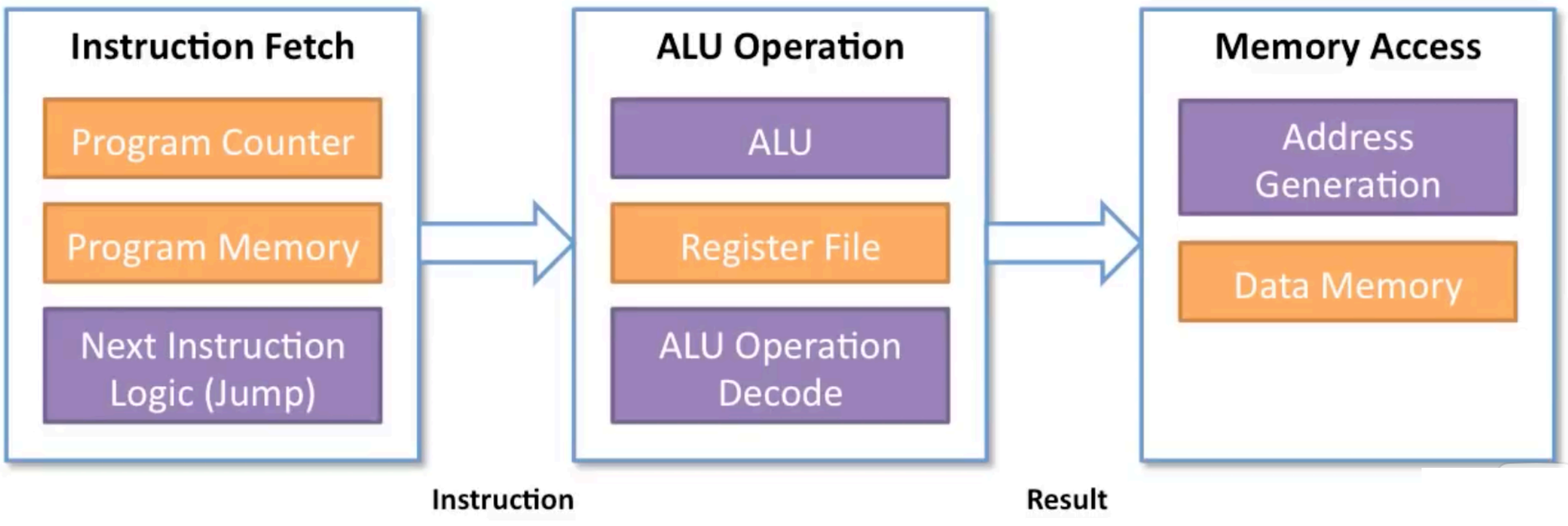
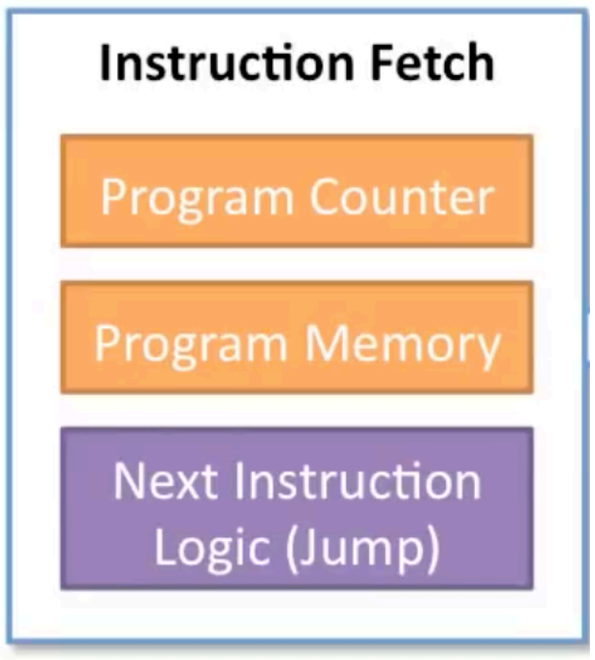


The Instruction Fetch



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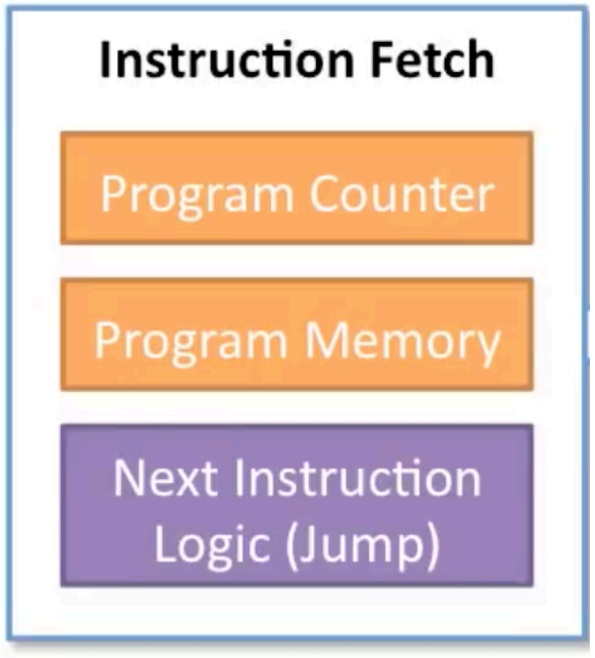

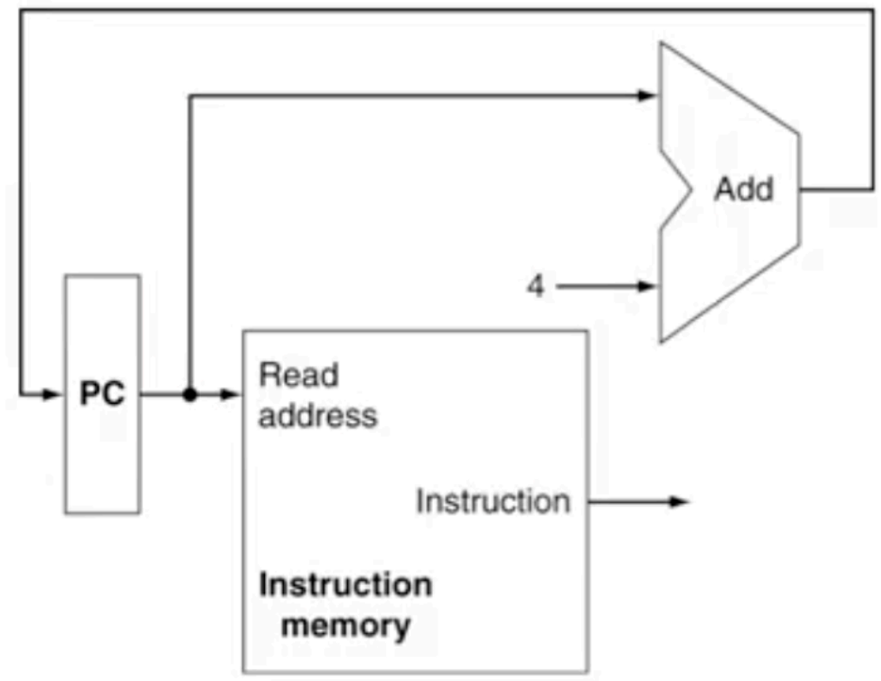

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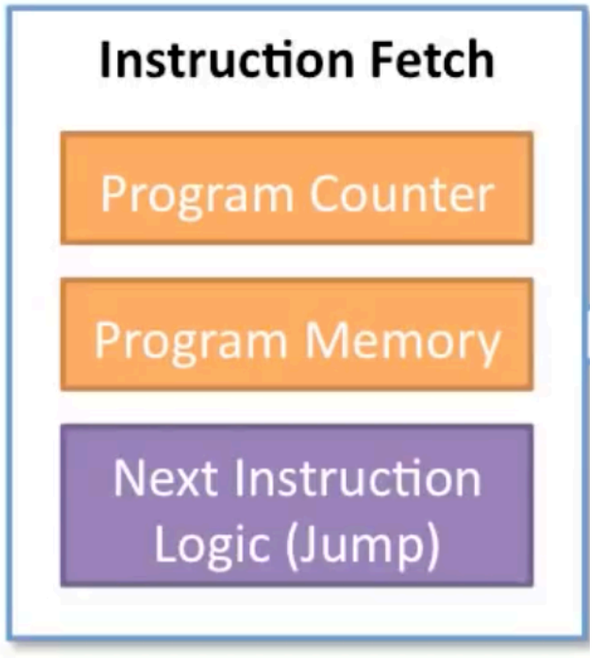

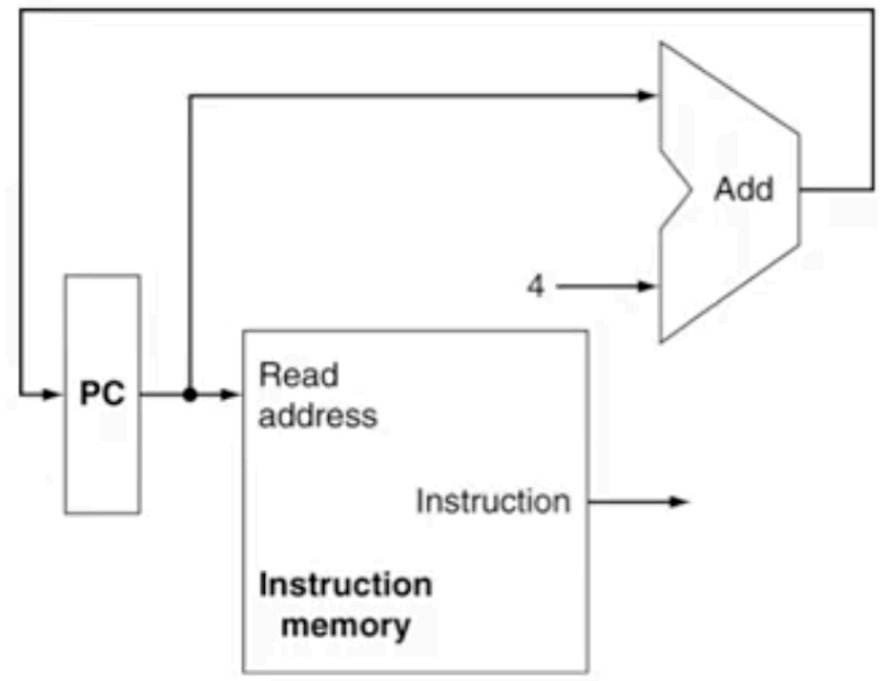

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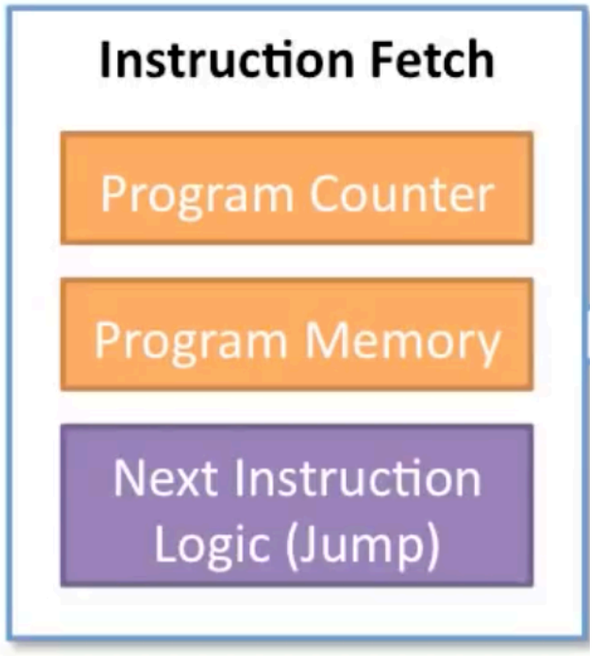

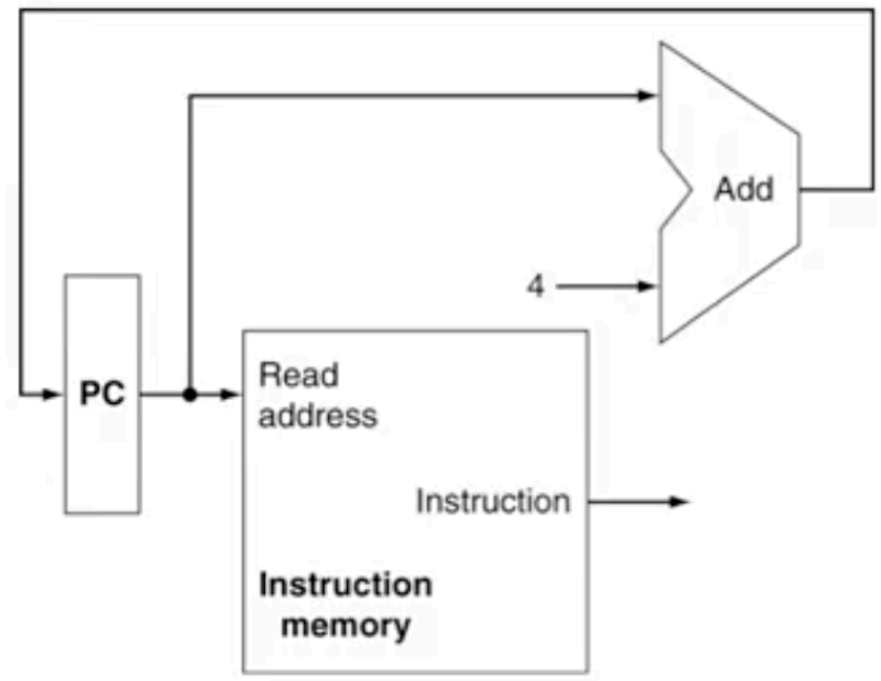

0	add R3, R0, R1
4	sub R4, R2, R3
8	sub R5, R2, R1
12	j 4
16	addi R6, R2, 12

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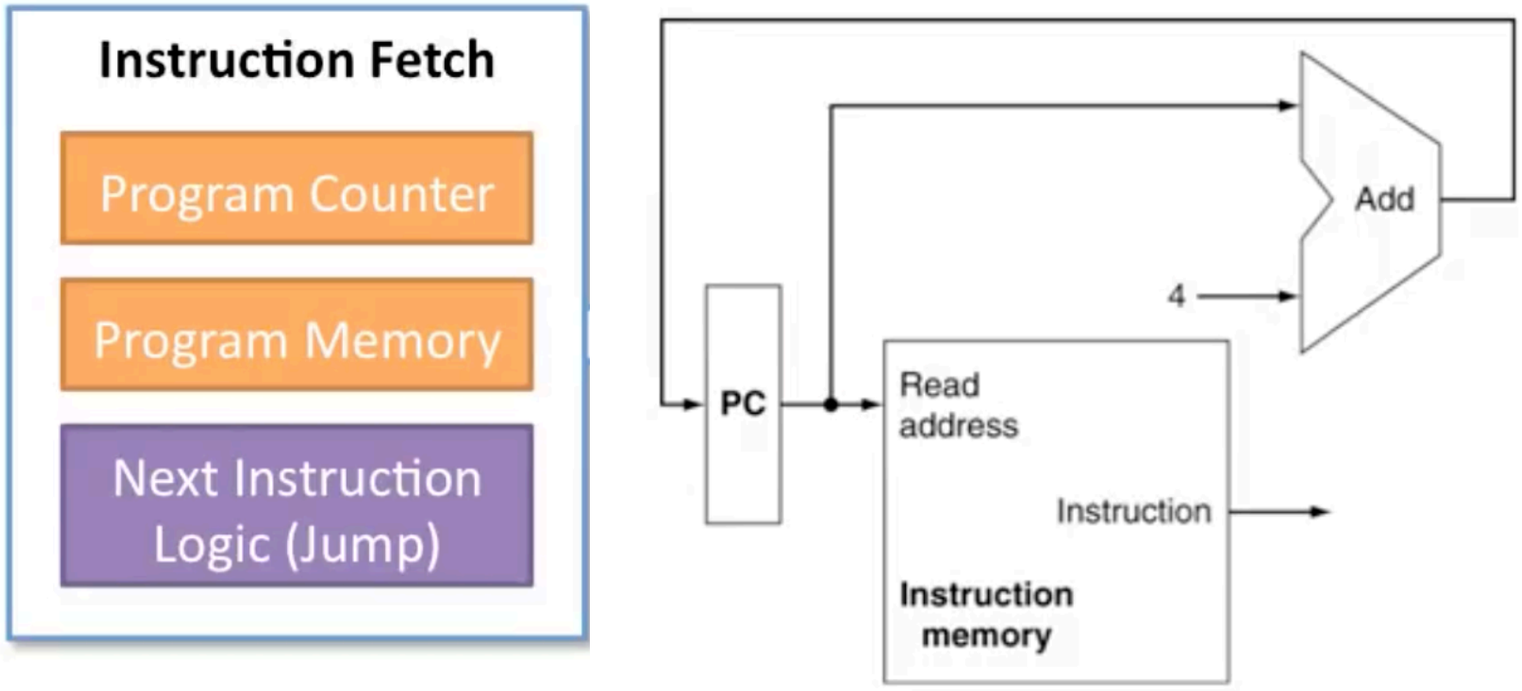

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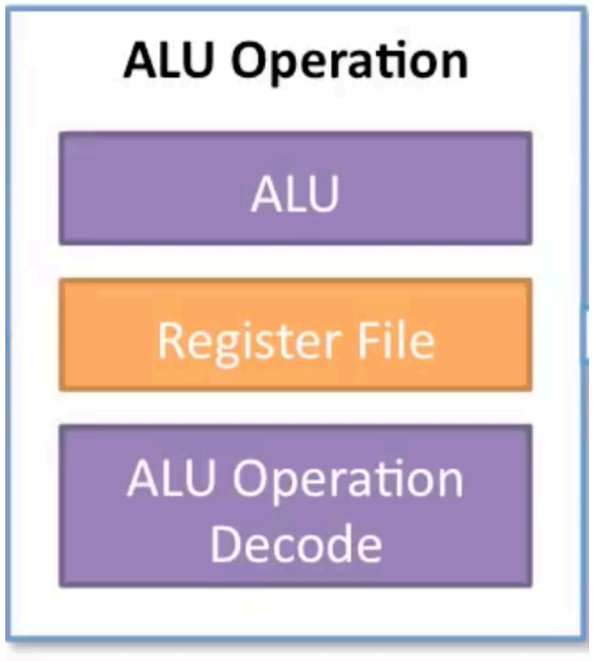

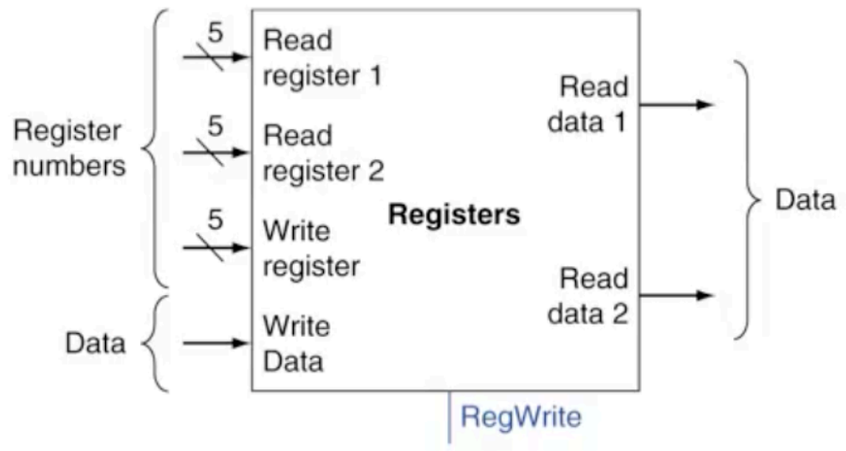

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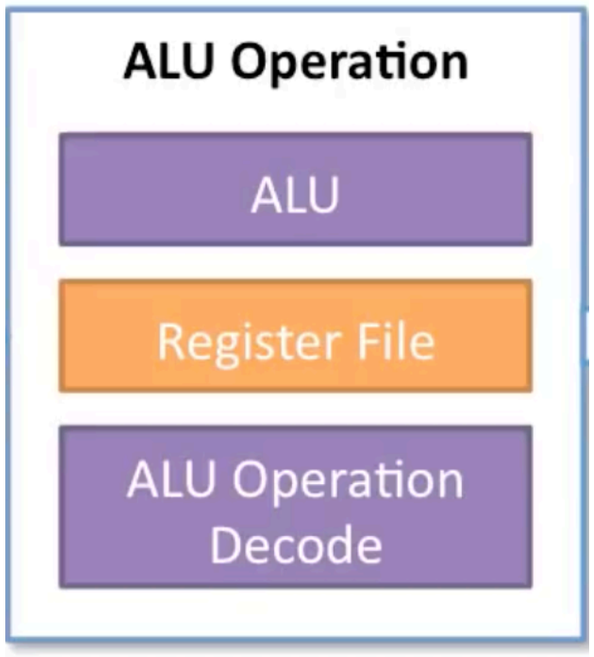

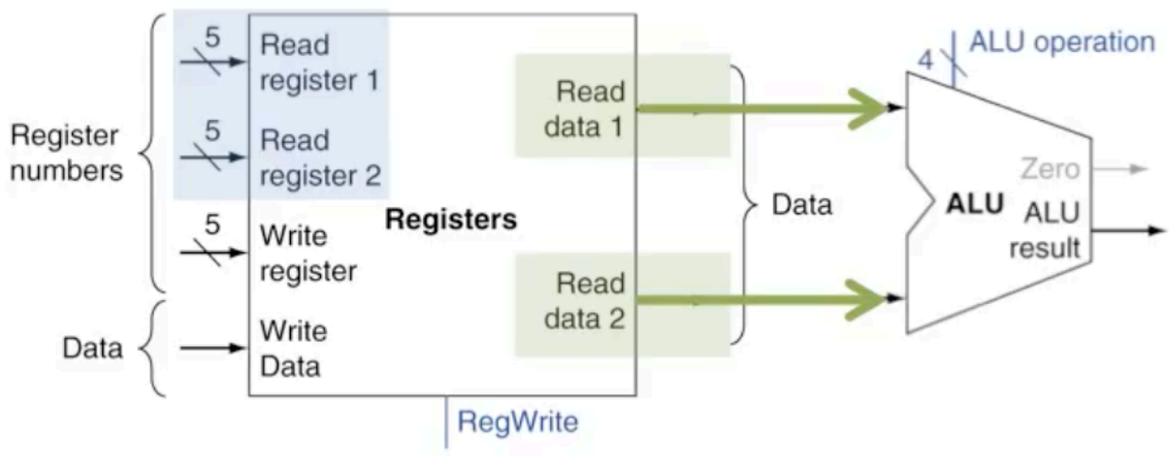

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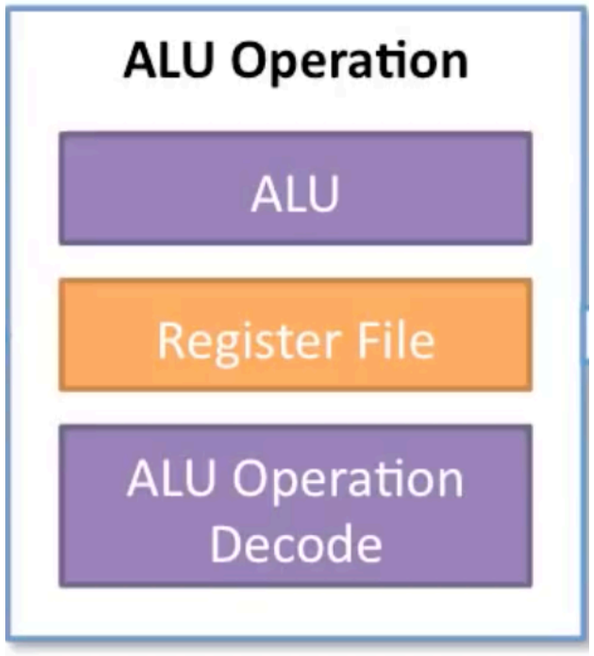
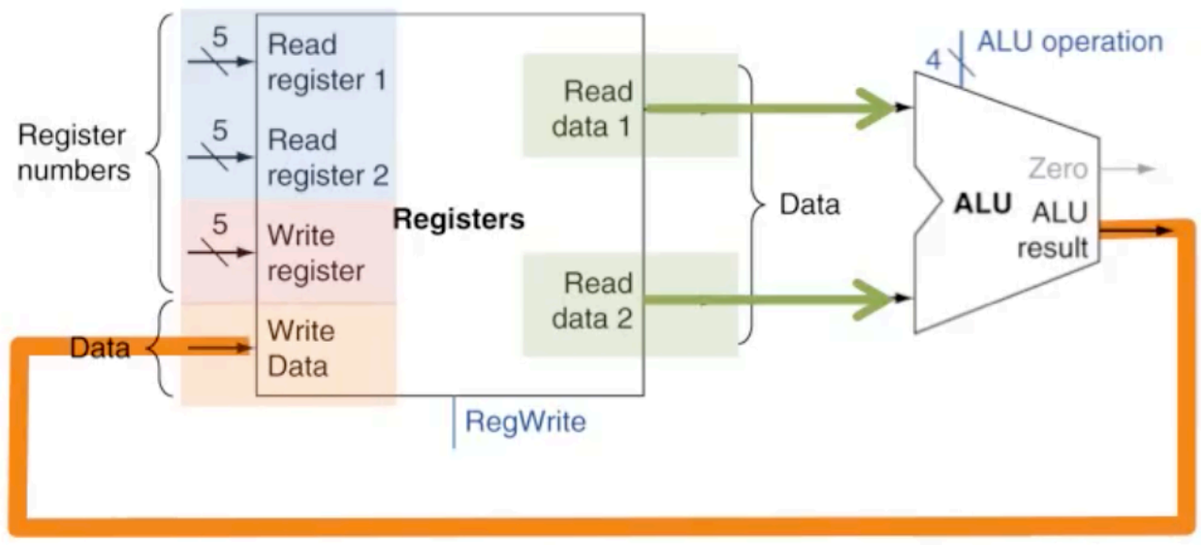


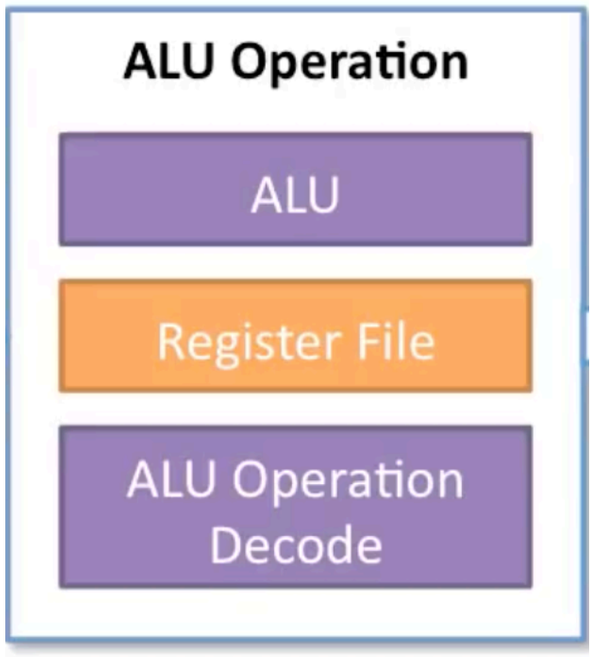


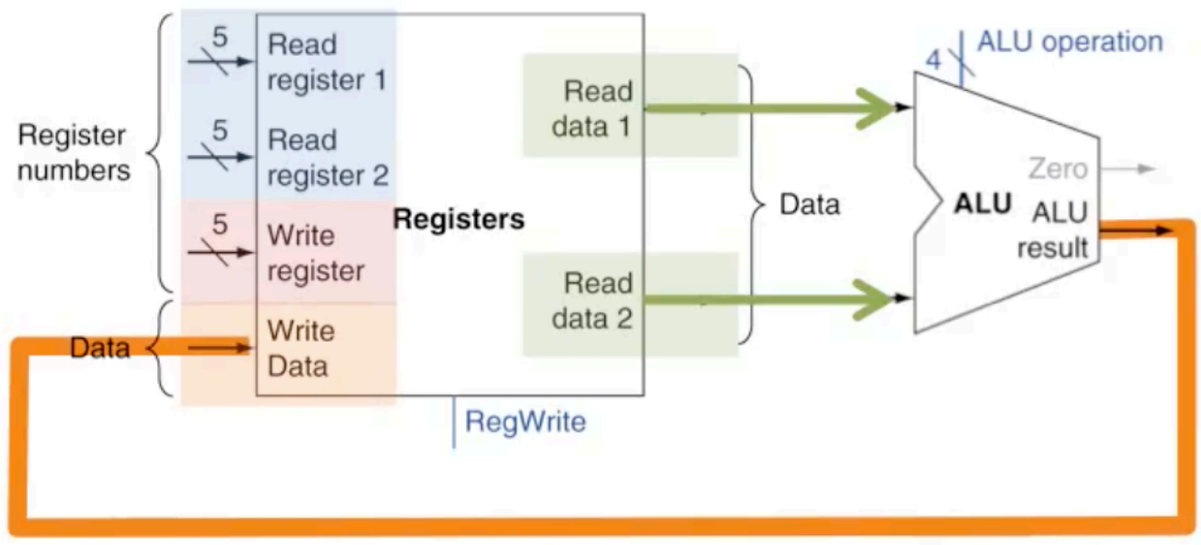
R0	0
R1	7
R2	13
R3	55
R4	83

Suppose your register file contains the values as shown on the right. What are the values of (a) Read register 1, (b) Read register 2, (c) Write register, (d) Read data 1 and (e) Read data 2 if the following instruction is executed?

add R3, R1, R2

The ALU Operation





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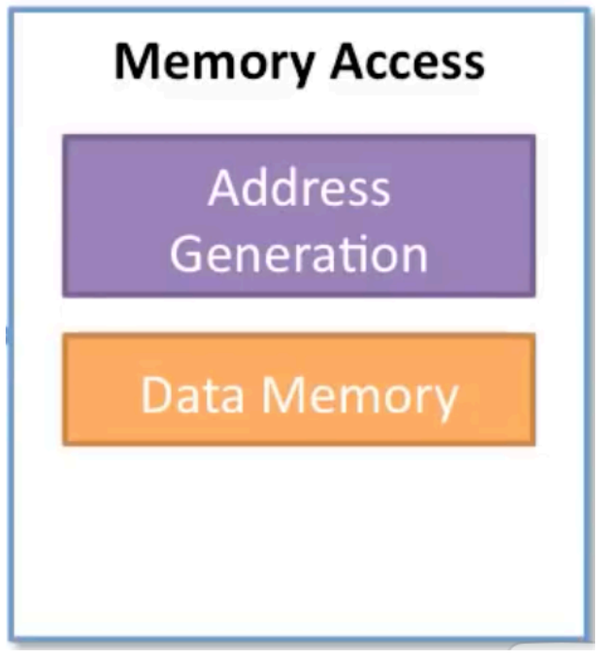

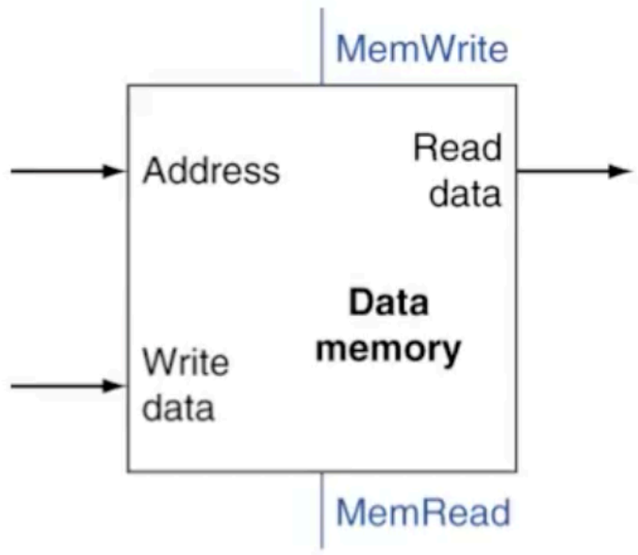

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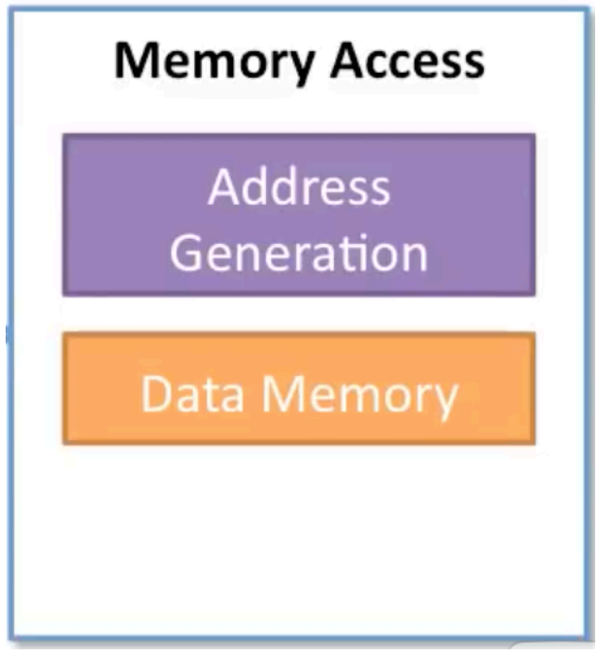
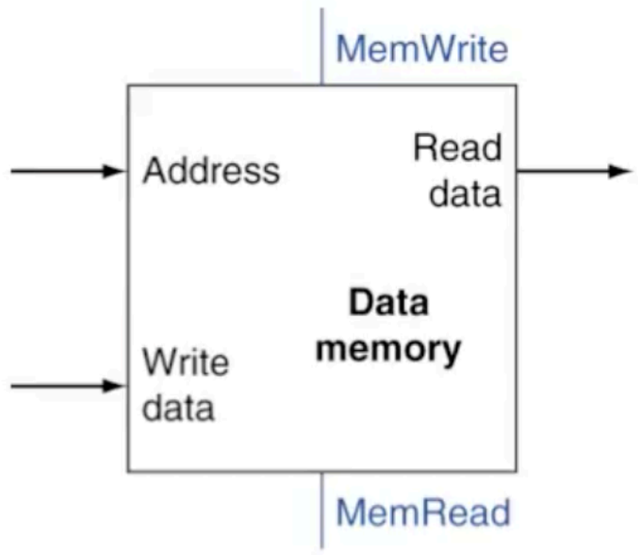
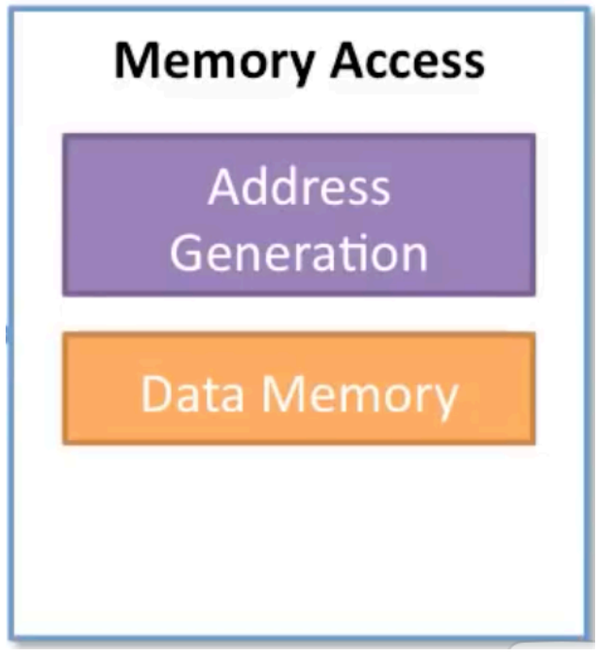


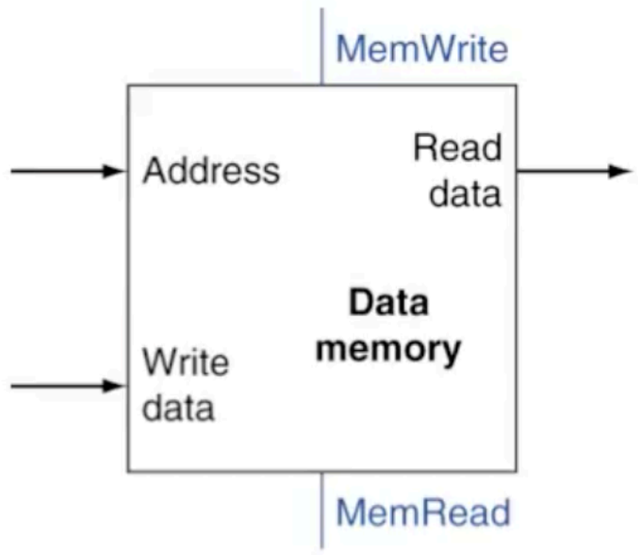


0	3
4	5
8	12
12	77
16	123

Suppose your data memory contains data as shown on the right. If the value of the address line is 8 and the value of MemWrite is 0 while MemRead is 1, what are the values of (a) Write data and (b) Read data lines?

The ALU Operation





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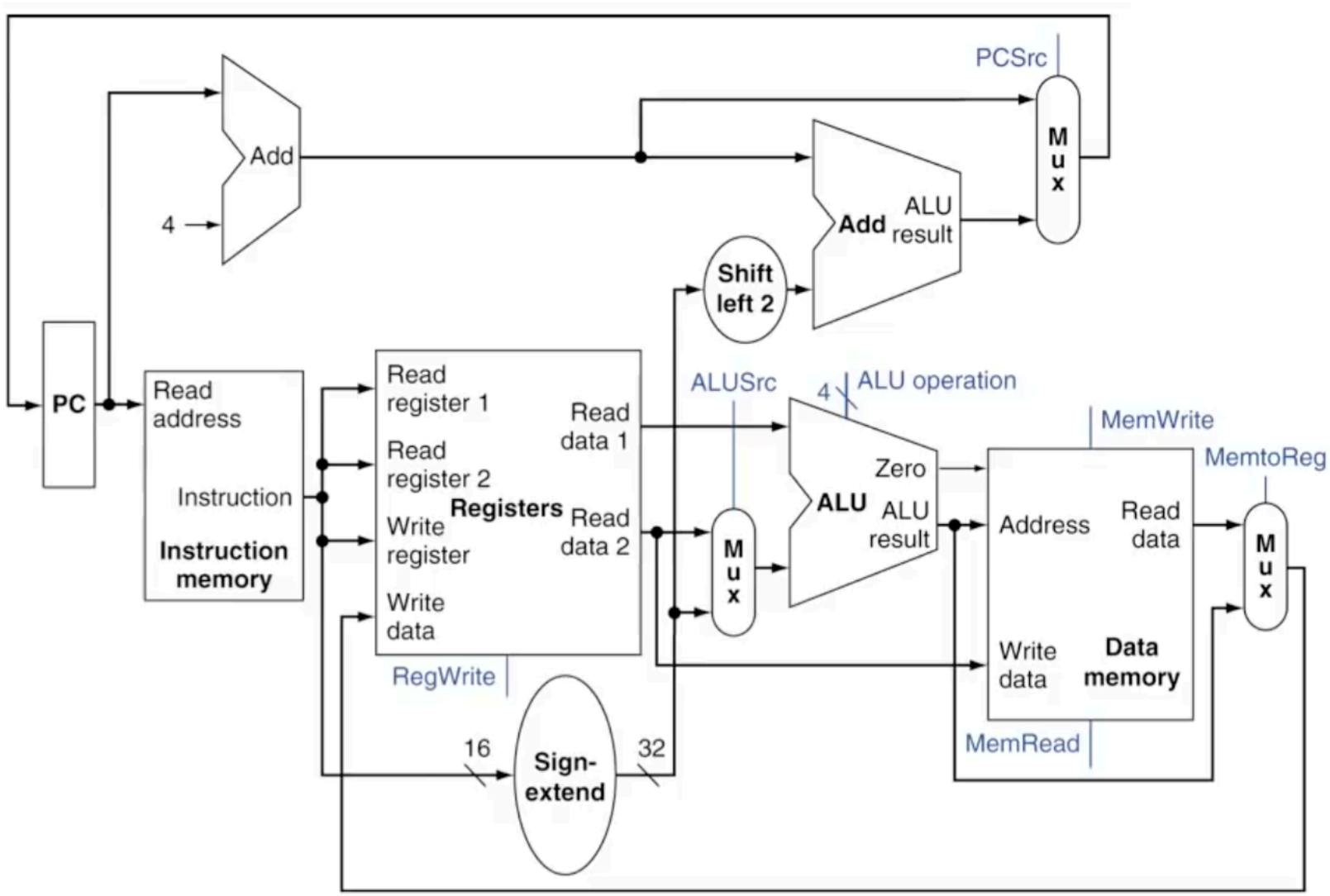
Putting It All Together

Whole datapath for (simple) MIPS



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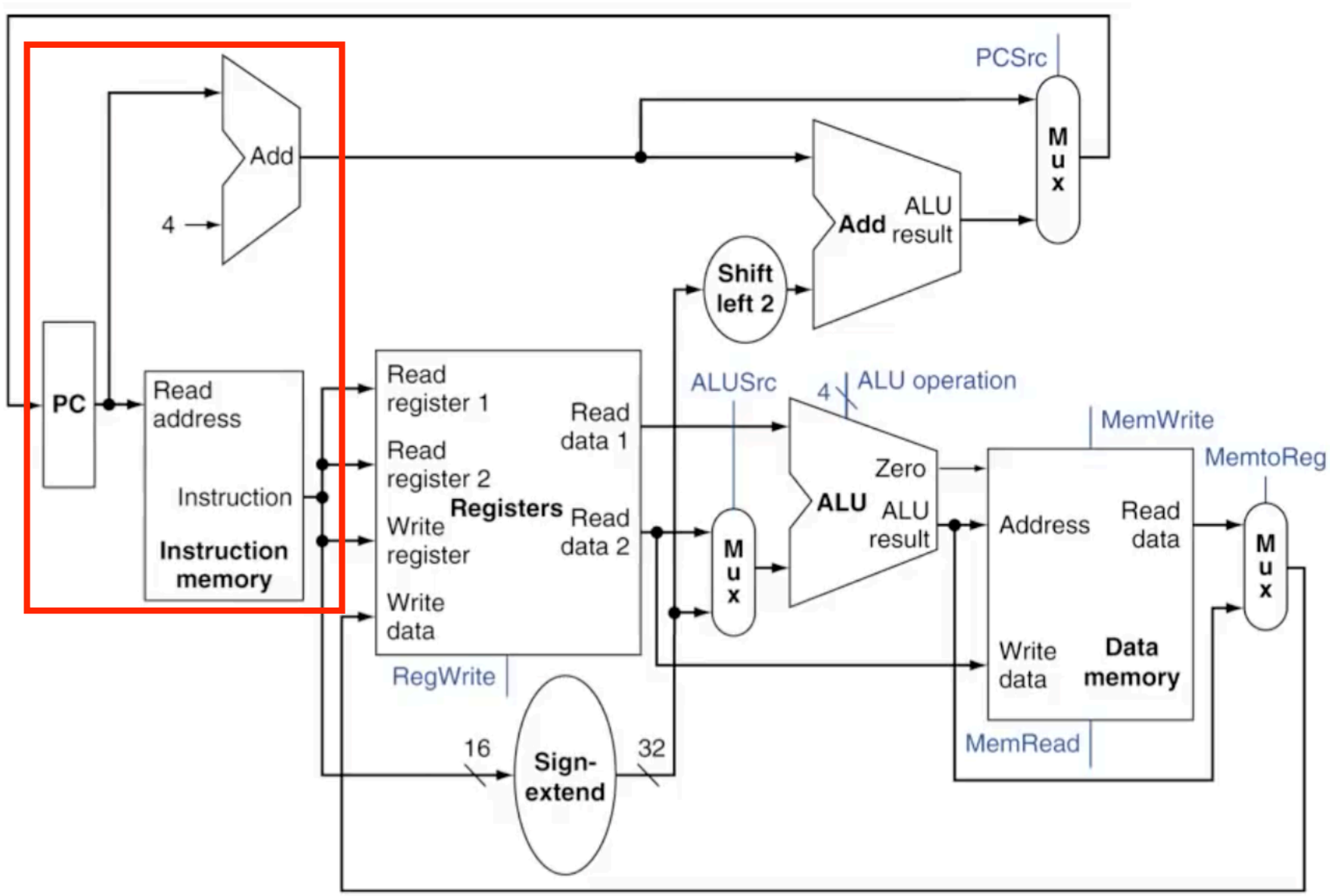

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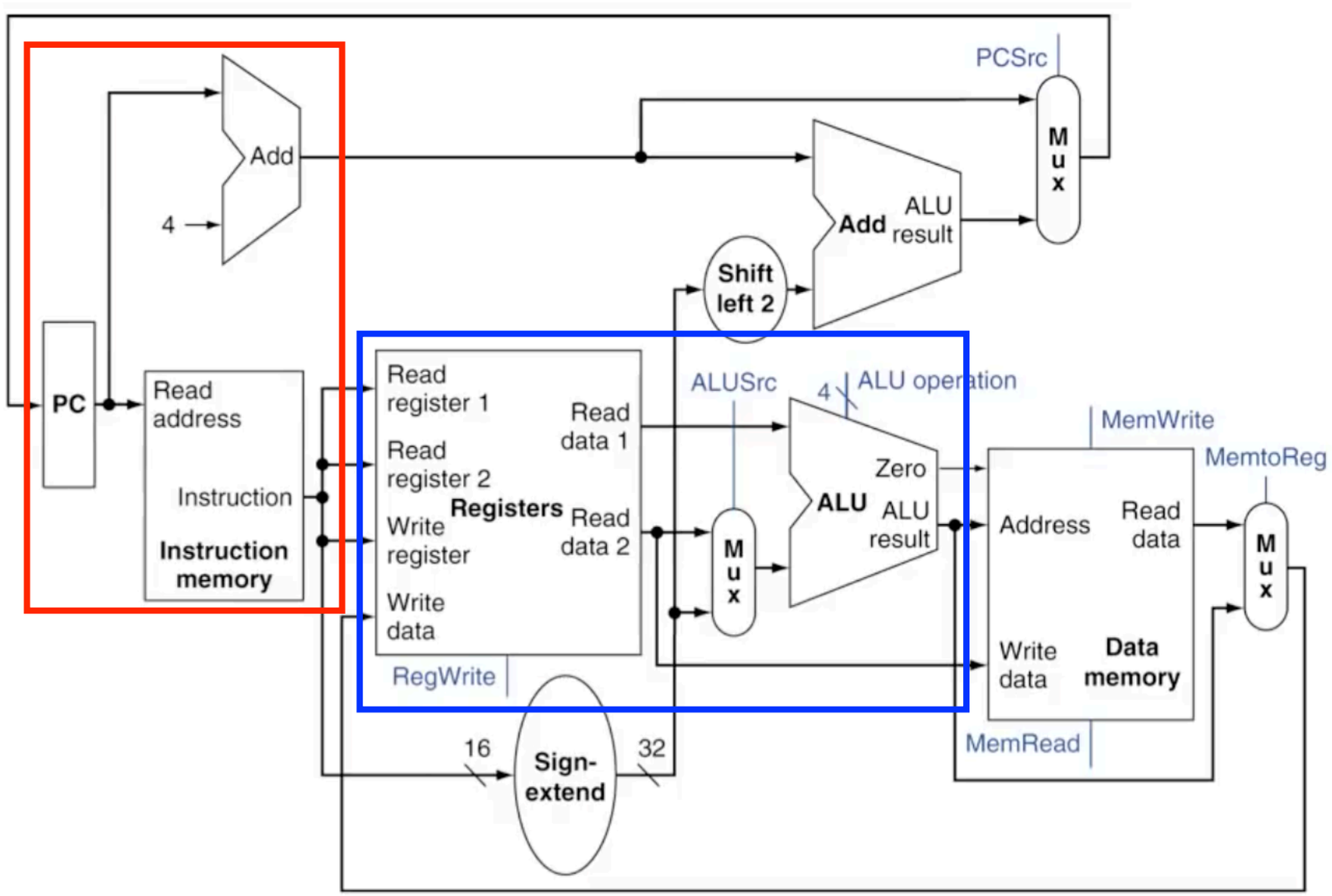

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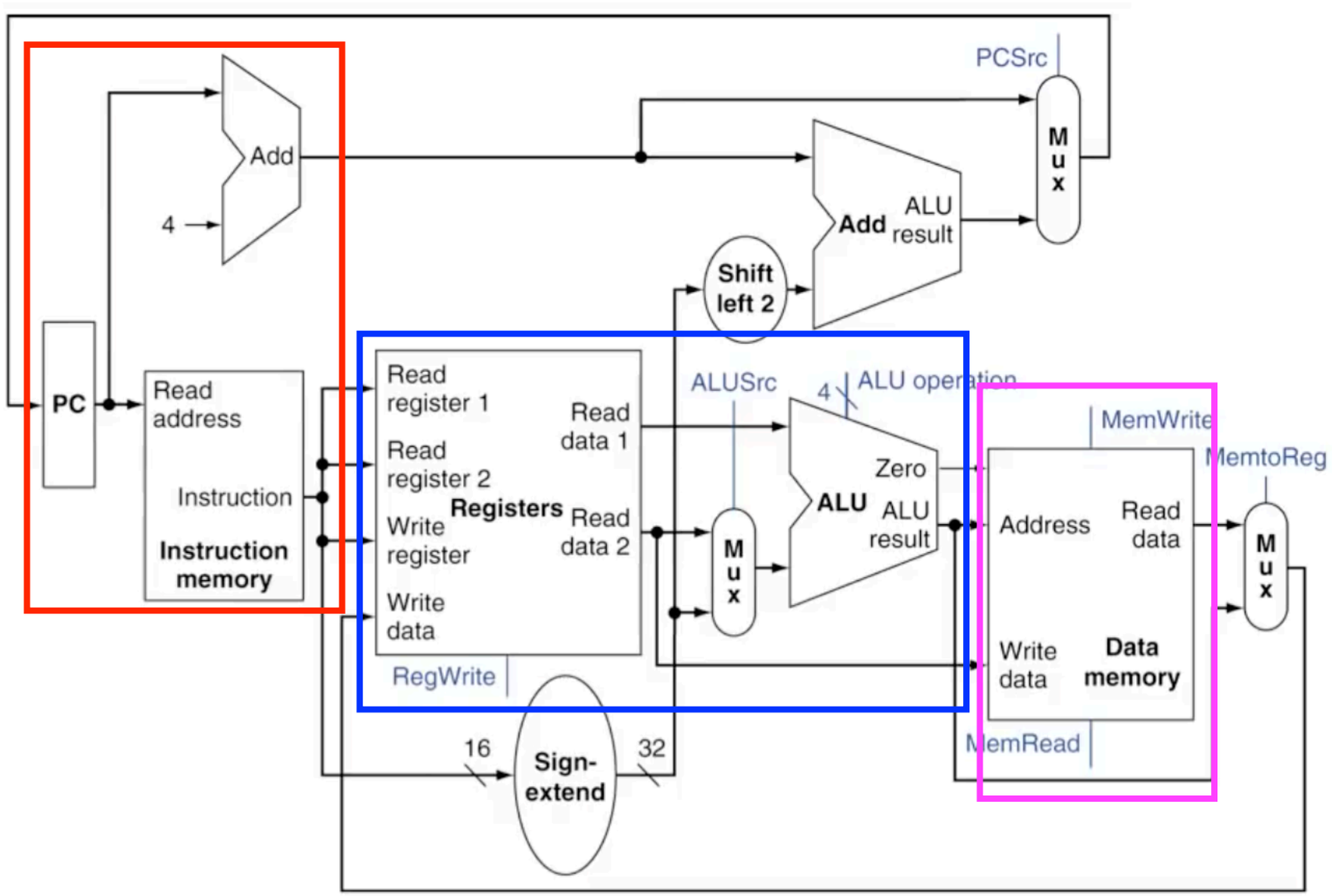

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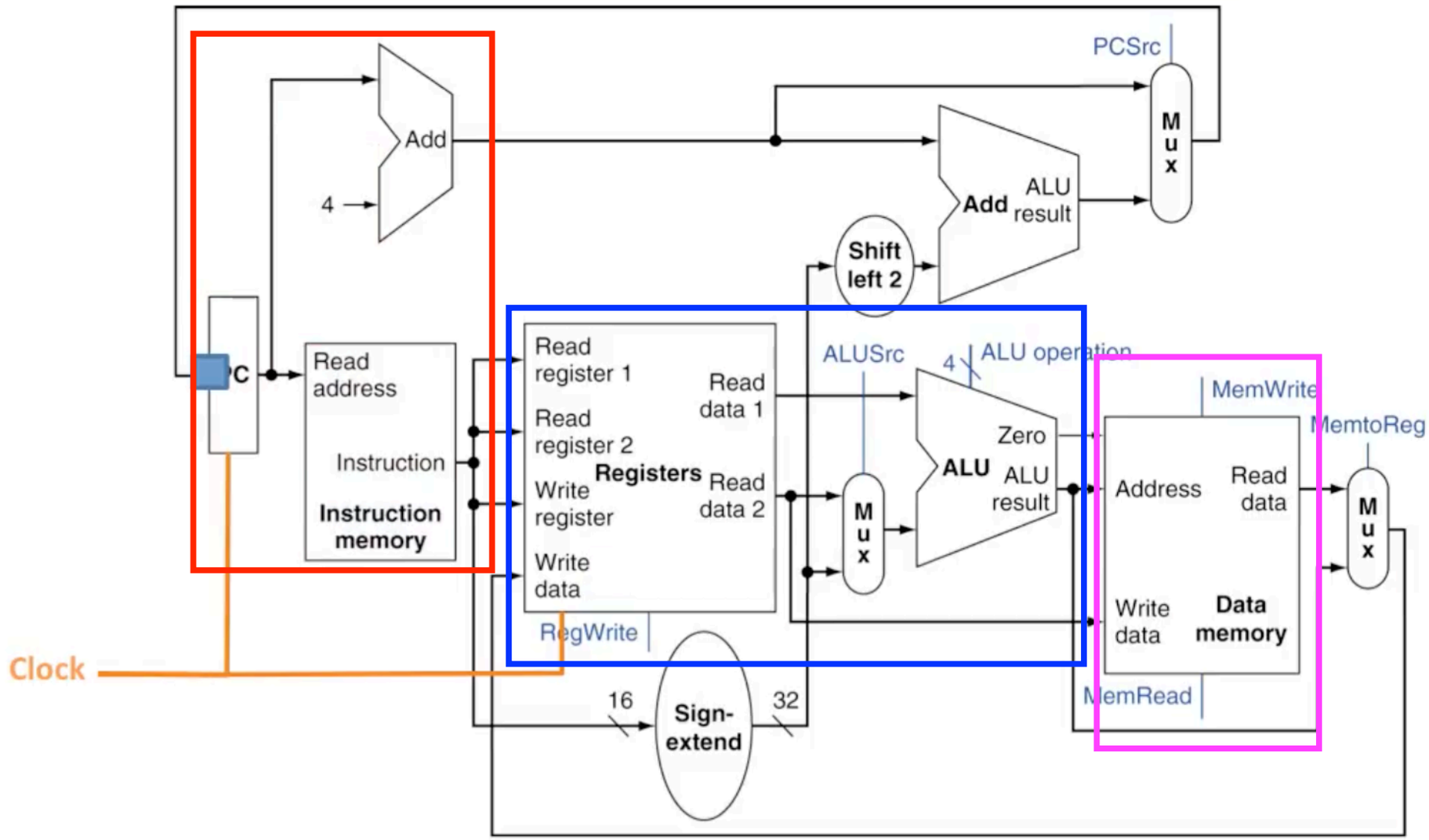

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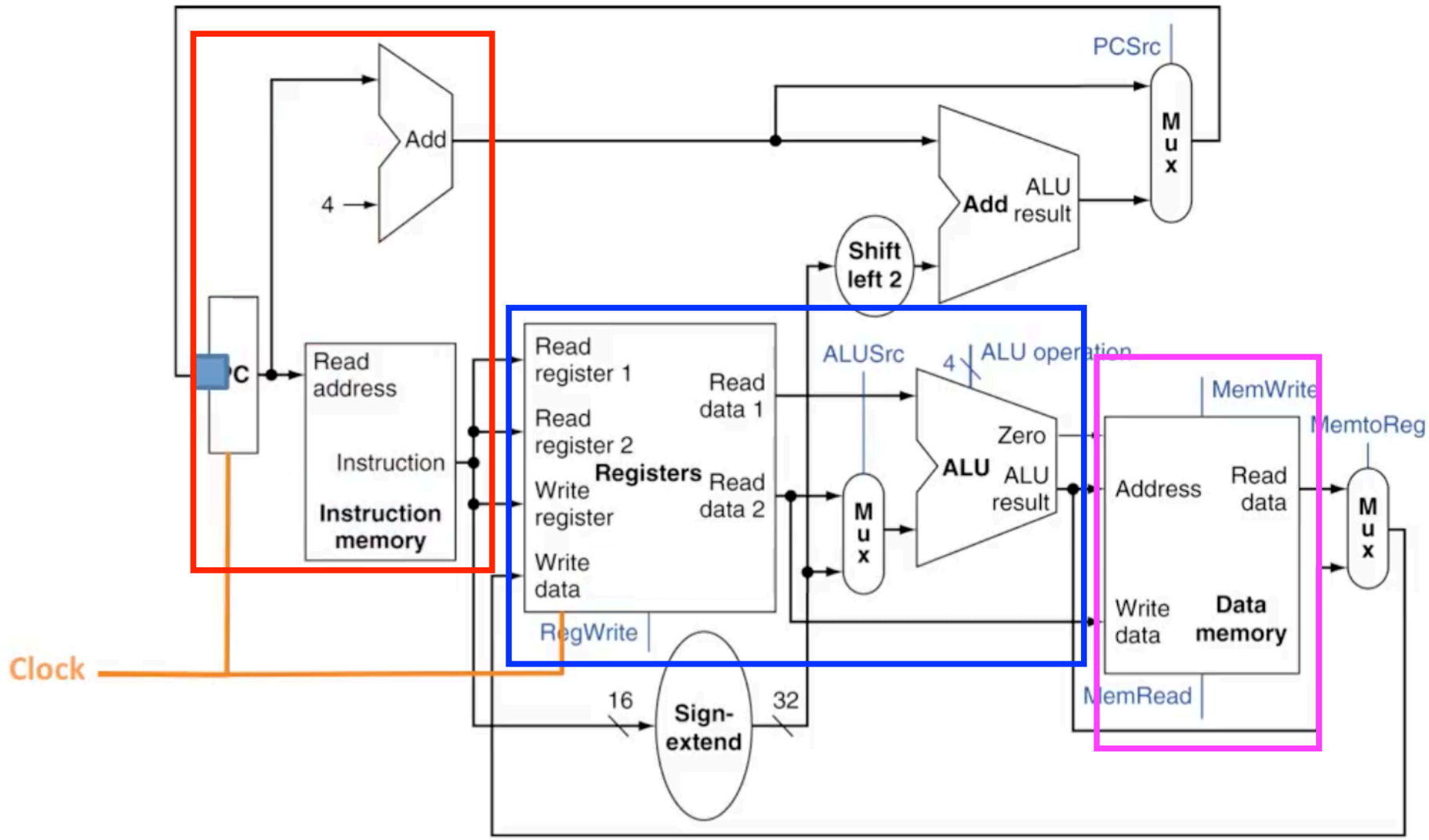

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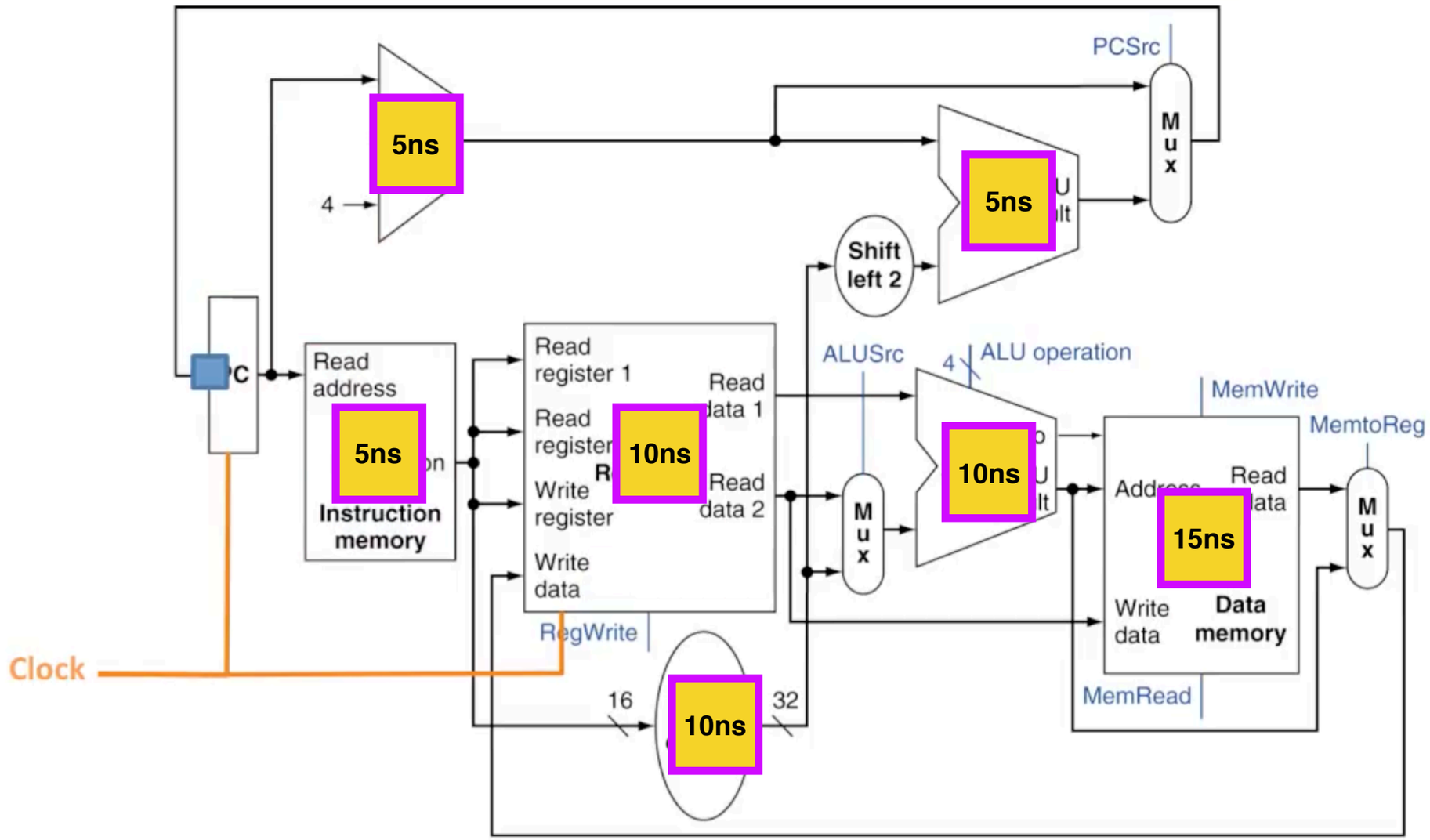

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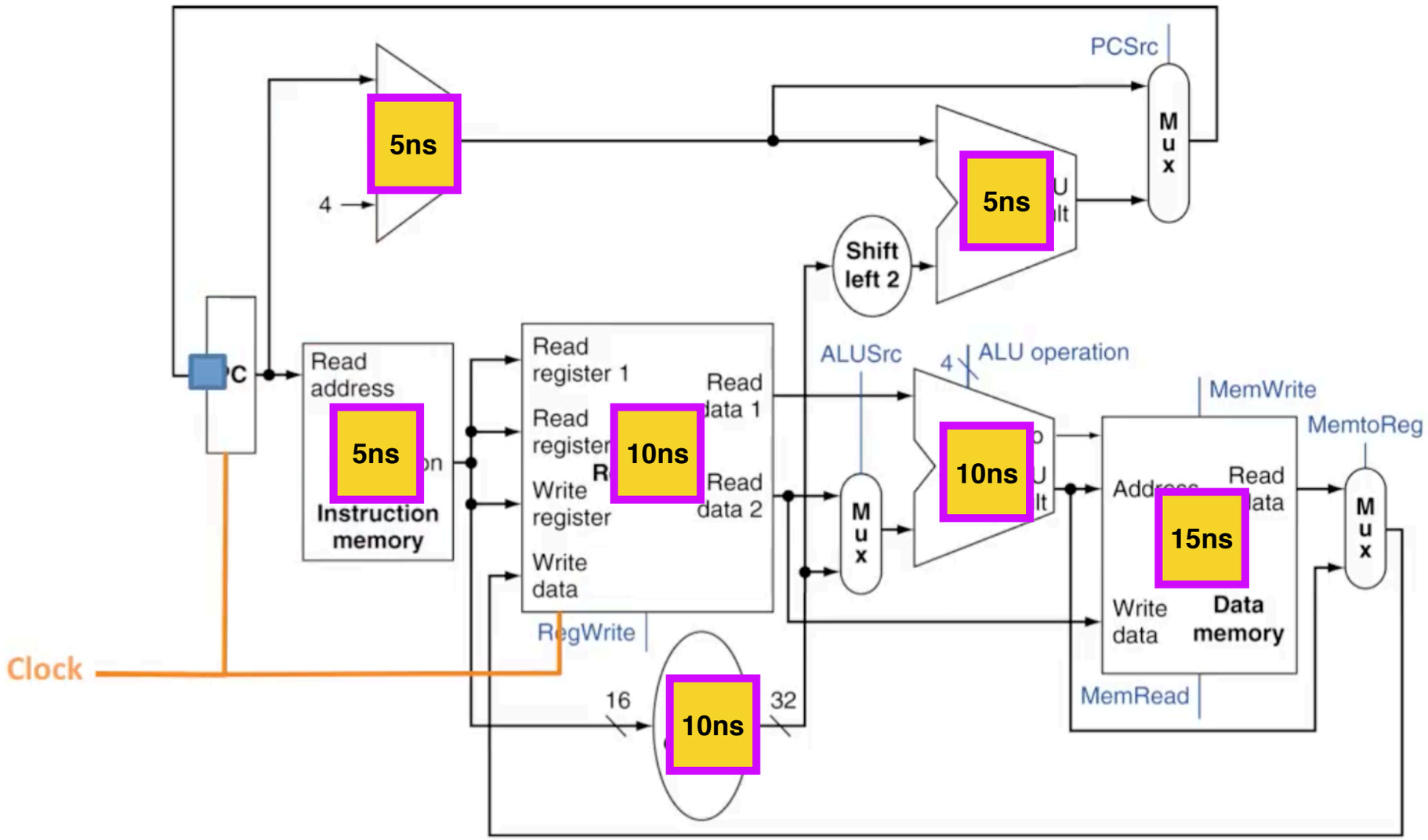

What is the speed of this processor in MHz? Hint: Find the longest path.

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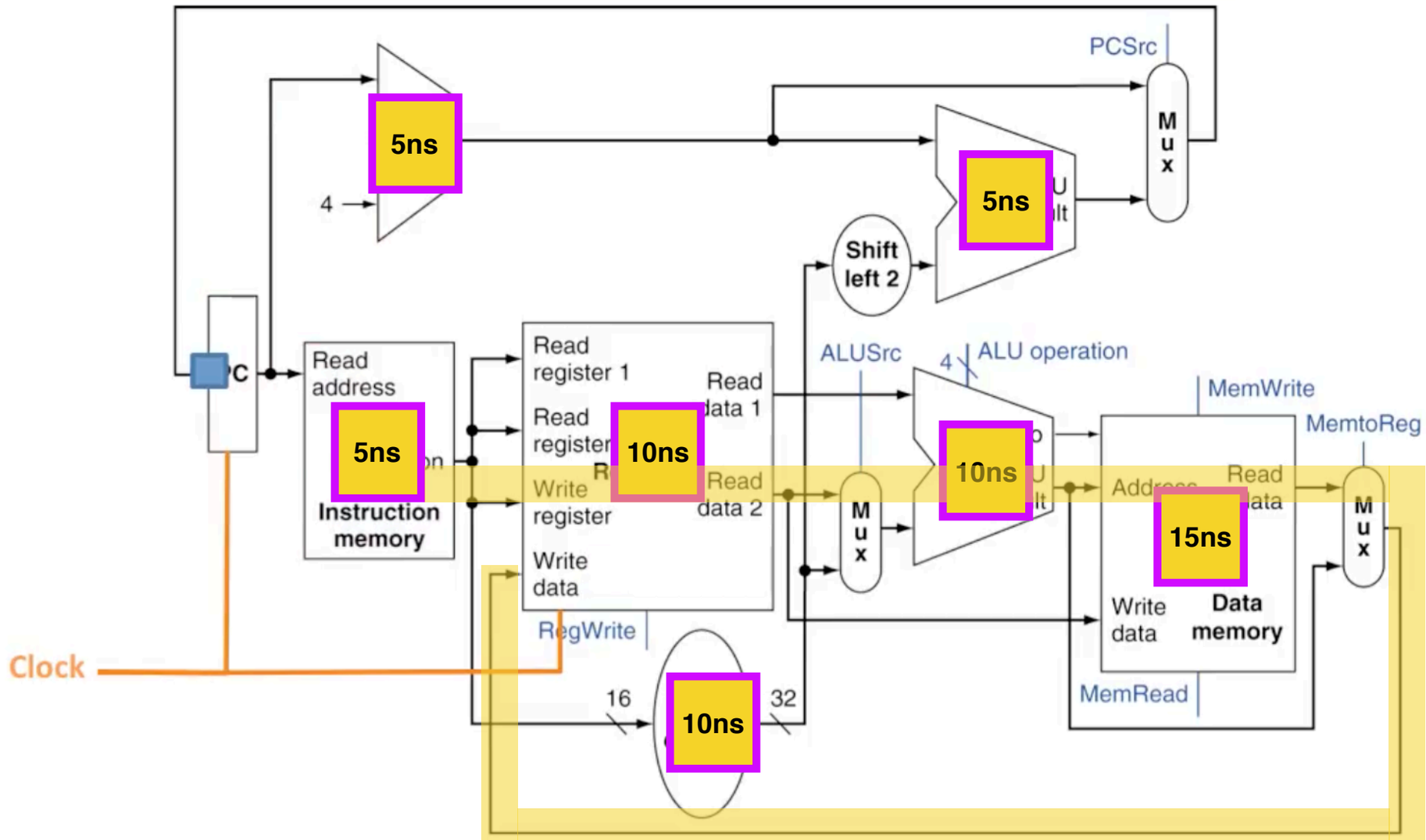


What is the speed of this processor in MHz? Hint: Find the longest path.

Putting It All Together

Whole datapath for (simple) MIPS

Calculating the speed…

Instruction Memory -> Register File (Read) -> ALU -> Data Memory -> Register File (Write)

Total Time = 5 + 10 + 10 + 15 + 10

Total Time = 50ns

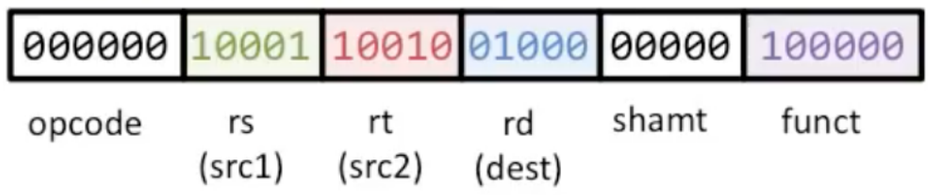
Speed = 1/Time *(this is actually frequency F; 1 instruction per unit time)*

Speed = 1/50ns

Speed = **20MHz**

Decoding Instructions

`add R8, R17, R18`



Decoding Instructions

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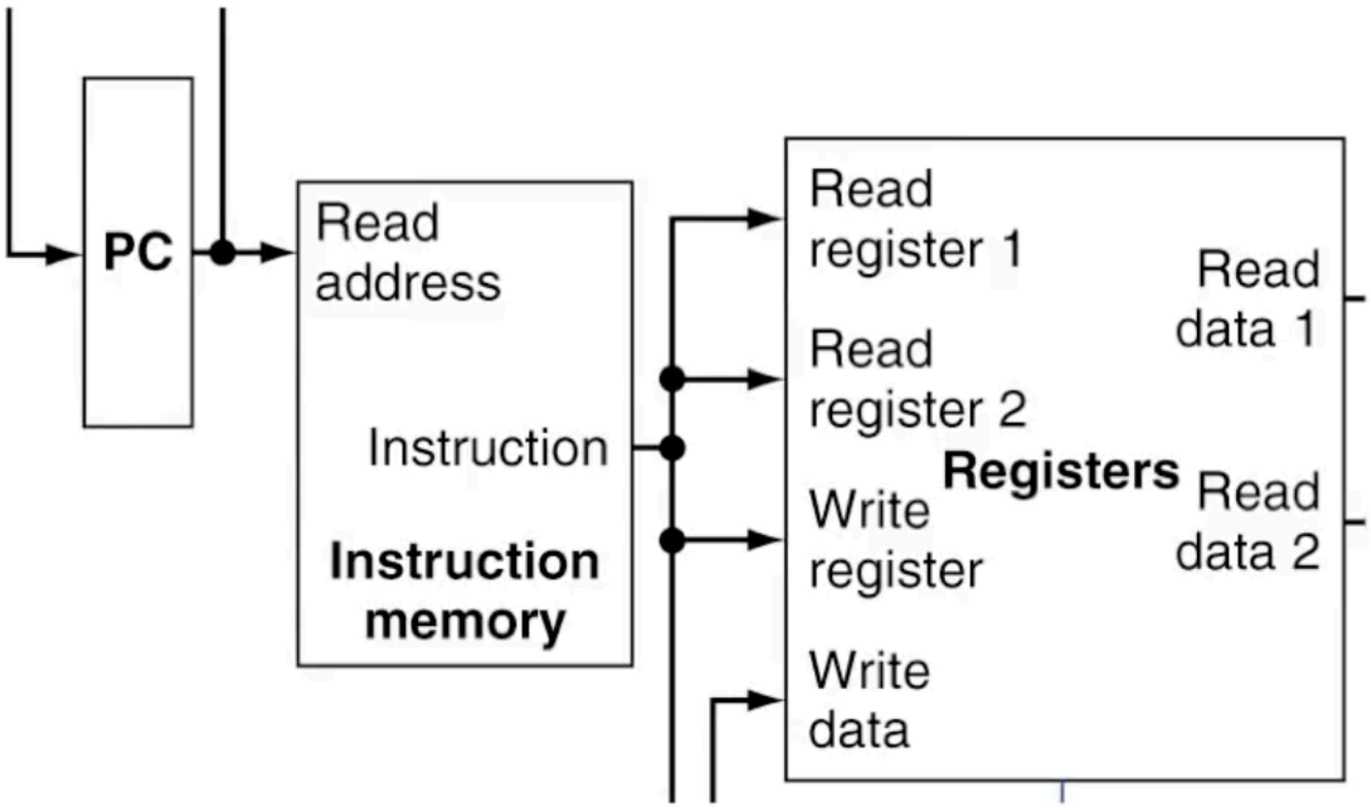
000000	10001	10010	01000	00000	100000
opcode	rs (src1)	rt (src2)	rd (dest)	shamt	funct



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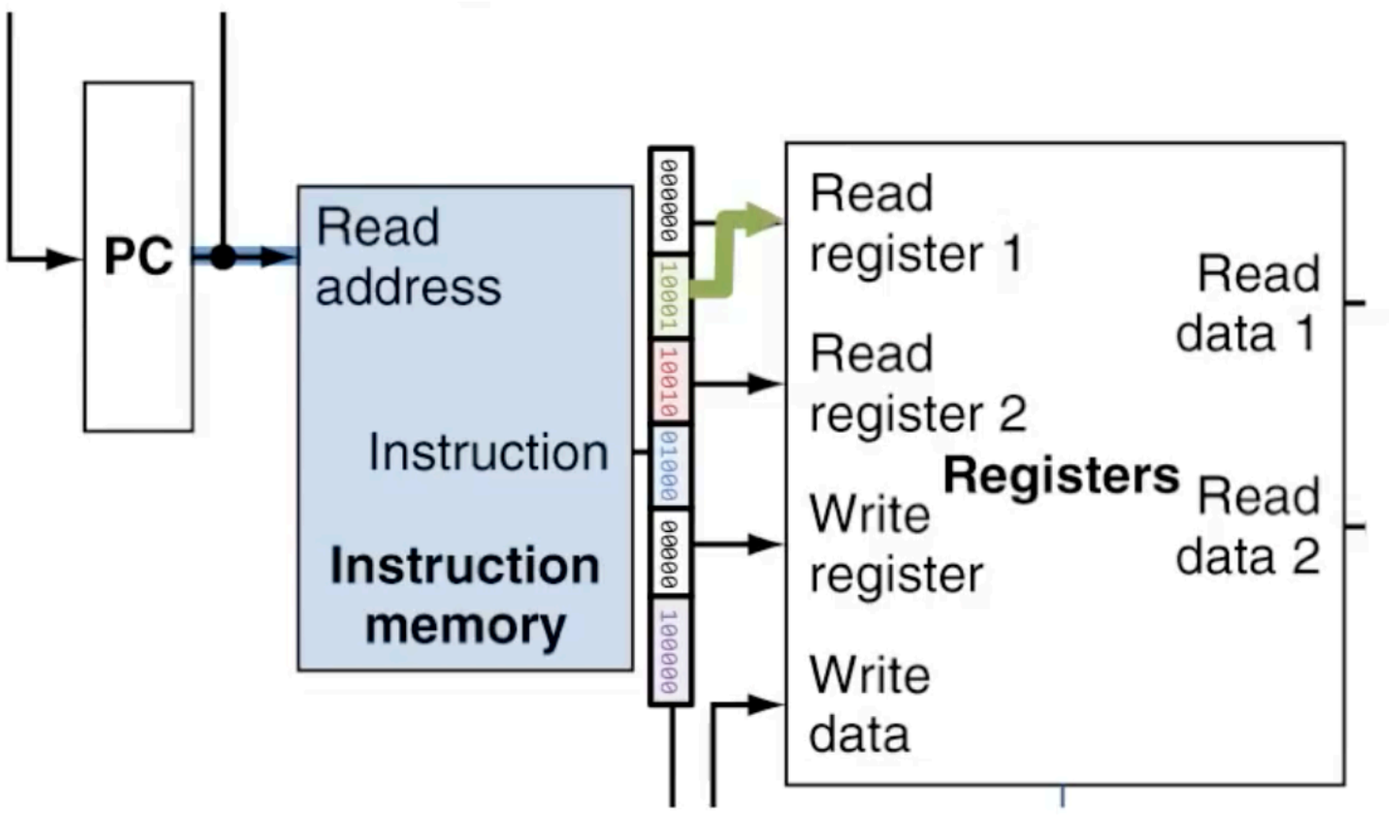

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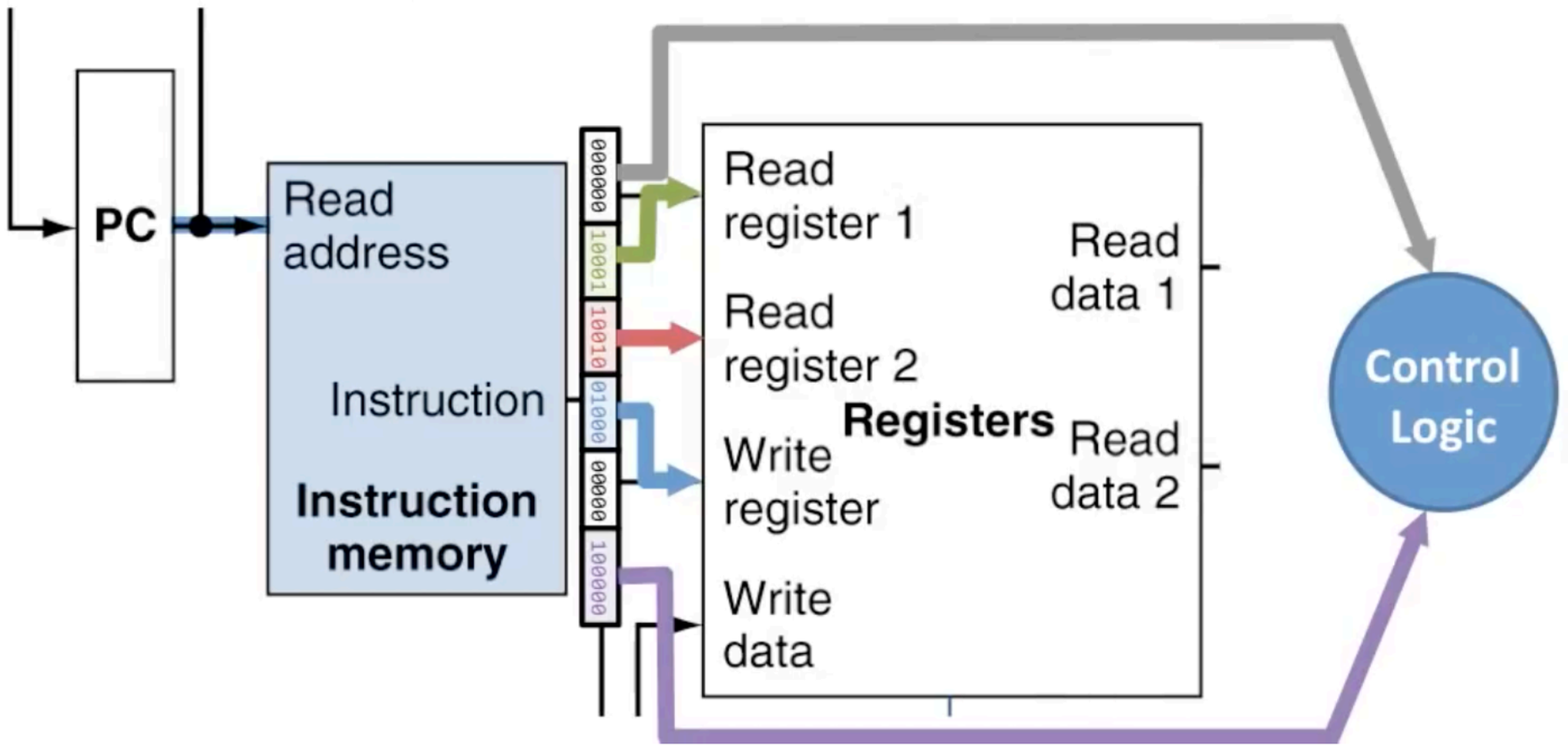

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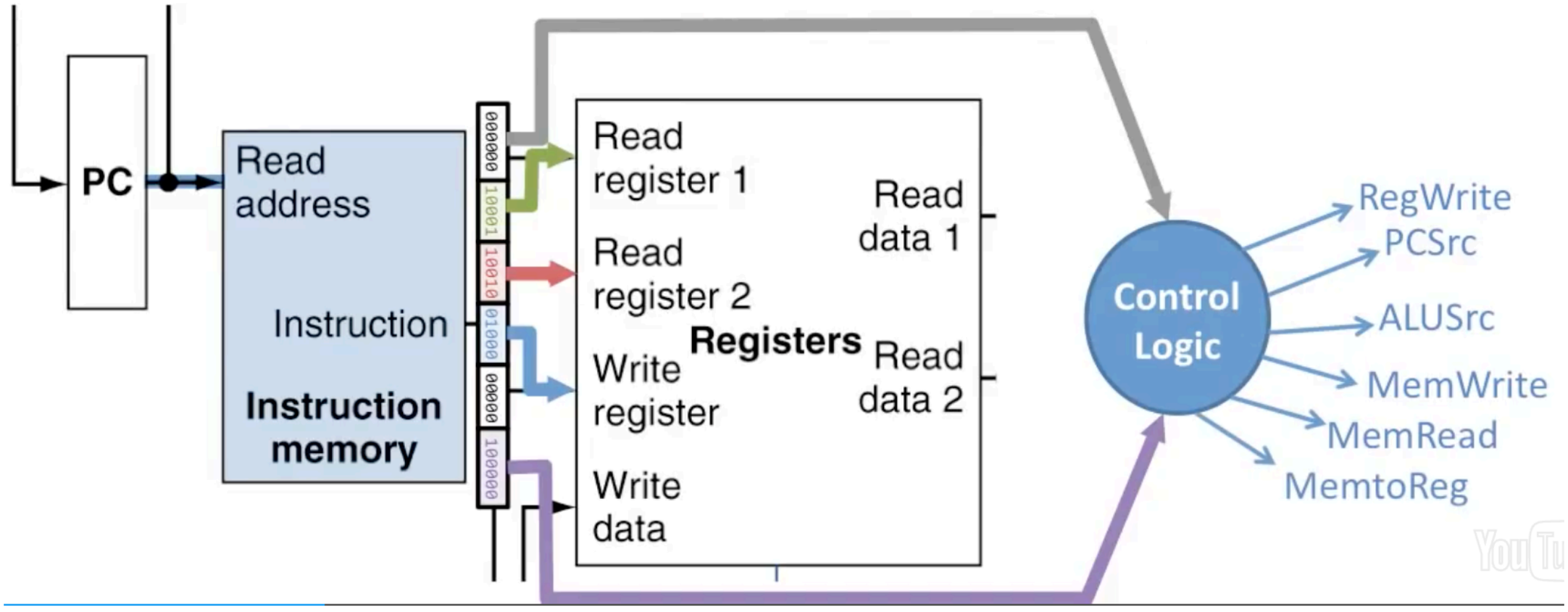

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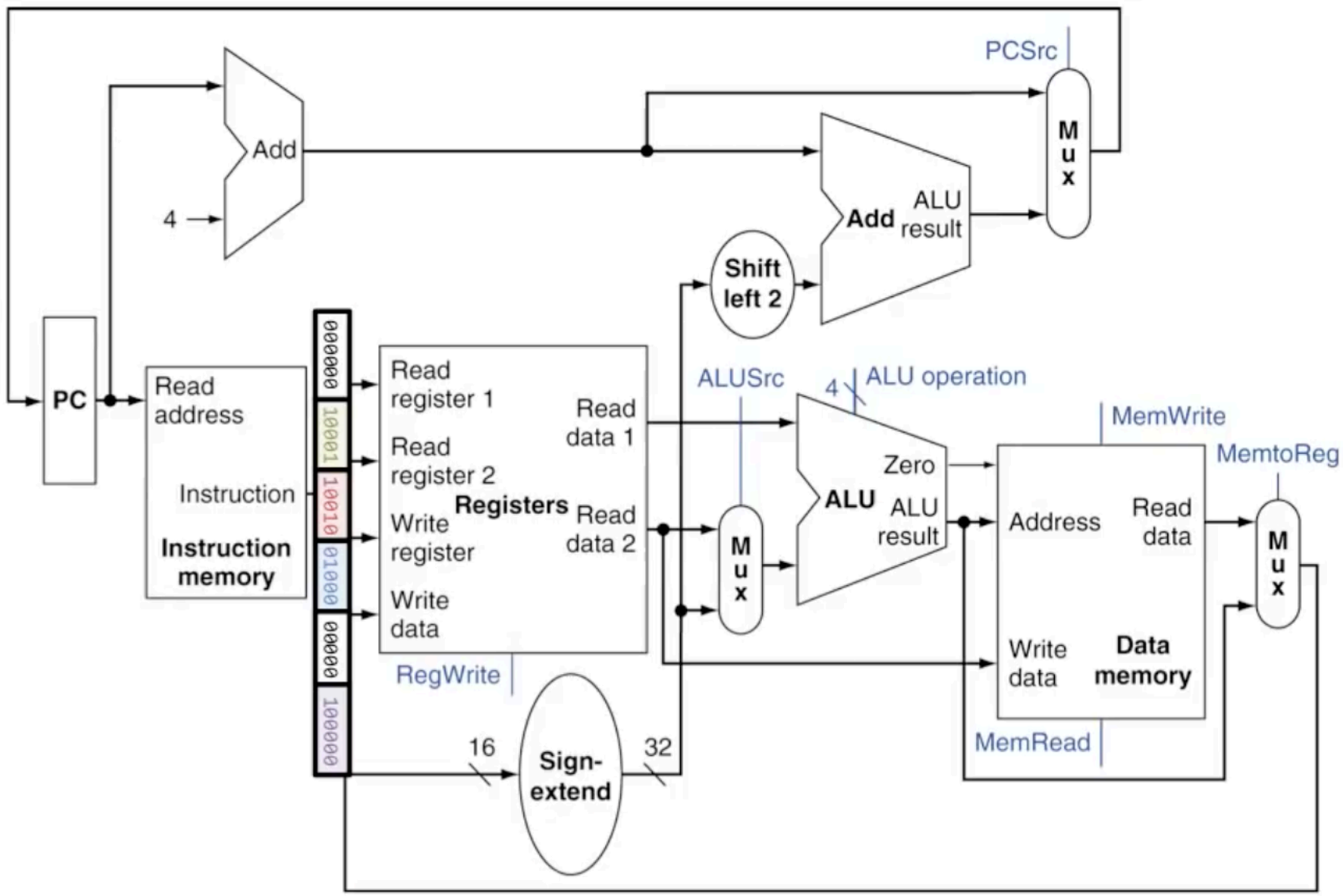

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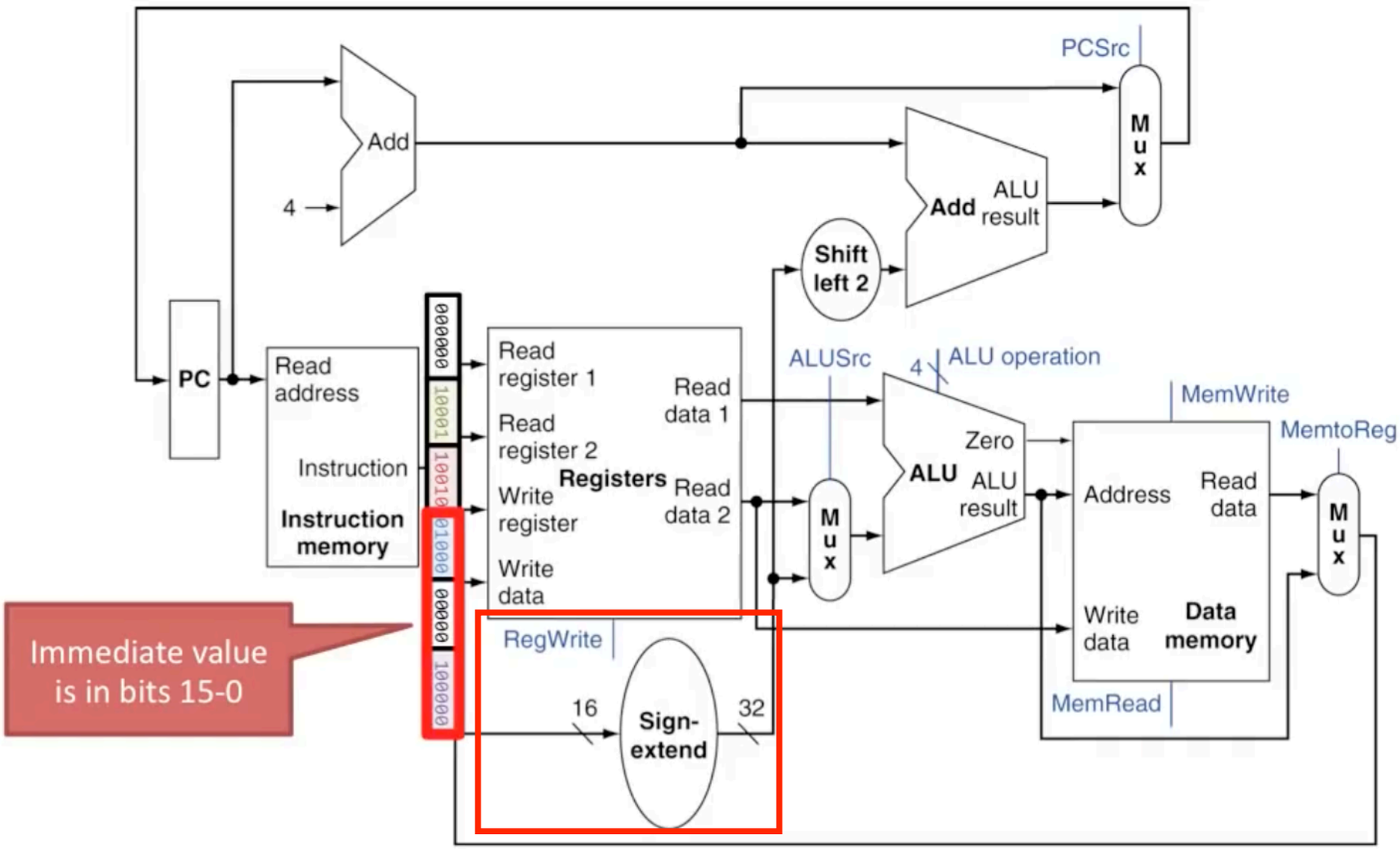

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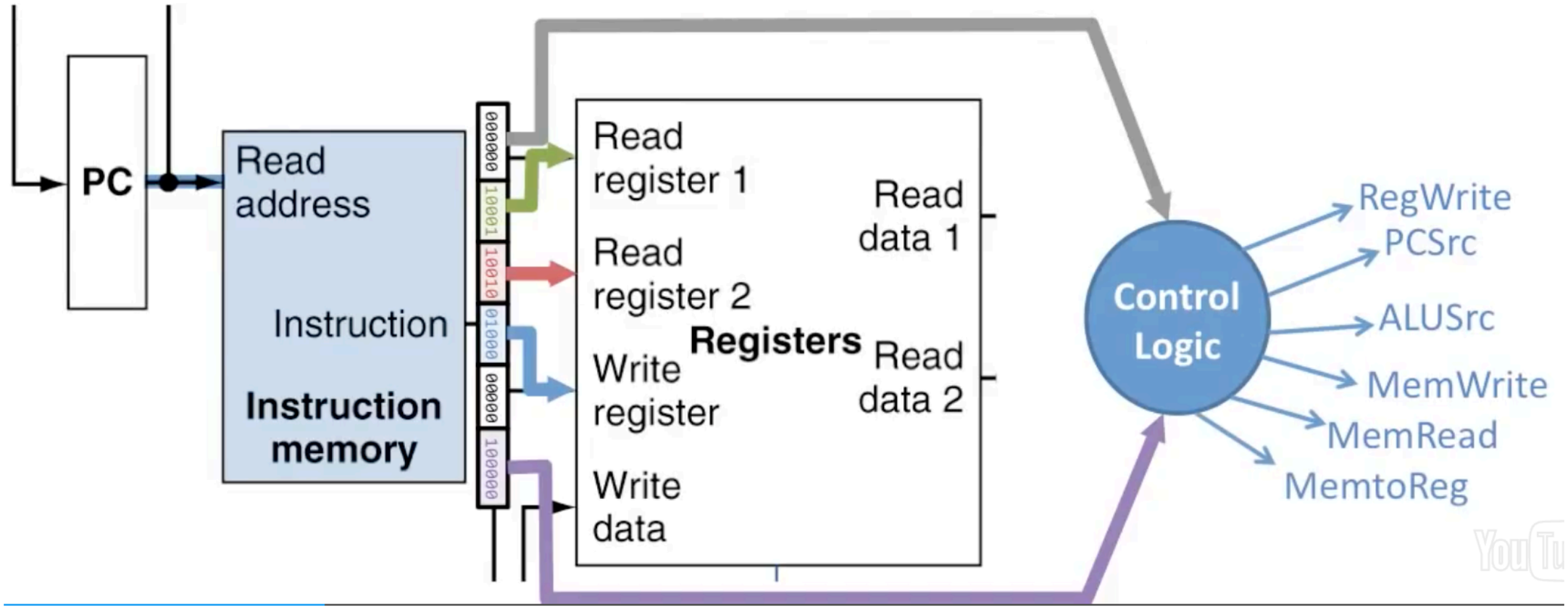
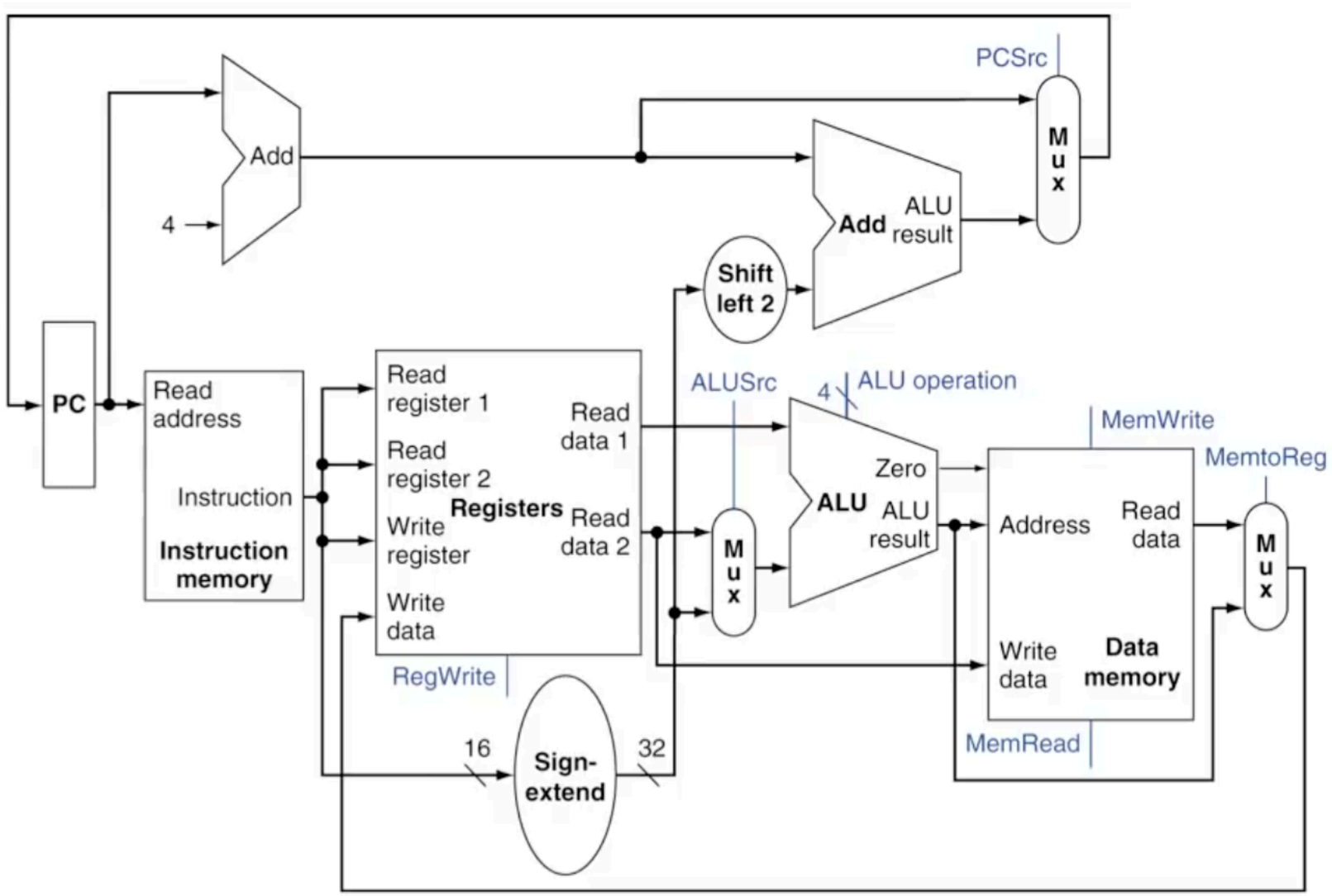



PCSrc
Add
4
M
u
x
ALU
Add
ALU
result
Shift
left 2
PC
Read
address
Instruction
Instruction
memory
Read
register 1
Read
register 2
Registers
Write
register
Write
data
Read
data 1
Read
data 2
RegWrite
ALUSrc
4
ALU operation
M
u
x
ALU
Zero
ALU
result
MemWrite
MemtoReg
Address
Read
data
Write
data
Data
memory
MemRead
M
u
x
16
Sign-
extend
32

Decoding Instructions

Control Signals

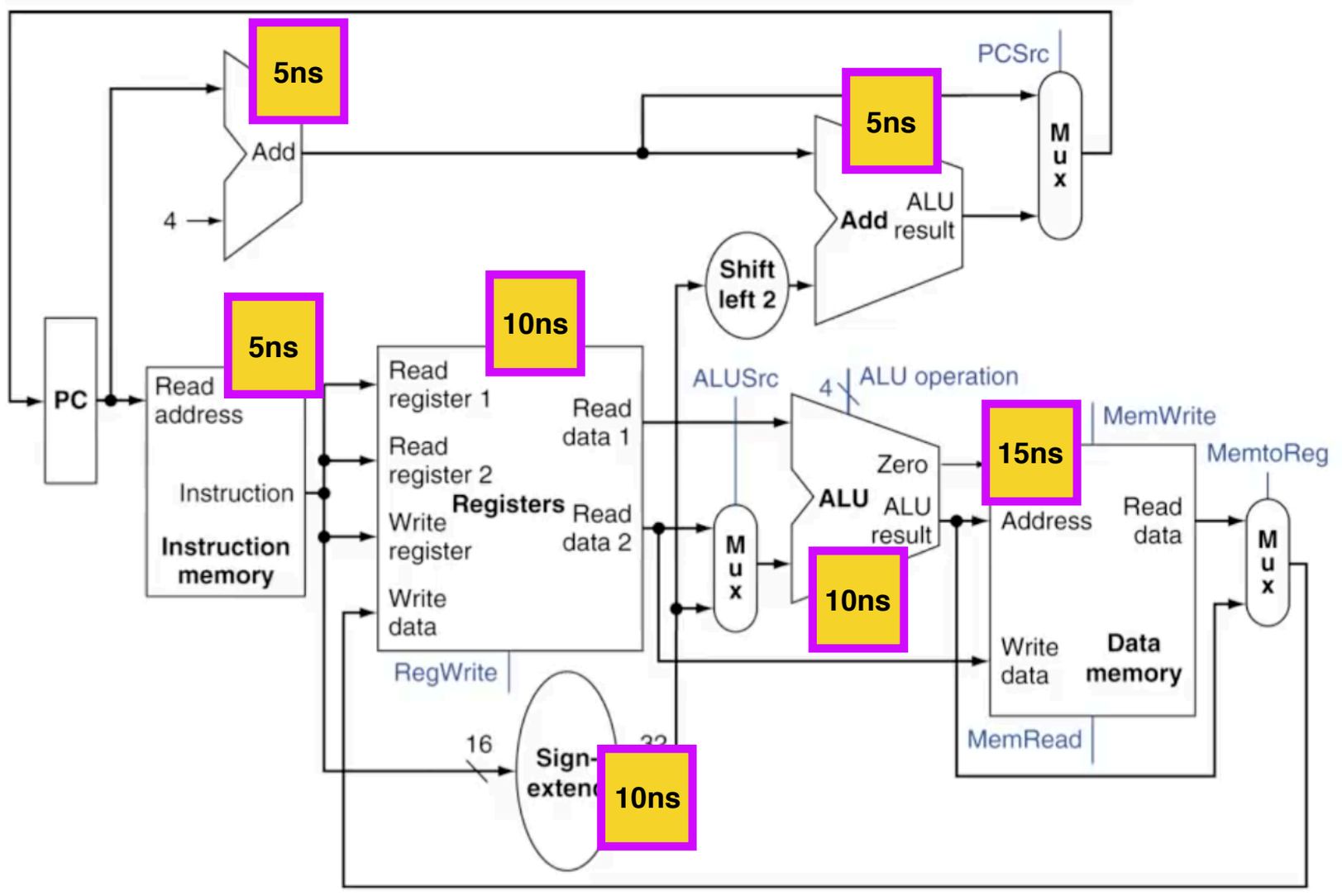
Signal	Meaning	When?
RegWrite	RF[Write register] ← write data (store write data in RF)	Any instruction that writes to the RF
ALUSrc	ALU uses sign-extended input (ALU operation with immediate)	Any I-format instruction
PCSrc	PC ← PC + 4 + Immediate (jump)	Branch taken
MemRead	Read from memory	loads
MemWrite	Write to memory	stores
MemtoReg	RF[Write register] ← memory (store memory data in RF)	loads
ALUop	ALU Operation	Any instruction that uses the ALU

Decoding Instructions

How long will it take for the following instruction to execute using the following processor?

add R8, R17, R18

Include in calculating total time the time spent in reading the instruction from instruction memory.



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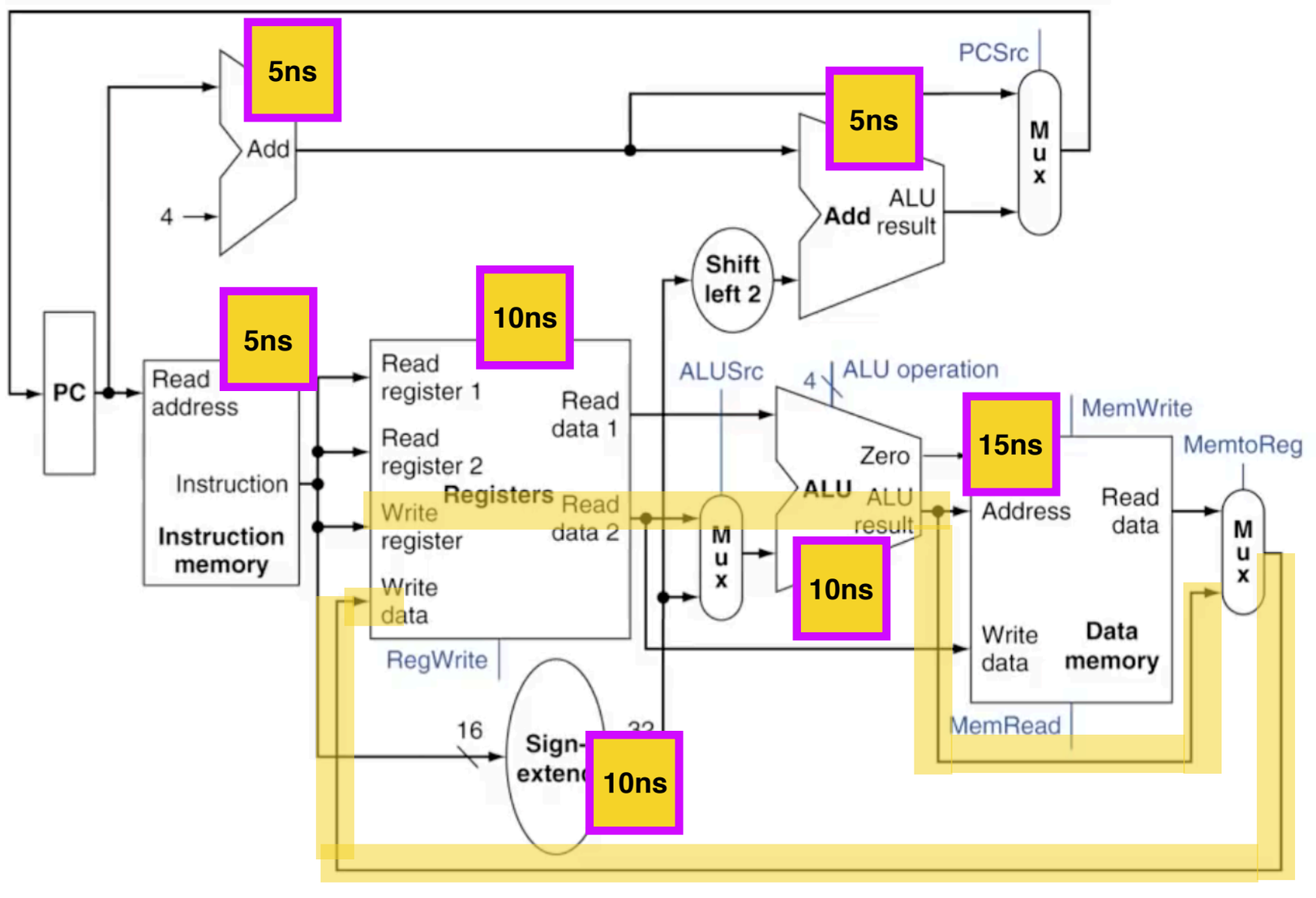

Decoding Instructions

How long will it take for the following instruction to execute using the following processor?

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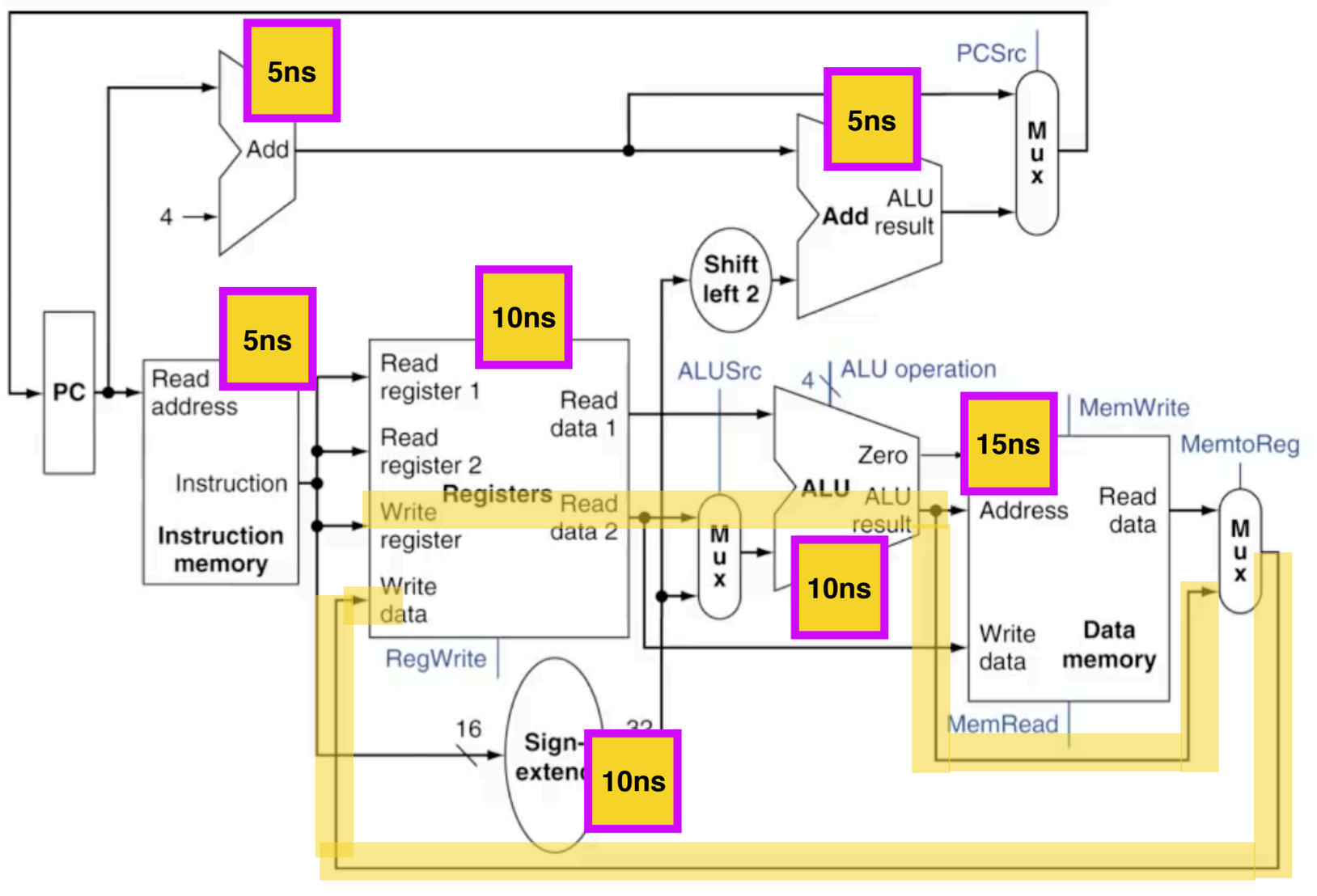
5ns

10ns

10ns

10ns

35ns



For Lab 2 (last lab)

- Study logisim