Department of Electrical and Computer Engineering
North South University

CSE231: Digital Logic Design
Design Project
Spring-2018

1. Introduction

The following project covers 10% of CSE231. The aim of the project is to access the students' ability to tie in theoretical and experimental knowledge from CSE231 to complete a practical project on Digital Logic Design and to work in a team. Information on groups and Team Leaders is outlined in Sec. 1.

The project consists of three phases. The project description is given in Sec. 2. Objectives and tasks for each phase of the project are described in Sec. 3. Each phase consists of an individual deadline that is summarized in Sec. 4. It is imperative that you meet all deadlines in order to complete the full project in due time. The mark distribution for the project is also summarized in Sec. 4.

2. Team Formation

Each group will have 4-5 members as assigned in the lab classes. Each group must assign a responsible Team Leader. The responsibilities of the team leader include (but are not limited to) the following:

- Hold meeting with group and decide on design.
- Hold regular meetings with group to ensure project is on track.
- Delegate tasks and deadlines to individual group members.
- Ensure group members complete their assigned tasks.
- Ensure project deadlines are met.
- Keep track of project budget, or assign another group member to do so.

3. Project Description

Consider the digital system shown in Fig. 1. Switching on the circuit through **ON/OFF Switch** results in the string of characters being displayed on the seven-segment display one character at a time at a set time interval of 2-3 seconds. At the end of the sequence, the string is repeated. However, the sequence of characters will depends on the input **Direction**.

The sequential logic circuit produces a sequence of codes to represent the string of characters "**SP18-CSE231-P-Team no**." if the **Direction** input is logic LOW and the reverse order ("**Team no. –P-132ESC-81PS**") if the **Direction** input is logic HIGH.

Example: The Team No. 9 will display the sequence "**SP18-CSE231-9**" if the **Direction** is LOW and display the sequence "**9-132ESC-81PS**" if the **Direction** is HIGH

The input **Direction** may be changed from logic HIGH to logic LOW (and vice-versa) at any time by the user. Upon change of the **Direction**, the sequence should continue from its current character (whatever showing at that time) and follow the direction (forward or reverse) accordingly based on the **Direction** input.

The sequential logic circuit is connected to an active high seven-segment display via a combinational logic circuit. The combinational logic circuit decodes the input codes from the sequential logic circuit in order to drive the individual segments of the seven-segment display to show each character `S', `P', '-' `C','S", 'E' `2','3' and `1' , `-' etc. as dictated by the sequence.

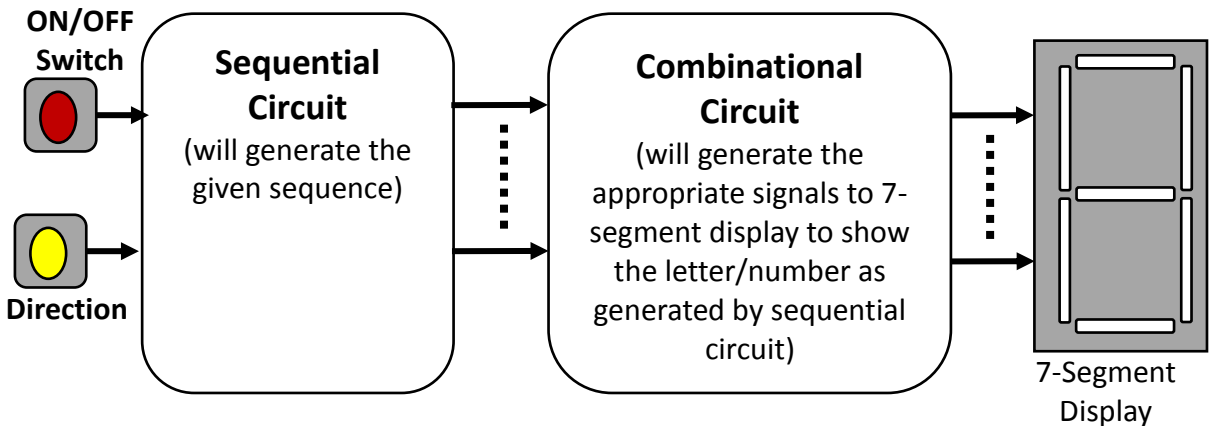

Fig. 1: Circuit block diagram. Sequential circuit produces a sequence of codes. Code from sequential circuit is decoded by combinational circuit to light up corresponding segments of a seven-segment display.

NOTE: Only ONE seven-segment display is to be used and the display will show one character at a time based on the sequence

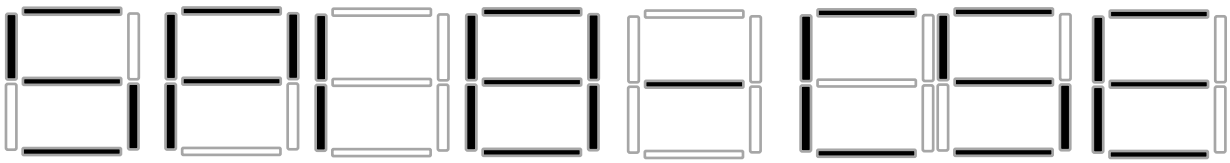

Fig.2: Example Display of "SP18-CSE" by a seven-segment display in a forward direction.

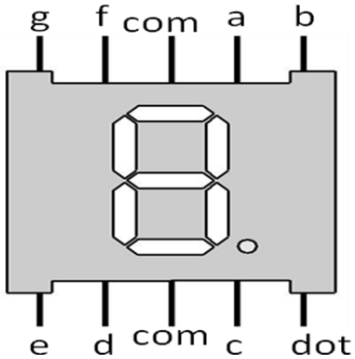

Fig. 3 shows the schematic of seven-segment display with its segments and corresponding input pins labelled (a - g). The COM ports are for V_{CC} and Gnd.

4. Objectives and Tasks

Phase 1: Combinational Circuit Design and Implementation (**Deadline: April 16, 2018)**

Design the combinational logic part of the system (described in Sec. 2) to display the characters of the string on a seven-segment display.

The team must complete design and working schematics of the combinational circuit using **Logisim** and **submit a hard-copy and a soft-copy of it**, on or before the deadline, and during the assigned office hours. The group must show the theoretical design steps of the circuits. The combinational circuit must be designed and simulated in the following forms:

a. Using universal / basic gates with Minimal logic implementation
b. Using Decoder
c. Using Multiplexer

It is at the discretion of the team to choose one of the option from the above for **circuit implementation.** However, the group must be able to provide rationale for their design choice and it must be using relevant material covered in the course. Think about number of bits, efficiency, complexity, cost consideration etc.

The team should ***demonstrate the implementation*** of their combinational design part of the project on or before the deadline.

Phase 2: Sequential Circuit design (**Deadline: April 23, 2018**)

Design the sequential logic part of the system described in Sec. 4, that is, the sequence generator for the string of characters "**SP18-CSE231-P-Team no**" in the correct order. Each character must be displayed for about 2-3 seconds.

The team must complete design and working schematics of the sequential circuit only using **Logisim** and **submit a hard-copy** and a **soft-copy** of it, on or before the deadline, and during the assigned office hours. The group must show the theoretical design steps of the circuit and ensure its compatibility with the combinational circuit.

Phase 3: Final Demonstration (**Deadline: April 30, 2018**)

Students are required to implement their digital electronics circuit (combinational and sequential) and demonstrate its working before or on the Final deadline. The circuit should loop through the chosen sequence ("**SP18-CSE231-P-Team no**." or ("**Team no. –P-132ESC-81PS**") at the set interval automatically once the circuit is **switched on**.

5. Task Deadlines and point distribution

Task	Points	Submission Deadline
Phase 1: Combination Circuit Design and Implementation	25 +25	**April 16**
Phase 2: Sequential Circuit Design	25	**April 23, 2018**
Phase 3: Final Report and Implementation (combining sequential and combinational part)	25	**April 30, 2018**

Final marks will only be confirmed upon satisfactory completion of the project. Marks will be given at the discretion of the faculty member considering the group is capable of the work submitted based on their overall performance.

Final marks of the project will be distributed among group members based on the appraisal submitted by the Team Leader. Each member of a group will be assessed individually and his/her mark may vary from other group members based on assessment during the presentation and the appraisal.

Late Submission

- Failure to meet each deadline will result in penalty of 2% per day delay

Plagiarism

Plagiarism will NOT be tolerated. Any form of plagiarism will result in an immediate award of 0 mark to the team for the entire project. Same applies to the hardware implementation. If multiple reports are found as copies, an immediate award of 0 mark shall be awarded to ALL parties without further deliberation.

6. Resources

Logisim: Logisim software can be downloaded from:

http://ozark.hendrix.edu/~burch/logisim/download.html