Logic Solver

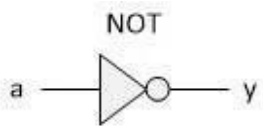
Rules:

1. Plagiarism is forbidden.
2. Write your program with C++.

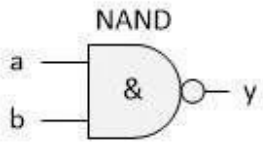
Problem Definition:

✓ You are given a combinational circuit with several logic gates, where the circuit has no feedback loops.

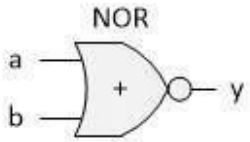
✓ The circuit is composed of three kinds of logic gates. They are INV(NOT), NAND and NOR respectively. The following are those gates' truth tables.



a	y
0	1
1	0



a	b	y
0	0	1
0	1	1
1	0	1
1	1	0



a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

✓ There are three types of wires: input wires, connection wires, and output wires. Input wires carry initial input logic and are not connected to any gate's output; in other words, they have no fan-in gates. In contrast, output wires carry output logic and are not connected to any gate's input, meaning they have no fan-out gates.

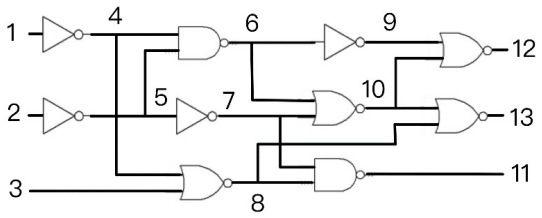
✓ Solve the logic on those output wires.

I/O Format:

Example 1: Input:

```
w1 w2 w3
0 1 0
w11 w12 w13
INV g1 w1 w4
INV g2 w2 w5
NAND g3 w4 w5 w6
INV g4 w5 w7
NOR g5 w4 w3 w8
INV g6 w6 w9
NOR g7 w6 w7 w10
NAND g8 w7 w8 w11
NOR g9 w9 w10 w12
NOR g10 w10 w8 w13
```

The circuit be like:

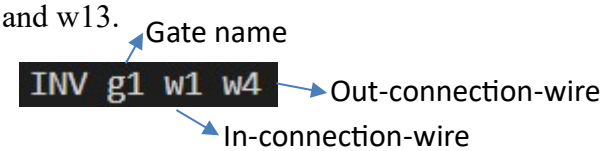


Output:

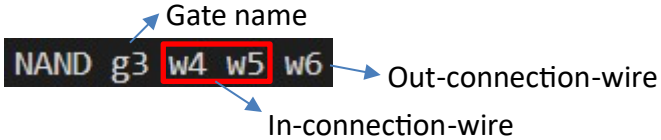
```
w11 1
w12 1
w13 1
```

Explanation:

- ✓ The input wires of above circuit are w1, w2 and w3. The following line stands for the initial logics of this circuit with the same order of input wires.
- ✓ The output wires of above circuit are w11, w12 and w13.
- ✓ The netlist structure of INV:



- ✓ The netlist structure of NAND and NOR:



Constraints:

- ✓ Follow the given output wires order to print out the answer