1. Description

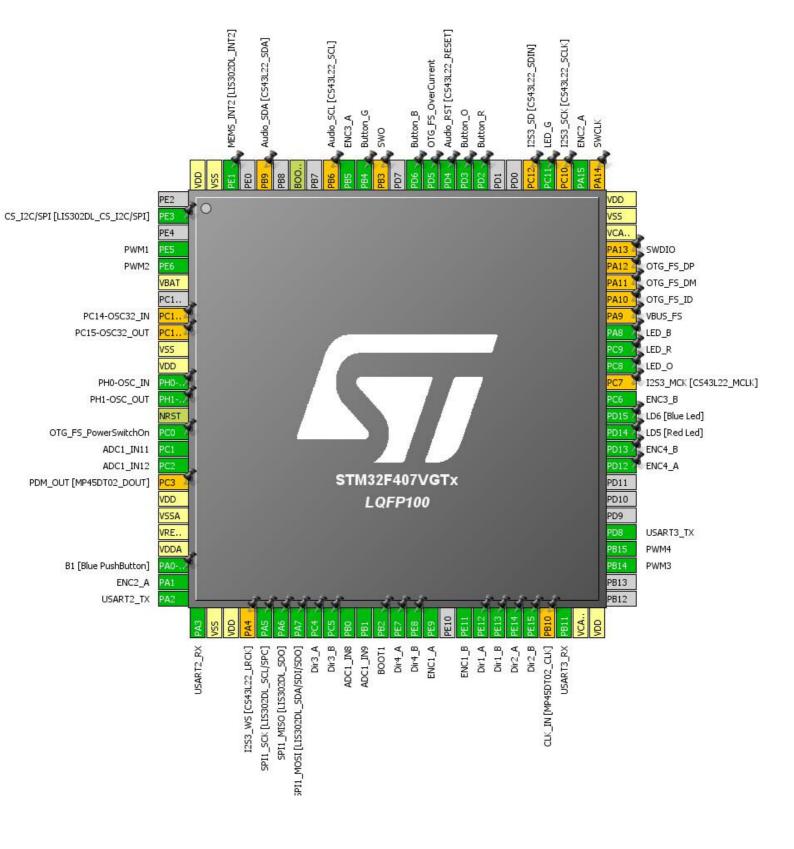
1.1. Project

Project Name	PooNim_CubeMX
Board Name	STM32F4DISCOVERY
Generated with:	STM32CubeMX 4.22.1
Date	10/12/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

Die Nursker	Die Nesse	Dia Tura	A It a wa a t a	Labal
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP100	(function after		Function(s)	
	reset)			
2	PE3 *	I/O	GPIO_Output	CS_I2C/SPI [LIS302DL_CS_I2C/SPI]
4	PE5	I/O	TIM9_CH1	PWM1
5	PE6	I/O	TIM9_CH2	PWM2
6	VBAT	Power		
8	PC14-OSC32_IN **	I/O	RCC_OSC32_IN	PC14-OSC32_IN
9	PC15-OSC32_OUT **	I/O	RCC_OSC32_OUT	PC15-OSC32_OUT
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	PH0-OSC_IN
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	PH1-OSC_OUT
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	OTG_FS_PowerSwitchOn
16	PC1	I/O	ADC1_IN11	
17	PC2	I/O	ADC1_IN12	
18	PC3 **	I/O	12S2_SD	PDM_OUT
				[MP45DT02_DOUT]
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	GPIO_EXTI0	B1 [Blue PushButton]
24	PA1	I/O	TIM2_CH2	ENC2_A
25	PA2	I/O	USART2_TX	
26	PA3	I/O	USART2_RX	
27	VSS	Power		
28	VDD	Power		
29	PA4 **	I/O	I2S3_WS	
30	PA5	I/O	SPI1_SCK	SPI1_SCK [LIS302DL_SCL/SPC]
31	PA6	I/O	SPI1_MISO	SPI1_MISO [LIS302DL_SDO]
32	PA7	I/O	SPI1_MOSI	SPI1_MOSI [LIS302DL_SDA/SDI/SDO]
33	PC4 *	I/O	GPIO_Output	Dir3_A
34	PC5 *	I/O	GPIO_Output	Dir3_B
35	PB0	I/O	ADC1_IN8	

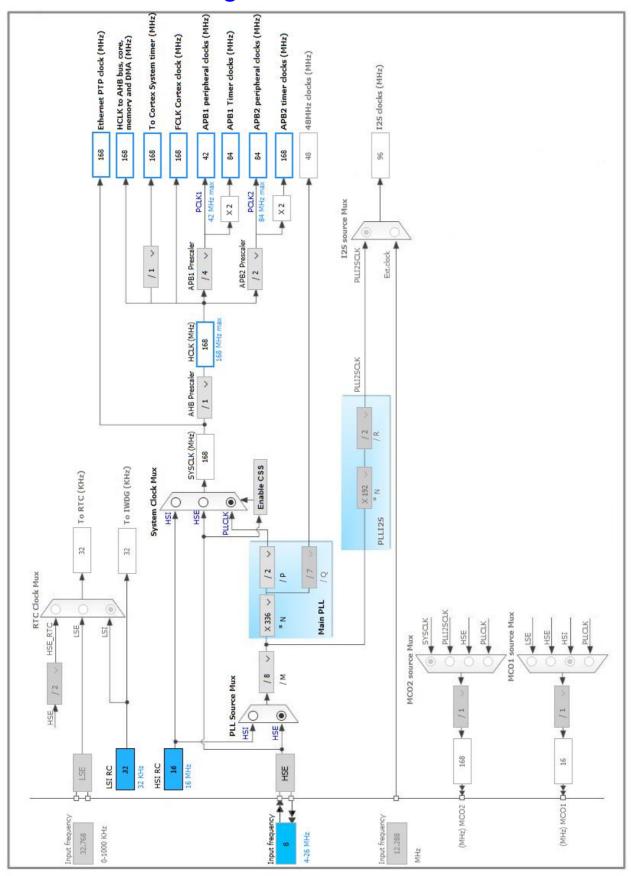
Pin Number LQFP100	Pin Name (function after	Pin Type	Alternate Function(s)	Label
	reset)			
36	PB1	I/O	ADC1_IN9	
37	PB2 *	I/O	GPIO_Input	BOOT1
38	PE7 *	I/O	GPIO_Output	Dir4_A
39	PE8 *	I/O	GPIO_Output	Dir4_B
40	PE9	I/O	TIM1_CH1	ENC1_A
42	PE11	I/O	TIM1_CH2	ENC1_B
43	PE12 *	I/O	GPIO_Output	Dir1_A
44	PE13 *	I/O	GPIO_Output	Dir1_B
45	PE14 *	I/O	GPIO_Output	Dir2_A
46	PE15 *	I/O	GPIO_Output	Dir2_B
47	PB10 **	I/O	I2S2_CK	CLK_IN [MP45DT02_CLK]
48	PB11	I/O	USART3_RX	,
49	VCAP_1	Power		
50	VDD	Power		
53	PB14	I/O	TIM12_CH1	PWM3
54	PB15	I/O	TIM12_CH2	PWM4
55	PD8	I/O	USART3_TX	
59	PD12	I/O	TIM4_CH1	ENC4_A
60	PD13	I/O	TIM4_CH2	ENC4_B
61	PD14 *	I/O	GPIO_Output	LD5 [Red Led]
62	PD15 *	I/O	GPIO_Output	LD6 [Blue Led]
63	PC6	I/O	TIM3_CH1	ENC3_B
64	PC7 **	I/O	12S3_MCK	12S3_MCK [CS43L22_MCLK]
65	PC8 *	I/O	GPIO_Output	LED_O
66	PC9 *	I/O	GPIO_Output	LED_R
67	PA8 *	I/O	GPIO_Output	LED_B
68	PA9 **	I/O	USB_OTG_FS_VBUS	VBUS_FS
69	PA10 **	I/O	USB_OTG_FS_ID	OTG_FS_ID
70	PA11 **	I/O	USB_OTG_FS_DM	OTG_FS_DM
71	PA12 **	I/O	USB_OTG_FS_DP	OTG_FS_DP
72	PA13 **	I/O	SYS_JTMS-SWDIO	SWDIO
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 **	I/O	SYS_JTCK-SWCLK	SWCLK
77	PA15	I/O	TIM2_CH1	ENC2_A
78	PC10 **	I/O	12S3_CK	I2S3_SCK [CS43L22_SCLK]
79	PC11 *	I/O	GPIO_Output	LED_G

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
80	PC12 **	I/O	I2S3_SD	I2S3_SD [CS43L22_SDIN]
83	PD2	I/O	GPIO_EXTI2	Button_R
84	PD3	I/O	GPIO_EXTI3	Button_O
85	PD4 *	I/O	GPIO_Output	Audio_RST [CS43L22_RESET]
86	PD5 *	I/O	GPIO_Input	OTG_FS_OverCurrent
87	PD6	I/O	GPIO_EXTI6	Button_B
89	PB3 **	I/O	SYS_JTDO-SWO	SWO
90	PB4	I/O	GPIO_EXTI4	Button_G
91	PB5	I/O	TIM3_CH2	ENC3_A
92	PB6 **	I/O	I2C1_SCL	Audio_SCL [CS43L22_SCL]
94	воото	Boot		
96	PB9 **	I/O	I2C1_SDA	Audio_SDA [CS43L22_SDA]
98	PE1	I/O	GPIO_EXTI1	MEMS_INT2 [LIS302DL_INT2]
99	VSS	Power		
100	VDD	Power		

^{*} The pin is affected with an I/O function

^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN8 mode: IN9 mode: IN11 mode: IN12

mode: Temperature Sensor Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment

Scan Conversion Mode

Enabled *

Continuous Conversion Mode

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

Right alignment

Enabled *

Enabled *

Enabled *

End Of Conversion Selection EOC flag at the end of all conversions *

ADC_Regular_ConversionMode:

Number Of Conversion 5 *

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel 8
Sampling Time 3 Cycles
Rank 2 *

Channel Channel 8
Sampling Time 3 Cycles

Rank 3 *

Channel 8
Sampling Time 3 Cycles
Rank 4 *

Channel 8

Sampling Time 3 Cycles
Rank 5 *

Channel 8
Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

5.3. SPI1

Mode: Full-Duplex Master

5.3.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola
Data Size 8 Bits
First Bit MSB First

Clock Parameters:	
Prescaler (for Baud Rate)	2
Baud Rate	42.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSS Signal Type	Software
<i>5.4.</i> SYS Timebase Source: SysTick	
5.5. TIM1 Combined Channels: Encoder Mod 5.5.1. Parameter Settings:	de
_	
Counter Settings:	0
Prescaler (PSC - 16 bits value) Counter Mode	0 Ha
Counter Mode Counter Period (AutoReload Register - 16 bits value)	Up
	2048 *
Internal Clock Division (CKD)	No Division 0
Repetition Counter (RCR - 8 bits value)	
Trigger Output (TRGO) Parameters:	Piceble (see some between this TIM (Master) and its Observe
Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)
Encoder:	
Encoder Mode	Encoder Mode TI1 and TI2 *
Parameters for Channel 1	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	5 *
Parameters for Channel 2	Pitter Educ
Polarity	Rising Edge
IC Selection Prescaler Division Ratio	Direct No division
Prescaler Division Ratio Input Filter	
mpat i moi	5 *

5.6. TIM2

Combined Channels: Encoder Mode

5.6.1. Parameter Settings:

Counter Settings:	
Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
Trigger Output (TRGO) Parameters:	
Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)
Encoder:	
Encoder Mode	Encoder Mode TI1
Parameters for Channel 1	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
Parameters for Channel 2	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.7. TIM3

Combined Channels: Encoder Mode

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 0

Internal Clock Division (CKD) No Division

Trigger Output (TRGO) Parameters:	
Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)
Encoder:	
Encoder Mode	Encoder Mode TI1
Parameters for Channel 1	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
Parameters for Channel 2	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
5.8 TIMA	
5.8. TIM4 Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD)	0 Up
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value)	0 Up 0
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD)	0 Up 0
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters:	0 Up 0 No Division
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder:	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR)
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder: Encoder Mode	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR) Encoder Mode TI1
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder: Encoder Mode Parameters for Channel 1	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR)
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder: Encoder Mode Parameters for Channel 1 Polarity	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR) Encoder Mode TI1 Rising Edge
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder: Encoder Mode Parameters for Channel 1 Polarity IC Selection	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR) Encoder Mode TI1 Rising Edge Direct
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder: Encoder Mode Parameters for Channel 1 Polarity IC Selection Prescaler Division Ratio	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR) Encoder Mode TI1 Rising Edge Direct No division
Combined Channels: Encoder Mo 5.8.1. Parameter Settings: Counter Settings: Prescaler (PSC - 16 bits value) Counter Mode Counter Period (AutoReload Register - 16 bits value) Internal Clock Division (CKD) Trigger Output (TRGO) Parameters: Master/Slave Mode Trigger Event Selection Encoder: Encoder Mode Parameters for Channel 1 Polarity IC Selection Prescaler Division Ratio Input Filter	0 Up 0 No Division Disable (no sync between this TIM (Master) and its Slaves Reset (UG bit from TIMx_EGR) Encoder Mode TI1 Rising Edge Direct No division

Prescaler Division Ratio No division

Input Filter 0

5.9. TIM5

mode: Clock Source

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 41999 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 199 *

Internal Clock Division (CKD)

No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection Reset (UG bit from TIMx_EGR)

5.10. TIM9

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 33599 *

Internal Clock Division (CKD)

No Division

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Fast Mode Disable CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Fast Mode Disable
CH Polarity High

5.11. TIM12

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 16799 *

Internal Clock Division (CKD) No Division

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0
Fast Mode Disable
CH Polarity High

5.12. USART2

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

5.13. USART3

Mode: Multiprocessor Communication

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity Non Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples Wake-Up Method Idle Line

^{*} User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
ADCI	PC2	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_SCK [LIS302DL_SCL/SPC]
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_MISO [LIS302DL_SDO]
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_MOSI [LIS302DL_SDA/SDI/SDO]
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	Pull-up *	Low	ENC1_A
	PE11	TIM1_CH2	Alternate Function Push Pull	Pull-up *	Low	ENC1_B
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	Pull-up *	Low	ENC2_A
	PA15	TIM2_CH1	Alternate Function Push Pull	Pull-up *	Low	ENC2_A
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	Pull-up *	Low	ENC3_B
	PB5	TIM3_CH2	Alternate Function Push Pull	Pull-up *	Low	ENC3_A
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	Pull-up *	Low	ENC4_A
	PD13	TIM4_CH2	Alternate Function Push Pull	Pull-up *	Low	ENC4_B
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	Pull-up *	High *	PWM1
	PE6	TIM9_CH2	Alternate Function Push Pull	Pull-up *	High *	PWM2
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	Pull-up *	High *	PWM3
	PB15	TIM12_CH2	Alternate Function Push Pull	Pull-up *	High *	PWM4
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	Very High	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	Very High	
USART3	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
Single Mapped	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	PC14-OSC32_IN
Signals	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	PC15-OSC32_OUT
	PC3	I2S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	PDM_OUT [MP45DT02_DOUT]
	PA4	12S3_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S3_WS [CS43L22_LRCK]
	PB10	12S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	CLK_IN [MP45DT02_CLK]
	PC7	I2S3_MCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	I2S3_MCK [CS43L22_MCLK]
	PA9	USB_OTG_FS_ VBUS	Input mode	No pull-up and no pull-down	n/a	VBUS_FS
	PA10	USB_OTG_FS_I D	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_ID
	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_DM
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_DP
	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	SWCLK
	PC10	12S3_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	12S3_SCK [CS43L22_SCLK]
	PC12	12S3_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	12S3_SD [CS43L22_SDIN]
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	Audio_SCL [CS43L22_SCL]
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	Audio_SDA [CS43L22_SDA]
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CS_I2C/SPI [LIS302DL_CS_I2C/SPI]
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_PowerSwitchOn
	PA0-WKUP	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC4	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir3_A
	PC5	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir3_B
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE7	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir4_A
	PE8	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir4_B
	PE12	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir1_A
	PE13	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir1_B
	PE14	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir2_A
	PE15	GPIO_Output	Output Push Pull	Pull-down *	Low	Dir2_B
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD5 [Red Led]
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD6 [Blue Led]
	PC8	GPIO_Output	Output Push Pull	Pull-down *	Low	LED_O
	PC9	GPIO_Output	Output Push Pull	Pull-down *	Low	LED_R
	PA8	GPIO_Output	Output Push Pull	Pull-down *	Low	LED_B
	PC11	GPIO_Output	Output Push Pull	Pull-down *	Low	LED_G
	PD2	GPIO_EXTI2	External Interrupt	No pull-up and no pull-down	n/a	Button_R
			Mode with Falling			
			edge trigger detection			
	PD3	GPIO_EXTI3	External Interrupt	No pull-up and no pull-down	n/a	Button_O
			Mode with Falling			
			edge trigger detection			
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Audio_RST [CS43L22_RESET]
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_FS_OverCurrent
	PD6	GPIO_EXTI6	External Interrupt	No pull-up and no pull-down	n/a	Button_B
			Mode with Falling			
			edge trigger detection			
	PB4	GPIO_EXTI4	External Interrupt	No pull-up and no pull-down	n/a	Button_G
			Mode with Falling			
			edge trigger detection			
	PE1	GPIO_EXTI1	External Event Mode	No pull-up and no pull-down	n/a	MEMS_INT2
			with Rising edge			[LIS302DL_INT2]
			trigger detection *			

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line2 interrupt	true	0	0
EXTI line3 interrupt	true	0	0
EXTI line4 interrupt	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	0	0
EXTI line[9:5] interrupts	true	0	0
USART2 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt		unused	
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
FPU global interrupt	unused		

^{*} User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

	1
Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	022152 Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.3