ARM926EJ-S Based

32-bit Microprocessor

NUC980 Series
Datasheet

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1 GENERAL DESCRIPTION

The NUC980 series 32-bit microprocessor is powered by the Arm926EJ-S™ processor core with 16 KB I-cache, 16 KB D-cache and MMU running up to 300 MHz. Its SDRAM interface supports SDR/DDR/DDR2/LPDDR type SDRAM running up to 150 MHz. The NUC980 series supports built-in 16KB embedded SRAM and 16.5 KB IBR (Internal Boot ROM) for booting from USB, NAND, SD/eMMC and SPI Flash, and industrial operating temperature from -40°C to 85°C. In addition, the NUC980 series provides built-in DDR in LQFP package to ease PCB design and reduce the BOM cost.

The NUC980 series is equipped with a large number of high speed digital peripherals, such as two 10/100 Mbps Ethernet MAC supporting RMII, a USB 2.0 high speed host/device, a USB 2.0 high speed host controller, up to six USB 2.0 full speed host lite interfaces, two CMOS sensor interfaces supporting CCIR601 and CCIR656 type sensor, two SD interfaces supporting SD/SDHC/SDIO card, a NAND Flash interface supporting SLC and MLC type NAND Flash, an I2S interface supporting I2S and PCM protocol, Also the NUC980 series offers a built-in hardware cryptography accelerator that supports RSA, ECC, AES, SHA, HMAC and a random number generator (RNG).

The NUC980 series provides up to ten UART interfaces, two ISO-7816-3 interfaces, a Quad-SPI interface, two SPI interfaces, up to four I2C interfaces, four CAN 2.0B interfaces, eight channels PWM output, eight channels 12-bit SAR ADC, six 32-bit timers, WDT (Watchdog Timer), WWDT(Window Watchdog Timer), 32.768 kHz XTL and RTC (Real Time Clock). The NUC980 series also supports two 10-channel peripheral DMA (PDMA) for automatic data transfer between memories and peripherals.

Key Features

- 300 MHz ARM® ARM926EJ-S™ MPU with 16 KB I-cache, 16 KB D-cache
- Memory Manager Unit (MMU)
- Built-in 64 MB /32 MB/16 MB/8 MB DDR Memory in LQFP package
- Supports booting from SPI ROM/SPI NAND Flash/NAND/eMMC/SD Card and USB device
- Supports up to 100MHz Quad-SPI
- Dual Ethernet MAC
- Four CAN 2.0B interfaces
- Six USB FS Lite hosts
- Two USB High speed hosts
- One USB High speed device
- Two CCIR656/601 Camera interfaces
- Supports PRNG, AES256, SHA, ECC, and RAS2048

Applications

- Smart Home gateway
- Fingerprint Machine.
- Power concentrator
- Data Collector
- Smart Home Appliance
- Serial server
- 2D/1D Barcode reader
- Barcode printer
- Power Distribution Unit
- Ethernet Industrial Control
- SNMP Card
- Ethernet RTU / DTU

2 FEATURES DESCRIPTION

Core And System	
Boot Loader	• Factory pre-loaded 16.5 KB mask ROM supporting four booting modes – Boot from USB – Boot from SD/eMMC – Boot from NAND Flash – Boot from SPI Flash (SPI-NOR/SPI-NAND)
Arm926EJ-S™	• Arm926EJ-S™ processor core running up to 300 MHz • Built-in 16 KB instruction cache and 16 KB data cache • Built-in Memory Management Unit (MMU) • Supports JTAG debug interface
Advanced Interrupt Controller	• Up to 64 interrupt sources including 4 external interrupts. • Configurable normal (IRQ) or fast interrupt mode (FIQ). • Configurable 8-level interrupt priority scheme.
Low Voltage Detect (LVD)	• Two-level LVD with low voltage detect interrupt. (2.8V/2.6V)
Low Voltage Reset (LVR)	• LVR with 2.4V threshold voltage level.
Memories	
SDRAM	• Supports SDR (Single-Data-Rate), DDR (Double-Data-Rate), DDR2 (Double-Data-Rate 2) and LPDDR (Low Power DDR) SDRAM • Clock speed up to 150 MHz • Supports 16-bit data width •
SRAM	• Up to 16 KB on-chip SRAM • Byte-, half-word- and word-access • PDMA operation
Peripheral DMA (PDMA)	• Two sets of PDMA with ten independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 12 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and

	low-power system operation
Internal Clock Source	• Two on-chip PLL up to 500 MHz on-chip PLL, sourced from HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain (VBAT33) • The RTC clock source includes Low-speed external crystal oscillator (LXT) • The RTC block includes 64 bytes backup registers • Able to wake up CPU • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Selectable 12-hour or 24-hour mode • Automatic leap year recognition • Supports 1 Hz clock to be Timer capture source for calibration
Timers	
32-bit Timer	• Six sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports internal capture source from RTC 1 Hz clock for interval measurement resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated
PWM (PWM)	• Eight 16-bit down-count counters with four 8-bit prescalar for eight PWM output channels. • Supports complementary mode for 4 complementary paired PWM output channels
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from HXT, HXT/512 (default selection), PCLK2/4096 or LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset.
Window Watchdog	• Clock sourced from HXT, HXT/512 (default selection), PCLK2/4096 or LXT; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• One 12-bit, 9-ch 200k SPS SAR ADC with up to 8 single-ended input channels; 10-bit accuracy is guaranteed. • One internal channels for band-gap VBG input.

	• Supports external V_{REF} pin.
Communication Interfaces	
Low-power UART	• 10 sets of UARTs with up to 17.45 MHz baud rate. • Auto-Baud Rate measurement and baud rate compensation function. • Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped. • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode. • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation.
Smart Card Interface	• Two sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function. • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal.
I^2C	• Four sets of I^2C devices with Master/Slave mode. • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
Quad SPI	• One set of SPI Quad controller with Master/Slave mode, up to 96 MHz at 2.7V~3.6V stsyem voltage. • Supports Dual and Quad I/O Transfer mode

	• Supports one/two data channel half-duplex transfer • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation.
SPI	• Up to two sets of SPI controllers with Master/Slave mode. • SPI provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers. • Able to communicate at up to 96 Mbit/s • Configurable bit length of a transfer word from 8 to 32-bit. • MSB first or LSB first transfer sequence. • Byte reorder function. • Supports Byte or Word Suspend mode. • Supports one data channel half-duplex transfer. • Supports receive-only mode. • PDMA operation.
I^2S	• One set of I^2S controller with I^2S protocol and PCM protocol. • Supports mono and stereo audio data with 8-, 16- and 24-bit word sizes. • Four 8-level 24-bit FIFO data buffers for left/right channel record and left/right playback. • Built-in DMA function • Supports 2 buffer address for left/right channel and 2 slots data transfer. **I^2S Mode** • Supports record and playback. • Supports master and slave mode. • Supports Philips standard and MSB-justified data format. **PCM Mode** • Supports record and playback. • Supports master mode. • Supports PCM standard data format.
Controller Area Network (CAN)	• Four CAN 2.0B interfaces • Each supports 32 Message Objects; each Message Object has its own identifier mask. • Programmable FIFO mode (concatenation of Message Object). • Disabled Automatic Re-transmission mode for Time Triggered CAN applications. • Supports power-down wake-up function.
Secure Digital Host Controller (SDHC)	• Two sets of Secure Digital Host Controllers, compliant with SD Memory Card Specification Version 2.0.

	• Supports 50 MHz to achieve 200 Mbps at 3.3V operation. • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card.
NAND Flash Controller	• Supports SLC and MLC type NAND Flash device. • Supports 2KB, 4KB and 8KB page size NAND Flash device. • 8-bit data width. • Supports ECC8, ECC12 and ECC24 BCH algorithm with ECC code generation, error detection and error correction. • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and NAND Flash.
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter. • Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space. • 8-/16-bit data width. • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R). • Supports address bus and data bus separate mode. • Supports LCD interface i80 mode. • PDMA operation.
GPIO	• Supports four I/O modes: Bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode. • Selectable TTL/Schmitt trigger input. • Configured as interrupt source with edge/level trigger setting. • Supports independent pull-up/pull-down control. • Supports 5V-tolerance function except analog I/O. (Except PB.0 ~ 7; All USB High Speed PIN.)
	•
Advanced Connectivity	
USB 2.0 Full Speed Host Lite	• Compliant with USB Revision 2.0 Specification. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Supports Control, Bulk, Interrupt, Isochronous and Split transfers. • Supports an integrated Root Hub. • Up to six USB Host Lite ports. • Built-in DMA.
USB 2.0 High Speed with on-chip transceiver	**USB 2.0 High Speed Host/Device** • One set of on-chip USB 2.0 high speed dual role transceiver configurable as host, device or ID-dependent. • One set of on-chip USB 2.0 high speed transceiver with host only. **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification. • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0.

	• Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Integrated with a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Built-in DMA. **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports one dedicate control endpoint and 12 configurable endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction. • 4096 bytes configurable RAM for endpoint buffer and up to 1024 bytes packet size. • Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode. • Suspend, resume and remote wake-up capability. • Built-in DMA.
Ethernet MAC	• IEEE Std. 802.3 CSMA/CD protocol. • Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol. • Two sets of Ethernet MAC. • Supports both half and full duplex for 10 Mbps or 100 Mbps operation. • RMII (Reduced Media Independent Interface) and serial management interface (MDC/MDIO). • Pause and remote pause function for flow control. • Long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception. • CAM function for Ethernet MAC address recognition. • Supports Magic Packet recognition to wake system up from Power-down mode. • Built-in DMA.
CMOS Sensor Interface	• Two sets of CMOS sensor interfaces supporting CCIR601 and CCIR656 type sensor. • Resolution up to 3M pixels. • Supports YUV422 and RGB565 color format for data output by CMOS image sensor. • Supports YUV422, RGB565, RGB555 and Y-only color format with planar and packet data format for data storing to system memory. • Supports image cropping and cropping window up to 4096x2048. • Supports vertical and horizontal scaling-down with N/M scaling factor. • Supports Negative, Sepia and Posterization color effects
Cryptography Accelerator	
Rivest、Shamir and Adleman Cryptography (RSA)	• Hardware RSA accelerator. • Supports both encryption and decryption. • Supports up to 2048 bits.
Elliptic Curve	• Hardware ECC accelerator.

Cryptography (ECC)	• Supports 192-bit and 256-bit key length. • Supports both prime field GF(p) and binary field GF(2m). • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes. • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes. • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes. • Supports point multiplication, addition and doubling operations in GF(p) and GF(2m). • Supports modulus division, multiplication, addition and subtraction operations in GF(p).
Advanced Encryption Standard (AES)	• Hardware AES accelerator. • Supports 128-bit, 192-bit and 256-bit key length and key expander, and compliant with FIPS 197. • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum.
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator. • Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512. • Compliant with FIPS 180/180-2.
keyed-Hash Message Authentication Code (HMAC)	• Hardware HMAC accelerator. • Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512. • Compliant with FIPS 180/180-2.
PRNG	• Supports 64-/128-/192-/256-bit random number generator.

3 PARTS INFORMATION

3.1 Package Type

Part No.	LQFP64-EP	LQFP128	LQFP216
NUC980	NUC980DRxxY	NUC980DKxxY, NUC980DKxxYC	NUC980DFxxYC

Figure 3-1 NUC980 Series Package Type

3.2 NUC980 Series Part Selection Guide

Part Number		NUC980					
		DF71YC	DK61YC	DK61Y	DK41Y	DR61Y	DR41Y
DDR Size(MB)		128	64		16	64	16
I/O		104	92			40	
32-bit Timer		6	6			6	
RTC		√	√			-	
Connectivity	UART	10	10			8	
	ISO-7816	2	2			2	
	Quad SPI	1	1			1	
	SPI	3	3			2	
	I^2S	1	1			1	
	I^2C	4	4			2	
	CAN	4	4	-		-	
	SDHC/SDIO	2	2			2	
Crypto	PRNG 256	√	√			√	
	AES 256	√	√			√	
	RSA 2048	√	√			√	
	ECC	√	√			√	
	HMAC SHA 512	√	√			√	
	SHA 512	√	√			√	
External Bus Interface		√	√			-	
Camera Interface		2	2			2	
SPI NAND		√	√			√	
NAND Flash Interface		√	√			√	
16-bit PWM		8	8			5	
10/100Mb Ethernet MAC		2	2			1	
USB 1.1 FS Host Lite		6	6	-		-	
USB 2.0 HS Host		1	1			-	
USB 2.0 HS Host / Device		1	1			1	
12-bit ADC		8	8			2	
Package		LQFP216	LQFP 128			LQFP 64 - EP	

Table 3.2-1 NUC980 Series Part Selection Guide

3.3 NUC980 Series Naming Rule

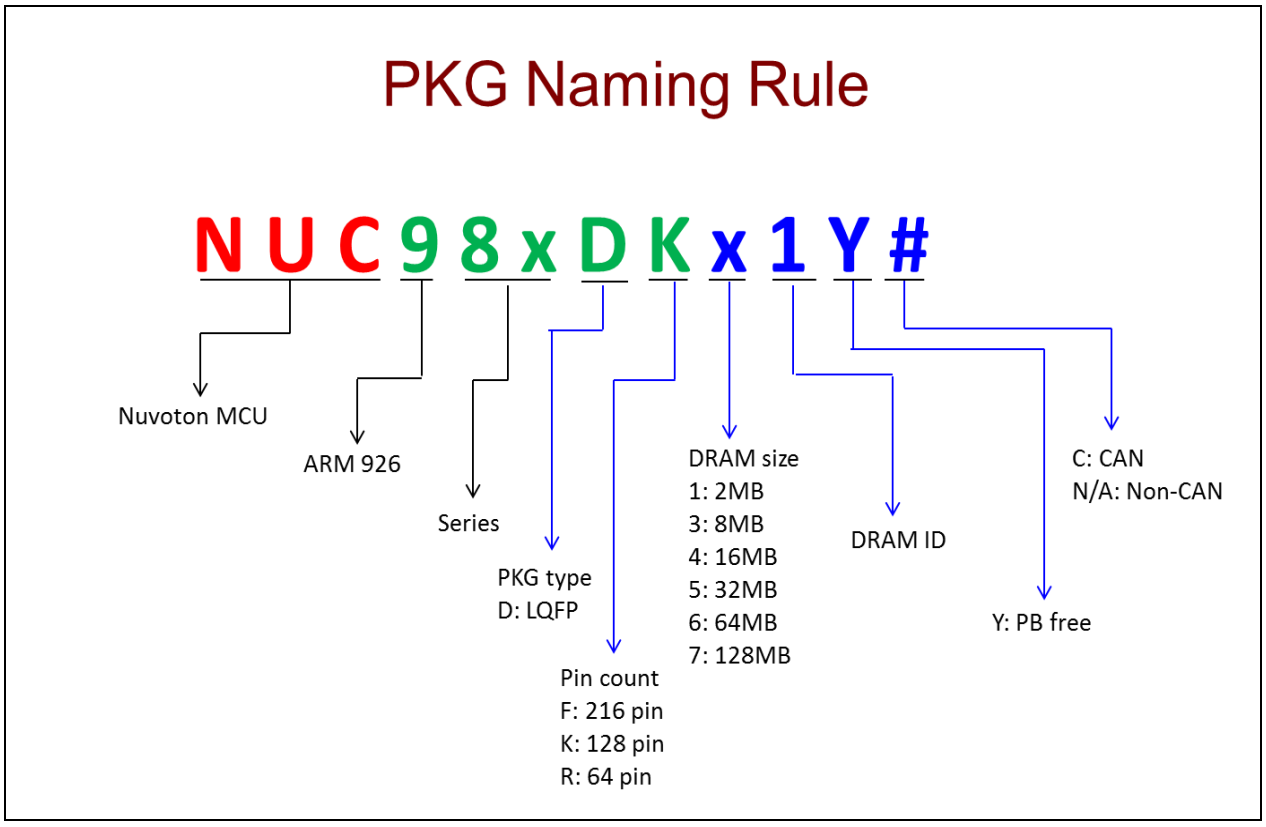


Figure 3.3-1 NUC980 Series Selection Code

4 PIN CONFIGURATION

4.1 Pin Configuration

4.1.1 NUC980DRxxY LQFP64-EP Pin Diagram

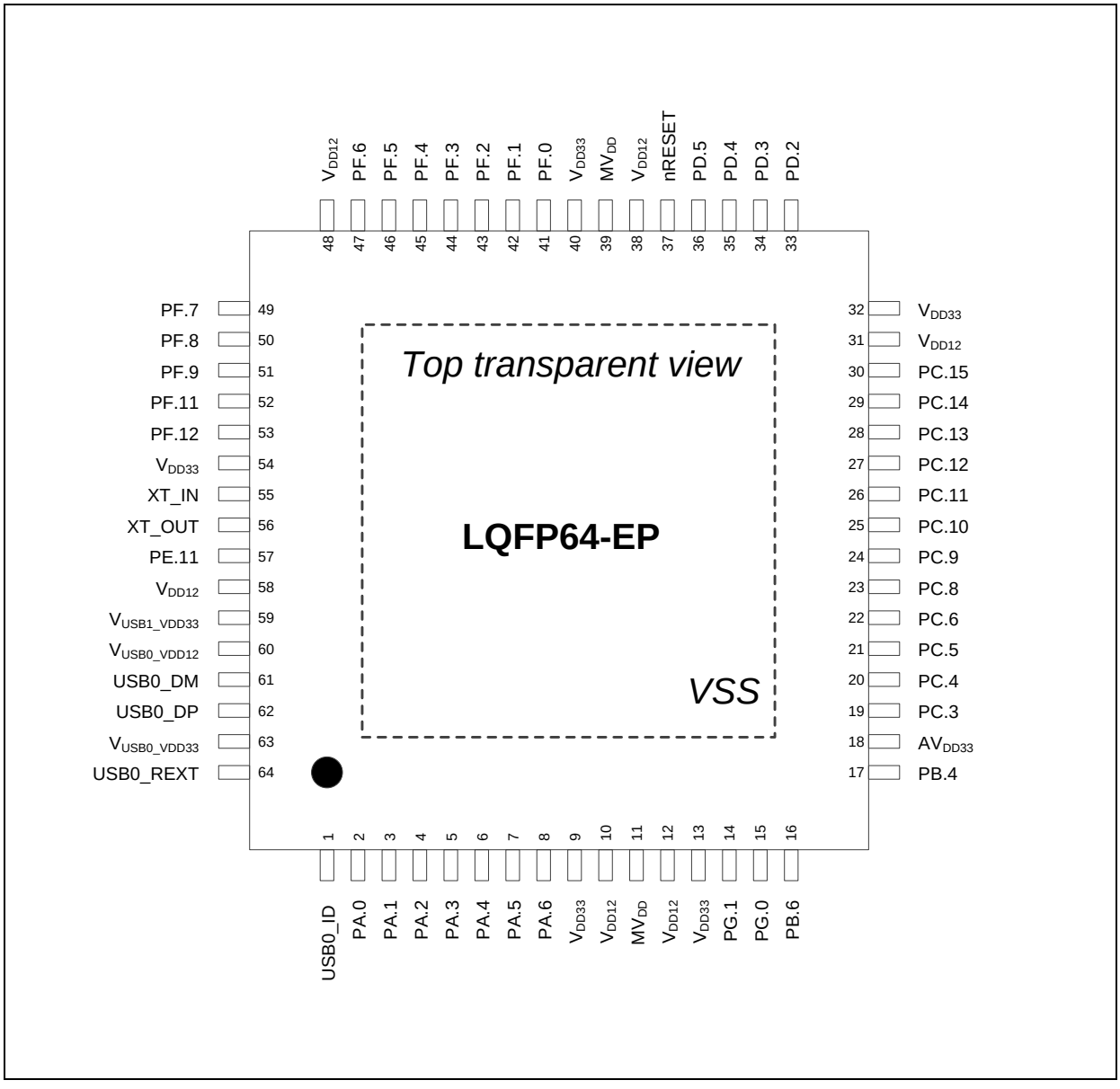


Figure 4.1-1 NUC980DRxxY LQFP 64-pin with EX-PAD Diagram

4.1.2 NUC980DKxxYx LQFP128 Pin Diagram

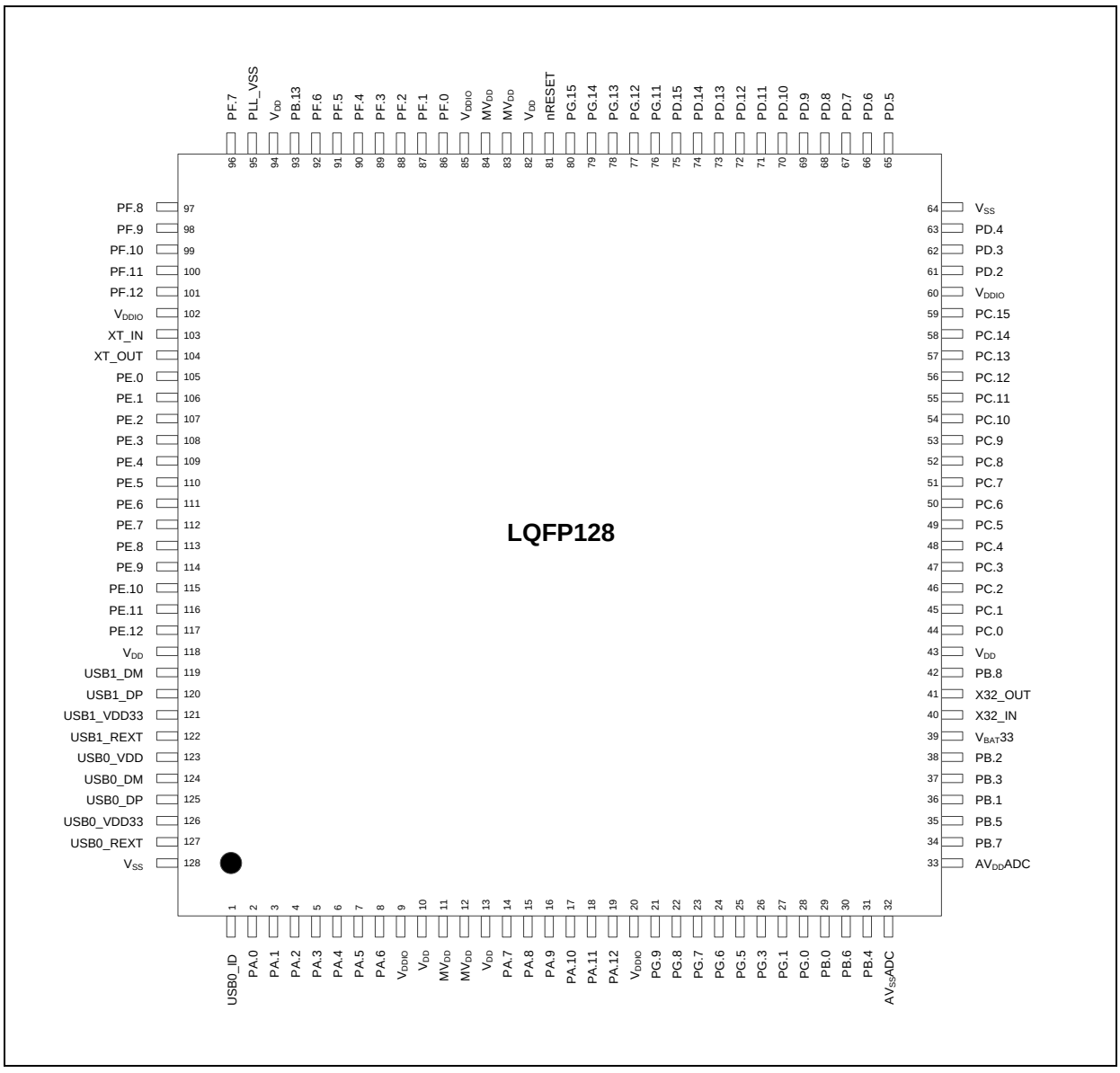


Figure 4.1-2 NUC980DKxxYx LQFP 128-pin Diagram

4.1.3 NUC980DFxxYC LQFP216 Pin Diagram

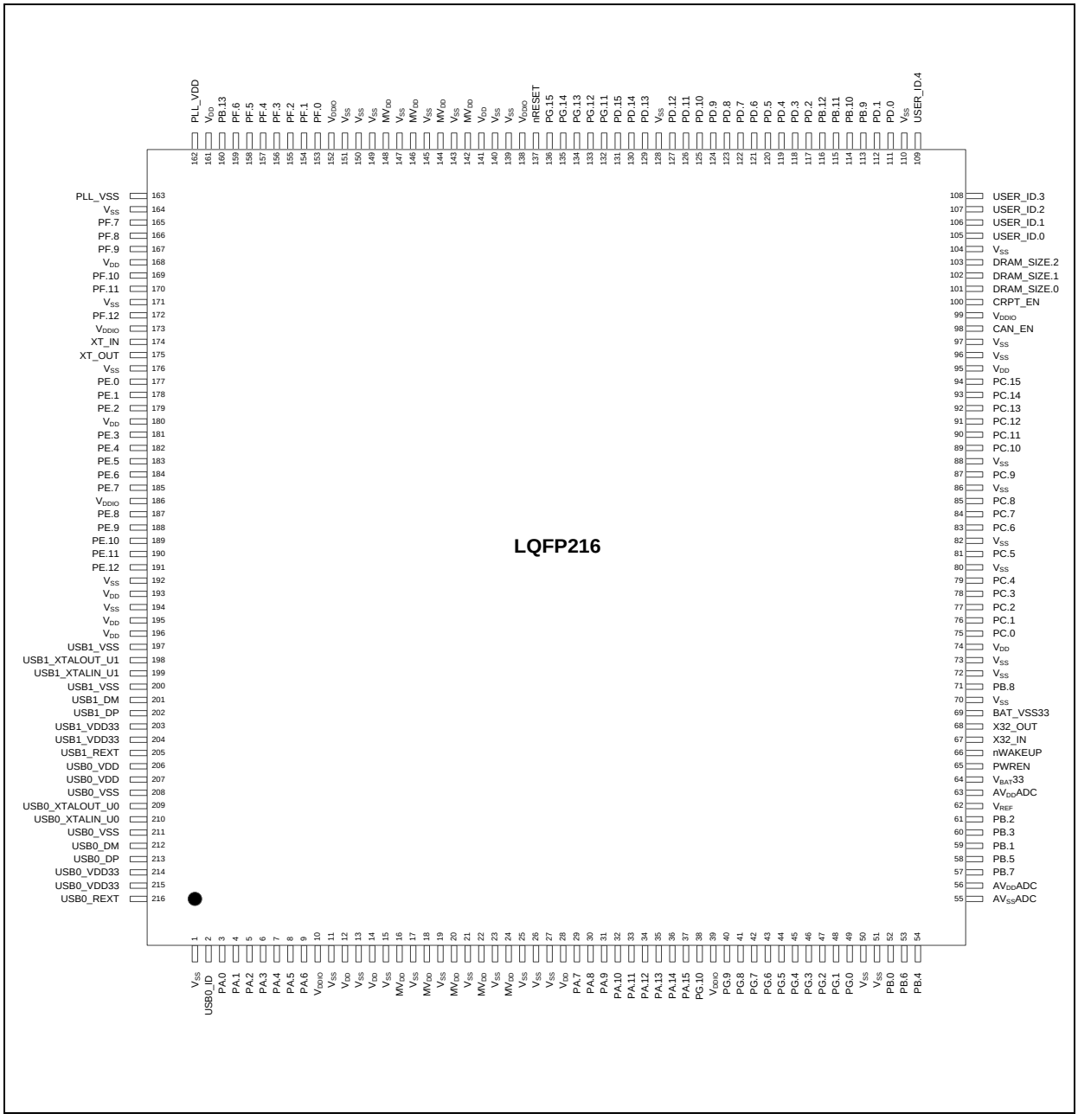


Figure 4.1-3 NUC980DFxxYC LQFP 216-pin Diagram

4.2 Pin Description

4.2.1 NUC980 Pin Description

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		1	V_{SS}	P	MFP0	Ground pin for digital circuit.
1	1	2	USB0_ID	IU	-	USB0 Host/Device identification with an internal pull-up. 1: Device (default) 0: Host
2	2	3	PA.0	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin.
			I2C0_SDA	I/O	MFP3	I^2C0 data input/output pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			EINT0	I	MFP5	External interrupt 0 input pin.
			TM0_ECNT	I/O	MFP6	Timer0 event counter input/toggle output pin.
			CAN3_RXD	I	MFP7	CAN3 bus receiver input.
3	3	4	PA.1	I/O	MFP0	General purpose digital I/O pin.
			EBI_nCS2	O	MFP1	EBI chip select 2 output pin.
			EBI_MCLK	O	MFP2	EBI external clock output pin.
			I2C0_SCL	I/O	MFP3	I^2C0 clock pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			EINT1	I	MFP5	External interrupt 1 input pin.
			TM1_ECNT	I/O	MFP6	Timer1 event counter input/toggle output pin.
			CAN3_TXD	O	MFP7	CAN3 bus transmitter output.
4	4	5	PA.2	I/O	MFP0	General purpose digital I/O pin.
			UART6_CTS	I	MFP1	UART6 clear to Send input pin.
			I2S_LRCK	O	MFP2	I^2S left right channel clock output pin.
			SC0_CD	I	MFP3	Smart Card 0 card detect pin.
			JTAG1_TDO	O	MFP4	JTAG1 data output pin.
			TM2_ECNT	I/O	MFP6	Timer2 event counter input/toggle output pin.
5	5	6	PA.3	I/O	MFP0	General purpose digital I/O pin.
			UART6_RTS	O	MFP1	UART6 request to Send output pin.
			I2S_BCLK	O	MFP2	I^2S bit clock output pin.
			SC0_PWR	O	MFP3	Smart Card 0 power pin.
			JTAG1_TCK	I	MFP4	JTAG1 clock input pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			TM3_ECNT	I/O	MFP6	Timer3 event counter input/toggle output pin.
6	6	7	PA.4	I/O	MFP0	General purpose digital I/O pin.
			UART6_RXD	I	MFP1	UART6 data receiver input pin.
			I2S_DI	I	MFP2	I^2S data input pin.
			SC0_DAT	I/O	MFP3	Smart Card 0 data pin.
			JTAG1_TMS	I	MFP4	JTAG1 test mode selection input pin.
			TM4_ECNT	I/O	MFP6	Timer4 event counter input/toggle output pin.
7	7	8	PA.5	I/O	MFP0	General purpose digital I/O pin.
			UART6_TXD	O	MFP1	UART6 data transmitter output pin.
			I2S_DO	O	MFP2	I^2S data output pin.
			SC0_CLK	O	MFP3	Smart Card 0 clock pin.
			JTAG1_TDI	I	MFP4	JTAG1 data input pin.
			TM5_ECNT	I/O	MFP6	Timer5 event counter input/toggle output pin.
8	8	9	PA.6	I/O	MFP0	General purpose digital I/O pin.
			EBI_nCS1	O	MFP1	EBI chip select 1 output pin.
			I2S_MCLK	O	MFP2	I^2S master clock output pin.
			SC0_RST	O	MFP3	Smart Card 0 reset pin.
			JTAG1_nTRST	I	MFP4	JTAG1 reset input pin.
9	9	10	V_{DD33}	P	MFP0	Power supply for I/O power pin.
		11	V_{SS}	P	MFP0	Ground pin for digital circuit.
10	10	12	V_{DD12}	P	MFP0	Power supply for Internal core power pin.
		13	V_{SS}	P	MFP0	Ground pin for digital circuit.
		14	V_{DD12}	P	MFP0	Power supply for Internal core power pin.
		15	V_{SS}	P	MFP0	Ground pin for digital circuit.
11	11	16	MV_{DD}	P	MFP0	Power supply for Memory ports.
		17	V_{SS}	P	MFP0	Ground pin for digital circuit.
		18	MV_{DD}	P	MFP0	Power supply for Memory ports.
		19	V_{SS}	P	MFP0	Ground pin for digital circuit.
		20	MV_{DD}	P	MFP0	Power supply for Memory ports.
		21	V_{SS}	P	MFP0	Ground pin for digital circuit.
	12	22	MV_{DD}	P	MFP0	Power supply for Memory ports.
		23	V_{SS}	P	MFP0	Ground pin for digital circuit.
		24	MV_{DD}	P	MFP0	Power supply for Memory ports.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		25	V_{SS}	P	MFP0	Ground pin for digital circuit.
		26	V_{SS}	P	MFP0	Ground pin for digital circuit.
		27	V_{SS}	P	MFP0	Ground pin for digital circuit.
12	13	28	V_{DD12}	P	MFP0	Power supply for Internal core power pin.
	14	29	PA.7	I/O	MFP0	General purpose digital I/O pin.
			EBI_nWE	O	MFP1	EBI write enable output pin.
			UART2_CTS	I	MFP2	UART2 clear to Send input pin.
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
	15	30	PA.8	I/O	MFP0	General purpose digital I/O pin.
			EBI_nRE	O	MFP1	EBI read enable output pin.
			UART2_RTS	O	MFP2	UART2 request to Send output pin.
			TM3_TGL	I/O	MFP3	Timer3 event counter input/toggle output pin.
	16	31	PA.9	I/O	MFP0	General purpose digital I/O pin.
			EBI_nCS0	O	MFP1	EBI chip select 0 output pin.
			UART2_RXD	I	MFP2	UART2 data receiver input pin.
			TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin.
	17	32	PA.10	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR10	O	MFP1	EBI address bus bit 10.
			UART2_TXD	O	MFP2	UART2 data transmitter output pin.
			TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin.
	18	33	PA.11	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR9	O	MFP1	EBI address bus bit 9.
			UART8_RXD	I	MFP2	UART8 data receiver input pin.
			TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
	19	34	PA.12	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR8	O	MFP1	EBI address bus bit 8.
			UART8_TXD	O	MFP2	UART8 data transmitter output pin.
			TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin.
		35	PA.13	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR13	O	MFP1	EBI address bus bit 13.
			I2C1_SDA	I/O	MFP2	I^2C1 data input/output pin.
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			USBHL5_DM	A	MFP4	USB 1.1 host lite port-5 differential signal D-.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			CAN1_RXD	I	MFP5	CAN1 bus receiver input.
			UART7_TXD	O	MFP6	UART7 data transmitter output pin.
			PWM03	O	MFP7	PWM03 counter synchronous trigger output pin.
			EINT0	I	MFP8	External interrupt 0 input pin.
		36	PA.14	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR14	O	MFP1	EBI address bus bit 14.
			I2C1_SCL	I/O	MFP2	I^2C1 clock pin.
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
			USBHL5_DP	A	MFP4	USB 1.1 host lite port-5 differential signal D+.
			CAN1_TXD	O	MFP5	CAN1 bus transmitter output.
			UART7_RXD	I	MFP6	UART7 data receiver input pin.
			PWM02	O	MFP7	PWM02 counter synchronous trigger output pin.
			EINT1	I	MFP8	External interrupt 1 input pin.
		37	PA.15	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR19	O	MFP1	EBI address bus bit 19.
			I2C0_SDA	I/O	MFP2	I^2C0 data input/output pin.
			TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin.
			USBHL4_DM	A	MFP4	USB 1.1 host lite port-4 differential signal D-.
			CAN2_RXD	I	MFP5	CAN2 bus receiver input.
			SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin.
			PWM01	O	MFP7	PWM01 counter synchronous trigger output pin.
			I2S_LRCK	O	MFP8	I^2S left right channel clock output pin.
		38	PG.10	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA0	I/O	MFP1	EBI data bus bit 0.
			I2C0_SCL	I/O	MFP2	I^2C0 clock pin.
			TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin.
			USBHL4_DP	A	MFP4	USB 1.1 host lite port-4 differential signal D+.
			CAN2_TXD	O	MFP5	CAN2 bus transmitter output.
			SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
			PWM00	O	MFP7	PWM00 counter synchronous trigger output pin.
			I2S_BCLK	O	MFP8	I^2S bit clock output pin.
13	20	39	V_{DD33}	P	MFP0	Power supply for I/O power pin.
	21	40	PG.9	I/O	MFP0	General purpose digital I/O pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			EBI_ADDR7	O	MFP1	EBI address bus bit 7.
			UART8_CTS	I	MFP2	UART8 clear to Send input pin.
			PWM13	O	MFP6	PWM13 counter synchronous trigger output pin.
			CFG.9_PwrOnSet9	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	22	41	PG.8	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR6	O	MFP1	EBI address bus bit 6.
			UART8_RTS	O	MFP2	UART8 request to Send output pin.
			PWM12	O	MFP6	PWM12 counter synchronous trigger output pin.
			CFG.8_PwrOnSet8	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	23	42	PG.7	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR5	O	MFP1	EBI address bus bit 5.
			UART5_TXD	O	MFP2	UART5 data transmitter output pin.
			PWM11	O	MFP6	PWM11 counter synchronous trigger output pin.
			CFG.7_PwrOnSet7	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	24	43	PG.6	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR4	O	MFP1	EBI address bus bit 4.
			UART5_RXD	I	MFP2	UART5 data receiver input pin.
			PWM10	O	MFP6	PWM10 counter synchronous trigger output pin.
			CFG.6_PwrOnSet6	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	25	44	PG.5	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR12	O	MFP1	EBI address bus bit 12.
			UART5_RTS	O	MFP2	UART5 request to Send output pin.
			CFG.5_PwrOnSet5	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
		45	PG.4	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR18	O	MFP1	EBI address bus bit 18.
			UART5_CTS	I	MFP2	UART5 clear to Send input pin.
			CFG.4_PwrOnSet4	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	26	46	PG.3	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR3	O	MFP1	EBI address bus bit 3.
			UART2_RTS	O	MFP2	UART2 request to Send output pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			PWM03	O	MFP6	PWM03 counter synchronous trigger output pin.
			CFG.3_PwrOnSet3	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
		47	PG.2	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR2	O	MFP1	EBI address bus bit 2.
			UART2_CTS	I	MFP2	UART2 clear to Send input pin.
			PWM02	O	MFP6	PWM02 counter synchronous trigger output pin.
			CFG.2_PwrOnSet2	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
14	27	48	PG.1	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR1	O	MFP1	EBI address bus bit 1.
			UART2_TXD	O	MFP2	UART2 data transmitter output pin.
			PWM01	O	MFP6	PWM01 counter synchronous trigger output pin.
			CFG.1_PwrOnSet1	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
15	28	49	PG.0	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR0	O	MFP1	EBI address bus bit 0.
			UART2_RXD	I	MFP2	UART2 data receiver input pin.
			CLK_OUT	O	MFP3	Internal clock selection output pin.
			PWM00	O	MFP6	PWM00 counter synchronous trigger output pin.
			CFG.0_PwrOnSet0	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
		50	V_{SS}	P	MFP0	Ground pin for digital circuit.
		51	V_{SS}	P	MFP0	Ground pin for digital circuit.
	29	52	PB.0	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR12	O	MFP1	EBI address bus bit 12.
			UART2_CTS	I	MFP2	UART2 clear to Send input pin.
			ADC_AIN0	A	MFP8	ADC channel 0 analog input.
16	30	53	PB.6	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR13	O	MFP1	EBI address bus bit 13.
			I2C1_SDA	I/O	MFP2	I^2C1 data input/output pin.
			I2S_LRCK	O	MFP3	I^2S left right channel clock output pin.
			USBHL0_DM	A	MFP4	USB 1.1 host lite port-0 differential signal D-.
			UART7_TXD	O	MFP5	UART7 data transmitter output pin.
			SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			ADC_AIN6	A	MFP8	ADC channel 6 analog input.
17	31	54	PB.4	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR14	O	MFP1	EBI address bus bit 14.
			I2C1_SCL	I/O	MFP2	I^2C1 clock pin.
			I2S_BCLK	O	MFP3	I^2S bit clock output pin.
			USBHL0_DP	A	MFP4	USB 1.1 host lite port-0 differential signal D+.
			UART7_RXD	I	MFP5	UART7 data receiver input pin.
			SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
			ADC_AIN4	A	MFP8	ADC channel 4 analog input.
	32	55	AV_{SS}	P	MFP0	Ground pin for analog SAR-ADC.
18	33	56	AV_{DD33}	P	MFP0	Power supply for analog SAR-ADC, DC3.3V.
	34	57	PB.7	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR15	O	MFP1	EBI address bus bit 15.
			I2C2_SDA	I/O	MFP2	I^2C2 data input/output pin.
			I2S_DI	I	MFP3	I^2S data input pin.
			USBHL0_DM	A	MFP4	USB 1.1 host lite port-0 differential signal D-.
			UART7_CTS	I	MFP5	UART7 clear to Send input pin.
			SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
			ADC_AIN7	A	MFP8	ADC channel 7 analog input.
	35	58	PB.5	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR16	O	MFP1	EBI address bus bit 16.
			I2C2_SCL	I/O	MFP2	I^2C2 clock pin.
			I2S_DO	O	MFP3	I^2S data output pin.
			USBHL0_DP	A	MFP4	USB 1.1 host lite port-0 differential signal D+.
			UART7_RTS	O	MFP5	UART7 request to Send output pin.
			SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
			ADC_AIN5	A	MFP8	ADC channel 5 analog input.
	36	59	PB.1	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR17	O	MFP1	EBI address bus bit 17.
			I2C3_SDA	I/O	MFP2	I^2C3 data input/output pin.
			I2S_MCLK	O	MFP3	I^2S master clock output pin.
			CAN2_RXD	I	MFP4	CAN2 bus receiver input.
			TM0_EXT	I/O	MFP5	Timer0 external capture input/toggle output pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			SPI1_SS1	I/O	MFP6	SPI1 slave select 1 pin.
			UART9_TXD	O	MFP7	UART9 data transmitter output pin.
			ADC_AIN1	A	MFP8	ADC channel 1 analog input.
	37	60	PB.3	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR18	O	MFP1	EBI address bus bit 18.
			I2C3_SCL	I/O	MFP2	I^2C3 clock pin.
			EINT2	I	MFP3	External interrupt 2 input pin.
			CAN2_TXD	O	MFP4	CAN2 bus transmitter output.
			TM0_TGL	I/O	MFP5	Timer0 event counter input/toggle output pin.
			SPI0_SS1	I/O	MFP6	SPI0 slave select 1 pin.
			UART9_RXD	I	MFP7	UART9 data receiver input pin.
			ADC_AIN3	A	MFP8	ADC channel 3 analog input.
	38	61	PB.2	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR2	O	MFP1	EBI address bus bit 2.
			UART9_RTS	O	MFP7	UART9 request to Send output pin.
			ADC_AIN2	A	MFP8	ADC channel 2 analog input.
		62	AV_{ref}	A	MFP0	ADC reference voltage input.
		63	AV_{DD33}	P	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
	39	64	V_{BAT33}	P	MFP0	Power supply by batteries for RTC.
		65	NC	-		
		66	NC	-		
	40	67	X32_IN	I	MFP0	External 32.768 kHz crystal input pin.
	41	68	X32_OUT	O	MFP0	External 32.768 kHz crystal output pin.
		69	V_{SS}	P	MFP0	Ground pin for digital circuit
		70	V_{SS}	P	MFP0	Ground pin for digital circuit.
	42	71	PB.8	I/O	MFP0	General purpose digital I/O pin.
			EBI_ADDR11	O	MFP1	EBI address bus bit 11.
			I2C2_SCL	I/O	MFP2	I^2C2 clock pin.
			CAN2_RXD	I	MFP3	CAN2 bus receiver input.
			UART8_TXD	O	MFP4	UART8 data transmitter output pin.
			SD0_nCD	I	MFP6	SD0 card detect input pin
			TM0_EXT	I/O	MFP7	Timer0 external capture input/toggle output pin.
		72	V_{SS}	P	MFP0	Ground pin for digital circuit.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		73	V_{SS}	P	MFP0	Ground pin for digital circuit.
	43	74	V_{DD12}	P	MFP0	Power supply Internal core power pin.
	44	75	PC.0	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA0	I/O	MFP1	EBI data bus bit 0.
			I2C2_SDA	I/O	MFP2	I^2C2 data input/output pin.
			CAN2_TXD	O	MFP3	CAN2 bus transmitter output.
			UART8_RXD	I	MFP4	UART8 data receiver input pin.
			SPI0_SS1	I/O	MFP5	SPI0 slave select 1 pin.
			TM0_TGL	I/O	MFP7	Timer0 event counter input/toggle output pin.
	45	76	PC.1	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA1	I/O	MFP1	EBI data bus bit 1.
			NAND_nCS0	O	MFP3	NAND flash chip enable input.
			UART7_TXD	O	MFP4	UART7 data transmitter output pin.
	46	77	PC.2	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA2	I/O	MFP1	EBI data bus bit 2.
			NAND_nWP	O	MFP3	NAND flash write protect input.
			UART7_RXD	I	MFP4	UART7 data receiver input pin.
19	47	78	PC.3	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA3	I/O	MFP1	EBI data bus bit 3.
			VCAP0_CLKO	O	MFP2	Video image interface-0 sensor clock pin.
			NAND_ALE	O	MFP3	NAND flash address latch enable.
			I2C1_SCL	I/O	MFP4	I^2C1 clock pin.
			UART3_TXD	O	MFP5	UART3 data transmitter output pin.
			CAN0_RXD	I	MFP7	CAN0 bus receiver input.
20	48	79	PC.4	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA4	I/O	MFP1	EBI data bus bit 4.
			VCAP0_PCLK	I	MFP2	Video image interface-0 pixel clock pin.
			NAND_CLE	O	MFP3	NAND flash command latch enable.
			I2C1_SDA	I/O	MFP4	I^2C1 data input/output pin.
			UART3_RXD	I	MFP5	UART3 data receiver input pin.
			SPI0_MOSI	I/O	MFP6	SPI0 MOSI (Master Out, Slave In) pin.
			CAN0_TXD	O	MFP7	CAN0 bus transmitter output.
		80	V_{SS}	P	MFP0	Ground pin for digital circuit.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
21	49	81	PC.5	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA5	I/O	MFP1	EBI data bus bit 5.
			VCAP0_HSYNC	I	MFP2	Video image interface-0 horizontal sync. pin.
			NAND_nWE	O	MFP3	NAND flash write enable.
			SPI0_SS0	I/O	MFP5	SPI0 slave select 0 pin.
			SD0_CMD/ eMMC0_CMD	I/O	MFP6	SD0 command/response pin eMMC0 command/response pin
			UART1_TXD	O	MFP7	UART1 data transmitter output pin.
		82	V_{SS}	P	MFP0	Ground pin for digital circuit.
22	50	83	PC.6	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA6	I/O	MFP1	EBI data bus bit 6.
			VCAP0_VSYNC	I	MFP2	Video image interface-0 vertical sync. pin.
			NAND_nRE	O	MFP3	NAND flash read enable.
			SC1_RST	O	MFP4	Smart Card 1 reset pin.
			SPI0_CLK	I/O	MFP5	SPI0 serial clock pin.
			SD0_CLK/ eMMC0_CLK	O	MFP6	SD0 clock output pin eMMC0 clock output pin
			UART1_RXD	I	MFP7	UART1 data receiver input pin.
	51	84	PC.7	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA7	I/O	MFP1	EBI data bus bit 7.
			VCAP0_FIELD	I	MFP2	Video image interface-0 frame sync. pin
			NAND_RDY0	I	MFP3	NAND flash ready/busy input.
			SC1_CLK	O	MFP4	Smart Card 1 clock pin.
			SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
			SD0_DATA0/ eMMC0_DATA0	I/O	MFP6	SD0 data line bit 0. eMMC0 data line bit 0.
			UART1_RTS	O	MFP7	UART1 request to Send output pin.
23	52	85	PC.8	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA8	I/O	MFP1	EBI data bus bit 8.
			VCAP0_DATA0	I	MFP2	Video image interface-0 data 0 pin.
			NAND_DATA0	I/O	MFP3	NAND flash data bus bit 0.
			SC1_DAT	I/O	MFP4	Smart Card 1 data pin.
			SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			SD0_DATA1/ eMMC0_DATA1	I/O	MFP6	SD0 data line bit 1. eMMC0 data line bit 1.
			UART1_CTS	I	MFP7	UART1 clear to Send input pin.
		86	V_{SS}	P	MFP0	Ground pin for digital circuit.
24	53	87	PC.9	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA9	I/O	MFP1	EBI data bus bit 9.
			VCAP0_DATA1	I	MFP2	Video image interface 0 data 1 pin.
			NAND_DATA1	I/O	MFP3	NAND flash data bus bit 1.
			SC1_PWR	O	MFP4	Smart Card 1 power pin.
			SD0_DATA2/ eMMC0_DATA2	I/O	MFP6	SD0 data line bit 2. eMMC0 data line bit 2.
			UART4_TXD	O	MFP7	UART4 data transmitter output pin.
		88	V_{SS}	P	MFP0	Ground pin for digital circuit.
25	54	89	PC.10	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA10	I/O	MFP1	EBI data bus bit 10.
			VCAP0_DATA2	I	MFP2	Video image interface 0 data 2 pin.
			NAND_DATA2	I/O	MFP3	NAND flash data bus bit 2.
			SC1_CD	I	MFP4	Smart Card 1 card detect pin.
			SD0_DATA3/ eMMC0_DATA3	I/O	MFP6	SD0 data line bit 3. eMMC0 data line bit 3.
			UART4_RXD	I	MFP7	UART4 data receiver input pin.
26	55	90	PC.11	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA11	I/O	MFP1	EBI data bus bit 11.
			VCAP0_DATA3	I	MFP2	Video image interface-0 data 3 pin.
			NAND_DATA3	I/O	MFP3	NAND flash data bus bit 3
			SC0_RST	O	MFP4	Smart Card 0 reset pin.
27	56	91	PC.12	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA12	I/O	MFP1	EBI data bus bit 12.
			VCAP0_DATA4	I	MFP2	Video image interface-0 data 4 pin.
			NAND_DATA4	I/O	MFP3	NAND flash data bus bit 4.
			SC0_CLK	O	MFP4	Smart Card 0 clock pin.
			SD0_nCD	I	MFP6	SD0 card detect input pin
			UART8_TXD	O	MFP7	UART8 data transmitter output pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
28	57	92	PC.13	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA13	I/O	MFP1	EBI data bus bit 13.
			VCAP0_DATA5	I	MFP2	Video image interface-0 data 5 pin.
			NAND_DATA5	I/O	MFP3	NAND flash data bus bit 5.
			SC0_DAT	I/O	MFP4	Smart Card 0 data pin.
			UART8_RXD	I	MFP7	UART8 data receiver input pin.
29	58	93	PC.14	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA14	I/O	MFP1	EBI data bus bit 14.
			VCAP0_DATA6	I	MFP2	Video image interface-0 data 6 pin.
			NAND_DATA6	I/O	MFP3	NAND flash data bus bit 6.
			SC0_PWR	O	MFP4	Smart Card 0 power pin.
			SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
			UART8_RTS	O	MFP7	UART8 request to Send output pin.
30	59	94	PC.15	I/O	MFP0	General purpose digital I/O pin.
			EBI_DATA15	I/O	MFP1	EBI data bus bit 15.
			VCAP0_DATA7	I	MFP2	Video image interface-0 data 7 pin.
			NAND_DATA7	I/O	MFP3	NAND flash date bus bit 7.
			SC0_CD	I	MFP4	Smart Card 0 card detect pin.
			UART8_CTS	I	MFP7	UART8 clear to Send input pin.
31		95	V_{DD12}	P	MFP0	Power supply for Internal core power pin.
		96	V_{SS}	P	MFP0	Ground pin for digital circuit.
		97	V_{SS}	P	MFP0	Ground pin for digital circuit.
		98	NC	-		
32	60	99	V_{DD33}	P	MFP0	Power supply for I/O power pin.
		100	NC	-		
		101	NC	-		
		102	NC	-		
		103	NC	-		
		104	V_{SS}	P	MFP0	Ground pin for digital circuit.
		105	NC	-		
		106	NC	-		
		107	NC	-		
		108	NC	-		

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		109	NC	-		
		110	V_{SS}	P	MFP0	Ground pin for digital circuit.
		111	PD.0	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin.
			UART5_TXD	O	MFP2	UART5 data transmitter output pin.
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
			EINT2	I	MFP4	External interrupt 2 input pin.
		112	PD.1	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin.
			UART5_RXD	I	MFP2	UART5 data receiver input pin.
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			EINT3	I	MFP4	External interrupt 3 input pin.
		113	PB.9	I/O	MFP0	General purpose digital I/O pin.
			UART3_TXD	O	MFP1	UART3 data transmitter output pin.
			PWM13	O	MFP2	PWM13 counter synchronous trigger output pin.
			TM0_TGL	I/O	MFP3	Timer0 event counter input/toggle output pin.
			USBHL0_DM	A	MFP4	USB 1.1 host lite port-0 differential signal D-.
			SPI1_SS0	I/O	MFP5	SPI1 slave select 0 pin.
		114	PB.10	I/O	MFP0	General purpose digital I/O pin.
			UART3_RXD	I	MFP1	UART3 data receiver input pin.
			PWM12	O	MFP2	PWM12 counter synchronous trigger output pin.
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
			USBHL0_DP	A	MFP4	USB 1.1 host lite port-0 differential signal D+.
			SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
		115	PB.11	I/O	MFP0	General purpose digital I/O pin.
			UART3_RTS	O	MFP1	UART3 request to Send output pin.
			PWM11	O	MFP2	PWM11 counter synchronous trigger output pin.
			TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin.
			USBHL5_DM	A	MFP4	USB 1.1 host lite port-0 differential signal D-.
			SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
		116	PB.12	I/O	MFP0	General purpose digital I/O pin.
			UART3_CTS	I	MFP1	UART3 clear to Send input pin.
			PWM10	O	MFP2	PWM10 counter synchronous trigger output pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin.
			USBHL5_DP	A	MFP4	USB 1.1 host lite port-5 differential signal D+.
			SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
33	61	117	PD.2	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_SS0	I/O	MFP1	Quad SPI0 slave select 0 pin.(booting)
			UART3_TXD	O	MFP2	UART3 data transmitter output pin.
			TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
34	62	118	PD.3	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_CLK	I/O	MFP1	Quad SPI0 serial clock pin.(booting)
			UART3_RXD	I	MFP2	UART3 data receiver input pin.
			TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin.
35	63	119	PD.4	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_MOSI0	I/O	MFP1	Quad SPI0 MOSI0 (Master Out, Slave In) pin. Data 0 of quad mode.(booting)
			UART3_RTS	O	MFP2	UART3 request to Send output pin.
			TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin.
	64		V_{SS}	P	MFP0	Ground pin for digital circuit.
36	65	120	PD.5	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_MISO0	I/O	MFP1	Quad SPI0 MISO0 (Master In, Slave Out) pin. Data 1 of quad mode.(booting)
			UART3_CTS	I	MFP2	UART3 clear to Send input pin.
			TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin.
	66	121	PD.6	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_MOSI1	I/O	MFP1	Quad SPI0 MOSI1 (Master Out, Slave In) pin. Data 2 of quad mode.(booting)
			UART2_TXD	O	MFP2	UART2 data transmitter output pin.
			TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin.
			CAN0_RXD	I	MFP4	CAN0 bus receiver input.
	67	122	PD.7	I/O	MFP0	General purpose digital I/O pin.
			QSPI0_MISO1	I/O	MFP1	Quad SPI0 MISO1 (Master In, Slave Out) pin. Data 3 of quad mode.(booting)
			UART2_RXD	I	MFP2	UART2 data receiver input pin.
			TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin.
			CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
	68	123	PD.8	I/O	MFP0	General purpose digital I/O pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			SPI0_SS0	I/O	MFP1	SPI0 slave select 0 pin.
			UART6_CTS	I	MFP2	UART6 clear to Send input pin.
			TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin.
	69	124	PD.9	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
			UART6_RTS	O	MFP2	UART6 request to Send output pin.
			TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin.
	70	125	PD.10	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI	I/O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
			UART6_TXD	O	MFP2	UART6 data transmitter output pin.
			TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin.
	71	126	PD.11	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO	I/O	MFP1	SPI0 MISO (Master In, Slave Out) pin.
			UART6_RXD	I	MFP2	UART6 data receiver input pin.
			TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin.
	72	127	PD.12	I/O	MFP0	General purpose digital I/O pin.
			UART4_TXD	O	MFP1	UART4 data transmitter output pin.
			TM2_TGL	I/O	MFP2	Timer2 event counter input/toggle output pin.
			CAN2_RXD	I	MFP4	CAN2 bus receiver input.
			PWM00	O	MFP6	PWM00 counter synchronous trigger output pin.
			EBI_DATA1	I/O	MFP8	EBI data bus bit 1.
		128	V_{SS}	P	MFP0	Ground pin for digital circuit.
	73	129	PD.13	I/O	MFP0	General purpose digital I/O pin.
			UART4_RXD	I	MFP1	UART4 data receiver input pin.
			TM2_EXT	I/O	MFP2	Timer2 external capture input/toggle output pin.
			CAN2_TXD	O	MFP4	CAN2 bus transmitter output.
			PWM01	O	MFP6	PWM01 counter synchronous trigger output pin.
			EBI_DATA2	I/O	MFP8	EBI data bus bit 2.
	74	130	PD.14	I/O	MFP0	General purpose digital I/O pin.
			UART4_RTS	O	MFP1	UART4 request to Send output pin.
			TM3_TGL	I/O	MFP2	Timer3 event counter input/toggle output pin.
			I2C3_SCL	I/O	MFP3	I^2C3 clock pin.
			CAN1_RXD	I	MFP4	CAN1 bus receiver input.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			USBHL0_DM	A	MFP5	USB 1.1 host lite port-0 differential signal D-.
			PWM02	O	MFP6	PWM02 counter synchronous trigger output pin.
			EBI_DATA3	I/O	MFP8	EBI data bus bit 3.
	75	131	PD.15	I/O	MFP0	General purpose digital I/O pin.
			UART4_CTS	I	MFP1	UART4 clear to Send input pin.
			TM3_EXT	I/O	MFP2	Timer3 external capture input/toggle output pin.
			I2C3_SDA	I/O	MFP3	I^2C3 data input/output pin.
			CAN1_TXD	O	MFP4	CAN1 bus transmitter output.
			USBHL0_DP	A	MFP5	USB 1.1 host lite port-0 differential signal D+.
			PWM03	O	MFP6	PWM03 counter synchronous trigger output pin.
			EBI_DATA4	I/O	MFP8	EBI data bus bit 4.
	76	132	PG.11	I/O	MFP0	General purpose digital I/O pin.
			SPI1_SS0	I/O	MFP2	SPI1 slave select 0 pin.
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
			CAN0_RXD	I	MFP4	CAN0 bus receiver input.
			UART5_CTS	I	MFP5	UART5 clear to Send input pin.
			PWM10	O	MFP6	PWM10 counter synchronous trigger output pin.
			JTAG0_TDO	O	MFP7	JTAG0 data output pin.
	77	133	PG.12	I/O	MFP0	General purpose digital I/O pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
			UART5_RTS	O	MFP5	UART5 request to Send output pin.
			PWM11	O	MFP6	PWM11 counter synchronous trigger output pin.
			JTAG0_TCK	I	MFP7	JTAG0 clock input pin.
	78	134	PG.13	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			CAN1_RXD	I	MFP4	CAN1 bus receiver input.
			UART5_RXD	I	MFP5	UART5 data receiver input pin.
			PWM12	O	MFP6	PWM12 counter synchronous trigger output pin.
			JTAG0_TMS	I	MFP7	JTAG0 test mode selection input pin.
	79	135	PG.14	I/O	MFP0	General purpose digital I/O pin.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			CAN1_TXD	O	MFP4	CAN1 bus transmitter output.
			UART5_TXD	O	MFP5	UART5 data transmitter output pin.
			PWM13	O	MFP6	PWM13 counter synchronous trigger output pin.
			JTAG0_TDI	I	MFP7	JTAG0 data input pin.
	80	136	PG.15	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin.
			SPI1_SS1	I/O	MFP2	SPI1 slave select 1 pin.
			EINT3	I	MFP4	External interrupt 3 input pin.
			JTAG0_nTRST	I	MFP7	JTAG0 reset input pin.
37	81	137	nRESET	IU	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
			WDT_nRST	O	MFP1	Watch dog timer reset trigger output.
		138	V_{DD33}	P	MFP0	Power supply for I/O power pin.
		139	V_{SS}	P	MFP0	Ground pin for digital circuit.
		140	V_{SS}	P	MFP0	Ground pin for digital circuit.
38	82	141	V_{DD12}	P	MFP0	Power supply for internal core power pin.
39	83	142	MV_{DD}	P	MFP0	Power supply for Memory ports.
		143	V_{SS}	P	MFP0	Ground pin for digital circuit.
		144	MV_{DD}	P	MFP0	Power supply for Memory ports.
		145	V_{SS}	P	MFP0	Ground pin for digital circuit.
	84	146	MV_{DD}	P	MFP0	Power supply for Memory ports.
		147	V_{SS}	P	MFP0	Ground pin for digital circuit.
		148	MV_{DD}	P	MFP0	Power supply for Memory ports.
		149	V_{SS}	P	MFP0	Ground pin for digital circuit.
		150	V_{SS}	P	MFP0	Ground pin for digital circuit.
		151	V_{SS}	P	MFP0	Ground pin for digital circuit.
40	85	152	V_{DD33}	P	MFP0	Power supply for I/O power pin.
41	86	153	PF.0	I/O	MFP0	General purpose digital I/O pin.
			RMII1_RXERR	I	MFP1	RMII1 Receive Data Error input pin.
			SD1_CMD/ eMMC1_CMD	I/O	MFP2	SD1 command/response pin eMMC1 command/response pin
			TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin.
			SC1_RST	O	MFP4	Smart Card 1 reset pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART7_CTS	I	MFP5	UART7 clear to Send input pin.
			USBHL1_DM	A	MFP6	USB 1.1 host lite port-1 differential signal D-.
			EBI_DATA5	I/O	MFP8	EBI data bus bit 5.
42	87	154	PF.1	I/O	MFP0	General purpose digital I/O pin.
			RMII1_CRSDV	I	MFP1	RMII1 Carrier Sense/Receive Data input pin.
			SD1_CLK/ eMMC1_CLK	O	MFP2	SD1 clock output pin eMMC1 clock output pin
			TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin.
			SC1_CLK	O	MFP4	Smart Card 1 clock pin.
			UART7_RTS	O	MFP5	UART7 request to Send output pin.
			USBHL1_DP	A	MFP6	USB 1.1 host lite port-1 differential signal D+.
			EBI_DATA6	I/O	MFP8	EBI data bus bit 6.
43	88	155	PF.2	I/O	MFP0	General purpose digital I/O pin.
			RMII1_RXD1	I	MFP1	RMII1 Receive Data bus bit 1.
			SD1_DATA0/ eMMC1_DATA0	I/O	MFP2	SD1 data line bit 0. eMMC1 data line bit 0.
			TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin.
			SC1_DAT	I/O	MFP4	Smart Card 1 data pin.
			UART7_RXD	I	MFP5	UART7 data receiver input pin.
			USBHL2_DM	A	MFP6	USB 1.1 host lite port-2 differential signal D-.
			EBI_DATA7	I/O	MFP8	EBI data bus bit 7.
44	89	156	PF.3	I/O	MFP0	General purpose digital I/O pin.
			RMII1_RXD0	I	MFP1	RMII1 Receive Data bus bit 0.
			SD1_DATA1/ eMMC1_DATA1	I/O	MFP2	SD1 data line bit 1. eMMC1 data line bit 1.
			TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin.
			SC1_PWR	O	MFP4	Smart Card 1 power pin.
			UART7_TXD	O	MFP5	UART7 data transmitter output pin.
			USBHL2_DP	A	MFP6	USB 1.1 host lite port-2 differential signal D+.
			EBI_DATA8	I/O	MFP8	EBI data bus bit 8.
45	90	157	PF.4	I/O	MFP0	General purpose digital I/O pin.
			RMII1_REFCLK	I	MFP1	RMII1 mode clock input pin.
			SD1_DATA2/ eMMC1_DATA2	I/O	MFP2	SD1 data line bit 2.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
						eMMC1 data line bit 2.
			TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin.
			SC1_CD	I	MFP4	Smart Card 1 card detect pin.
			UART3_CTS	I	MFP5	UART3 clear to Send input pin.
			USBHL3_DM	A	MFP6	USB 1.1 host lite port-3 differential signal D-.
			EBI_DATA9	I/O	MFP8	EBI data bus bit 9.
46	91	158	PF.5	I/O	MFP0	General purpose digital I/O pin.
			RMII1_TXEN	O	MFP1	RMII1 Transmit Enable output pin.
			SD1_DATA3/ eMMC1_DATA3	I/O	MFP2	SD1 data line bit 3. eMMC1 data line bit 3.
			TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin.
			PWM00	O	MFP4	PWM00 counter synchronous trigger output pin.
			UART3_RTS	O	MFP5	UART3 request to Send output pin.
			USBHL3_DP	A	MFP6	USB 1.1 host lite port-3 differential signal D+.
			EBI_DATA10	I/O	MFP8	EBI data bus bit 10.
47	92	159	PF.6	I/O	MFP0	General purpose digital I/O pin.
			RMII1_TXD1	O	MFP1	RMII1 Transmit Data bus bit 1.
			SD1_nCD	I	MFP2	SD1 card detect input pin
			TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
			PWM01	O	MFP4	PWM01 counter synchronous trigger output pin.
			UART3_RXD	I	MFP5	UART3 data receiver input pin.
			USBHL4_DM	A	MFP6	USB 1.1 host lite port-4 differential signal D-.
			EBI_DATA11	I/O	MFP8	EBI data bus bit 11.
	93	160	PB.13	I/O	MFP0	General purpose digital I/O pin.
			EINT2	I	MFP2	External interrupt 2 input pin.
			TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin.
			PWM02	O	MFP4	PWM02 counter synchronous trigger output pin.
			UART3_TXD	O	MFP5	UART3 data transmitter output pin.
			USBHL4_DP	A	MFP6	USB 1.1 host lite port-4 differential signal D+.
			EBI_DATA0	I/O	MFP8	EBI data bus bit 0.
48	94	161	V_{DD12}	P	MFP0	Power supply for internal core power pin.
		162	V_{DD12}	P	MFP0	Power supply for internal core power pin
		163	V_{SS}	P	MFP0	Ground pin for digital circuit.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
	95	164	V_{SS}	P	MFP0	Ground pin for digital circuit.
49	96	165	PF.7	I/O	MFP0	General purpose digital I/O pin.
			RMII1_TXD0	O	MFP1	RMII1 Transmit Data bus bit 0.
			UART1_CTS	I	MFP2	UART1 clear to Send input pin.
			TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin.
			PWM02	O	MFP4	PWM02 counter synchronous trigger output pin.
			UART3_TXD	O	MFP5	UART3 data transmitter output pin.
			USBHL4_DP	A	MFP6	USB 1.1 host lite port-4 differential signal D+.
			EBI_DATA12	I/O	MFP8	EBI data bus bit 12.
50	97	166	PF.8	I/O	MFP0	General purpose digital I/O pin.
			RMII1_MDIO	I/O	MFP1	RMII1 PHY Management Data pin.
			UART1_RTS	O	MFP2	UART1 request to Send output pin.
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
			PWM03	O	MFP4	PWM03 counter synchronous trigger output pin.
			USBHL5_DM	A	MFP6	USB 1.1 host lite port-5 differential signal D-.
			EBI_DATA13	I/O	MFP8	EBI data bus bit 13.
51	98	167	PF.9	I/O	MFP0	General purpose digital I/O pin.
			RMII1_MDC	O	MFP1	RMII1 PHY Management Clock output pin.
			UART1_RXD	I	MFP2	UART1 data receiver input pin.
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
			PWM10	O	MFP4	PWM10 counter synchronous trigger output pin.
			USBHL5_DP	A	MFP6	USB 1.1 host lite port-5 differential signal D+.
			EBI_DATA14	I/O	MFP8	EBI data bus bit 14.
		168	V_{DD12}	P	MFP0	Power supply for internal core power pin.
	99	169	PF.10	I/O	MFP0	General purpose digital I/O pin.
			UART1_TXD	O	MFP2	UART1 data transmitter output pin.
			TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin.
			PWM11	O	MFP4	PWM11 counter synchronous trigger output pin.
			VCAP1_PCLK	I	MFP7	Video image interface-1 pixel clock pin.
			EBI_DATA15	I/O	MFP8	EBI data bus bit 15.
52	100	170	PF.11	I/O	MFP0	General purpose digital I/O pin.
			UART0_RXD	I	MFP1	UART0 data receiver input pin.
		171	V_{SS}	P	MFP0	Ground pin for digital circuit.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
53	101	172	PF.12	I/O	MFP0	General purpose digital I/O pin.
			UART0_TXD	O	MFP1	UART0 data transmitter output pin.
54	102	173	V_{DD33}	P	MFP0	Power supply for I/O power pin.
55	103	174	XT_IN	I	MFP0	External 12 MHz crystal input pin.
56	104	175	XT_OUT	O	MFP0	External 12 MHz crystal output pin.
		176	V_{SS}	P	MFP0	Ground pin for digital circuit.
	105	177	PE.0	I/O	MFP0	General purpose digital I/O pin.
			RMII0_RXERR	I	MFP1	RMII0 Receive Data Error input pin.
			CAN0_RXD	I	MFP2	CAN0 bus receiver input.
			UART4_CTS	I	MFP5	UART4 clear to Send input pin.
			USBHL1_DM	A	MFP6	USB 1.1 host lite port-1 differential signal D-.
			VCAP1_HSYNC	I	MFP7	Video image interface-1 horizontal sync. pin.
	106	178	PE.1	I/O	MFP0	General purpose digital I/O pin.
			RMII0_CRSDV	I	MFP1	RMII0 Carrier Sense/Receive Data input pin.
			CAN0_TXD	O	MFP2	CAN0 bus transmitter output.
			UART4_RTS	O	MFP5	UART4 request to Send output pin.
			USBHL1_DP	A	MFP6	USB 1.1 host lite port-1 differential signal D+.
			VCAP1_VSYNC	I	MFP7	Video image interface-1 vertical sync. pin.
	107	179	PE.2	I/O	MFP0	General purpose digital I/O pin.
			RMII0_RXD1	I	MFP1	RMII0 Receive Data bus bit 1.
			CAN1_RXD	I	MFP2	CAN1 bus receiver input.
			UART4_RXD	I	MFP5	UART4 data receiver input pin.
			USBHL2_DM	A	MFP6	USB 1.1 host lite port-2 differential signal D-.
			VCAP1_DATA0	I	MFP7	Video image interface-1 data 0 pin.
		180	V_{DD12}	P	MFP0	Power supply for internal core power pin.
	108	181	PE.3	I/O	MFP0	General purpose digital I/O pin.
			RMII0_RXD0	I	MFP1	RMII0 Receive Data bus bit 0.
			CAN1_TXD	O	MFP2	CAN1 bus transmitter output.
			UART4_TXD	O	MFP5	UART4 data transmitter output pin.
			USBHL2_DP	A	MFP6	USB 1.1 host lite port-2 differential signal D+.
			VCAP1_DATA1	I	MFP7	Video image interface-1 data 1 pin.
	109	182	PE.4	I/O	MFP0	General purpose digital I/O pin.
			RMII0_REFCLK	I	MFP1	RMII0 mode clock input pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			CAN2_RXD	I	MFP2	CAN2 bus receiver input.
			UART9_CTS	I	MFP5	UART9 clear to Send input pin.
			USBHL3_DM	A	MFP6	USB 1.1 host lite port-3 differential signal D-.
			VCAP1_DATA2	I	MFP7	Video image interface-1 data 2 pin.
	110	183	PE.5	I/O	MFP0	General purpose digital I/O pin.
			RMII0_TXEN	O	MFP1	RMII0 Transmit Enable output pin.
			CAN2_TXD	O	MFP2	CAN2 bus transmitter output.
			UART9_RTS	O	MFP5	UART9 request to Send output pin.
			USBHL3_DP	A	MFP6	USB 1.1 host lite port-3 differential signal D+.
			VCAP1_DATA3	I	MFP7	Video image interface-1 data 3 pin.
	111	184	PE.6	I/O	MFP0	General purpose digital I/O pin.
			RMII0_TXD1	O	MFP1	RMII0 Transmit Data bus bit 1.
			CAN3_RXD	I	MFP2	CAN3 bus receiver input.
			UART9_RXD	I	MFP5	UART9 data receiver input pin.
			USBHL4_DM	A	MFP6	USB 1.1 host lite port-4 differential signal D-.
			VCAP1_DATA4	I	MFP7	Video image interface-1 data 4 pin.
	112	185	PE.7	I/O	MFP0	General purpose digital I/O pin.
			RMII0_TXD0	O	MFP1	RMII0 Transmit Data bus bit 0.
			CAN3_TXD	O	MFP2	CAN3 bus transmitter output.
			UART9_TXD	O	MFP5	UART9 data transmitter output pin.
			USBHL4_DP	A	MFP6	USB 1.1 host lite port-4 differential signal D+.
			VCAP1_DATA5	I	MFP7	Video image interface-1 data 5 pin.
		186	V_{DD33}	P	MFP0	Power supply for I/O power pin.
	113	187	PE.8	I/O	MFP0	General purpose digital I/O pin.
			RMII0_MDIO	I/O	MFP1	RMII0 PHY Management Data pin.
			UART6_RXD	I	MFP5	UART6 data receiver input pin.
			USBHL5_DM	A	MFP6	USB 1.1 host lite port-5 differential signal D-.
			VCAP1_DATA6	I	MFP7	Video image interface-1 data 6 pin.
	114	188	PE.9	I/O	MFP0	General purpose digital I/O pin.
			RMII0_MDC	O	MFP1	RMII0 PHY Management Clock output pin.
			UART6_TXD	O	MFP5	UART6 data transmitter output pin.
			USBHL5_DP	A	MFP6	USB 1.1 host lite port-5 differential signal D+.
			VCAP1_DATA7	I	MFP7	Video image interface-1 data 7 pin.

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
	115	189	PE.10	I/O	MFP0	General purpose digital I/O pin.
			USB_OVC	I	MFP1	HSUSB host bus power over voltage detector.
			CAN3_RXD	I	MFP2	CAN3 bus receiver input.
			UART9_RXD	I	MFP3	UART9 data receiver input pin.
			PWM12	O	MFP4	PWM12 counter synchronous trigger output pin.
			EINT2	I	MFP5	External interrupt 2 input pin.
			I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin.
			VCAP1_FIELD	I	MFP7	Video image interface-1 frame sync. pin.
57	116	190	PE.11	I/O	MFP0	General purpose digital I/O pin.
			USB0_VBUSVLD	I	MFP1	USB0 VBUS vaild indication pin.
	117	191	PE.12	I/O	MFP0	General purpose digital I/O pin.
			USBH_PWREN	O	MFP1	HSUSB host power control pin.
			CAN3_TXD	O	MFP2	CAN3 bus transmitter output.
			UART9_TXD	O	MFP3	UART9 data transmitter output pin.
			PWM13	O	MFP4	PWM13 counter synchronous trigger output pin.
			EINT3	I	MFP5	External interrupt 3 input pin.
			I2C0_SCL	I/O	MFP6	I^2C0 clock pin.
			VCAP1_CLKO	O	MFP7	Video image interface sensor-1 clock pin.
		192	V_{SS}	P	MFP0	Ground pin for digital circuit.
58	118	193	V_{DD12}	P	MFP0	Power supply for internal core power pin.
		194	V_{SS}	P	MFP0	Ground pin for digital circuit.
		195	V_{USB1_VDD12}	P	MFP0	Power supply for USB1 VDD12
		196	V_{USB1_VDD12}	P	MFP0	Power supply for USB1 VDD12
		197	V_{USB1_VSS}	P	MFP0	Ground pin for USB1.
		198	NC			
		199	NC			
		200	V_{USB1_VSS}	P	MFP0	Ground pin for USB1.
	119	201	USB1_DM	A	MFP0	USB1 differential signal D-.
	120	202	USB1_DP	A	MFP0	USB1 differential signal D+.
59	121	203	V_{USB1_VDD33}	P	MFP0	Power supply for USB1 VDD33
		204	V_{USB1_VDD33}	P	MFP0	Power supply for USB1 VDD33
	122	205	USB1_REXT	A	MFP0	USB1 module reference resister (external 12.1K to GND)
60	123	206	V_{USB0_VDD12}	P	MFP0	Power supply for USB0 VDD12

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		207	V_{USB0_VDD12}	P	MFP0	Power supply for USB0 VDD12
		208	V_{USB0_VSS}	P	MFP0	Ground pin for USB0.
		209	NC			
		210	NC			
		211	V_{USB0_VSS}	P	MFP0	Ground pin for USB0.
61	124	212	USB0_DM	A	MFP0	USB0 differential signal D-.
62	125	213	USB0_DP	A	MFP0	USB0 differential signal D+.
63	126	214	V_{USB0_VDD33}	P	MFP0	Power supply for USB0 VDD33
		215	V_{USB0_VDD33}	P	MFP0	Power supply for USB0 VDD33
64	127	216	USB0_REXT	A	MFP0	USB0 module reference resister (external 12.1K to GND)
EPAD	128		V_{SS}	P	MFP0	Ground pin for digital circuit.

Note: Pin Type: I = Digital Input, IU= Digital Input with internal pull high; O = Digital Output; AI = Analog Input; AO = Analog Output; P = Power Pin; AP = Analog Power.

4.2.2 NUC980 Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ADC	ADC_AIN0	PB.0	MFP8	A	ADC channel 0 analog input.
	ADC_AIN1	PB.1	MFP8	A	ADC channel 1 analog input.
	ADC_AIN2	PB.2	MFP8	A	ADC channel 2 analog input.
	ADC_AIN3	PB.3	MFP8	A	ADC channel 3 analog input.
	ADC_AIN4	PB.4	MFP8	A	ADC channel 4 analog input.
	ADC_AIN5	PB.5	MFP8	A	ADC channel 5 analog input.
	ADC_AIN6	PB.6	MFP8	A	ADC channel 6 analog input.
	ADC_AIN7	PB.7	MFP8	A	ADC channel 7 analog input.
CAN0	CAN0_RXD	PC.3	MFP7	I	CAN0 bus receiver input.
		PD.6	MFP4	I	
		PG.11	MFP4	I	
		PE.0	MFP2	I	
	CAN0_TXD	PC.4	MFP7	O	CAN0 bus transmitter output.
		PD.7	MFP4	O	
		PG.12	MFP4	O	
		PE.1	MFP2	O	
CAN1	CAN1_RXD	PA.13	MFP5	I	CAN1 bus receiver input.
		PD.14	MFP4	I	
		PG.13	MFP4	I	
		PE.2	MFP2	I	
	CAN1_TXD	PA.14	MFP5	O	CAN1 bus transmitter output.
		PD.15	MFP4	O	
		PG.14	MFP4	O	
		PE.3	MFP2	O	
CAN2	CAN2_RXD	PA.15	MFP5	I	CAN2 bus receiver input.
		PB.1	MFP4	I	
		PB.8	MFP3	I	
		PD.12	MFP4	I	
		PE.4	MFP2	I	
	CAN2_TXD	PG.10	MFP5	O	CAN2 bus transmitter output.
		PB.3	MFP4	O	
		PC.0	MFP3	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.13	MFP4	O	
		PE.5	MFP2	O	
CAN3	CAN3_RXD	PA.0	MFP7	I	CAN3 bus receiver input.
		PE.6	MFP2	I	
		PE.10	MFP2	I	
	CAN3_TXD	PA.1	MFP7	O	CAN3 bus transmitter output.
		PE.7	MFP2	O	
		PE.12	MFP2	O	
CFG.0	CFG.0_PwrOnSet0	PG.0	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.1	CFG.1_PwrOnSet1	PG.1	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.2	CFG.2_PwrOnSet2	PG.2	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.3	CFG.3_PwrOnSet3	PG.3	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.4	CFG.4_PwrOnSet4	PG.4	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.5	CFG.5_PwrOnSet5	PG.5	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.6	CFG.6_PwrOnSet6	PG.6	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.7	CFG.7_PwrOnSet7	PG.7	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.8	CFG.8_PwrOnSet8	PG.8	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.9	CFG.9_PwrOnSet9	PG.9	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CLK	CLK_OUT	PG.0	MFP3	O	Internal clock selection output pin.
EBI	EBI_ADDR0	PG.0	MFP1	O	EBI address bus bit 0.
	EBI_ADDR1	PG.1	MFP1	O	EBI address bus bit 1.
	EBI_ADDR2	PG.2	MFP1	O	EBI address bus bit 2.
		PB.2	MFP1	O	
	EBI_ADDR3	PG.3	MFP1	O	EBI address bus bit 3.

Group	Pin Name	GPIO	MFP	Type	Description
	EBI_ADDR4	PG.6	MFP1	O	EBI address bus bit 4.
	EBI_ADDR5	PG.7	MFP1	O	EBI address bus bit 5.
	EBI_ADDR6	PG.8	MFP1	O	EBI address bus bit 6.
	EBI_ADDR7	PG.9	MFP1	O	EBI address bus bit 7.
	EBI_ADDR8	PA.12	MFP1	O	EBI address bus bit 8.
	EBI_ADDR9	PA.11	MFP1	O	EBI address bus bit 9.
	EBI_ADDR10	PA.10	MFP1	O	EBI address bus bit 10.
	EBI_ADDR11	PB.8	MFP1	O	EBI address bus bit 11.
	EBI_ADDR12	PG.5	MFP1	O	EBI address bus bit 12.
		PB.0	MFP1	O	
	EBI_ADDR13	PA.13	MFP1	O	EBI address bus bit 13.
		PB.6	MFP1	O	
	EBI_ADDR14	PA.14	MFP1	O	EBI address bus bit 14.
		PB.4	MFP1	O	
	EBI_ADDR15	PB.7	MFP1	O	EBI address bus bit 15.
	EBI_ADDR16	PB.5	MFP1	O	EBI address bus bit 16.
	EBI_ADDR17	PB.1	MFP1	O	EBI address bus bit 17.
	EBI_ADDR18	PG.4	MFP1	O	EBI address bus bit 18.
		PB.3	MFP1	O	
	EBI_ADDR19	PA.15	MFP1	O	EBI address bus bit 19.
	EBI_DATA0	PG.10	MFP1	I/O	EBI data bus bit 0.
		PC.0	MFP1	I/O	
		PB.13	MFP8	I/O	
	EBI_DATA1	PC.1	MFP1	I/O	EBI data bus bit 1.
		PD.12	MFP8	I/O	
	EBI_DATA2	PC.2	MFP1	I/O	EBI data bus bit 2.
		PD.13	MFP8	I/O	
	EBI_DATA3	PC.3	MFP1	I/O	EBI data bus bit 3.
		PD.14	MFP8	I/O	
	EBI_DATA4	PC.4	MFP1	I/O	EBI data bus bit 4.
		PD.15	MFP8	I/O	
	EBI_DATA5	PC.5	MFP1	I/O	EBI data bus bit 5.
		PF.0	MFP8	I/O	
	EBI_DATA6	PC.6	MFP1	I/O	EBI data bus bit 6.

Group	Pin Name	GPIO	MFP	Type	Description
		PF.1	MFP8	I/O	
	EBI_DATA7	PC.7	MFP1	I/O	EBI data bus bit 7.
		PF.2	MFP8	I/O	
	EBI_DATA8	PC.8	MFP1	I/O	EBI data bus bit 8.
		PF.3	MFP8	I/O	
	EBI_DATA9	PC.9	MFP1	I/O	EBI data bus bit 9.
		PF.4	MFP8	I/O	
	EBI_DATA10	PC.10	MFP1	I/O	EBI data bus bit 10.
		PF.5	MFP8	I/O	
	EBI_DATA11	PC.11	MFP1	I/O	EBI data bus bit 11.
		PF.6	MFP8	I/O	
	EBI_DATA12	PC.12	MFP1	I/O	EBI data bus bit 12.
		PF.7	MFP8	I/O	
	EBI_DATA13	PC.13	MFP1	I/O	EBI data bus bit 13.
		PF.8	MFP8	I/O	
	EBI_DATA14	PC.14	MFP1	I/O	EBI data bus bit 14.
		PF.9	MFP8	I/O	
	EBI_DATA15	PC.15	MFP1	I/O	EBI data bus bit 15.
		PF.10	MFP8	I/O	
	EBI_MCLK	PA.1	MFP2	O	EBI external clock output pin.
	EBI_nCS0	PA.9	MFP1	O	EBI chip select 0 output pin.
	EBI_nCS1	PA.6	MFP1	O	EBI chip select 1 output pin.
	EBI_nCS2	PA.1	MFP1	O	EBI chip select 2 output pin.
	EBI_nRE	PA.8	MFP1	O	EBI read enable output pin.
	EBI_nWE	PA.7	MFP1	O	EBI write enable output pin.
EINT0	EINT0	PA.0	MFP5	I	External interrupt 0 input pin.
		PA.13	MFP8	I	
EINT1	EINT1	PA.1	MFP5	I	External interrupt 1 input pin.
		PA.14	MFP8	I	
EINT2	EINT2	PB.3	MFP3	I	External interrupt 2 input pin.
		PD.0	MFP4	I	
		PB.13	MFP2	I	
		PE.10	MFP5	I	
EINT3	EINT3	PD.1	MFP4	I	External interrupt 3 input pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PG.15	MFP4	I	
		PE.12	MFP5	I	
I2C0	I2C0_SCL	PA.1	MFP3	I/O	I2C0 clock pin.
		PG.10	MFP2	I/O	
		PE.12	MFP6	I/O	
	I2C0_SDA	PA.0	MFP3	I/O	I2C0 data input/output pin.
		PA.15	MFP2	I/O	
		PE.10	MFP6	I/O	
I2C1	I2C1_SCL	PA.14	MFP2	I/O	I2C1 clock pin.
		PB.4	MFP2	I/O	
		PC.3	MFP4	I/O	
	I2C1_SDA	PA.13	MFP2	I/O	I2C1 data input/output pin.
		PB.6	MFP2	I/O	
		PC.4	MFP4	I/O	
I2C2	I2C2_SCL	PB.5	MFP2	I/O	I2C2 clock pin.
		PB.8	MFP2	I/O	
	I2C2_SDA	PB.7	MFP2	I/O	I2C2 data input/output pin.
		PC.0	MFP2	I/O	
I2C3	I2C3_SCL	PB.3	MFP2	I/O	I2C3 clock pin.
		PD.14	MFP3	I/O	
	I2C3_SDA	PB.1	MFP2	I/O	I2C3 data input/output pin.
		PD.15	MFP3	I/O	
I2S	I2S_BCLK	PA.3	MFP2	O	I2S_ bit clock output pin.
		PG.10	MFP8	O	
		PB.4	MFP3	O	
	I2S_DI	PA.4	MFP2	I	I2S_ data input pin.
		PB.7	MFP3	I	
	I2S_DO	PA.5	MFP2	O	I2S_ data output pin.
		PB.5	MFP3	O	
	I2S_LRCK	PA.2	MFP2	O	I2S_ left right channel clock output pin.
		PA.15	MFP8	O	
		PB.6	MFP3	O	
	I2S_MCLK	PA.6	MFP2	O	I2S_ master clock output pin.
		PB.1	MFP3	O	

Group	Pin Name	GPIO	MFP	Type	Description
JTAG0	JTAG0_TCK	PG.12	MFP7	I	JTAG0 clock input pin.
	JTAG0_TDI	PG.14	MFP7	I	JTAG0 data input pin.
	JTAG0_TDO	PG.11	MFP7	O	JTAG0 data output pin.
	JTAG0_TMS	PG.13	MFP7	I	JTAG0 test mode selection input pin.
	JTAG0_nTRST	PG.15	MFP7	I	JTAG0 reset input pin.
JTAG1	JTAG1_TCK	PA.3	MFP4	I	JTAG1 clock input pin.
	JTAG1_TDI	PA.5	MFP4	I	JTAG1 data input pin.
	JTAG1_TDO	PA.2	MFP4	O	JTAG1 data output pin.
	JTAG1_TMS	PA.4	MFP4	I	JTAG1 test mode selection input pin.
	JTAG1_nTRST	PA.6	MFP4	I	JTAG1 reset input pin.
NAND	NAND_ALE	PC.3	MFP3	O	NAND Flash address latch enable.
	NAND_CLE	PC.4	MFP3	O	NAND Flash command latch enable.
	NAND_DATA0	PC.8	MFP3	I/O	NAND Flash data bus bit 0.
	NAND_DATA1	PC.9	MFP3	I/O	NAND Flash data bus bit 1.
	NAND_DATA2	PC.10	MFP3	I/O	NAND Flash data bus bit 2.
	NAND_DATA3	PC.11	MFP3	I/O	NAND Flash data bus bit 3.
	NAND_DATA4	PC.12	MFP3	I/O	NAND Flash data bus bit 4.
	NAND_DATA5	PC.13	MFP3	I/O	NAND Flash data bus bit 5.
	NAND_DATA6	PC.14	MFP3	I/O	NAND Flash data bus bit 6.
	NAND_DATA7	PC.15	MFP3	I/O	NAND Flash data bus bit 7.
	NAND_RDY0	PC.7	MFP3	I	NAND Flash ready/busy pin.
	NAND_nCS0	PC.1	MFP3	O	NAND Flash chip enable input.
	NAND_nRE	PC.6	MFP3	O	NAND Flash read enable.
	NAND_nWE	PC.5	MFP3	O	NAND Flash write enable.
	NAND_nWP	PC.2	MFP3	O	NAND Flash write protect input.
PWM0	PWM00	PG.10	MFP7	O	PWM00 counter synchronous trigger output pin.
		PG.0	MFP6	O	
		PD.12	MFP6	O	
		PF.5	MFP4	O	
	PWM01	PA.15	MFP7	O	PWM01 counter synchronous trigger output pin.
		PG.1	MFP6	O	
		PD.13	MFP6	O	
		PF.6	MFP4	O	
	PWM02	PA.14	MFP7	O	PWM02 counter synchronous trigger output pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PG.2	MFP6	O	
		PD.14	MFP6	O	
		PB.13	MFP4	O	
		PF.7	MFP4	O	
	PWM03	PA.13	MFP7	O	PWM03 counter synchronous trigger output pin.
		PG.3	MFP6	O	
		PD.15	MFP6	O	
		PF.8	MFP4	O	
PWM1	PWM10	PG.6	MFP6	O	PWM10 counter synchronous trigger output pin.
		PB.12	MFP2	O	
		PG.11	MFP6	O	
		PF.9	MFP4	O	
	PWM11	PG.7	MFP6	O	PWM11 counter synchronous trigger output pin.
		PB.11	MFP2	O	
		PG.12	MFP6	O	
		PF.10	MFP4	O	
	PWM12	PG.8	MFP6	O	PWM12 counter synchronous trigger output pin.
		PB.10	MFP2	O	
		PG.13	MFP6	O	
		PE.10	MFP4	O	
	PWM13	PG.9	MFP6	O	PWM13 counter synchronous trigger output pin.
		PB.9	MFP2	O	
		PG.14	MFP6	O	
		PE.12	MFP4	O	
QSPI0	QSPI0_CLK	PD.3	MFP1	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	PD.5	MFP1	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	PD.7	MFP1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	PD.4	MFP1	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	PD.6	MFP1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS0	PD.2	MFP1	I/O	Quad SPI0 slave select 0 pin.
	QSPI0_SS1	PA.0	MFP1	I/O	Quad SPI0 slave select 1 pin.
		PD.0	MFP1	I/O	
RMII0	RMII0_CRSDV	PE.1	MFP1	I	RMII0 Carrier Sense/Receive Data input pin.
	RMII0_MDC	PE.9	MFP1	O	RMII0 PHY Management Clock output pin.

Group	Pin Name	GPIO	MFP	Type	Description
	RMII0_MDIO	PE.8	MFP1	I/O	RMII0 PHY Management Data pin.
	RMII0_REFCLK	PE.4	MFP1	I	RMII0 mode clock input pin.
	RMII0_RXD0	PE.3	MFP1	I	RMII0 Receive Data bus bit 0.
	RMII0_RXD1	PE.2	MFP1	I	RMII0 Receive Data bus bit 1.
	RMII0_RXERR	PE.0	MFP1	I	RMII0 Receive Data Error input pin.
	RMII0_TXD0	PE.7	MFP1	O	RMII0 Transmit Data bus bit 0.
	RMII0_TXD1	PE.6	MFP1	O	RMII0 Transmit Data bus bit 1.
	RMII0_TXEN	PE.5	MFP1	O	RMII0 Transmit Enable output pin.
RMII1	RMII1_CRSDV	PF.1	MFP1	I	RMII1 Carrier Sense/Receive Data input pin.
	RMII1_MDC	PF.9	MFP1	O	RMII1 PHY Management Clock output pin.
	RMII1_MDIO	PF.8	MFP1	I/O	RMII1 PHY Management Data pin.
	RMII1_REFCLK	PF.4	MFP1	I	RMII1 mode clock input pin.
	RMII1_RXD0	PF.3	MFP1	I	RMII1 Receive Data bus bit 0.
	RMII1_RXD1	PF.2	MFP1	I	RMII1 Receive Data bus bit 1.
	RMII1_RXERR	PF.0	MFP1	I	RMII1 Receive Data Error input pin.
	RMII1_TXD0	PF.7	MFP1	O	RMII1 Transmit Data bus bit 0.
	RMII1_TXD1	PF.6	MFP1	O	RMII1 Transmit Data bus bit 1.
	RMII1_TXEN	PF.5	MFP1	O	RMII1 Transmit Enable output pin.
SC0	SC0_CD	PA.2	MFP3	I	Smart Card 0 card detect pin.
		PC.15	MFP4	I	
	SC0_CLK	PA.5	MFP3	O	Smart Card 0 clock pin.
		PC.12	MFP4	O	
	SC0_DAT	PA.4	MFP3	I/O	Smart Card 0 data pin.
		PC.13	MFP4	I/O	
	SC0_PWR	PA.3	MFP3	O	Smart Card 0 power pin.
		PC.14	MFP4	O	
	SC0_RST	PA.6	MFP3	O	Smart Card 0 reset pin.
		PC.11	MFP4	O	
SC1	SC1_CD	PC.10	MFP4	I	Smart Card 1 card detect pin.
		PF.4	MFP4	I	
	SC1_CLK	PC.7	MFP4	O	Smart Card 1 clock pin.
		PF.1	MFP4	O	
	SC1_DAT	PC.8	MFP4	I/O	Smart Card 1 data pin.
		PF.2	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SC1_PWR	PC.9	MFP4	O	Smart Card 1 power pin.
		PF.3	MFP4	O	
	SC1_RST	PC.6	MFP4	O	Smart Card 1 reset pin.
		PF.0	MFP4	O	
SD0	SD0_CLK	PC.6	MFP6	O	SD0 clock output pin
	SD0_CMD	PC.5	MFP6	I/O	SD0 command/response pin
	SD0_DATA0	PC.7	MFP6	I/O	SD0 data line bit 0.
	SD0_DATA1	PC.8	MFP6	I/O	SD0 data line bit 1.
	SD0_DATA2	PC.9	MFP6	I/O	SD0 data line bit 2.
	SD0_DATA3	PC.10	MFP6	I/O	SD0 data line bit 3.
	SD0_nCD	PB.8	MFP6	I	SD0 card detect input pin
		PC.12	MFP6	I	
SD1	SD1_CLK	PF.1	MFP2	O	SD1 clock output pin
	SD1_CMD	PF.0	MFP2	I/O	SD1 command/response pin
	SD1_DATA0	PF.2	MFP2	I/O	SD1 data line bit 0.
	SD1_DATA1	PF.3	MFP2	I/O	SD1 data line bit 1.
	SD1_DATA2	PF.4	MFP2	I/O	SD1 data line bit 2.
	SD1_DATA3	PF.5	MFP2	I/O	SD1 data line bit 3.
	SD1_nCD	PF.6	MFP2	I	SD1 card detect input pin
SPI0	SPI0_CLK	PC.6	MFP5	I/O	SPI0 serial clock pin.
		PD.9	MFP1	I/O	
	SPI0_MISO	PC.8	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PD.11	MFP1	I/O	
	SPI0_MOSI	PC.4	MFP6	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PC.7	MFP5	I/O	
		PC.14	MFP5	I/O	
		PD.10	MFP1	I/O	
	SPI0_SS0	PC.5	MFP5	I/O	SPI0 slave select 0 pin.
		PD.8	MFP1	I/O	
	SPI0_SS1	PB.3	MFP6	I/O	SPI0 slave select 1 pin.
		PC.0	MFP5	I/O	
		PD.1	MFP1	I/O	
		PG.15	MFP1	I/O	
SPI1	SPI1_CLK	PG.10	MFP6	I/O	SPI1 serial clock pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PB.4	MFP6	I/O	
		PB.10	MFP5	I/O	
		PG.12	MFP2	I/O	
	SPI1_MISO	PB.5	MFP6	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PB.12	MFP5	I/O	
		PG.14	MFP2	I/O	
	SPI1_MOSI	PB.7	MFP6	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PB.11	MFP5	I/O	
		PG.13	MFP2	I/O	
	SPI1_SS0	PA.15	MFP6	I/O	SPI1 slave select 0 pin.
		PB.6	MFP6	I/O	
		PB.9	MFP5	I/O	
		PG.11	MFP2	I/O	
	SPI1_SS1	PB.1	MFP6	I/O	SPI1 slave select 1 pin.
		PG.15	MFP2	I/O	
TM0	TM0_EXT	PB.1	MFP5	I/O	Timer0 external capture input/toggle output pin.
		PB.8	MFP7	I/O	
		PB.10	MFP3	I/O	
	TM0_ECNT	PA.0	MFP6	I/O	Timer0 event counter input/toggle output pin.
		PD.6	MFP3	I/O	
		PF.0	MFP3	I/O	
	TM0_TGL	PB.3	MFP5	I/O	Timer0 event counter input/toggle output pin.
		PC.0	MFP7	I/O	
		PB.9	MFP3	I/O	
TM1	TM1_EXT	PA.13	MFP3	I/O	Timer1 external capture input/toggle output pin.
		PD.1	MFP3	I/O	
		PG.12	MFP3	I/O	
		PF.9	MFP3	I/O	
	TM1_ECNT	PA.1	MFP6	I/O	Timer1 event counter input/toggle output pin.
		PD.7	MFP3	I/O	
		PF.1	MFP3	I/O	
	TM1_TGL	PA.14	MFP3	I/O	Timer1 event counter input/toggle output pin.
		PD.0	MFP3	I/O	
		PG.11	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.8	MFP3	I/O	
TM2	TM2_EXT	PA.9	MFP3	I/O	Timer2 external capture input/toggle output pin.
		PB.11	MFP3	I/O	
		PD.13	MFP2	I/O	
	TM2_ECNT	PA.2	MFP6	I/O	Timer2 event counter input/toggle output pin.
		PD.8	MFP3	I/O	
		PF.2	MFP3	I/O	
	TM2_TGL	PA.10	MFP3	I/O	Timer2 event counter input/toggle output pin.
		PB.12	MFP3	I/O	
		PD.12	MFP2	I/O	
TM3	TM3_EXT	PA.7	MFP3	I/O	Timer3 external capture input/toggle output pin.
		PD.15	MFP2	I/O	
	TM3_ECNT	PA.3	MFP6	I/O	Timer3 event counter input/toggle output pin.
		PD.9	MFP3	I/O	
		PF.3	MFP3	I/O	
	TM3_TGL	PA.8	MFP3	I/O	Timer3 event counter input/toggle output pin.
		PD.14	MFP2	I/O	
TM4	TM4_EXT	PA.11	MFP3	I/O	Timer4 external capture input/toggle output pin.
		PD.2	MFP3	I/O	
		PF.6	MFP3	I/O	
	TM4_ECNT	PA.4	MFP6	I/O	Timer4 event counter input/toggle output pin.
		PD.10	MFP3	I/O	
		PF.4	MFP3	I/O	
	TM4_TGL	PA.12	MFP3	I/O	Timer4 event counter input/toggle output pin.
		PD.3	MFP3	I/O	
		PB.13	MFP3	I/O	
TM5	TM5_EXT	PA.15	MFP3	I/O	Timer5 external capture input/toggle output pin.
		PD.4	MFP3	I/O	
		PF.7	MFP3	I/O	
	TM5_ECNT	PA.5	MFP6	I/O	Timer5 event counter input/toggle output pin.
		PD.11	MFP3	I/O	
		PF.5	MFP3	I/O	
	TM5_TGL	PG.10	MFP3	I/O	Timer5 event counter input/toggle output pin.
		PD.5	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.10	MFP3	I/O	
UART0	UART0_RXD	PF.11	MFP1	I	UART0 data receiver input pin.
	UART0_TXD	PF.12	MFP1	O	UART0 data transmitter output pin.
UART1	UART1_CTS	PC.8	MFP7	I	UART1 clear to Send input pin.
		PF.7	MFP2	I	
	UART1_RTS	PC.7	MFP7	O	UART1 request to Send output pin.
		PF.8	MFP2	O	
	UART1_RXD	PA.0	MFP4	I	UART1 data receiver input pin.
		PC.6	MFP7	I	
		PF.9	MFP2	I	
	UART1_TXD	PA.1	MFP4	O	UART1 data transmitter output pin.
		PC.5	MFP7	O	
		PF.10	MFP2	O	
UART2	UART2_CTS	PA.7	MFP2	I	UART2 clear to Send input pin.
		PG.2	MFP2	I	
		PB.0	MFP2	I	
	UART2_RTS	PA.8	MFP2	O	UART2 request to Send output pin.
		PG.3	MFP2	O	
	UART2_RXD	PA.9	MFP2	I	UART2 data receiver input pin.
		PG.0	MFP2	I	
		PD.7	MFP2	I	
	UART2_TXD	PA.10	MFP2	O	UART2 data transmitter output pin.
		PG.1	MFP2	O	
		PD.6	MFP2	O	
UART3	UART3_CTS	PB.12	MFP1	I	UART3 clear to Send input pin.
		PD.5	MFP2	I	
		PF.4	MFP5	I	
	UART3_RTS	PB.11	MFP1	O	UART3 request to Send output pin.
		PD.4	MFP2	O	
		PF.5	MFP5	O	
	UART3_RXD	PC.4	MFP5	I	UART3 data receiver input pin.
		PB.10	MFP1	I	
		PD.3	MFP2	I	
		PF.6	MFP5	I	

Group	Pin Name	GPIO	MFP	Type	Description
	UART3_TXD	PC.3	MFP5	O	UART3 data transmitter output pin.
		PB.9	MFP1	O	
		PD.2	MFP2	O	
		PB.13	MFP5	O	
		PF.7	MFP5	O	
UART4	UART4_CTS	PD.15	MFP1	I	UART4 clear to Send input pin.
		PE.0	MFP5	I	
	UART4_RTS	PD.14	MFP1	O	UART4 request to Send output pin.
		PE.1	MFP5	O	
	UART4_RXD	PC.10	MFP7	I	UART4 data receiver input pin.
		PD.13	MFP1	I	
		PE.2	MFP5	I	
	UART4_TXD	PC.9	MFP7	O	UART4 data transmitter output pin.
		PD.12	MFP1	O	
		PE.3	MFP5	O	
UART5	UART5_CTS	PG.4	MFP2	I	UART5 clear to Send input pin.
		PG.11	MFP5	I	
	UART5_RTS	PG.5	MFP2	O	UART5 request to Send output pin.
		PG.12	MFP5	O	
	UART5_RXD	PG.6	MFP2	I	UART5 data receiver input pin.
		PD.1	MFP2	I	
		PG.13	MFP5	I	
	UART5_TXD	PG.7	MFP2	O	UART5 data transmitter output pin.
		PD.0	MFP2	O	
		PG.14	MFP5	O	
UART6	UART6_CTS	PA.2	MFP1	I	UART6 clear to Send input pin.
		PD.8	MFP2	I	
	UART6_RTS	PA.3	MFP1	O	UART6 request to Send output pin.
		PD.9	MFP2	O	
	UART6_RXD	PA.4	MFP1	I	UART6 data receiver input pin.
		PD.11	MFP2	I	
		PE.8	MFP5	I	
	UART6_TXD	PA.5	MFP1	O	UART6 data transmitter output pin.
		PD.10	MFP2	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.9	MFP5	O	
UART7	UART7_CTS	PB.7	MFP5	I	UART7 clear to Send input pin.
		PF.0	MFP5	I	
	UART7_RTS	PB.5	MFP5	O	UART7 request to Send output pin.
		PF.1	MFP5	O	
	UART7_RXD	PA.14	MFP6	I	UART7 data receiver input pin.
		PB.4	MFP5	I	
		PC.2	MFP4	I	
		PF.2	MFP5	I	
	UART7_TXD	PA.13	MFP6	O	UART7 data transmitter output pin.
		PB.6	MFP5	O	
		PC.1	MFP4	O	
		PF.3	MFP5	O	
UART8	UART8_CTS	PG.9	MFP2	I	UART8 clear to Send input pin.
		PC.15	MFP7	I	
	UART8_RTS	PG.8	MFP2	O	UART8 request to Send output pin.
		PC.14	MFP7	O	
	UART8_RXD	PA.11	MFP2	I	UART8 data receiver input pin.
		PC.0	MFP4	I	
		PC.13	MFP7	I	
	UART8_TXD	PA.12	MFP2	O	UART8 data transmitter output pin.
		PB.8	MFP4	O	
		PC.12	MFP7	O	
UART9	UART9_CTS	PE.4	MFP5	I	UART9 clear to Send input pin.
	UART9_RTS	PB.2	MFP7	O	UART9 request to Send output pin.
		PE.5	MFP5	O	
	UART9_RXD	PB.3	MFP7	I	UART9 data receiver input pin.
		PE.6	MFP5	I	
		PE.10	MFP3	I	
	UART9_TXD	PB.1	MFP7	O	UART9 data transmitter output pin.
		PE.7	MFP5	O	
		PE.12	MFP3	O	
USB0	USB0_VBUSVLD	PE.11	MFP1	I	USB0 external VBUS regulator status pin.
USBHL0	USBHL0_DM	PB.6	MFP4	A	USB 1.1 Host Lite 0 differential signal D-.

Group	Pin Name	GPIO	MFP	Type	Description
		PB.7	MFP4	A	
		PB.9	MFP4	A	
		PD.14	MFP5	A	
	USBHL0_DP	PB.4	MFP4	A	USB 1.1 Host Lite 0 differential signal D+.
		PB.5	MFP4	A	
		PB.10	MFP4	A	
		PD.15	MFP5	A	
USBHL1	USBHL1_DM	PF.0	MFP6	A	USB 1.1 Host Lite 1 differential signal D-.
		PE.0	MFP6	A	
	USBHL1_DP	PF.1	MFP6	A	USB 1.1 Host Lite 1 differential signal D+.
		PE.1	MFP6	A	
USBHL2	USBHL2_DM	PF.2	MFP6	A	USB 1.1 Host Lite 2 differential signal D-.
		PE.2	MFP6	A	
	USBHL2_DP	PF.3	MFP6	A	USB 1.1 Host Lite 2 differential signal D+.
		PE.3	MFP6	A	
USBHL3	USBHL3_DM	PF.4	MFP6	A	USB 1.1 Host Lite 3 differential signal D-.
		PE.4	MFP6	A	
	USBHL3_DP	PF.5	MFP6	A	USB 1.1 Host Lite 3 differential signal D+.
		PE.5	MFP6	A	
USBHL4	USBHL4_DM	PA.15	MFP4	A	USB 1.1 Host Lite 4 differential signal D-.
		PF.6	MFP6	A	
		PE.6	MFP6	A	
	USBHL4_DP	PG.10	MFP4	A	USB 1.1 Host Lite 4 differential signal D+.
		PB.13	MFP6	A	
		PF.7	MFP6	A	
		PE.7	MFP6	A	
USBHL5	USBHL5_DM	PA.13	MFP4	A	USB 1.1 Host Lite 5 differential signal D-.
		PB.11	MFP4	A	
		PF.8	MFP6	A	
		PE.8	MFP6	A	
	USBHL5_DP	PA.14	MFP4	A	USB 1.1 Host Lite 5 differential signal D+.
		PB.12	MFP4	A	
		PF.9	MFP6	A	
		PE.9	MFP6	A	

Group	Pin Name	GPIO	MFP	Type	Description
USBH	USBH_PWREN	PE.12	MFP1	O	HSUSB external VBUS regulator enable pin.
USB	USB_OVC	PE.10	MFP1	I	USB host bus power over voltage detector.
VCAP0	VCAP0_CLKO	PC.3	MFP2	O	Video image interface 0 sensor clock pin.
	VCAP0_DATA0	PC.8	MFP2	I	Video image interface 0 data 0 pin.
	VCAP0_DATA1	PC.9	MFP2	I	Video image interface 0 data 1 pin.
	VCAP0_DATA2	PC.10	MFP2	I	Video image interface 0 data 2 pin.
	VCAP0_DATA3	PC.11	MFP2	I	Video image interface 0 data 3 pin.
	VCAP0_DATA4	PC.12	MFP2	I	Video image interface 0 data 4 pin.
	VCAP0_DATA5	PC.13	MFP2	I	Video image interface 0 data 5 pin.
	VCAP0_DATA6	PC.14	MFP2	I	Video image interface 0 data 6 pin.
	VCAP0_DATA7	PC.15	MFP2	I	Video image interface 0 data 7 pin.
	VCAP0_FIELD	PC.7	MFP2	I	Video image interface 0 frame sync. pin.
	VCAP0_HSYNC	PC.5	MFP2	I	Video image interface 0 horizontal sync. pin.
	VCAP0_PCLK	PC.4	MFP2	I	Video image interface 0 pixel clock pin.
	VCAP0_VSYNC	PC.6	MFP2	I	Video image interface 0 vertical sync. pin.
VCAP1	VCAP1_CLKO	PE.12	MFP7	O	Video image interface 1 sensor clock pin.
	VCAP1_DATA0	PE.2	MFP7	I	Video image interface 1 data 0 pin.
	VCAP1_DATA1	PE.3	MFP7	I	Video image interface 1 data 1 pin.
	VCAP1_DATA2	PE.4	MFP7	I	Video image interface 1 data 2 pin.
	VCAP1_DATA3	PE.5	MFP7	I	Video image interface 1 data 3 pin.
	VCAP1_DATA4	PE.6	MFP7	I	Video image interface 1 data 4 pin.
	VCAP1_DATA5	PE.7	MFP7	I	Video image interface 1 data 5 pin.
	VCAP1_DATA6	PE.8	MFP7	I	Video image interface 1 data 6 pin.
	VCAP1_DATA7	PE.9	MFP7	I	Video image interface 1 data 7 pin.
	VCAP1_FIELD	PE.10	MFP7	I	Video image interface 1 frame sync. pin.
	VCAP1_HSYNC	PE.0	MFP7	I	Video image interface 1 horizontal sync. pin.
	VCAP1_PCLK	PF.10	MFP7	I	Video image interface 1 pixel clock pin.
	VCAP1_VSYNC	PE.1	MFP7	I	Video image interface 1 vertical sync. pin.
WDT	WDT_nRST	nRESET	MFP1	O	Watch dog timer reset trigger output.
eMMC0	eMMC0_CLK	PC.6	MFP6	O	eMMC0 clock output pin
	eMMC0_CMD	PC.5	MFP6	I/O	eMMC0 command/response pin
	eMMC0_DATA0	PC.7	MFP6	I/O	eMMC0 data line bit 0.
	eMMC0_DATA1	PC.8	MFP6	I/O	eMMC0 data line bit 1.
	eMMC0_DATA2	PC.9	MFP6	I/O	eMMC0 data line bit 2.

Group	Pin Name	GPIO	MFP	Type	Description
	eMMC0_DATA3	PC.10	MFP6	I/O	eMMC0 data line bit 3.
eMMC1	eMMC1_CLK	PF.1	MFP2	O	eMMC1 clock output pin
	eMMC1_CMD	PF.0	MFP2	I/O	eMMC1 command/response pin
	eMMC1_DATA0	PF.2	MFP2	I/O	eMMC1 data line bit 0.
	eMMC1_DATA1	PF.3	MFP2	I/O	eMMC1 data line bit 1.
	eMMC1_DATA2	PF.4	MFP2	I/O	eMMC1 data line bit 2.
	eMMC1_DATA3	PF.5	MFP2	I/O	eMMC1 data line bit 3.

4.2.3 NUC980 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin.
	I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
	UART1_RXD	I	MFP4	UART1 data receiver input pin.
	EINT0	I	MFP5	External interrupt 0 input pin.
	TM0_ECNT	I/O	MFP6	Timer0 event counter input/toggle output pin.
	CAN3_RXD	I	MFP7	CAN3 bus receiver input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS2	O	MFP1	EBI chip select 2 output pin.
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	I2C0_SCL	I/O	MFP3	I2C0 clock pin.
	UART1_TXD	O	MFP4	UART1 data transmitter output pin.
	EINT1	I	MFP5	External interrupt 1 input pin.
	TM1_ECNT	I/O	MFP6	Timer1 event counter input/toggle output pin.
	CAN3_TXD	O	MFP7	CAN3 bus transmitter output.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	UART6_CTS	I	MFP1	UART6 clear to Send input pin.
	I2S_LRCK	O	MFP2	I2S_ left right channel clock output pin.
	SC0_CD	I	MFP3	Smart Card 0 card detect pin.
	JTAG1_TDO	O	MFP4	JTAG1 data output pin.
	TM2_ECNT	I/O	MFP6	Timer2 event counter input/toggle output pin.
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	UART6_RTS	O	MFP1	UART6 request to Send output pin.
	I2S_BCLK	O	MFP2	I2S_ bit clock output pin.
	SC0_PWR	O	MFP3	Smart Card 0 power pin.
	JTAG1_TCK	I	MFP4	JTAG1 clock input pin.
	TM3_ECNT	I/O	MFP6	Timer3 event counter input/toggle output pin.
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	UART6_RXD	I	MFP1	UART6 data receiver input pin.
	I2S_DI	I	MFP2	I2S_ data input pin.
	SC0_DAT	I/O	MFP3	Smart Card 0 data pin.
	JTAG1_TMS	I	MFP4	JTAG1 test mode selection input pin.
	TM4_ECNT	I/O	MFP6	Timer4 event counter input/toggle output pin.

	Pin Name	Type	MFP	Description
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	UART6_TXD	O	MFP1	UART6 data transmitter output pin.
	I2S_DO	O	MFP2	I2S_ data output pin.
	SC0_CLK	O	MFP3	Smart Card 0 clock pin.
	JTAG1_TDI	I	MFP4	JTAG1 data input pin.
	TM5_ECNT	I/O	MFP6	Timer5 event counter input/toggle output pin.
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS1	O	MFP1	EBI chip select 1 output pin.
	I2S_MCLK	O	MFP2	I2S_ master clock output pin.
	SC0_RST	O	MFP3	Smart Card 0 reset pin.
	JTAG1_nTRST	I	MFP4	JTAG1 reset input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_nWE	O	MFP1	EBI write enable output pin.
	UART2_CTS	I	MFP2	UART2 clear to Send input pin.
	TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_nRE	O	MFP1	EBI read enable output pin.
	UART2_RTS	O	MFP2	UART2 request to Send output pin.
	TM3_TGL	I/O	MFP3	Timer3 event counter input/toggle output pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS0	O	MFP1	EBI chip select 0 output pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR10	O	MFP1	EBI address bus bit 10.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR9	O	MFP1	EBI address bus bit 9.
	UART8_RXD	I	MFP2	UART8 data receiver input pin.
	TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
PA.12	PA.12	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR8	O	MFP1	EBI address bus bit 8.
	UART8_TXD	O	MFP2	UART8 data transmitter output pin.

	Pin Name	Type	MFP	Description
	TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin.
PA.13	PA.13	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR13	O	MFP1	EBI address bus bit 13.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
	USBHL5_DM	A	MFP4	USB 1.1 Host Lite 5 differential signal D-.
	CAN1_RXD	I	MFP5	CAN1 bus receiver input.
	UART7_TXD	O	MFP6	UART7 data transmitter output pin.
	PWM03	O	MFP7	PWM03 counter synchronous trigger output pin.
	EINT0	I	MFP8	External interrupt 0 input pin.
PA.14	PA.14	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR14	O	MFP1	EBI address bus bit 14.
	I2C1_SCL	I/O	MFP2	I2C1 clock pin.
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
	USBHL5_DP	A	MFP4	USB 1.1 Host Lite 5 differential signal D+.
	CAN1_TXD	O	MFP5	CAN1 bus transmitter output.
	UART7_RXD	I	MFP6	UART7 data receiver input pin.
	PWM02	O	MFP7	PWM02 counter synchronous trigger output pin.
	EINT1	I	MFP8	External interrupt 1 input pin.
PA.15	PA.15	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR19	O	MFP1	EBI address bus bit 19.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin.
	USBHL4_DM	A	MFP4	USB 1.1 Host Lite 4 differential signal D-.
	CAN2_RXD	I	MFP5	CAN2 bus receiver input.
	SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin.
	PWM01	O	MFP7	PWM01 counter synchronous trigger output pin.
	I2S_LRCK	O	MFP8	I2S_ left right channel clock output pin.
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR12	O	MFP1	EBI address bus bit 12.
	UART2_CTS	I	MFP2	UART2 clear to Send input pin.
	ADC_AIN0	A	MFP8	ADC channel 0 analog input.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR17	O	MFP1	EBI address bus bit 17.

	Pin Name	Type	MFP	Description
	I2C3_SDA	I/O	MFP2	I2C3 data input/output pin.
	I2S_MCLK	O	MFP3	I2S_ master clock output pin.
	CAN2_RXD	I	MFP4	CAN2 bus receiver input.
	TM0_EXT	I/O	MFP5	Timer0 external capture input/toggle output pin.
	SPI1_SS1	I/O	MFP6	SPI1 slave select 1 pin.
	UART9_TXD	O	MFP7	UART9 data transmitter output pin.
	ADC_AIN1	A	MFP8	ADC channel 1 analog input.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR2	O	MFP1	EBI address bus bit 2.
	UART9_RTS	O	MFP7	UART9 request to Send output pin.
	ADC_AIN2	A	MFP8	ADC channel 2 analog input.
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR18	O	MFP1	EBI address bus bit 18.
	I2C3_SCL	I/O	MFP2	I2C3 clock pin.
	EINT2	I	MFP3	External interrupt 2 input pin.
	CAN2_TXD	O	MFP4	CAN2 bus transmitter output.
	TM0_TGL	I/O	MFP5	Timer0 event counter input/toggle output pin.
	SPI0_SS1	I/O	MFP6	SPI0 slave select 1 pin.
	UART9_RXD	I	MFP7	UART9 data receiver input pin.
	ADC_AIN3	A	MFP8	ADC channel 3 analog input.
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR14	O	MFP1	EBI address bus bit 14.
	I2C1_SCL	I/O	MFP2	I2C1 clock pin.
	I2S_BCLK	O	MFP3	I2S_ bit clock output pin.
	USBHL0_DP	A	MFP4	USB 1.1 Host Lite 0 differential signal D+.
	UART7_RXD	I	MFP5	UART7 data receiver input pin.
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
	ADC_AIN4	A	MFP8	ADC channel 4 analog input.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR16	O	MFP1	EBI address bus bit 16.
	I2C2_SCL	I/O	MFP2	I2C2 clock pin.
	I2S_DO	O	MFP3	I2S_ data output pin.
	USBHL0_DP	A	MFP4	USB 1.1 Host Lite 0 differential signal D+.
	UART7_RTS	O	MFP5	UART7 request to Send output pin.

	Pin Name	Type	MFP	Description
	SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
	ADC_AIN5	A	MFP8	ADC channel 5 analog input.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR13	O	MFP1	EBI address bus bit 13.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	I2S_LRCK	O	MFP3	I2S_ left right channel clock output pin.
	USBHL0_DM	A	MFP4	USB 1.1 Host Lite 0 differential signal D-.
	UART7_TXD	O	MFP5	UART7 data transmitter output pin.
	SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin.
	ADC_AIN6	A	MFP8	ADC channel 6 analog input.
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR15	O	MFP1	EBI address bus bit 15.
	I2C2_SDA	I/O	MFP2	I2C2 data input/output pin.
	I2S_DI	I	MFP3	I2S_ data input pin.
	USBHL0_DM	A	MFP4	USB 1.1 Host Lite 0 differential signal D-.
	UART7_CTS	I	MFP5	UART7 clear to Send input pin.
	SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
	ADC_AIN7	A	MFP8	ADC channel 7 analog input.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR11	O	MFP1	EBI address bus bit 11.
	I2C2_SCL	I/O	MFP2	I2C2 clock pin.
	CAN2_RXD	I	MFP3	CAN2 bus receiver input.
	UART8_TXD	O	MFP4	UART8 data transmitter output pin.
	SD0_nCD	I	MFP6	SD0 card detect input pin
	TM0_EXT	I/O	MFP7	Timer0 external capture input/toggle output pin.
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	UART3_TXD	O	MFP1	UART3 data transmitter output pin.
	PWM13	O	MFP2	PWM13 counter synchronous trigger output pin.
	TM0_TGL	I/O	MFP3	Timer0 event counter input/toggle output pin.
	USBHL0_DM	A	MFP4	USB 1.1 Host Lite 0 differential signal D-.
	SPI1_SS0	I/O	MFP5	SPI1 slave select 0 pin.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	UART3_RXD	I	MFP1	UART3 data receiver input pin.
	PWM12	O	MFP2	PWM12 counter synchronous trigger output pin.

	Pin Name	Type	MFP	Description
	TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin.
	USBHL0_DP	A	MFP4	USB 1.1 Host Lite 0 differential signal D+.
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	UART3_RTS	O	MFP1	UART3 request to Send output pin.
	PWM11	O	MFP2	PWM11 counter synchronous trigger output pin.
	TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin.
	USBHL5_DM	A	MFP4	USB 1.1 Host Lite 5 differential signal D-.
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	UART3_CTS	I	MFP1	UART3 clear to Send input pin.
	PWM10	O	MFP2	PWM10 counter synchronous trigger output pin.
	TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin.
	USBHL5_DP	A	MFP4	USB 1.1 Host Lite 5 differential signal D+.
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.
	EINT2	I	MFP2	External interrupt 2 input pin.
	TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin.
	PWM02	O	MFP4	PWM02 counter synchronous trigger output pin.
	UART3_TXD	O	MFP5	UART3 data transmitter output pin.
	USBHL4_DP	A	MFP6	USB 1.1 Host Lite 4 differential signal D+.
	EBI_DATA0	I/O	MFP8	EBI data bus bit 0.
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA0	I/O	MFP1	EBI data bus bit 0.
	I2C2_SDA	I/O	MFP2	I2C2 data input/output pin.
	CAN2_TXD	O	MFP3	CAN2 bus transmitter output.
	UART8_RXD	I	MFP4	UART8 data receiver input pin.
	SPI0_SS1	I/O	MFP5	SPI0 slave select 1 pin.
	TM0_TGL	I/O	MFP7	Timer0 event counter input/toggle output pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA1	I/O	MFP1	EBI data bus bit 1.
	NAND_nCS0	O	MFP3	NAND Flash chip enable input.
	UART7_TXD	O	MFP4	UART7 data transmitter output pin.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_DATA2	I/O	MFP1	EBI data bus bit 2.
	NAND_nWP	O	MFP3	NAND Flash write protect input.
	UART7_RXD	I	MFP4	UART7 data receiver input pin.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA3	I/O	MFP1	EBI data bus bit 3.
	VCAP0_CLKO	O	MFP2	Video image interface 0 sensor clock pin.
	NAND_ALE	O	MFP3	NAND Flash address latch enable.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	UART3_TXD	O	MFP5	UART3 data transmitter output pin.
	CAN0_RXD	I	MFP7	CAN0 bus receiver input.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA4	I/O	MFP1	EBI data bus bit 4.
	VCAP0_PCLK	I	MFP2	Video image interface 0 pixel clock pin.
	NAND_CLE	O	MFP3	NAND Flash command latch enable.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	UART3_RXD	I	MFP5	UART3 data receiver input pin.
	SPI0_MOSI	I/O	MFP6	SPI0 MOSI (Master Out, Slave In) pin.
	CAN0_TXD	O	MFP7	CAN0 bus transmitter output.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA5	I/O	MFP1	EBI data bus bit 5.
	VCAP0_HSYNC	I	MFP2	Video image interface 0 horizontal sync. pin.
	NAND_nWE	O	MFP3	NAND Flash write enable.
	SPI0_SS0	I/O	MFP5	SPI0 slave select 0 pin.
	SD0_CMD/eMMC0_CMD	I/O	MFP6	SD0 command/response pin eMMC0 command/response pin
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA6	I/O	MFP1	EBI data bus bit 6.
	VCAP0_VSYNC	I	MFP2	Video image interface 0 vertical sync. pin.
	NAND_nRE	O	MFP3	NAND Flash read enable.
	SC1_RST	O	MFP4	Smart Card 1 reset pin.
	SPI0_CLK	I/O	MFP5	SPI0 serial clock pin.
	SD0_CLK/eMMC0_CLK	O	MFP6	SD0 clock output pin eMMC0 clock output pin

	Pin Name	Type	MFP	Description
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA7	I/O	MFP1	EBI data bus bit 7.
	VCAP0_FIELD	I	MFP2	Video image interface 0 frame sync. pin.
	NAND_RDY0	I	MFP3	NAND Flash ready/busy pin.
	SC1_CLK	O	MFP4	Smart Card 1 clock pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	SD0_DATA0/eMMC0_DATA0	I/O	MFP6	SD0 data line bit 0. eMMC0 data line bit 0.
	UART1_RTS	O	MFP7	UART1 request to Send output pin.
PC.8	PC.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA8	I/O	MFP1	EBI data bus bit 8.
	VCAP0_DATA0	I	MFP2	Video image interface 0 data 0 pin.
	NAND_DATA0	I/O	MFP3	NAND Flash data bus bit 0.
	SC1_DAT	I/O	MFP4	Smart Card 1 data pin.
	SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin.
	SD0_DATA1/eMMC0_DATA1	I/O	MFP6	SD0 data line bit 1. eMMC0 data line bit 1.
	UART1_CTS	I	MFP7	UART1 clear to Send input pin.
PC.9	PC.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA9	I/O	MFP1	EBI data bus bit 9.
	VCAP0_DATA1	I	MFP2	Video image interface 0 data 1 pin.
	NAND_DATA1	I/O	MFP3	NAND Flash data bus bit 1.
	SC1_PWR	O	MFP4	Smart Card 1 power pin.
	SD0_DATA2/eMMC0_DATA2	I/O	MFP6	SD0 data line bit 2. eMMC0 data line bit 2.
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
PC.10	PC.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA10	I/O	MFP1	EBI data bus bit 10.
	VCAP0_DATA2	I	MFP2	Video image interface 0 data 2 pin.
	NAND_DATA2	I/O	MFP3	NAND Flash data bus bit 2.
	SC1_CD	I	MFP4	Smart Card 1 card detect pin.
	SD0_DATA3/eMMC0_DATA3	I/O	MFP6	SD0 data line bit 3. eMMC0 data line bit 3.

	Pin Name	Type	MFP	Description
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
PC.11	PC.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA11	I/O	MFP1	EBI data bus bit 11.
	VCAP0_DATA3	I	MFP2	Video image interface 0 data 3 pin.
	NAND_DATA3	I/O	MFP3	NAND Flash data bus bit 3.
	SC0_RST	O	MFP4	Smart Card 0 reset pin.
PC.12	PC.12	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA12	I/O	MFP1	EBI data bus bit 12.
	VCAP0_DATA4	I	MFP2	Video image interface 0 data 4 pin.
	NAND_DATA4	I/O	MFP3	NAND Flash data bus bit 4.
	SC0_CLK	O	MFP4	Smart Card 0 clock pin.
	SD0_nCD	I	MFP6	SD0 card detect input pin
	UART8_TXD	O	MFP7	UART8 data transmitter output pin.
PC.13	PC.13	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA13	I/O	MFP1	EBI data bus bit 13.
	VCAP0_DATA5	I	MFP2	Video image interface 0 data 5 pin.
	NAND_DATA5	I/O	MFP3	NAND Flash data bus bit 5.
	SC0_DAT	I/O	MFP4	Smart Card 0 data pin.
	UART8_RXD	I	MFP7	UART8 data receiver input pin.
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA14	I/O	MFP1	EBI data bus bit 14.
	VCAP0_DATA6	I	MFP2	Video image interface 0 data 6 pin.
	NAND_DATA6	I/O	MFP3	NAND Flash data bus bit 6.
	SC0_PWR	O	MFP4	Smart Card 0 power pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	UART8_RTS	O	MFP7	UART8 request to Send output pin.
PC.15	PC.15	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA15	I/O	MFP1	EBI data bus bit 15.
	VCAP0_DATA7	I	MFP2	Video image interface 0 data 7 pin.
	NAND_DATA7	I/O	MFP3	NAND Flash data bus bit 7.
	SC0_CD	I	MFP4	Smart Card 0 card detect pin.
	UART8_CTS	I	MFP7	UART8 clear to Send input pin.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin.

	Pin Name	Type	MFP	Description
	UART5_TXD	O	MFP2	UART5 data transmitter output pin.
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
	EINT2	I	MFP4	External interrupt 2 input pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin.
	UART5_RXD	I	MFP2	UART5 data receiver input pin.
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
	EINT3	I	MFP4	External interrupt 3 input pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_SS0	I/O	MFP1	Quad SPI0 slave select 0 pin.
	UART3_TXD	O	MFP2	UART3 data transmitter output pin.
	TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_CLK	I/O	MFP1	Quad SPI0 serial clock pin.
	UART3_RXD	I	MFP2	UART3 data receiver input pin.
	TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin.
PD.4	PD.4	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MOSI0	I/O	MFP1	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	UART3_RTS	O	MFP2	UART3 request to Send output pin.
	TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin.
PD.5	PD.5	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MISO0	I/O	MFP1	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	UART3_CTS	I	MFP2	UART3 clear to Send input pin.
	TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin.
PD.6	PD.6	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MOSI1	I/O	MFP1	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin.
	CAN0_RXD	I	MFP4	CAN0 bus receiver input.
PD.7	PD.7	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MISO1	I/O	MFP1	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin.
	CAN0_TXD	O	MFP4	CAN0 bus transmitter output.

	Pin Name	Type	MFP	Description
PD.8	PD.8	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS0	I/O	MFP1	SPI0 slave select 0 pin.
	UART6_CTS	I	MFP2	UART6 clear to Send input pin.
	TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin.
PD.9	PD.9	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
	UART6_RTS	O	MFP2	UART6 request to Send output pin.
	TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin.
PD.10	PD.10	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	UART6_TXD	O	MFP2	UART6 data transmitter output pin.
	TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin.
PD.11	PD.11	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	UART6_RXD	I	MFP2	UART6 data receiver input pin.
	TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin.
PD.12	PD.12	I/O	MFP0	General purpose digital I/O pin.
	UART4_TXD	O	MFP1	UART4 data transmitter output pin.
	TM2_TGL	I/O	MFP2	Timer2 event counter input/toggle output pin.
	CAN2_RXD	I	MFP4	CAN2 bus receiver input.
	PWM00	O	MFP6	PWM00 counter synchronous trigger output pin.
	EBI_DATA1	I/O	MFP8	EBI data bus bit 1.
PD.13	PD.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_RXD	I	MFP1	UART4 data receiver input pin.
	TM2_EXT	I/O	MFP2	Timer2 external capture input/toggle output pin.
	CAN2_TXD	O	MFP4	CAN2 bus transmitter output.
	PWM01	O	MFP6	PWM01 counter synchronous trigger output pin.
	EBI_DATA2	I/O	MFP8	EBI data bus bit 2.
PD.14	PD.14	I/O	MFP0	General purpose digital I/O pin.
	UART4_RTS	O	MFP1	UART4 request to Send output pin.
	TM3_TGL	I/O	MFP2	Timer3 event counter input/toggle output pin.
	I2C3_SCL	I/O	MFP3	I2C3 clock pin.
	CAN1_RXD	I	MFP4	CAN1 bus receiver input.
	USBHL0_DM	A	MFP5	USB 1.1 Host Lite 0 differential signal D-.

	Pin Name	Type	MFP	Description
	PWM02	O	MFP6	PWM02 counter synchronous trigger output pin.
	EBI_DATA3	I/O	MFP8	EBI data bus bit 3.
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin.
	UART4_CTS	I	MFP1	UART4 clear to Send input pin.
	TM3_EXT	I/O	MFP2	Timer3 external capture input/toggle output pin.
	I2C3_SDA	I/O	MFP3	I2C3 data input/output pin.
	CAN1_TXD	O	MFP4	CAN1 bus transmitter output.
	USBHL0_DP	A	MFP5	USB 1.1 Host Lite 0 differential signal D+.
	PWM03	O	MFP6	PWM03 counter synchronous trigger output pin.
	EBI_DATA4	I/O	MFP8	EBI data bus bit 4.
PE.0	PE.0	I/O	MFP0	General purpose digital I/O pin.
	RMII0_RXERR	I	MFP1	RMII0 Receive Data Error input pin.
	CAN0_RXD	I	MFP2	CAN0 bus receiver input.
	UART4_CTS	I	MFP5	UART4 clear to Send input pin.
	USBHL1_DM	A	MFP6	USB 1.1 Host Lite 1 differential signal D-.
	VCAP1_HSYNC	I	MFP7	Video image interface 1 horizontal sync. pin.
PE.1	PE.1	I/O	MFP0	General purpose digital I/O pin.
	RMII0_CRSDV	I	MFP1	RMII0 Carrier Sense/Receive Data input pin.
	CAN0_TXD	O	MFP2	CAN0 bus transmitter output.
	UART4_RTS	O	MFP5	UART4 request to Send output pin.
	USBHL1_DP	A	MFP6	USB 1.1 Host Lite 1 differential signal D+.
	VCAP1_VSYNC	I	MFP7	Video image interface 1 vertical sync. pin.
PE.2	PE.2	I/O	MFP0	General purpose digital I/O pin.
	RMII0_RXD1	I	MFP1	RMII0 Receive Data bus bit 1.
	CAN1_RXD	I	MFP2	CAN1 bus receiver input.
	UART4_RXD	I	MFP5	UART4 data receiver input pin.
	USBHL2_DM	A	MFP6	USB 1.1 Host Lite 2 differential signal D-.
	VCAP1_DATA0	I	MFP7	Video image interface 1 data 0 pin.
PE.3	PE.3	I/O	MFP0	General purpose digital I/O pin.
	RMII0_RXD0	I	MFP1	RMII0 Receive Data bus bit 0.
	CAN1_TXD	O	MFP2	CAN1 bus transmitter output.
	UART4_TXD	O	MFP5	UART4 data transmitter output pin.
	USBHL2_DP	A	MFP6	USB 1.1 Host Lite 2 differential signal D+.
	VCAP1_DATA1	I	MFP7	Video image interface 1 data 1 pin.

	Pin Name	Type	MFP	Description
PE.4	PE.4	I/O	MFP0	General purpose digital I/O pin.
	RMII0_REFCLK	I	MFP1	RMII0 mode clock input pin.
	CAN2_RXD	I	MFP2	CAN2 bus receiver input.
	UART9_CTS	I	MFP5	UART9 clear to Send input pin.
	USBHL3_DM	A	MFP6	USB 1.1 Host Lite 3 differential signal D-.
	VCAP1_DATA2	I	MFP7	Video image interface 1 data 2 pin.
PE.5	PE.5	I/O	MFP0	General purpose digital I/O pin.
	RMII0_TXEN	O	MFP1	RMII0 Transmit Enable output pin.
	CAN2_TXD	O	MFP2	CAN2 bus transmitter output.
	UART9_RTS	O	MFP5	UART9 request to Send output pin.
	USBHL3_DP	A	MFP6	USB 1.1 Host Lite 3 differential signal D+.
	VCAP1_DATA3	I	MFP7	Video image interface 1 data 3 pin.
PE.6	PE.6	I/O	MFP0	General purpose digital I/O pin.
	RMII0_TXD1	O	MFP1	RMII0 Transmit Data bus bit 1.
	CAN3_RXD	I	MFP2	CAN3 bus receiver input.
	UART9_RXD	I	MFP5	UART9 data receiver input pin.
	USBHL4_DM	A	MFP6	USB 1.1 Host Lite 4 differential signal D-.
	VCAP1_DATA4	I	MFP7	Video image interface 1 data 4 pin.
PE.7	PE.7	I/O	MFP0	General purpose digital I/O pin.
	RMII0_TXD0	O	MFP1	RMII0 Transmit Data bus bit 0.
	CAN3_TXD	O	MFP2	CAN3 bus transmitter output.
	UART9_TXD	O	MFP5	UART9 data transmitter output pin.
	USBHL4_DP	A	MFP6	USB 1.1 Host Lite 4 differential signal D+.
	VCAP1_DATA5	I	MFP7	Video image interface 1 data 5 pin.
PE.8	PE.8	I/O	MFP0	General purpose digital I/O pin.
	RMII0_MDIO	I/O	MFP1	RMII0 PHY Management Data pin.
	UART6_RXD	I	MFP5	UART6 data receiver input pin.
	USBHL5_DM	A	MFP6	USB 1.1 Host Lite 5 differential signal D-.
	VCAP1_DATA6	I	MFP7	Video image interface 1 data 6 pin.
PE.9	PE.9	I/O	MFP0	General purpose digital I/O pin.
	RMII0_MDC	O	MFP1	RMII0 PHY Management Clock output pin.
	UART6_TXD	O	MFP5	UART6 data transmitter output pin.
	USBHL5_DP	A	MFP6	USB 1.1 Host Lite 5 differential signal D+.
	VCAP1_DATA7	1	MFP7	Video image interface 1 ata 7 pin.

	Pin Name	Type	MFP	Description
PE.10	PE.10	I/O	MFP0	General purpose digital I/O pin.
	USB_OVC	I	MFP1	USB host bus power over voltage detector.
	CAN3_RXD	I	MFP2	CAN3 bus receiver input.
	UART9_RXD	I	MFP3	UART9 data receiver input pin.
	PWM12	O	MFP4	PWM12 counter synchronous trigger output pin.
	EINT2	I	MFP5	External interrupt 2 input pin.
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
	VCAP1_FIELD	I	MFP7	Video image interface 1 frame sync. pin.
PE.11	PE.11	I/O	MFP0	General purpose digital I/O pin.
	USB0_VBUSVLD	I	MFP1	USB0 external VBUS regulator status pin.
PE.12	PE.12	I/O	MFP0	General purpose digital I/O pin.
	USBH_PWREN	O	MFP1	HSUSB external VBUS regulator enable pin.
	CAN3_TXD	O	MFP2	CAN3 bus transmitter output.
	UART9_TXD	O	MFP3	UART9 data transmitter output pin.
	PWM13	O	MFP4	PWM13 counter synchronous trigger output pin.
	EINT3	I	MFP5	External interrupt 3 input pin.
	I2C0_SCL	I/O	MFP6	I2C0 clock pin.
	VCAP1_CLKO	O	MFP7	Video image interface 1 sensor clock pin.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	RMII1_RXERR	I	MFP1	RMII1 Receive Data Error input pin.
	SD1_CMD/eMMC1_CMD	I/O	MFP2	SD1 command/response pin eMMC1 command/response pin
	TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin.
	SC1_RST	O	MFP4	Smart Card 1 reset pin.
	UART7_CTS	I	MFP5	UART7 clear to Send input pin.
	USBHL1_DM	A	MFP6	USB 1.1 Host Lite 1 differential signal D-.
	EBI_DATA5	I/O	MFP8	EBI data bus bit 5.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	RMII1_CRSDV	I	MFP1	RMII1 Carrier Sense/Receive Data input pin.
	SD1_CLK/eMMC1_CLK	O	MFP2	SD1 clock output pin eMMC1 clock output pin
	TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin.
	SC1_CLK	O	MFP4	Smart Card 1 clock pin.
	UART7_RTS	O	MFP5	UART7 request to Send output pin.

	Pin Name	Type	MFP	Description
	USBHL1_DP	A	MFP6	USB 1.1 Host Lite 1 differential signal D+.
	EBI_DATA6	I/O	MFP8	EBI data bus bit 6.
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	RMII1_RXD1	I	MFP1	RMII1 Receive Data bus bit 1.
	SD1_DATA0/eMMC1_DATA0	I/O	MFP2	SD1 data line bit 0. eMMC1 data line bit 0.
	TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin.
	SC1_DAT	I/O	MFP4	Smart Card 1 data pin.
	UART7_RXD	I	MFP5	UART7 data receiver input pin.
	USBHL2_DM	A	MFP6	USB 1.1 Host Lite 2 differential signal D-.
	EBI_DATA7	I/O	MFP8	EBI data bus bit 7.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	RMII1_RXD0	I	MFP1	RMII1 Receive Data bus bit 0.
	SD1_DATA1/eMMC1_DATA1	I/O	MFP2	SD1 data line bit 1. eMMC1 data line bit 1.
	TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin.
	SC1_PWR	O	MFP4	Smart Card 1 power pin.
	UART7_TXD	O	MFP5	UART7 data transmitter output pin.
	USBHL2_DP	A	MFP6	USB 1.1 Host Lite 2 differential signal D+.
	EBI_DATA8	I/O	MFP8	EBI data bus bit 8.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	RMII1_REFCLK	I	MFP1	RMII1 mode clock input pin.
	SD1_DATA2/eMMC1_DATA2	I/O	MFP2	SD1 data line bit 2. eMMC1 data line bit 2.
	TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin.
	SC1_CD	I	MFP4	Smart Card 1 card detect pin.
	UART3_CTS	I	MFP5	UART3 clear to Send input pin.
	USBHL3_DM	A	MFP6	USB 1.1 Host Lite 3 differential signal D-.
	EBI_DATA9	I/O	MFP8	EBI data bus bit 9.
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	RMII1_TXEN	O	MFP1	RMII1 Transmit Enable output pin.
	SD1_DATA3/eMMC1_DATA3	I/O	MFP2	SD1 data line bit 3. eMMC1 data line bit 3.
	TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin.

	Pin Name	Type	MFP	Description
	PWM00	O	MFP4	PWM00 counter synchronous trigger output pin.
	UART3_RTS	O	MFP5	UART3 request to Send output pin.
	USBHL3_DP	A	MFP6	USB 1.1 Host Lite 3 differential signal D+.
	EBI_DATA10	I/O	MFP8	EBI data bus bit 10.
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.
	RMII1_TXD1	O	MFP1	RMII1 Transmit Data bus bit 1.
	SD1_nCD	I	MFP2	SD1 card detect input pin
	TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
	PWM01	O	MFP4	PWM01 counter synchronous trigger output pin.
	UART3_RXD	I	MFP5	UART3 data receiver input pin.
	USBHL4_DM	A	MFP6	USB 1.1 Host Lite 4 differential signal D-.
	EBI_DATA11	I/O	MFP8	EBI data bus bit 11.
PF.7	PF.7	I/O	MFP0	General purpose digital I/O pin.
	RMII1_TXD0	O	MFP1	RMII1 Transmit Data bus bit 0.
	UART1_CTS	I	MFP2	UART1 clear to Send input pin.
	TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin.
	PWM02	O	MFP4	PWM02 counter synchronous trigger output pin.
	UART3_TXD	O	MFP5	UART3 data transmitter output pin.
	USBHL4_DP	A	MFP6	USB 1.1 Host Lite 4 differential signal D+.
	EBI_DATA12	I/O	MFP8	EBI data bus bit 12.
PF.8	PF.8	I/O	MFP0	General purpose digital I/O pin.
	RMII1_MDIO	I/O	MFP1	RMII1 PHY Management Data pin.
	UART1_RTS	O	MFP2	UART1 request to Send output pin.
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
	PWM03	O	MFP4	PWM03 counter synchronous trigger output pin.
	USBHL5_DM	A	MFP6	USB 1.1 Host Lite 5 differential signal D-.
	EBI_DATA13	I/O	MFP8	EBI data bus bit 13.
PF.9	PF.9	I/O	MFP0	General purpose digital I/O pin.
	RMII1_MDC	O	MFP1	RMII1 PHY Management Clock output pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
	PWM10	O	MFP4	PWM10 counter synchronous trigger output pin.
	USBHL5_DP	A	MFP6	USB 1.1 Host Lite 5 differential signal D+.
	EBI_DATA14	I/O	MFP8	EBI data bus bit 14.

	Pin Name	Type	MFP	Description
PF.10	PF.10	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin.
	PWM11	O	MFP4	PWM11 counter synchronous trigger output pin.
	VCAP1_PCLK	I	MFP7	Video image interface 1 pixel clock pin.
	EBI_DATA15	I/O	MFP8	EBI data bus bit 15.
PF.11	PF.11	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP1	UART0 data receiver input pin.
PF.12	PF.12	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP1	UART0 data transmitter output pin.
PG.0	PG.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR0	O	MFP1	EBI address bus bit 0.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	CLK_OUT	O	MFP3	Internal clock selection output pin.
	PWM00	O	MFP6	PWM00 counter synchronous trigger output pin.
	CFG.0_PwrOnSet0	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.1	PG.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR1	O	MFP1	EBI address bus bit 1.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	PWM01	O	MFP6	PWM01 counter synchronous trigger output pin.
	CFG.1_PwrOnSet1	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.2	PG.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR2	O	MFP1	EBI address bus bit 2.
	UART2_CTS	I	MFP2	UART2 clear to Send input pin.
	PWM02	O	MFP6	PWM02 counter synchronous trigger output pin.
	CFG.2_PwrOnSet2	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.3	PG.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR3	O	MFP1	EBI address bus bit 3.
	UART2_RTS	O	MFP2	UART2 request to Send output pin.
	PWM03	O	MFP6	PWM03 counter synchronous trigger output pin.
	CFG.3_PwrOnSet3	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.4	PG.4	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_ADDR18	O	MFP1	EBI address bus bit 18.
	UART5_CTS	I	MFP2	UART5 clear to Send input pin.
	CFG.4_PwrOnSet4	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.5	PG.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR12	O	MFP1	EBI address bus bit 12.
	UART5_RTS	O	MFP2	UART5 request to Send output pin.
	CFG.5_PwrOnSet5	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.6	PG.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR4	O	MFP1	EBI address bus bit 4.
	UART5_RXD	I	MFP2	UART5 data receiver input pin.
	PWM10	O	MFP6	PWM10 counter synchronous trigger output pin.
	CFG.6_PwrOnSet6	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.7	PG.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR5	O	MFP1	EBI address bus bit 5.
	UART5_TXD	O	MFP2	UART5 data transmitter output pin.
	PWM11	O	MFP6	PWM11 counter synchronous trigger output pin.
	CFG.7_PwrOnSet7	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.8	PG.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR6	O	MFP1	EBI address bus bit 6.
	UART8_RTS	O	MFP2	UART8 request to Send output pin.
	PWM12	O	MFP6	PWM12 counter synchronous trigger output pin.
	CFG.8_PwrOnSet8	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.9	PG.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADDR7	O	MFP1	EBI address bus bit 7.
	UART8_CTS	I	MFP2	UART8 clear to Send input pin.
	PWM13	O	MFP6	PWM13 counter synchronous trigger output pin.
	CFG.9_PwrOnSet9	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
PG.10	PG.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_DATA0	I/O	MFP1	EBI data bus bit 0.
	I2C0_SCL	I/O	MFP2	I2C0 clock pin.
	TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin.

	Pin Name	Type	MFP	Description
	USBHL4_DP	A	MFP4	USB 1.1 Host Lite 4 differential signal D+.
	CAN2_TXD	O	MFP5	CAN2 bus transmitter output.
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
	PWM00	O	MFP7	PWM00 counter synchronous trigger output pin.
	I2S_BCLK	O	MFP8	I2S_ bit clock output pin.
PG.11	PG.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS0	I/O	MFP2	SPI1 slave select 0 pin.
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin.
	CAN0_RXD	I	MFP4	CAN0 bus receiver input.
	UART5_CTS	I	MFP5	UART5 clear to Send input pin.
	PWM10	O	MFP6	PWM10 counter synchronous trigger output pin.
	JTAG0_TDO	O	MFP7	JTAG0 data output pin.
PG.12	PG.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin.
	CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
	UART5_RTS	O	MFP5	UART5 request to Send output pin.
	PWM11	O	MFP6	PWM11 counter synchronous trigger output pin.
	JTAG0_TCK	I	MFP7	JTAG0 clock input pin.
PG.13	PG.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	CAN1_RXD	I	MFP4	CAN1 bus receiver input.
	UART5_RXD	I	MFP5	UART5 data receiver input pin.
	PWM12	O	MFP6	PWM12 counter synchronous trigger output pin.
	JTAG0_TMS	I	MFP7	JTAG0 test mode selection input pin.
PG.14	PG.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
	CAN1_TXD	O	MFP4	CAN1 bus transmitter output.
	UART5_TXD	O	MFP5	UART5 data transmitter output pin.
	PWM13	O	MFP6	PWM13 counter synchronous trigger output pin.
	JTAG0_TDI	I	MFP7	JTAG0 data input pin.
PG.15	PG.15	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin.
	SPI1_SS1	I/O	MFP2	SPI1 slave select 1 pin.

	Pin Name	Type	MFP	Description
	EINT3	I	MFP4	External interrupt 3 input pin.
	JTAG0_nTRST	I	MFP7	JTAG0 reset input pin.

5 BLOCK DIAGRAM

5.1 NUC980 Series Block Diagram

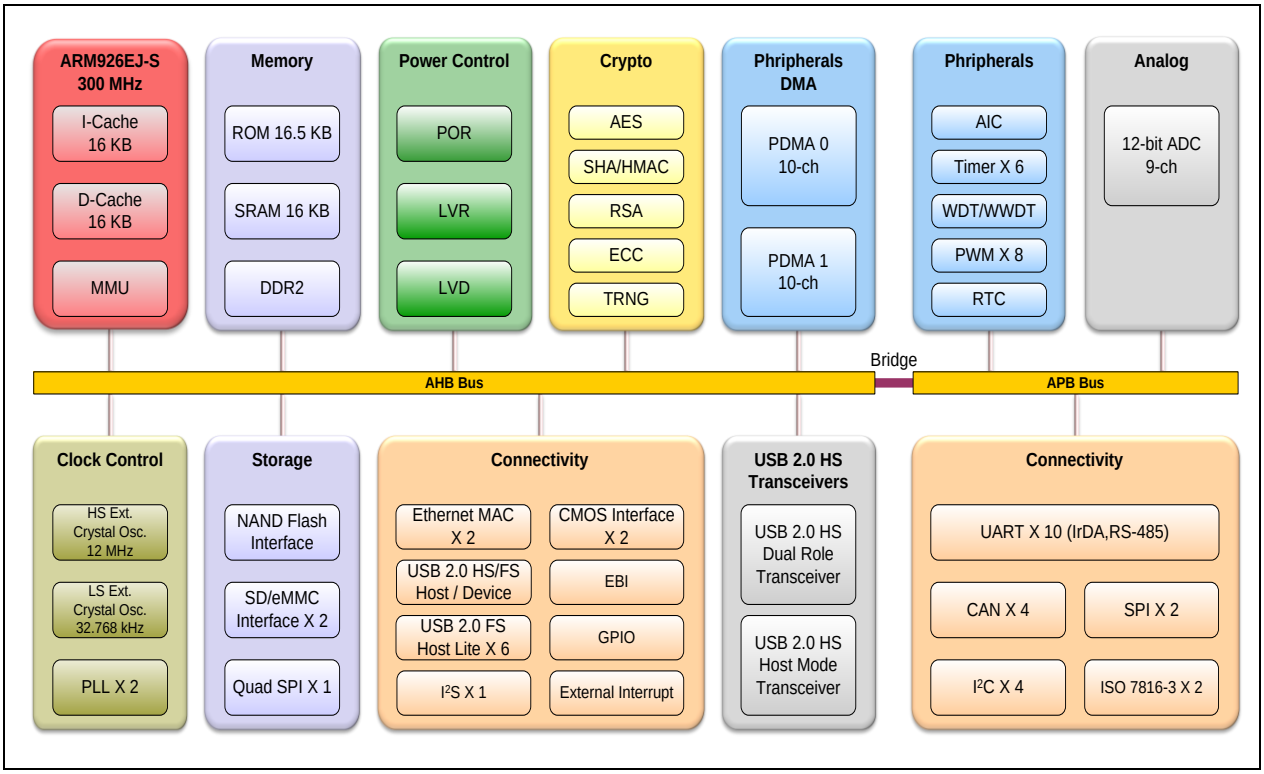


Figure 5.1-1 NUC980 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® ARM926EJ-S CPU Core

6.1.1 Overview

The ARM926EJ-S CPU core is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S CPU core is targeted at multi-tasking applications where full memory management, high performance, and low power are all important.

The ARM926EJ-S CPU core supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to choose between high performance and high code density. The ARM926EJ-S CPU core includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead.

The ARM926EJ-S processor provides support for external coprocessor enabling floating-point or other application-specific hardware acceleration to be added. The ARM926EJ-S CPU core implements ARM architecture version 5TEJ.

The ARM926EJ-S processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core.
- A Memory Management Unit (MMU).
- Separate instruction and data cache.
- Separate instruction and data AMBA AHB bus interfaces.

6.2 System Manager

6.2.1 Overview

The system management describes the following information and functions.

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Product Identifier (PDID), Power-On Setting, System Wake-Up, Reset Control for on-chip controllers/peripherals, and multi-function pin control.
- System Control registers

6.3 Clock Controller

6.3.1 Overview

The clock controller generates all clocks for Video, Audio, CPU, system bus and all functionalities. This chip includes two PLL modules. The clock source for each functionality comes from the PLL, or from the external crystal input directly. For each clock there is a bit on the CLKEN register to control the clock ON or OFF individually, and the divider setting is in the CLK_DIVCTL register. The register can also be used to control the clock enable or disable for power control.

6.3.2 Features,

- Supports two PLLs, up to 500 MHz, for high performance system operation
- External 12 MHz high speed crystal input for precise timing operation
- External 32.768 kHz low speed crystal input for RTC function and low speed clock source

6.4 Advanced Interrpt Controller

6.4.1 Overview

An interrupt temporarily changes the sequence of program execution to react to a particular event such as power failure, watchdog timer timeout, transmit/receive request from Ethernet MAC Controller, and so on. The CPU processor provides two modes of interrupt, the Fast Interrupt (FIQ) mode for critical session and the Interrupt (IRQ) mode for general purpose. The IRQ request is occurred when the nIRQ input is asserted. Similarly, the FIQ request is occurred when the nFIQ input is asserted. The FIQ has privilege over the IRQ and can preempt an ongoing IRQ. It is possible to ignore the FIQ and the IRQ by setting the F and I bits in the current program status register (CPSR).

The Advanced Interrupt Controller (AIC) is capable of processing the interrupt requests up to 64 different sources. Currently, 621 interrupt sources are defined. Each interrupt source is uniquely assigned to an interrupt channel. For example, the watchdog timer interrupt is assigned to channel 1. The AIC implements a proprietary eight-level priority scheme that categories the available 621 interrupt sources into eight priority levels. Interrupt sources within the priority level 0 is the highest priority and the priority level 7 is the lowest. In order to make this scheme work properly, a certain priority level must be specified to each interrupt source during power-on initialization; otherwise, the system shall behave unexpectedly. Within each priority level, interrupt source that is positioned in a lower channel has a higher priority. Interrupt source that is active, enabled, and positioned in the lowest channel with priority level 0 is promoted to the FIQ. Interrupt sources within the priority levels other than 0 are routed to the IRQ. The IRQ can be preempted by the occurrence of the FIQ. Interrupt nesting is performed automatically by the AIC.

Though interrupt sources originated from the chip itself are intrinsically high-level sensitive, the AIC can be configured as either low-level sensitive, high-level sensitive, negative-edge triggered, or positive-edge triggered to each interrupt source.

6.4.2 Features,

- AMBA APB bus interface
- External interrupts can be programmed as either edge-triggered or level-sensitive
- External interrupts can be programmed as either low-active or high-active
- Flags to reflect the status of each interrupt source
- Individual mask for each interrupt source
- Support proprietary 8-level interrupt scheme to employ the priority scheme.
- Priority methodology is adopted to allow for interrupt daisy-chaining
- Automatically masking out the lower priority interrupt during interrupt nesting
- Automatically clearing the interrupt flag when the external interrupt source is programmed to be edge-triggered

6.5 SDRAM Interface Controller

6.5.1 Overview

The SDRAM Controller support SDR, DDR, Low-Power DDR and DDR2 type SDRAM. The memory device size type can be from 16M bit and up to 1G bits. Only 16-bit data bus width is supported. The total system memory size can be from 2M bytes and up to 256M bytes for different SDRAM configuration.

The SDRAM controller interface to three isolated AHB. All these AHB masters can access the memory independent. Except the memory access, the masters of AHB also could access the SDRAM control registers.

For performance and function issue, the SDRAM controller also supports the proprietary Enhanced-AHB. The EAHB add the down-count address mode, byte-enable signal and explicit burst access number. The explicit access number function is reached by modify the HBURST signal to EHBURST and it represent the access number. The maximum EAHB access number is 16. The SDRAM controller also builds a BIST module to test the external memory device.

An internal arbiter is used to schedule the access from the masters and the BIST request, the BIST request with the highest priority and the then the AHB3 master, AHB2 master and AHB1 master.

The SDRAM controller uses 3 pipe queues to improve the SDRAM command and data bus efficiency. The request in queue0 is the SDRAM active data access request. Simultaneous, the requests in queue1 can request the controller to issue the ACTIVE or PRECHARGE command to reduce the access latency for the later command. The queue1 also can issue the READ or WRITE command to close the SDRAM command when advance pipe queue

The SDRAM refresh rate is programmable. The Refresh and Power-on control module generate the refresh request signal and SDRAM power on sequence. The SDRAM controller also supports software reset, SDRAM self-refresh and auto power down function.

6.5.2 Features

- Support DDR, DDR2 and LPDDR SDRAM
- Clock speed up to 150 MHz
- Support 16-bit data bus width
- Support two chip selects
- Support total memory size up to 256M bytes (each chip select for 128M bytes)

6.6 External Bus Interface

6.6.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.6.2 Features,

- Supports up to three memory banks.
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports address bus and data bus separate mode

6.7 General Purpose I/O

6.7.1 Overview

This chip has up to 104 General-Purpose I/O (GPIO) pins and can be shared with other function pins depending on the chip configuration. These 104 pins are arranged in 7 ports named as PA, PB, PC, PD, PE, PF and PG. PA, PC, PD and PG has 16 pins on port. PB has 14 pins on port. PE and PF has 13 pins on port. Each of the 104 I/O pins is independent and can be easily configured by user to meet various system configurations and design requirements.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output or Open-drain output. After reset, all 104 I/O pins are configured in General-Purpose I/O Input mode. Each I/O pin has a very weakly individual pull-up resistor which is about 50K for VDD is from 5.5 V to 1.65 V.

6.7.2 Features,

- Three I/O modes:
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Enabling the pin interrupt function will also enable the wake-up function

6.8 Peripheral DMA Controller

6.8.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 20 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.8.2 Features,

- Supports 2 PDMA controller, PDMA0 and PDMA1
- Supports 10 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, SPI, I2C and Timer request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function from channel 0 to channel 9
- Supports stride function from channel 0 to channel 5

6.9 Timer Controller (TMR)

6.9.1 Overview

The timer controller includes six 32-bit timers, Timer0 ~ Timer5, allowing user to easily implement a timer control applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.9.2 Features,

- Six sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent Clock Source for each Timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function to count input event from pin TMx_ECNT (x = 0~5)
- Supports toggle output to pin TMx_TGL (x = 0~5)
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports event capture from external pin TMx_EXT (x = 0~5) for interval measurement
- Supports event capture from RTC 1Hz signal for RTC clock calibration
- Supports event capture from external pin TMx_EXT (x = 0~5) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports time-out interrupt or capture interrupt to trigger ADC and PDMA.
- Supports Inter-Timer trigger that Timer 0 can trigger Timer 1, Timer 2 can trigger Timer 3, and Timer4 can trigger Timer5.

6.10 Pulse Width Modulation (PWM)

6.10.1 Overview

This chip has 2 PWM controllers, PWMAPWM0 and PWMBPWM1. Each PWM controller has 4 independent PWM outputs.

PWMAPWM0 has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators. PWMBPWM1 has 4 independent PWM outputs, CH4~CH7, or as 2 complementary PWM pairs, (CH4, CH5), (CH6, CH7) with 2 programmable dead-zone generators. Each PWM pair has one prescaler, one clock divider, two clock selectors, two 16-bit PWM counters, two 16-bit comparators, and one Dead-Zone generator. They are all driven by APB system clock (PCLK) in chip. Each PWM channel can be used as a timer and issue interrupt independently.

Two channels PWM Timers in one pair share the same prescaler. The Clock divider provides each PWM channel with 5 divided clock sources (1, 1/2, 1/4, 1/8, 1/16). Each channel receives its own clock signal from clock divider which receives clock from 8-bit prescaler. The 16-bit down-counter in each channel receive clock signal from clock selector and can be used to handle one PWM period. The 16-bit comparator compares PWM counter value with threshold value in register CMR (PWM_CMR[15:0]) loaded previously to generate PWM duty cycle. The clock signal from clock divider is called PWM clock. Dead-Zone generator utilize PWM clock as clock source. Once Dead-Zone generator is enabled, two outputs of the corresponding PWM channel pair will be replaced by the output of Dead-Zone generator. The Dead-Zone generator is used to control off-chip power device.

To prevent PWM driving output pin with unsteady waveform, 16-bit down-counter and 16-bit comparator are implemented with double buffering feature. User can feel free to write data to counter buffer register and comparator buffer register without generating glitch. When 16-bit down-counter reaches zero, the interrupt request is generated to inform CPU that time is up. When counter reaches zero, if counter is set as periodic mode, it is reloaded automatically and start to generate next cycle. User can set PWM counter as one-shot mode instead of periodic mode. If counter is set as one-shot mode, counter will stop and generate one interrupt request when it reaches zero. The value of comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

6.10.2 Features,

- PWM channels with a 16-bit down counter and an interrupt each
- 4 complementary PWM pairs, (CH0, CH1), (CH2, CH3), (CH4, CH5), (CH6, CH7), with a programmable dead-zone generator each
- Internal 8-bit prescaler and a clock divider for each PWM paired channel
- Independent clock source selection for each PWM channel
- Internal 16-bit down counter and 16-bit comparator for each independent PWM channel
- PWM down-counter supports One-shot or Periodic mode

6.11 Watchdog Timer

6.11.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.11.2 Features,

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24 ~ 220) and the time-out interval is 0.48828125ms ~ 32s if WDT_CLK = 32.768 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting WDTON (SYS_PWRON [3])
- Supports WDT time-out wake-up function only if WDT clock source is selected as LXT.

6.12 Windowed Watchdog Timer (WWDT)

6.12.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.12.2 Features,

- 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible.
- Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter.

6.13 Real Time Clock (RTC)

6.13.1 Overview

The Real Time Clock (RTC) controller provides the real time clock and calendar information. The clock source of RTC controller is from an external 32.768 kHz low-speed crystal which connected at pins X32_IN and X32_OUT (refer to pin Description). The RTC controller provides the real time clock (hour, minute, second) in RTC_TIME (RTC Time Loading Register) as well as calendar information (year, month, day) in RTC_CAL (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in RTC_TALM (RTC Time Alarm Register) and alarm calendar in RTC_CALM (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD (Binary Coded Decimal) format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by RTC_TICK (RTC_TICK[2:0] Time Tick Register). When real time and calendar message in RTC_TIME and RTC_CAL are equal to alarm time and calendar settings in RTC_TALM and RTC_CALM, the ALMIF (RTC_INTSTS [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the ALMIEN (RTC_INTEN [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the corresponding interrupt enable bit (ALMIEN or TICKIEN) is set to 1 before chip enters Idle or Power-down mode.

Real Time Clock (RTC) block can operate with independent power supply (RTC_VDD) while the system power is off.

6.13.2 Features,

- Supports real time counter and calendar counter for RTC time and calendar check.
- Supports time (hour, minute, second) and calendar (year, month, day) alarm and alarm mask settings.
- Selectable 12-hour or 24-hour time scale.
- Supports Leap Year indication.
- Supports Day of the Week counter.
- Supports frequency compensation mechanism for 32.768 kHz clock source.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm match interrupt.
- Supports chip wake-up from Idle or Power-down mode while alarm or relative alarm interrupt is generated.
- Supports 64 bytes spare registers to store user's important information.
- Supports power on/off control mechanism to control system core power.

6.14 UART Interface Controller (UART)

6.14.1 Overview

The chip provides ten channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and, RS-485 function modes and auto-baud rate measuring function.

6.14.2 Features,

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART1 /UART2 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
- Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

6.15 Smart Card Host Interface

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features,

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Reset (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.16 I²C Serial Interface Controller

6.16.1 Overview

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are four sets of I2C controllers which support Power-down wake-up function.

6.16.2 Features,

- The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I2C bus include:
- Supports up to three I2C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports setup/hold time programmable

6.17 Serial Peripheral Interface (SPI)

6.17.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer.

6.17.2 Features,

- Up to two sets of SPI controllers
- Supports Master or Slave mode operation
- Master mode up to 100 MHz and Slave mode up to 30 MHz (when chip works at VDD = 2.7~3.6V)
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 4-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.18 Quad Serial Peripheral Interface (QSPI)

6.18.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.18.2 Features,

- Supports Master or Slave mode operation
- Master mode up to 100 MHz and Slave mode up to 100 MHz (when chip works at VDD = 2.7~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.19 I²S Controller (I²S)

6.19.1 Overview

The I2S controller consists of I2S and PCM protocols to interface with external audio CODEC. The I2S and PCM interface supports 8, 16, 18, 20 and 24-bit left/right precision in record and playback. When operating in 18/20/24-bit precision, each left/right-channel sample is stored in a 32-bit word. Each left/right-channel sample has 24/20/18 MSB bits of valid data and other LSB bits are the padding zeros. When operating in 16-bit precision, right-channel sample is stored in MSB of a 32-bit word and left-channel sample is stored in LSB of a 32-bit word.

The following are the property of the DMA.

- When 16-bit precision, the DMA always 8-beat incrementing burst (FIFO_TH = 0) or 4-beat incrementing burst (FIFO_TH = 1).
- When 24/20/18-bit precision, the DMA always 16-beat incrementing burst (FIFO_TH = 0) or 8-beat incrementing burst (FIFO_TH = 1).
- Always bus lock when 4-beat or 8-beat or 16-beat incrementing burst.
- When reach eighth, quarter, middle and end address of destination address, a DMA_IRQ is triggered to CPU automatically.

An AHB master port and an AHB slave port are offered in I2S controller.

6.19.2 Features,

- Support I2S interface record and playback
  - Left/right channel
  - 8, 16, 20, 24-bit data precision
  - Mater and slave mode
- Support PCM interface record and playback
  - Two slots
  - 8, 16, 20, 24-bit data precision
  - Master mode
- Use DMA to playback and record data, with interrupt
- Support two addresses for left/right channel data and different slots

6.20 Ethernet MAC Controller (EMAC)

6.20.1 Overview

This chip provides 2 Ethernet MAC Controller (EMAC) for Network application.

The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for recognizing Ethernet MAC addresses; Transmit-FIFO, Receive-FIFO, TX/RX state machine controller, time stamping engine for IEEE 1588, Magic Packet parsing engine and status controller.

The EMAC supports RMII (Reduced MII) interface to connect with external Ethernet PHY.

6.20.2 Features,

- Supports IEEE Std. 802.3 CSMA/CD protocol
- Supports Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol
- Supports both half and full duplex for 10 Mbps or 100 Mbps operation
- Supports RMII interface
- Supports MII Management function to control external Ethernet PHY
- Supports pause and remote pause function for flow control
- Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception
- Supports 16 entries CAM function for Ethernet MAC address recognition
- Supports Magic Packet recognition to wake system up from power-down mode
- Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
- Supports DMA function

6.21 High Speed USB 2.0 Device Controller (HSUSBD)

6.21.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISOCHRONOUS. The USB device controller has a built-in DMA to relieve the load of CPU.

6.21.2 Features,

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint — Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4096 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

6.22 USB 2.0 Host Controller (USBH)

6.22.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

6.22.2 Features,

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports two USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

6.23 Controller Area Network (CAN)

6.23.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.23.2 Features,

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.24 Flash Memory Interface (FMI)

6.24.1 Overview

The Flash Memory Interface (FMI) in this chip has DMA unit and FMI unit. The DMA unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory (ex. SDRAM) and shared buffer (128 bytes), and the FMI unit control the interface of SD0/eMMC0 or NAND Flash. The interface controller can support SD0/eMMC0 and NAND-type Flash and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.24.2 Features,

- Supports single DMA channel and address in non-word boundary.
- Supports hardware Scatter-Gather function.
- Supports 128Bytes shared buffer for data exchange between system memory and Flash device. (Separate into two 64 bytes ping-pong FIFO).
- Supports SD0/eMMC0 Flash device.
- Supports SLC and MLC NAND type Flash.
- Adjustable NAND page sizes. (2048B+spare area, 4096B+spare area and 8192B+spare area).
- Supports up to 8bit/12bit/24bit hardware ECC calculation circuit to protect data communication.
- Supports programmable NAND timing cycle

6.25 Secure Digital Host Controller (SDH)

6.25.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SD Host Controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.25.2 Features,

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function..
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.26 Cryptographic Accelerator (CRYPTO)

6.26.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, SHA, HMAC, RSA and ECC algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512 and corresponding HMAC algorithms.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

The RSA accelerator is an implementation fully compliant with 1024 and 2048 bit RSA cryptography.

6.26.2 Features,

- PRNG
  - Supports 64 bits, 128 bits , 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB , CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512
- HMAC
  - Supports FIPS NIST 180, 180-2
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512
- ECC
  - Supports both prime field GF(p) and binary filed GF(2m)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2m)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)
- RSA

- Supports both encryption and decryption
- Supports up to 2048 bits

6.27 Capture Sensor Interface Controller (CAP)

6.27.1 Overview

The Image Capture Interface is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then FIFO output them into frame buffer.

6.27.2 Features,

- 8-bit RGB565 sensor
- 8-bit YUV422 sensor
- Supports CCIR601 YCbCr color range scale to full YUV color range
- Supports 4 packaging format for packet data output: YUYV, Y only, RGB565, RGB555
- Supports YUV422 planar data output
- Supports the CROP function to crop input image to the required size for digital application.
- Supports the down scaling function to scale input image to the required size for digital application.
- Supports frame rate control
- Supports field detection and even/odd field skip mechanism
- Supports packet output dual buffer control through hardware buffer controller
- Supports negative/sepia/posterization color effect

6.28 Analog to Digitial Converter (ADC)

6.28.1 Overview

The NUC980 series contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with 9 input channels.

6.28.2 Features,

- Resolution: 12-bit resolution
- DNL: +/-1.5 LSB, INL: +/-3 LSB
- Data Rate up to 200kSPS
- Analog Input Range: V_{REF} to AGND, can be rail-to-rail
- Analog Supply: 2.7-3.6V
- Digital Supply: 1.2V
- 9 Single-Ended analog inputs
- Auto Power Down
- Low Power Consumption: 2170uW (at 200k SPS), < 1uA

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
V_{VDD12}–V_{VSS}	Core DC Power Supply	-0.3	+1.5	V
V_{VDD33}–V_{VSS}	I/O DC Power Supply	-0.3	+4.6	V
MV_{DD} – $MV_{SS\ (1)}$	I/O DC Power Supply for SDR Type SDRAM	-0.3	+4.6	V
MV_{DD} - $MV_{VSS(2)}$	I/O DC Power Supply for DDR,DDR2 Type SDRAM	-0.3	+2.3	V
V_{IN}	Input Voltage	V_{VSS}-0.3	+5	V
T_A	Operating Temperature	-40	+85	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into CORE_VDD	-	200	mA
I_{SS}	Maximum Current out of CORE_VSS	-	200	mA
I_{IO}	Maximum Current sunk by a I/O pin	-	20	mA
	Maximum Current sourced by a I/O pin	-	30	mA
	Maximum Current sunk by total I/O pins	-	200	mA
	Maximum Current sourced by total I/O pins	-	200	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

7.2.1 NUC980 Series DC Electrical Characteristics

(VDD33-VSS=3.3V, TA = 25°C, FOSC = 12 MHz unless otherwise specified.)

Parameter	Sym.	Specification				Test Conditions
		MIN.	TYP.	Max.	Unit	
Core Operation voltage	V_{DD12}	1.14	1.2	1.32	V	
I/O Operation Voltage	V_{DD33}	2.97	3.3	3.63	V	
Memory I/O Operation Voltage for DDR or DDR2	$MV_{DD\ (1)}$	1.70	1.8	1.90	V	
Memory I/O Operation Voltage for SDR Type SDRAM	$MV_{DD\ (2)}$	2.97	3.3	3.63	V	
Battery Operation Voltage	V_{BAT33}	TBD	3.3	3.63	V	
USB Operation Voltage (1)	V_{USB0_VDD12} V_{USB1_VDD12}	1.14	1.2	1.32	V	
USB Operation Voltage (2)	V_{USB0_VDD33} V_{USB1_VDD33}	2.97	3.3	3.63	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD33}	2.97	3.3	3.63	V	
Analog Reference Voltage	AVref	0		AV_{DD33}	V	
Current Consumption of Normal Operating Mode 1	I_{VDD12}		150		mA	V_{DD12} = 1.2V MV_{DD} = 1.8V V_{DD33} = 3.3V TA = 25°C, F_{OSC} = 12 MHz Frequency of CPUCLK/DDR_CLK is 300/150 MHz. All IPs on, all GPIO are input with pull-up.
	I_{MVDD_1}		50		mA	
	$I_{USB0\_VDD12\_1}$		7.5		mA	
	$I_{USB1\_VDD12\_1}$		7.5		mA	
	$I_{USB0\_VDD33\_1}$		35		mA	
	$I_{USB1\_VDD33\_1}$		35		mA	
	I_{VBAT33_1}		100		uA	
Current Consumption of Normal Operating Mode 2	I_{VDD12}		165		mA	V_{DD12} = 1.2V MV_{DD} = 1.8V V_{DD33} = 3.3V TA = 25°C, F_{OSC} = 12 MHz Frequency of CPUCLK/DDR_CLK is 264/132 MHz. All IPs on, all GPIO are input with pull-up.
	I_{MVDD_2}		45		mA	
	$I_{USB0\_VDD12\_2}$		7.5		mA	
	$I_{USB1\_VDD12\_2}$		7.5		mA	
	$I_{USB0\_VDD33\_2}$		35		mA	
	$I_{USB1\_VDD33\_2}$		35		mA	
	I_{VBAT33_2}		100		uA	

Parameter	Sym.	Specification				Test Conditions
		MIN.	TYP.	Max.	Unit	
Current Consumption of Power Down Mode	I_{STDBY_VDD12}		3		mA	V_{DD12} = 1.2V
	I_{STDBY_MVDD}		6		mA	MV_{DD} = 1.8V
	I_{STDBY_VDD33}		5		µA	V_{DD33} = 3.3V
	$I_{STDBY\_USB0\_VDD33}$		0		µA	V_{USB0_VDD33} = 3.3V
	$I_{STDBY\_USB1\_VDD33}$		0		µA	V_{USB1_VDD33} = 3.3V
	$I_{STDBY\_USB0\_VDD12}$		2.5		µA	V_{USB0_VDD12} = 1.2V
	$I_{STDBY\_USB1\_VDD12}$		2.5		µA	V_{USB1_VDD12} = 1.2V
	I_{STDBY_AVDD33}		25		µA	AV_{DD33} = 3.3V
	I_{STDBY_VBAT33}		TBD		µA	V_{BAT33} = 3.3V
System Power Off & RTC V_{BAT33} Power only	I_{VBAT33}		TBD		uA	

7.2.2 NUC980 Series GPIO Characteristics

(V_{DD33}-V_{SS}=3.3 V, TA = 25°C, F_{OSC} = 12 MHz unless otherwise specified.)

Input Leakage Current PA, PB, PC, PD, PE, PF, PG	I_{LK1}	-10	-	10	μA	V_{VDD33} = 3.63V 0V < V_{IN} < V_{VDD33}
Input Low Voltage PA, PB, PC, PD, PE, PF, PG (TTL input)	V_{IL1}	-	-	0.8	V	V_{DD33} = 3.63V
Input High Voltage PA, PB, PC, PD, PE, PF, PG (TTL input)	V_{IH1}	2.0	-	-	V	V_{DD33} = 3.63V
Input Low Voltage PA, PB, PC, PD, PE, PF, PG, (Schmitt input)	V_{IL2}			0.3*V_{DD33}	V	
Input High Voltage PA, PB, PC, PD, PE, PF, PG, (Schmitt input)	V_{IH2}	0.7*V_{DD33}			V	
Hysteresis voltage PA, PB, PC, PD, PE, PF, PG (Schmitt input)	V_{HY}		0.2*V_{DD33}		V	
Source Current PA, PB, PC, PD, PE, PF, PG, (Push-pull Mode)	I_{SR21}		8		mA	V_{DD33} = 3.63V V_{IN}=V_{DD33}-0.4
Sink Current PA, PB, PC, PD, PE, PF, PG (Push-pull Mode)	I_{SK1}		8		mA	V_{DD33} = 3.63V V_{IN}=V_{SS}+0.4
Input Pull-up Resistance PA, PB, PC, PD, PE, PF, PG, HDS	R_{PU}	-	-	82	kΩ	V_{DD33}=3.63V, apply GPIO pin Vin= 0V and measure the input current Reverse the current to Resistor value, R=V/I
Input Pull-down Resistance PA, PB, PC, PD, PE, PF, PG	R_{PD}	-	-	91	kΩ	V_{DD33}=3.63V, apply GPIO pin Vin= 3.63V and measure the input current Reverse the current to Resistor value, R=V/I

7.3 AC Electrical Characteristics

7.3.1 External 12MHz High Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.97	3.3	3.63	V	$V_{HXT} = V_{DD33}$
T_A	Temperature	-40	-	85	°C	-
f_{HXT}	Clock Frequency	-	12	-	MHz	-
I_{HXT}	Operating Current	-	0.8	-	mA	TA=25°C, AV_{DD33}=3.3V

Note: Guaranteed by characterization results, not tested in production.

7.3.1.1 Typical Crystal Application Circuits

Crystal	ESR (ohm)	C1, C2
12 MHz	< 50	15 pf

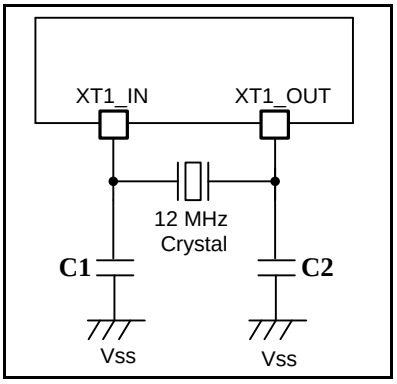


Figure 7.3-1 Typical HXT Crystal Application Circuit

7.3.2 External 32.768 kHz Low Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{LXT}	Operation Voltage	2.97	3.3	3.63	V	$V_{LXT} = V_{BAT33}$
T_A	Temperature	-40	-	85	°C	-
f_{LXT}	Clock Frequency	-	32.768	-	kHz	-
I_{LXT}	Operating Current		1.6		uA	TA=25°C, V_{BAT33}=3.3V

Note: Guaranteed by characterization results, not tested in production.

7.3.2.1 Typical Crystal Application Circuits

Crystal	C1	C2
32.768 kHz	15 pf	15 pf

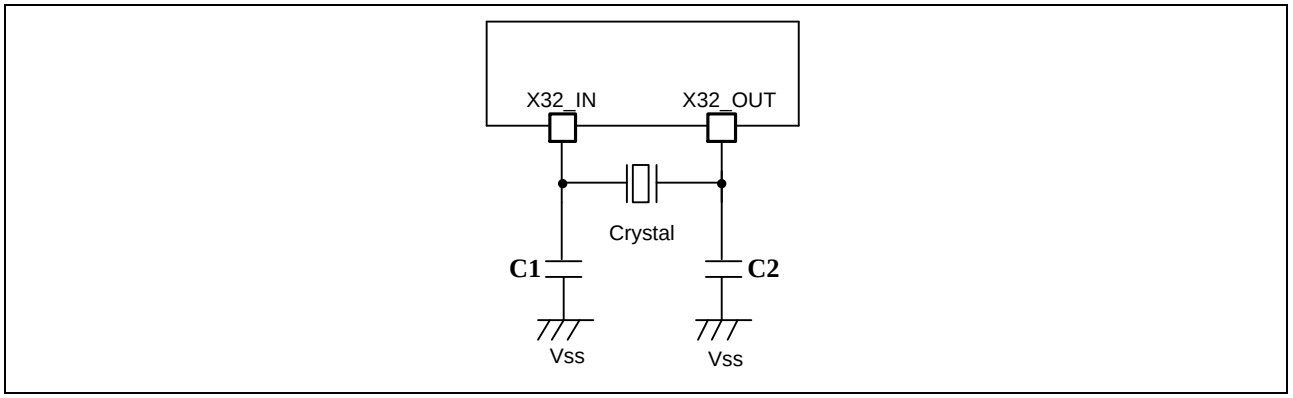


Figure 7.3-2 Typical LXT Crystal Application Circuit

7.3.3 Power Sequence & nRESET Timing

7.3.3.1 Power up Sequence

Power up Sequence & nRESET Timing Case 1

When $T_{VDD33} \geq T_{MVDD} \geq T_{VDD12}$ (the time of delay gap between < 0.5mS is prefer).

Note:

1. The time of delay gap is meaning that timing between T_{VDD33} with T_{MVDD}.
2. If the time of delay gap < 0.5mS will be effective to prevent that transient phenomenon by power-on.

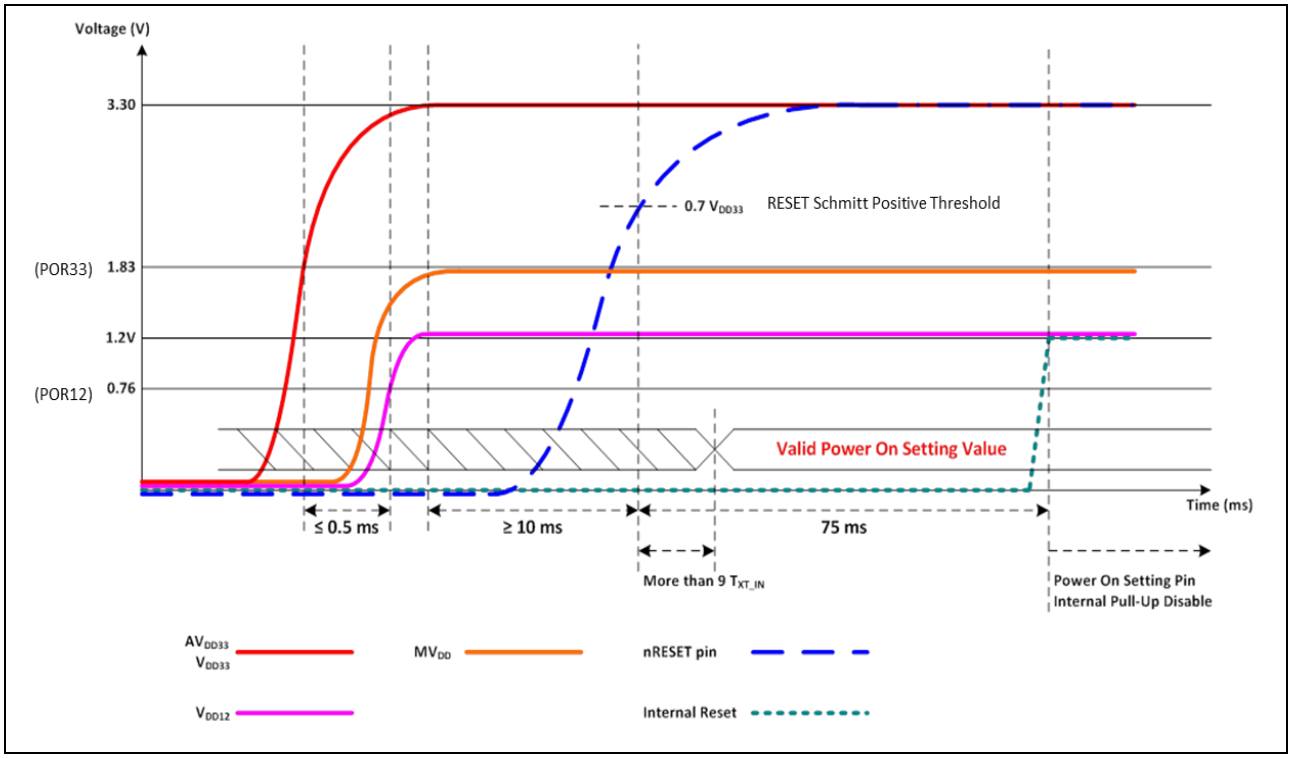


Figure 7.3-3 Power up Sequence & nRESET timing Case 1

Power up Sequence & nRESET Timing Case 2

When $T_{VDD12} \geq T_{MVDD} \geq T_{VDD33}$, it is acceptable as the 錯誤! 找不到參照來源。. (the time of delay gap between < 1mS is prefer)

Note:

1. The time of delay gap is meaning that timing between T_{VDD12} with T_{VDD33}.
2. The time of delay gap < 1mS is prefer although NUC980 has anti-latchup protection.

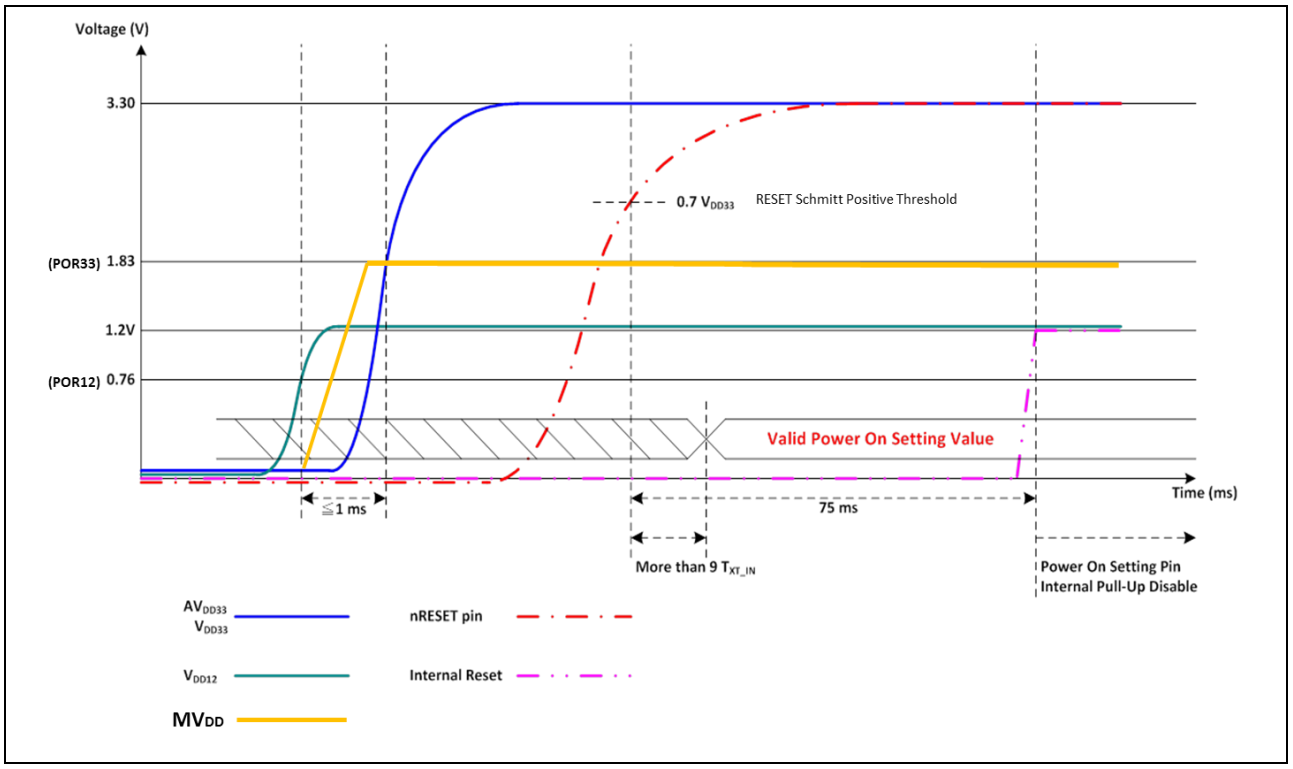


Figure 7.3-4 Power up Sequence & nRESET timing Case 2

7.3.3.2 Power down Sequence,

Power down sequence between AV_{DD33}/V_{DD33}, V_{DD12} and MV_{DD} is don't care.

Note:

1. T_{VDD12} represents V_{DD12} powered time.
2. T_{MVDD} represents MV_{DD} powered time.
3. T_{VDD33} represents V_{DD33}/AV_{DD33} powered.

7.3.4 nRESET PIN characteristics

Symbol	Parameter	Min.	Typ.	Max.	unit	Test Conditions
V_{ILR}	Negative going threshold (Schmitt input), nRESET	-	-	0.3*V_{DD33}	V	V_{DD33} = 3.3V
V_{IHR}	Positive going threshold (Schmitt Input), nRESET	0.7*V_{DD33}	-	-	V	V_{DD33} = 3.3V
R_{RST}	Internal nRESET pin pull up resistor	-	-	84	KΩ	V_{DD33}=3.63V, apply nRESET pin Vin= 3.63V and measure the input current Reverse the current to Resistor value, R=V/I
t_{FR1}	nRESET input filtered time		32		uS	V_{DD33} = 3.3V

Note: Guaranteed by characterization and design results, not tested in production.

7.3.5 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock			12		MHz
f_{PLL_OUT}	PLL multiplier output clock		25		500	MHz
T_S	PLL stable time[*1]		100		200	µs
Jitter	Cycle-to-cycle Jitter[*2]	Peak to peak @ 480M		250		ps
I_{DD12}	Power consumption	V_{DD12}=1.2V@500MHz			3	mA

Note: Guaranteed by characterization and design results, not tested in production.

7.3.6 EBI Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{tACS}	Address Setup Time to EBI_nCS Falling Edge	-	0	-	T_{HCLK}[1]	-
T_{tCOS}	EBI_nCS Setup Time to EBI_nWE or EBI_nOE Falling Edge	-	1	-	T_{HCLK}[1]	-
T_{tACC}	EBI_nWE or EBI_nOE Active Low Time	1	-	32	T_{HCLK}[1]	-
T_{tCOH}	EBI_nCS Hold Time from EBI_nWE or EBI_nOE Rising Edge	0	-	8	T_{HCLK}[1]	-
$T_{SU\_EBI\_RD}$	EBI_DATA Read Setup Time to EBI_nOE Rising Edge	1	-	-	T_{HCLK}[1]	-

Notes:

1. T_{HCLK} is the period of EBI's operating clock.

Table 7.3-1 EBI Characteristics

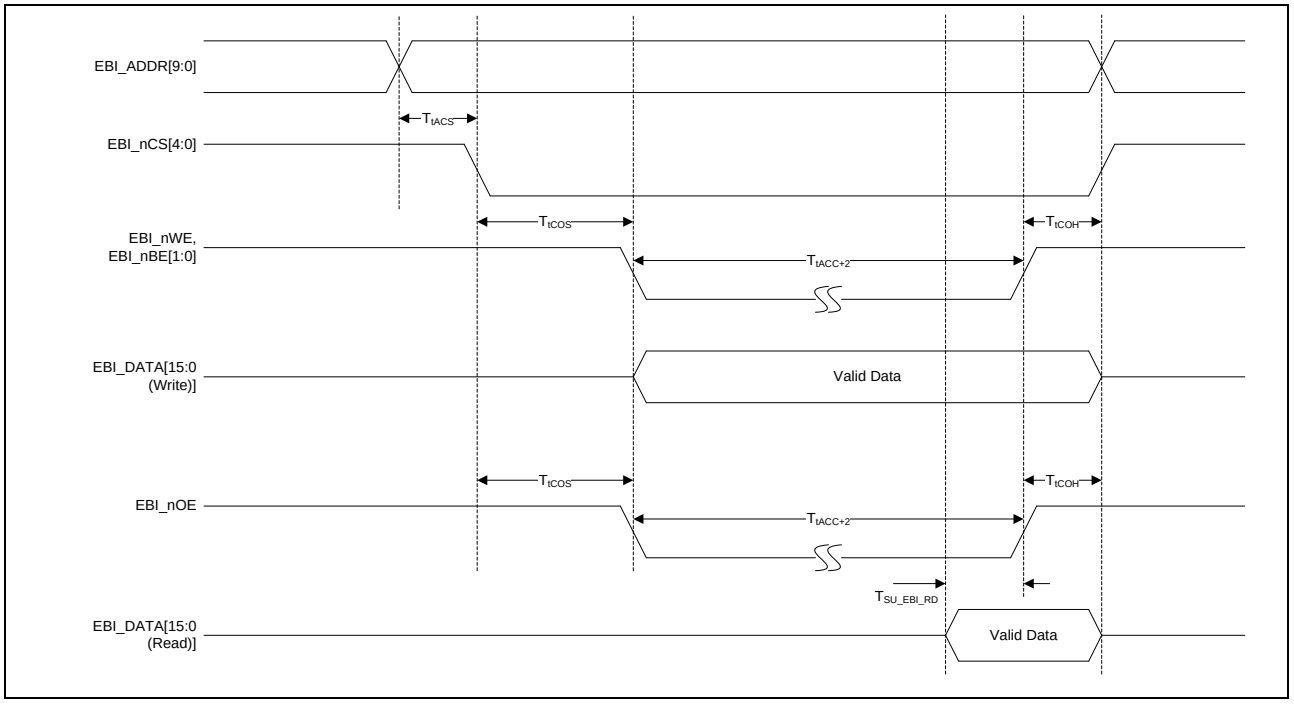


Figure 7.3-5 External Bus Interface Timing Diagram

7.3.7 I2C Interface Timing

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 7.3-2 I^2C Interface Characteristics

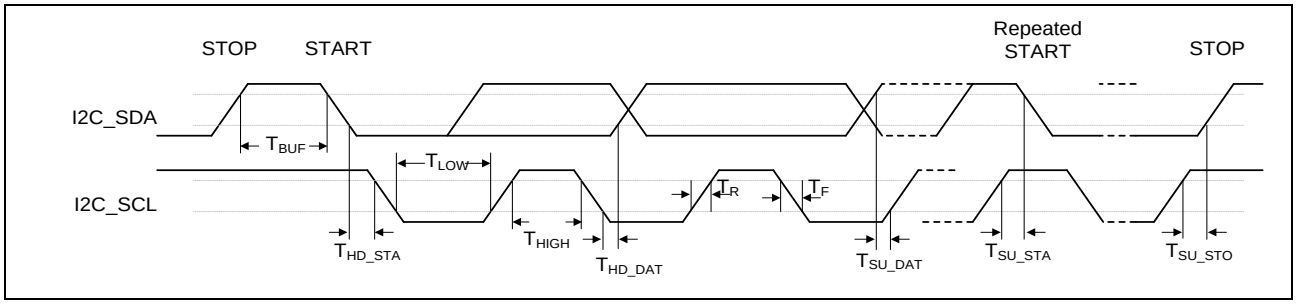


Figure 7.3-6 I2C Interface Timing Diagram

7.3.8 SPI Interface Timing

7.3.8.1 SPI Master Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	100	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	1.8	-	-	ns	
t_{DH}	Data input hold time	3.8	-	-	ns	
t_V	Data output valid time	-	-	1.1	ns	
Note:						

Table 7.3-3 SPI Master Mode Characteristics

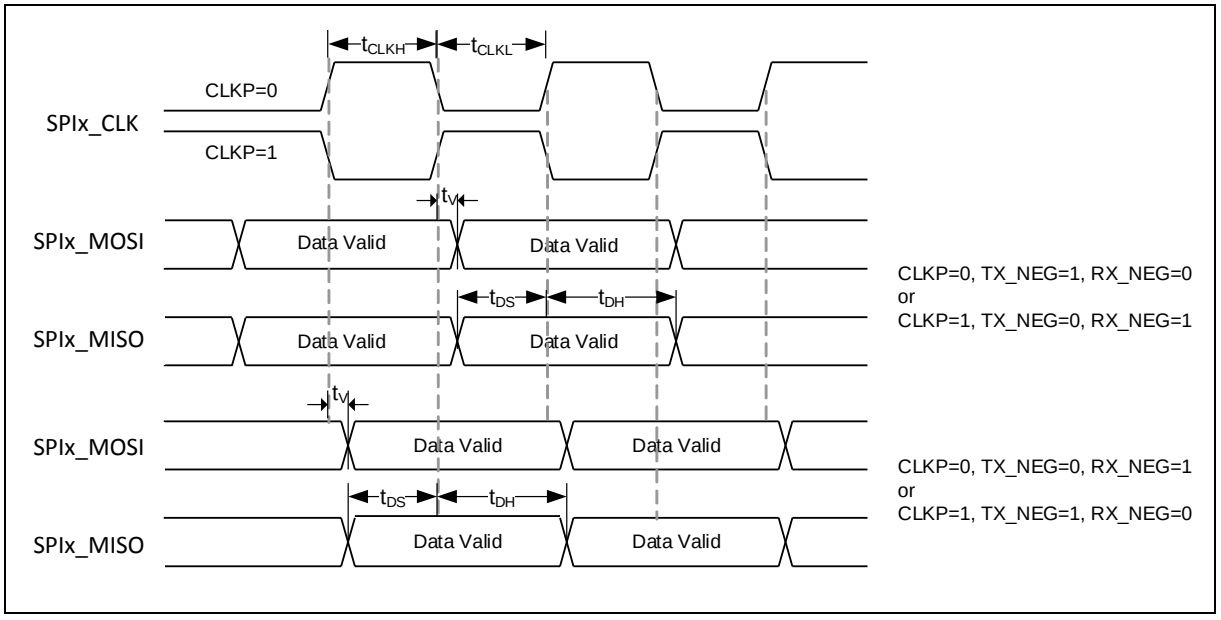


Figure 7.3-7 SPI Master Mode Timing Diagram

7.3.8.2 SPI Slave Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	30	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	1	-	-	ns	
t_{DH}	Data input hold time	3	-	-	ns	
t_V	Data output valid time	-	-	10	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
Note:						

Table 7.3-4 SPI Slave Mode Characteristics

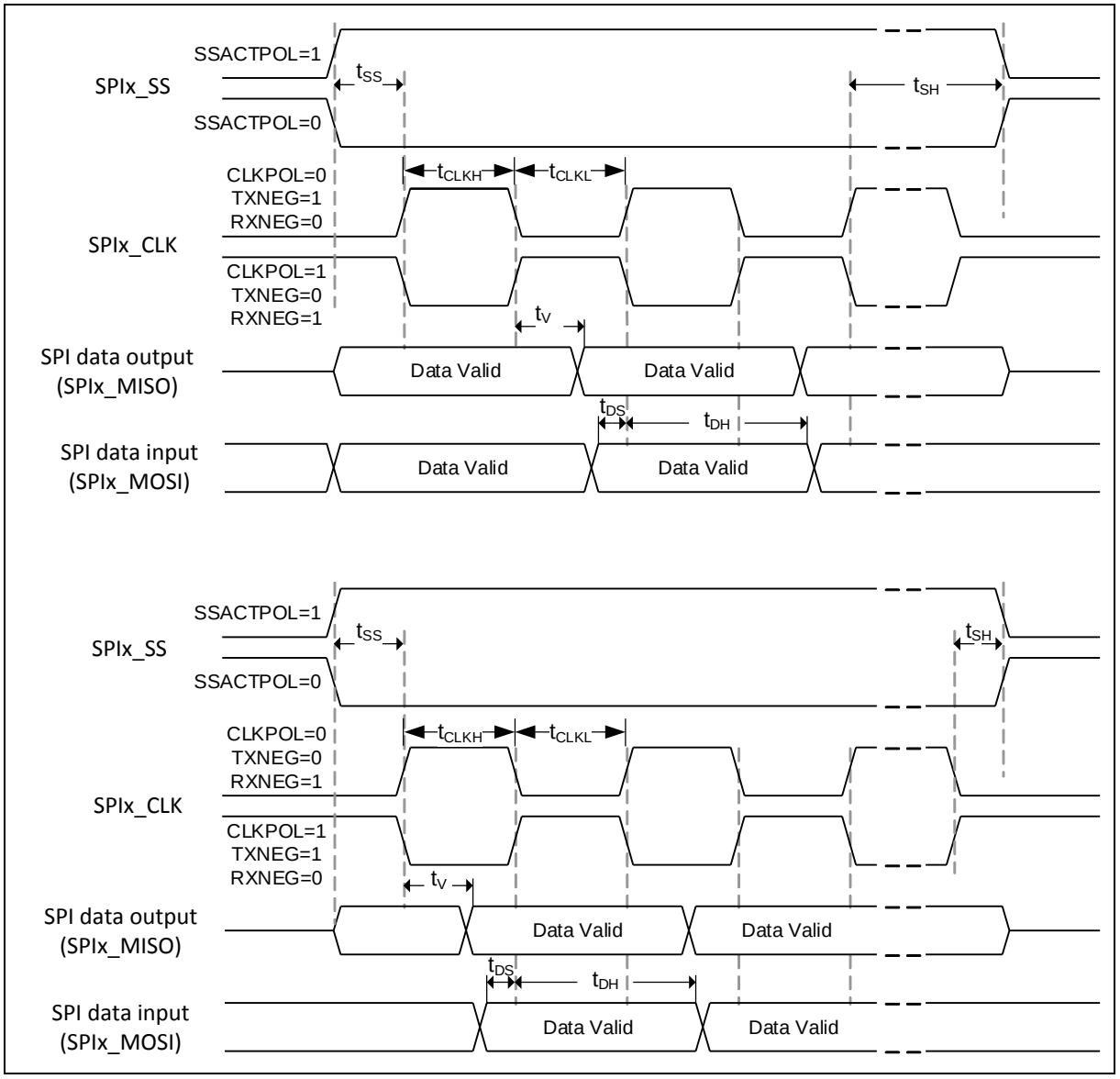


Figure 7.3-8 SPI Slave Mode Timing Diagram

7.3.9 QSPI Interface Timing

7.3.9.1 QSPI Master Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	100	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	1.8	-	-	ns	
t_{DH}	Data input hold time	3.8	-	-	ns	
t_V	Data output valid time	-	-	1.5	ns	
Note:						

Table 7.3-5 QSPI Master Mode Characteristics

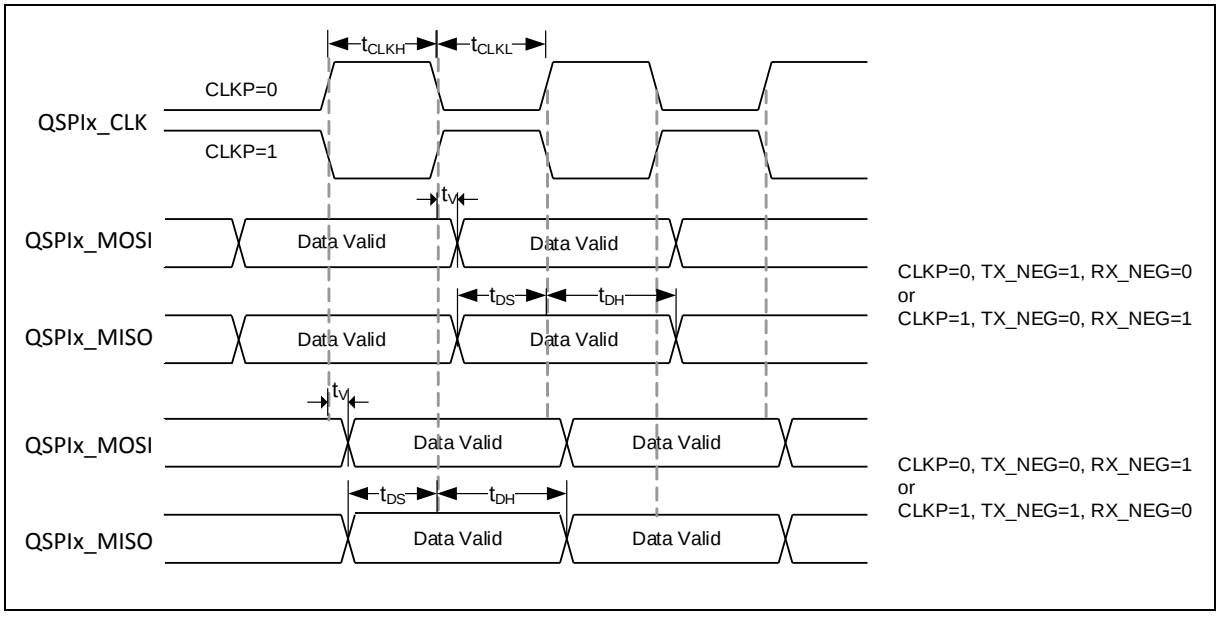


Figure 7.3-9 QSPI Master Mode Timing Diagram

7.3.9.2 QSPI Slave Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	30	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	2.1	-	-	ns	
t_{DH}	Data input hold time	4.1	-	-	ns	
t_V	Data output valid time	-	-	11.5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
Note:						

Table 7.3-6 QSPI Slave Mode Characteristics

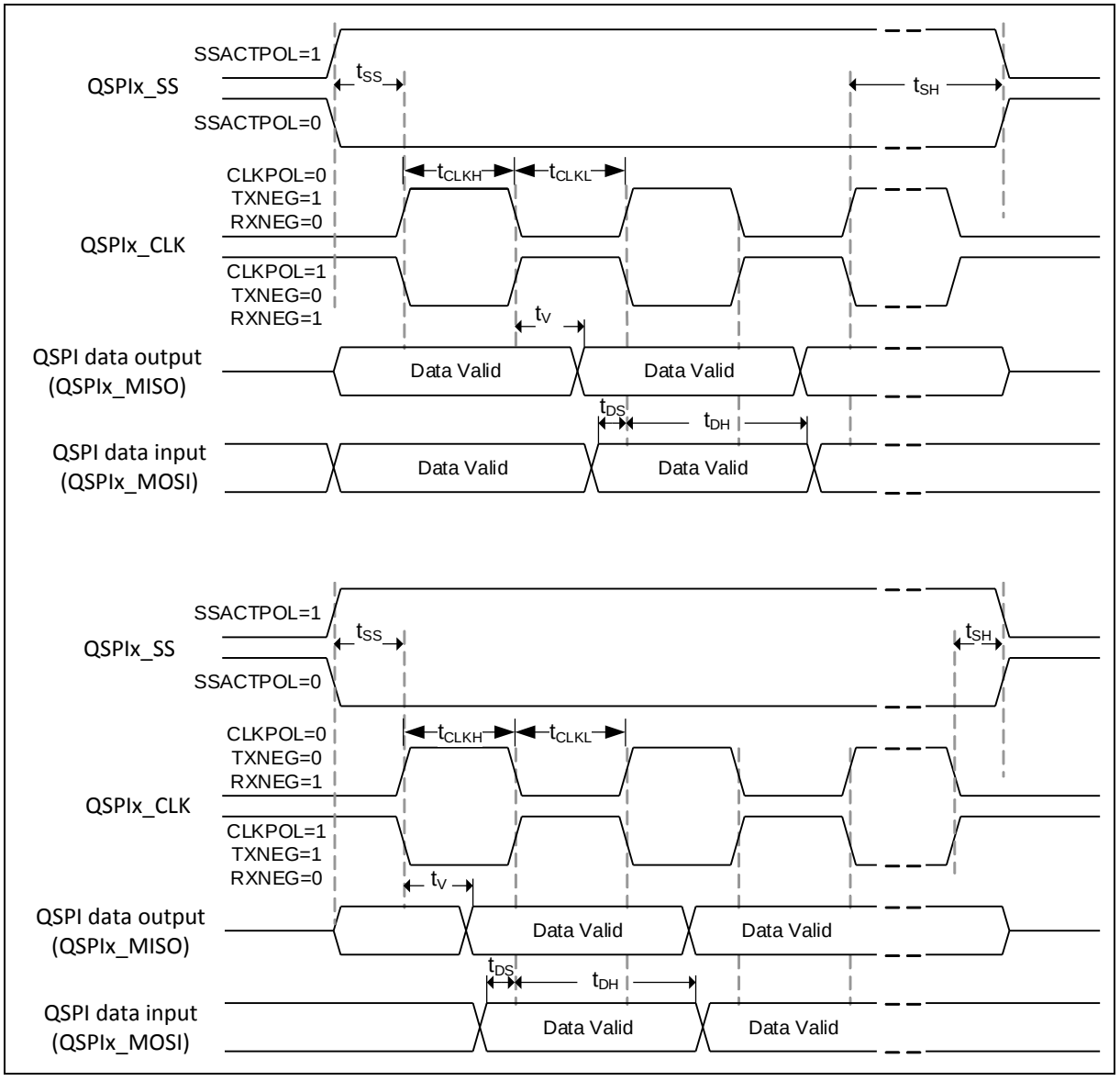


Figure 7.3-10 QSPI Slave Mode Timing Diagram

7.3.10 I2S Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_I2S\_BITCLK}$	I2S_BITCLK Period	50	-	-	ns	-
$T_{H\_I2S\_BITCLK}$	I2S_BITCLK High Time	25	-	-	ns	-
$T_{L\_I2S\_BITCLK}$	I2S_BITCLK Low Time	25	-	-	ns	-
$T_{DLY\_I2S\_DO}$	I2S_BITCLK Rising to Valid I2S_WS or I2S_DATAO Delay	-	-	6	ns	-
$T_{HD\_I2S\_DO}$	I2S_WS or I2S_DATAO Hold Time from I2S_BITCLK Rising	1	-	-	ns	
$T_{SU\_I2S\_DI}$	I2S_DATAI Setup Time to I2S_BITCLK Rising	5	-	-	ns	-
$T_{HD\_I2S\_DI}$	I2S_DATAI Hold Time from I2S_BITCLK Rising	3	-	-	ns	-

Table 7.3-7 I^2S Interface Characteristics

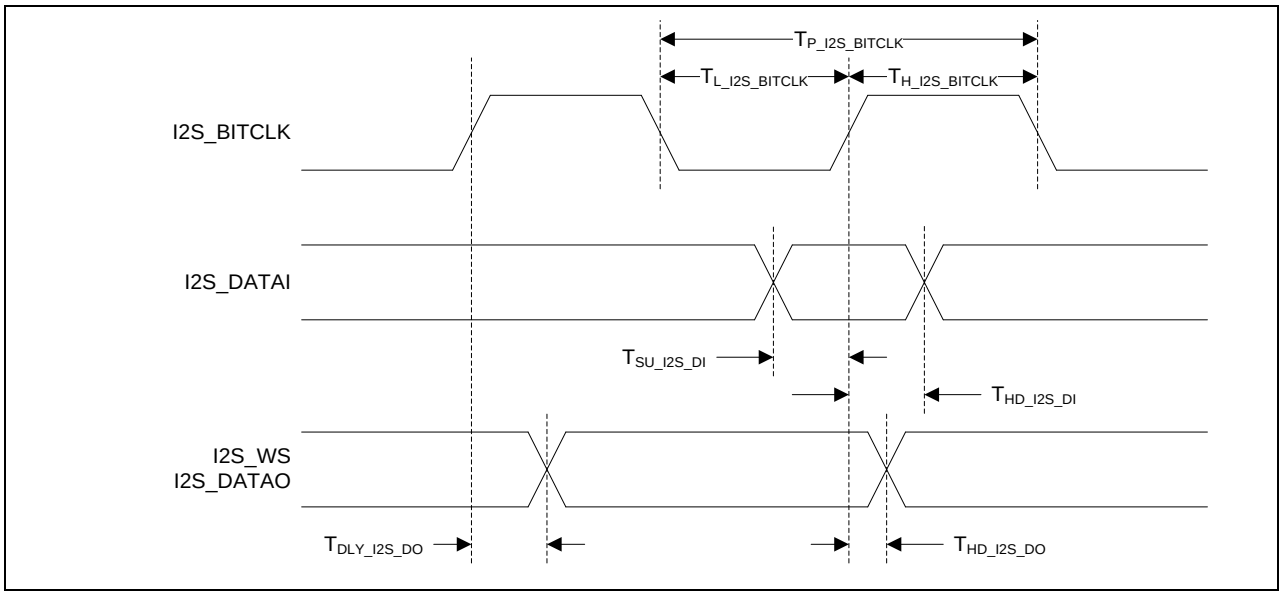


Figure 7.3-11 I2S Interface Timing Diagram

7.3.11 Ethernet Interface Timing

7.3.11.1 RMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY\_RMII\_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	17.3	ns	-
$T_{SU\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

Table 7.3-8 RMII Interface Characteristics

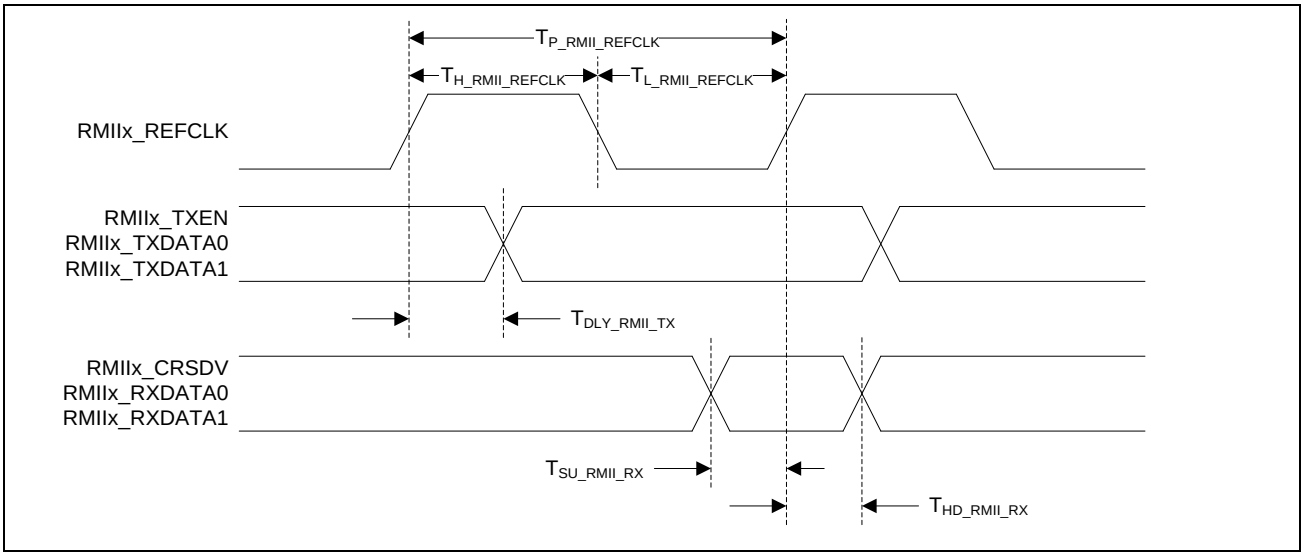


Figure 7.3-12 RMII Interface Timing Diagram

7.3.11.2 Ethernet PHY Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H\_RMII\_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L\_RMII\_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY\_RMII\_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU\_RMII\_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD\_RMII\_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

Table 7.3-9 Ethernet PHY Management Interface Characteristics

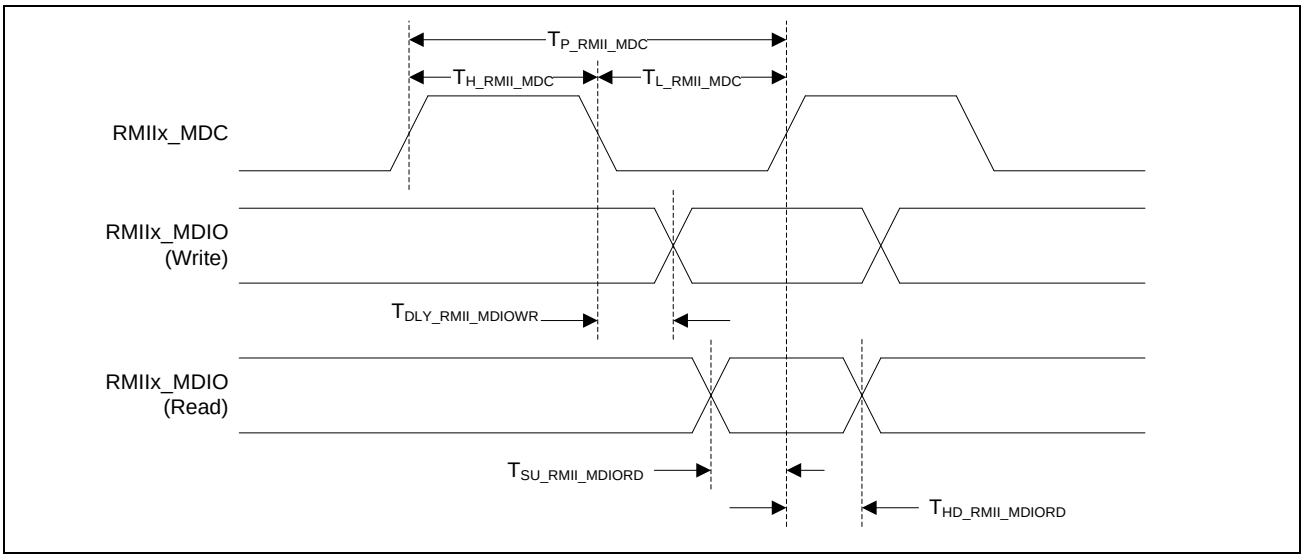


Figure 7.3-13 Ethernet PHY Management Interface Timing Diagram

7.3.12 NAND Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{H\_NAND\_nWE}$	NAND_nWE High Time	-	13.34[1]	-	ns	-
$T_{L\_NAND\_nWE}$	NAND_nWE Low Time	-	40[2]	-	ns	-
$T_{DLY\_DATA\_OUT}$	NAND_nRE Falling to Valid NAND_DATA Delay	-	-	35[3]	ns	-
$T_{HD\_DATA\_OUT}$	NAND_DATA Hold Time from NAND_nRE Rising	-	-	30[3]	ns	-
$T_{SU\_DATA\_IN}$	NAND_DATA Setup Time to NAND_nWE Rising	20[3]	-	-	ns	-
$T_{HD\_DATA\_IN}$	NAND_DATA Hold Time from NAND_nWE Rising	10[3]	-	-	ns	-

Notes:

1. NAND controller operating clock is 150 MHz and HI_WID (FMI_NANDTMCTL[15:8]) is 0x1.
2. NAND controller operating clock is 150 MHz and LO_WID (FMI_NANDTMCTL[7:0]) is 0x5.
3. NAND controller operating clock is 150 MHz.

Table 7.3-10 NAND Interface Characteristics

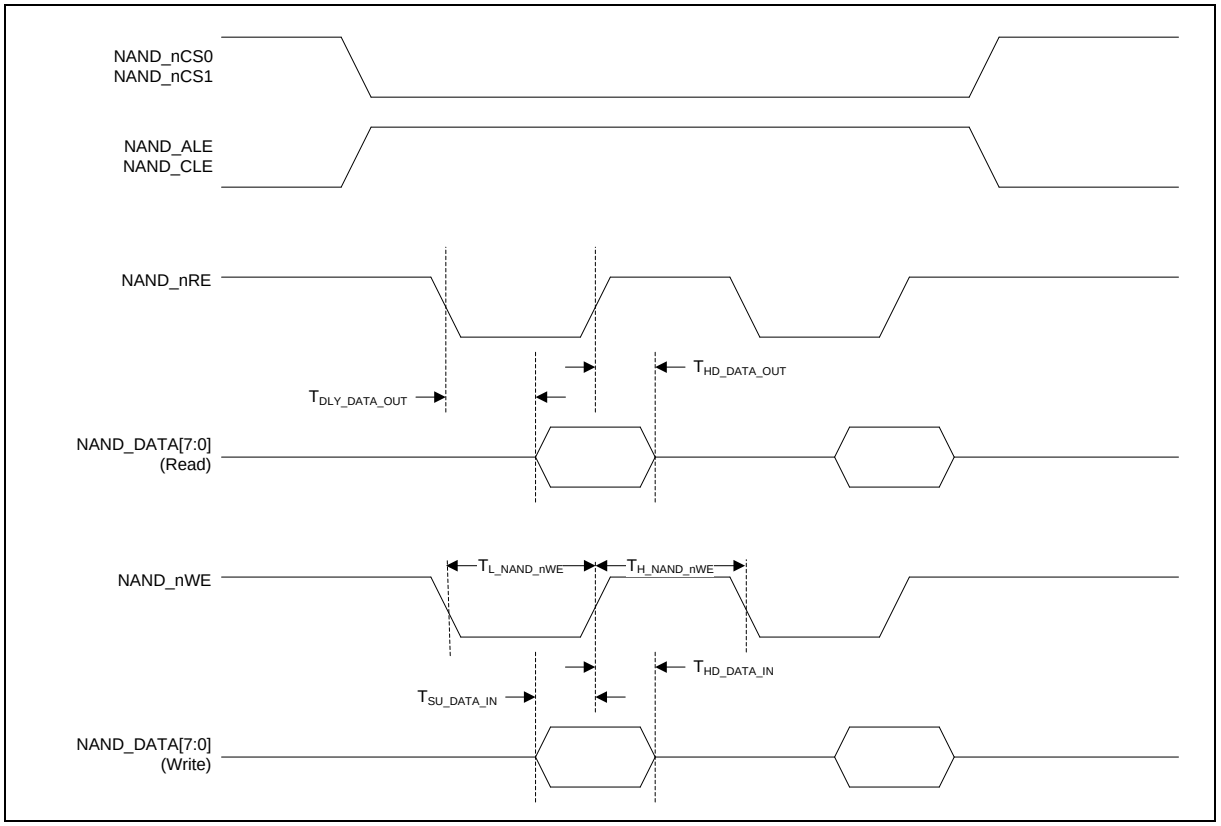


Figure 7.3-14 NAND Interface Timing Diagram

7.3.13 SD Interface Timing

7.3.13.1 Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Table 7.3-11 SD Interface Default Mode Characteristics

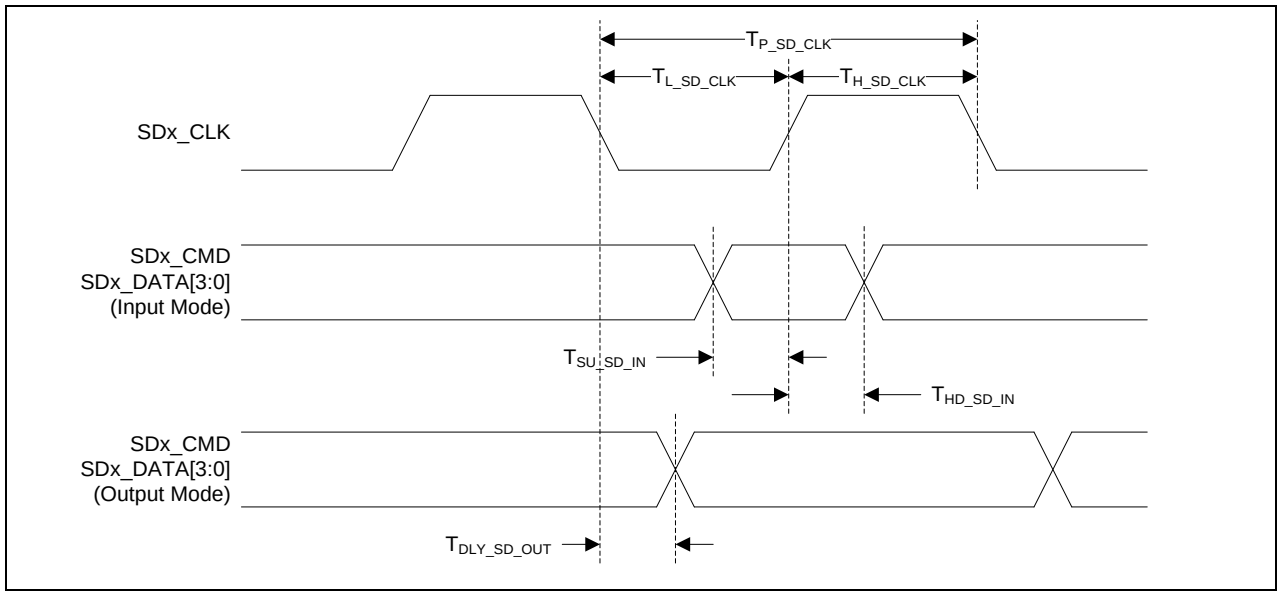


Figure 7.3-15 SD Interface Default Mode Timing Diagram

7.3.13.2 High-Speed Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Table 7.3-12 SD Interface High-Speed Mode Characteristics

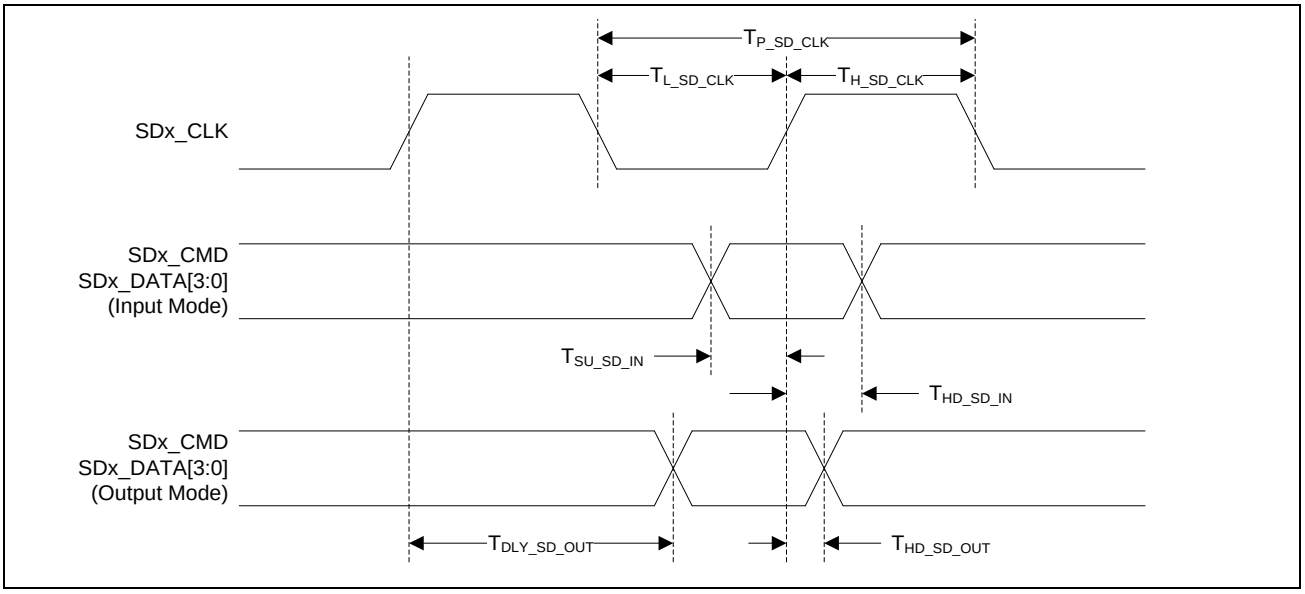


Figure 7.3-16 SD Interface High-Speed Mode Timing Diagram

7.3.14 Capture Sensor Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_VCAP\_PCLK}$	VCAP_PCLK Period	20	-	-	ns	-
$T_{H\_VCAP\_PCLK}$	VCAP_PCLK High Time	-	10.0	-	ns	-
$T_{L\_VCAP\_PCLK}$	VCAP_PCLK Low Time	-	10.0	-	ns	-
$T_{SU\_VCAP\_IN}$	VCAP_HSYNC, VCAP_VSYNC, VCAP_FIELD and VCAP_DATA Setup Time to VCAP_PCLK Rising	4	-	-	ns	-
$T_{HD\_VCAP\_IN}$	VCAP_HSYNC, VCAP_VSYNC, VCAP_FIELD and VCAP_DATA Hold Time from VCAP_PCLK Rising	1	-	-	ns	-

Table 7.3-13 Capture Sensor Interface Characteristics

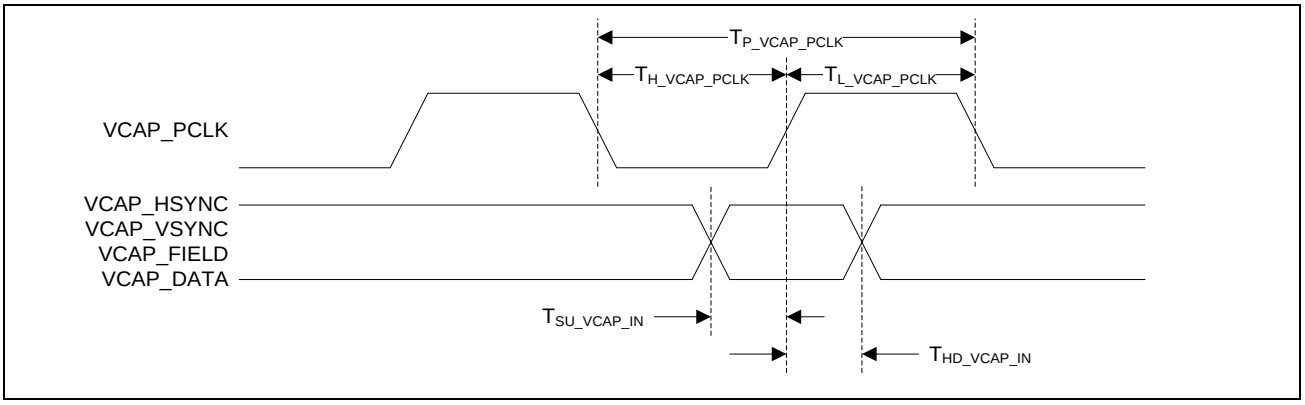


Figure 7.3-17 Capture Sensor Interface Timing Diagram

7.4 Analog Characteristics

7.4.1 12-bit SARADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
-	Resolution	-	12	-	Bit	
DNL	Differential Nonlinearity Error	-	±1	-	LSB	V_{REF} is external AV_{ref} pin
INL	Integral Nonlinearity Error	-	-1.2	-	LSB	V_{REF} is external AV_{ref} pin
E_O	Offset Error	-	+3.7	-	LSB	V_{REF} is external AV_{ref} pin
E_G	Gain Error (Transfer Gain)	-	-6.6	-	LSB	V_{REF} is external AV_{ref} pin
E_A	Absolute Error	-	4.2	-	LSB	V_{REF} is external AV_{ref} pin
-	Monotonic	Guaranteed				
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	
T_{ADC}	Conversion Time	-	20		Clock	
F_S	Sample Rate		-	200k	SPS	
AV_{DD33}	Supply Voltage	2.97	3.3	3.63	V	
I_{DDA1}	Supply Current (Avg.)	-	1.2		mA	ADC channel 1 high speed mode
I_{DDA2}	Supply Current (Avg.)	-	1.0		mA	ADC channel 1 low speed mode
I_{DDA3}	Supply Current (Avg.)	-	0.4		mA	
I_{LK}	Leakage Current	-	0.1	-	uA	
AV_{REF}	Reference Voltage	2	-	AV_{DD33}	V	
V_{IN}	Analog Input Voltage	0	-	AV_{ref}	V	
R_{IN}	Analog Input Impedance	-	-	2	MΩ	
C_{IN}	Capacitance	-	25.6		pF	
VBG	Band-gap 2.5V voltage output		2.5		V	VBG no trim for VREF output, the accuracy is 6% typically at 100ppm/℃

7.4.2 Low Voltage Detection (LVD) and Low Voltage Reset (LVR)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
AV_{DD33}	Operation Voltage	2.0	3.3	3.63	V	-
I_{LVDR}	Operating Current		21		uA	-
I_{LK}	Quiescent Current	-	0.1	0.5	uA	LVR_EN (SYS_LVRDCR[0]) = 0, LVD_EN (SYS_LVRDCR[8]) = 0
T_A	Temperature	-40	-	85	°C	-
V_{TH_LVD}	LVD Threshold Voltage	2.295	2.55	2.805	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		2.475	2.75	3.025	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{TH_LVR}	LVR Threshold Voltage	2.115	2.35	2.585	V	-
V_{HY_LVD}	LVD Hysteresis	0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{HY_LVR}	LVR Hysteresis	0.045	0.05	0.055	V	-

Note: Guaranteed by characterization results, not tested in production.

7.4.3 3.3V Power-On Reset (POR33)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	°C	-
V_{POR33}	Reset Voltage	-	1.83	-	V	AV_{DD33} rising from 0V to 3.3V
I_{POR33}	Quiescent current	-	5	-	nA	Vin > reset voltage

Note: Guaranteed by characterization results, not tested in production.

7.4.4 1.2V Power-On Reset (POR12)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	°C	-
V_{POR12}	Reset Voltage	-	0.76	-	V	V_{DD12} rising from 0V to 1.2V
I_{POR12}	Quiescent current	-	10	-	nA	Vin > reset voltage

Note: Guaranteed by characterization results, not tested in production.

7.4.5 USB 2.0 PHY

7.4.5.1 Low/Full-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OL}	Output Low (Driven)	-	-	0.3	V	1.5K RPU on DP to 3.6v
V_{OH}	Output High (Driven)	2.8	-	-	V	15K RPD on DP, DM to GND
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	$\lvert V_{USB0\_DP}–V_{USB0\_DM}\rvert$
V_{CM}	Differential Common-Mode Range	0.8	-	2.5	V	
V_{IL}	Single-Ended Input Low	-	-	0.8	V	-
V_{IH}	Single-Ended Input High	2.0	-	-	V	-
R_{PU}	Pull-Up Resistor	1.35	1.5	1.65	kΩ	
R_{PD_DP}	D+ Pull-Down Resistor	13.5	15	16.5	kΩ	
R_{PD_DM}	D- Pull-Down Resistor	13.5	15	16.5	kΩ	
Z_{DRV}	Driver Output Resistance	28	-	44	Ω	Steady state drive[1]
C_{IN}	Transceiver Low-Speed Donwstream Port Capacitance	200		600	pF	Pin to GND
C_{IN}	Transceiver Low-Speed Upstream Port Capacitance	50		150	pF	Pin to GND
C_{IN}	Transceiver Full-Speed Capacitance		50		pF	

Note:

1. Driver output resistance doesn't include series resistor resistance.
2. Guaranteed by characterization results, not tested in production.

7.4.5.2 High-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HSDI}	High Speed Differential Input Signal Level	150	-	-	mV	$\lvert V_{USB0\_DP}–V_{USB0\_DM}\rvert$
V_{HSQ}	High Speed Squelch Detection Threshold	100	125	150	mV	$\lvert V_{USB0\_DP}–V_{USB0\_DM}\rvert$
V_{HSCM}	High Speed Common Mode Voltage Range	-50	-	500	mV	
V_{HSOH}	High Speed Data Signaling High	300	400	440	mV	
V_{HSOL}	High Speed Data Signaling Low	-10	0	10	mV	
V_{CHIRPJ}	Chirp J Level	700	-	1100	mV	
V_{CHIRPK}	Chirp K Level	-900	-	-500	mV	
R_{HSDRV}	High Speed Driver Output Resistance	40.5	45	49.5	Ω	

Note: Guaranteed by characterization results, not tested in production.

7.4.5.3 USB Low-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{LRISE}	Rise Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
T_{LFALL}	Fall Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{LCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Note: Guaranteed by characterization results, not tested in production.

7.4.5.4 USB Full-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FRISE}	Rise Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FFALL}	Fall Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Note: Guaranteed by characterization results, not tested in production.

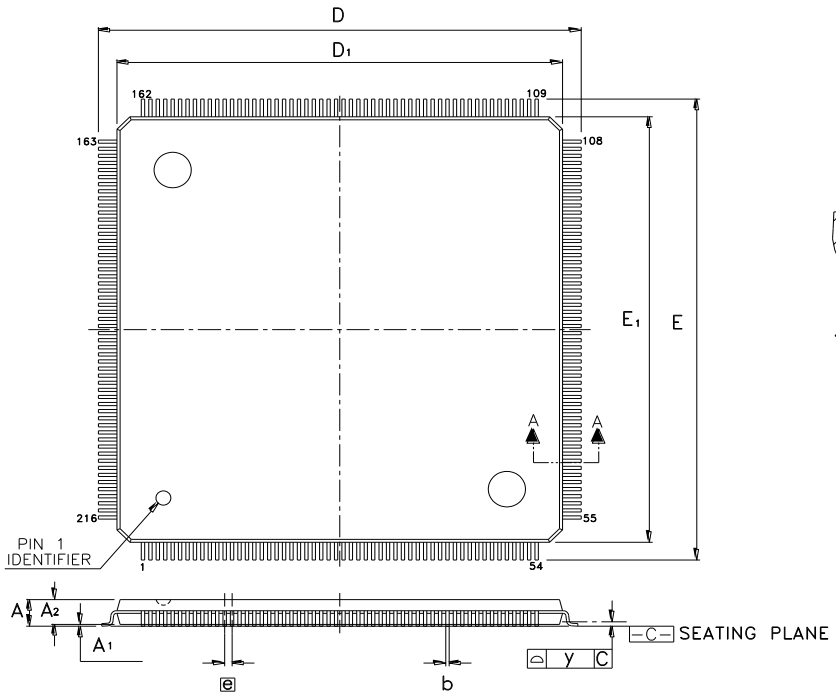
7.4.5.5 USB High-Speed Driver AC Electrical Characteristics

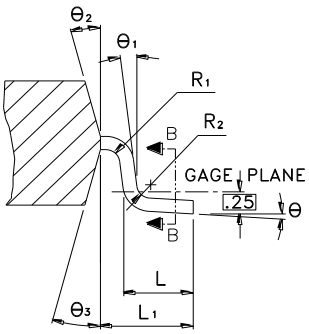
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HRISE}	High Speed Driver Rise Time	500	-	900	ps	CL<10pF
V_{HFALL}	High Speed Driver Fall Time	500	-	900	ps	CL<10pF

Note: Guaranteed by characterization results, not tested in production.

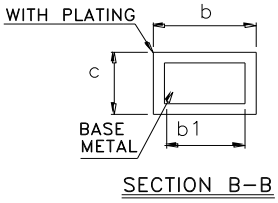
8 PACKAGE DIMENSIONS

8.1 LQFP 216L (24x24x1.4mm footprint 2.0mm)





SECTION A–A

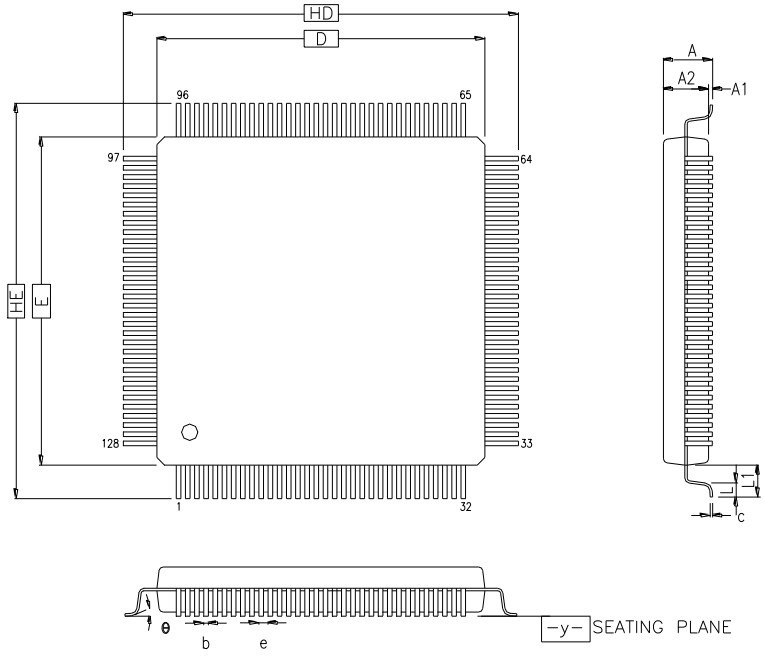


SECTION B–B

Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
y	0.08			0.00314		

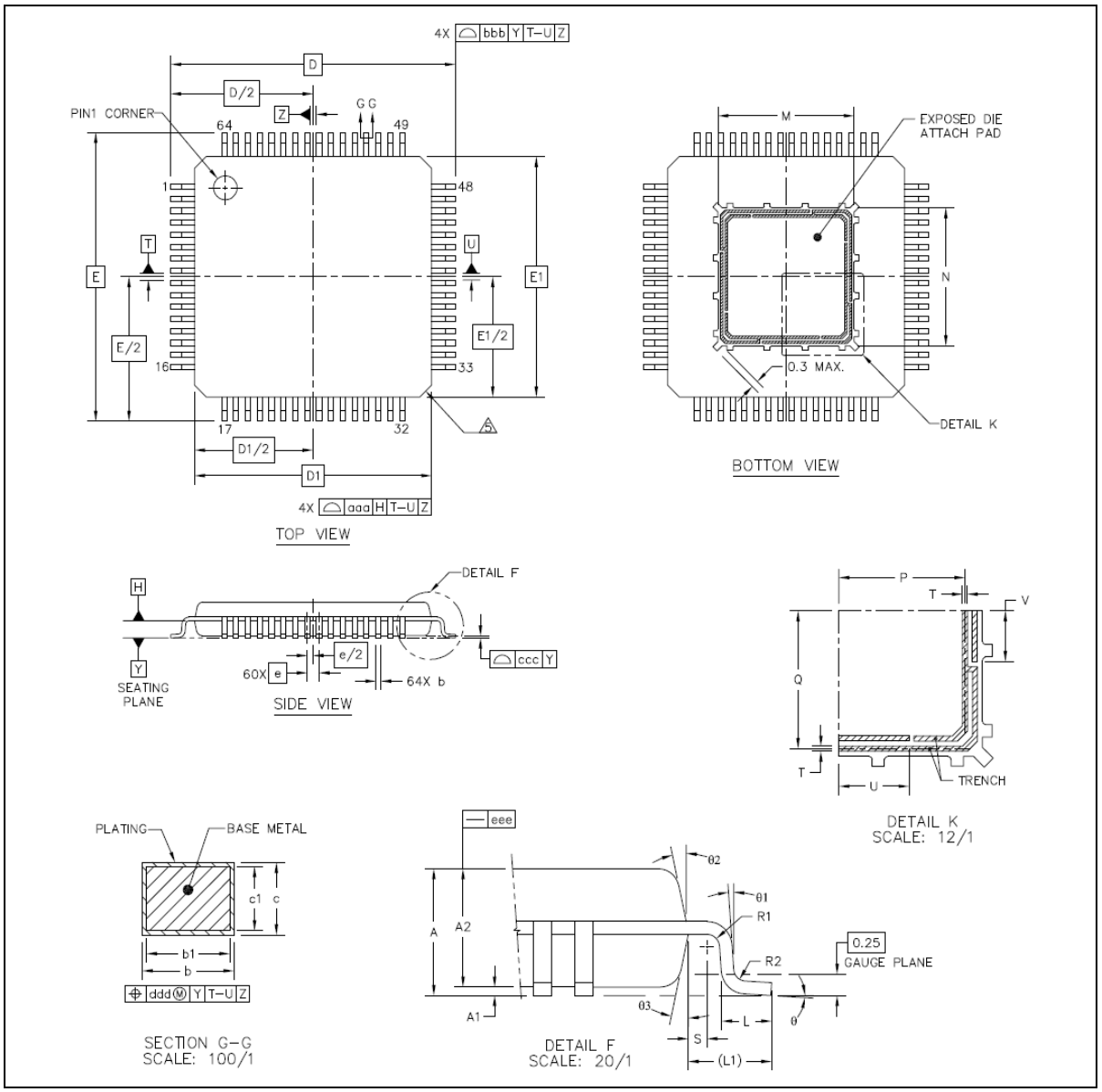
8.2 128L LQFP (14x14x1.4mm footprint 2.0mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

8.3 LQFP 64L EX-PAD (10x10x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	12 BSC		
	Y	E	12 BSC		
BODY SIZE	X	D1	10 BSC		
	Y	E1	10 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	5.64	5.74	5.84
	Y	N	5.64	5.74	5.84
		P	2.47	2.52	2.57
		Q	2.67	2.72	2.77
		T	0.05	---	0.15
		U	1.35	---	1.45
		V	0.95	---	1.05
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8.4 Thermal Characteristics

8.4.1 Thermal Performance of LQFP under Forced Convection

PKG Type	PCB condition	θ ja (℃/W)			θ jc (℃/W)	θ jb (℃/W)
		0 m/s	1 m/s	2m/s		
LQFP 216L 24mmx24mm	JEDEC 1S1P (2-layers)	42.5	35.9	33.8	9.2	35.16
	JEDEC 2S2P (4-layers)	39.8	33.5	31.7	9	32.08
LQFP 64 EX-PAD 10x10mm	JEDEC 1S1P (2-layers)	35.9	29	27.2	16.5	22
	JEDEC 2S2P (4-layers)	28.5	22.5	21	14.3	15.56
LQFP 128L 14mmx14mm	JEDEC 1S1P (2-layers)	-	-	-	-	-
	JEDEC 2S2P (4-layers)	38.5	33.8	32	9.9	-

Table 8.4-1 Thermal Performance of LQFP

8.4.2 Thermal Performance Terminology

The major thermal dissipation paths can be illustrated as following

TJ: the maximum junction temperature;

TA: the ambient or environment temperature;

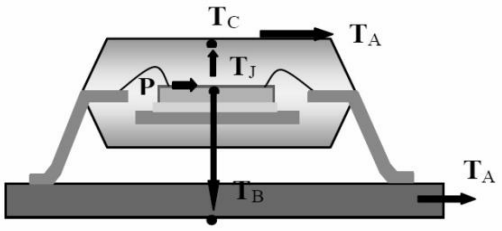
TC: the top center of compound surface temperature;

TB: the bottom center of PCB surface temperature;

P: total input power

1. Junction to ambient thermal resistance, θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \; ; \qquad (1)$$



Thermal Dissipation of LQFP package

Figure 8.4-1 Junction to Ambient Thermal Resistance

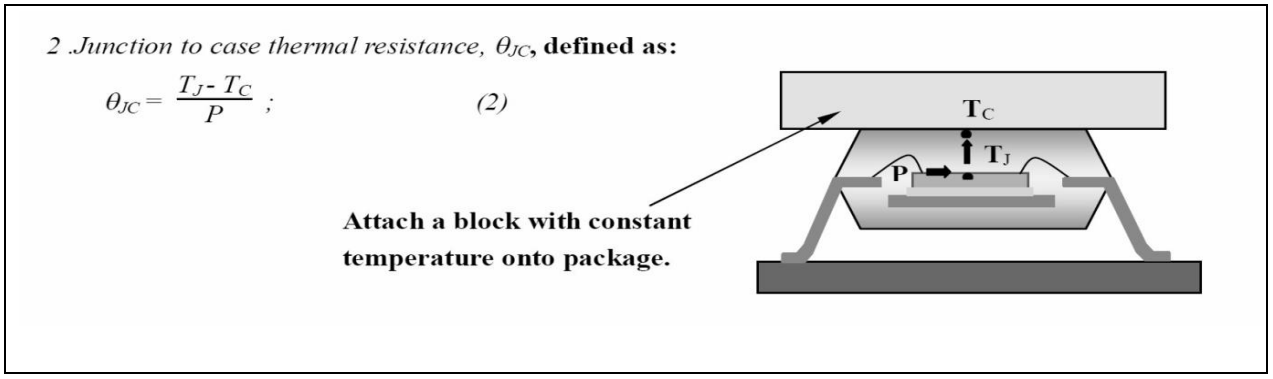


Figure 8.4-2 Junction to Case Thermal Resistance

8.4.3 Simulation Conditions

Input Power	Top Die: 0.6W Bottom die: 0.6 W
Test Board (PCB)	FR4 Cu=1-OZ PCB size = 3"x4.5" PCB thickness= 1.6mm
Control Condition	Air Flow = 0, 1, 2, 3 m/s

Table 8.4-2 Thermal Characteristics Simulation Conditions

8.5 PCB Reflow Profile Suggestion

8.5.1 Profile Setting Consideration

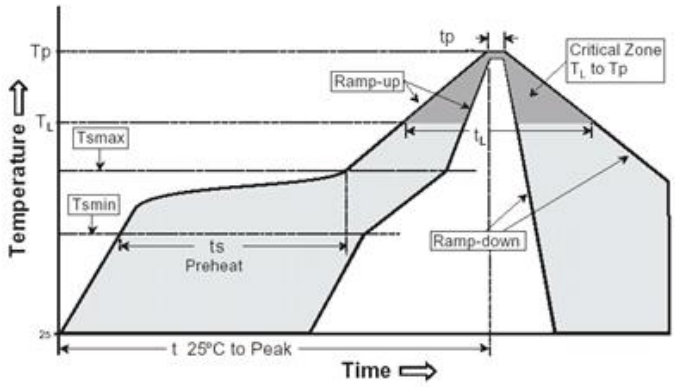


Figure 8.5-1 PCB Reflow Profile Diagram

Profile Feature	Sn-Pb Eutestic Assembly		Pb-Free Eutestic Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	< 3°C/second		< 3°C/second	
Preheat • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (min to max) (ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Time maintained above: • Temperature (T_L) • Time (t_L)	183°C 60-150 seconds		1217°C 60-150 seconds	
Peak Temperature (T_p)	225+0/-5°C		245+5/-5°C	
Time within 5°C of actual Peak Temperature (t_p)	10-20 seconds		10-30 seconds	
Ramp-down Rate	3°C/second max.		3°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	
Notes: 1. All temperatures refer to topside of the package, measured on the package body surface. 2. Depends on other parts on board density and follower solder paste manufacturer's guideline.				

Table 8.5-1 PCB Reflow Profile Parameters

8.5.2 Profile Suggestion

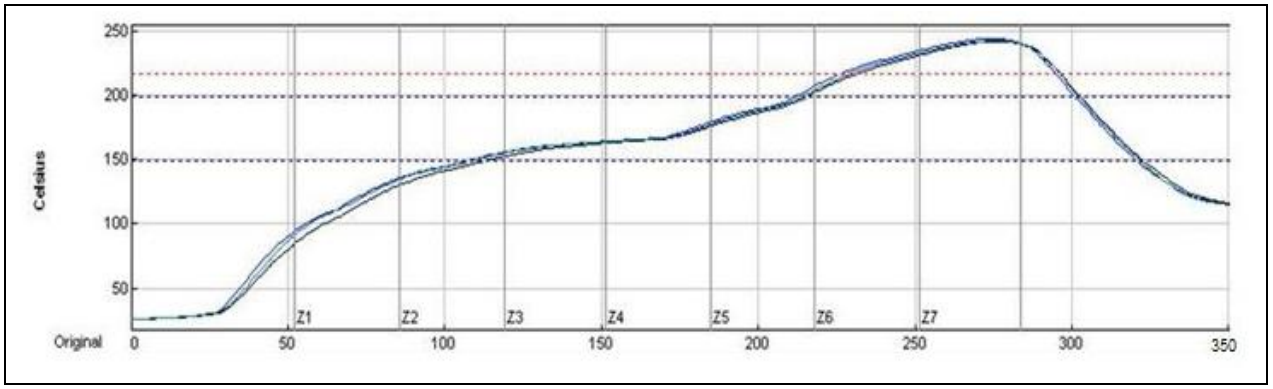


Figure 8.5-2 Profile Suggestion for NUC980 series

Reheat time	**150°C-200°C: 105+/-15sec**
Dwell time	Over 220°C: 70+5/-10 sec
Peak Temp	240+10/-5°C
Ramp Up/Dwon Rate	Up: 3 +0/-2°C/sec Down: 2+0/-1°C/sec

Table 8.5-2 Profile Parameters for NUC980 Series

8.6 PKG Baking and Vacuumed

The moisture-sensitivity caution label (see Figure 8.6-1) is applied to the outside of the sealed moisture-barrier bag. This label contains detailed information specific to the device (moisture-sensitivity level, shelf life, etc.).

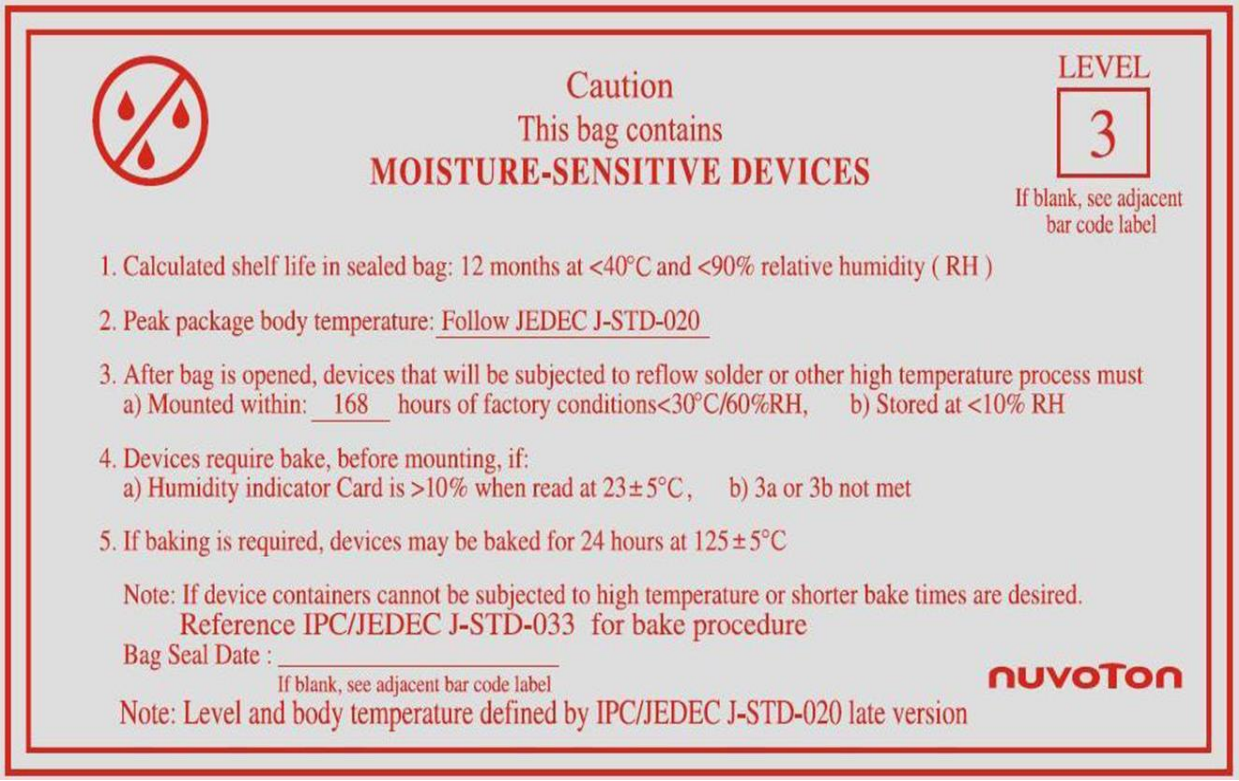


Figure 8.6-1 Cautions for PKG Baking

9 ABBREVIATIONS

9.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AIC	Advanced Interrupt Controller
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
AMBA	Advanced Microprocessor Bus Architecture
BCH	Bose–Chaudhuri–Hocquenghem
BPS	Bit Per Second
CAN	Controller Area Network
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DDR	Double Data Rate
DDR2	Double Data Rate 2
DMA	Direct Memory Access
EBI	External Bus Interface
ECC	Elliptic Curve Cryptography
ECC	Error Correcting code
EHCI	Enhance Host Controller Interface
EINT	External Interrupt pin
EMAC	Ethernet MAC Controller
eMMC	Embedded Multimedia Card
ETU	Elementary time unit
FIFO	First In, First Out
FIQ	Fast Interrupt
FMI	Flash Memory Interface
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HMAC	keyed-Hash Message Authentication Code
HSUSBD	High Speed USB 2.0 Device Controller
HXT	12 MHz External High Speed Crystal Oscillator
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
LIN	Local Interconnect Network

LPDDR	Low Power DDR
LSB	Least Significant Bit
LVD	Low Voltage Detect
LVR	Low Voltage Reset
LXT	32.748 kHz External Low Speed Crystal Oscillator
MLC	Multi-Level Cell NAND Flash
MMU	Memory Management Unit
MSB	Most Significant Bit
OHCI	Open Host Controller Interface
PCLK	The Clock of Advanced Peripheral Bus
PCM	Pulse Code Modulation
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PMBus	Power Management Bus
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
RMII	Reduced Media Independent Interface
RSA	Rivest、Shamir and Adleman Cryptography
RTC	Real Time Clock
SC	Smart Card
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIC	SDRAM Interface Controller
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SHA	Secure Hash Algorithm
SLC	Single Level Cell NAND Flash
SMBus	System Management Bus
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

10 REVISION HISTORY

Date	Revision	Description
2018.10.11	1.00	1. Initial version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.