

5

4

3

2

1

D

D

C

C


B

B

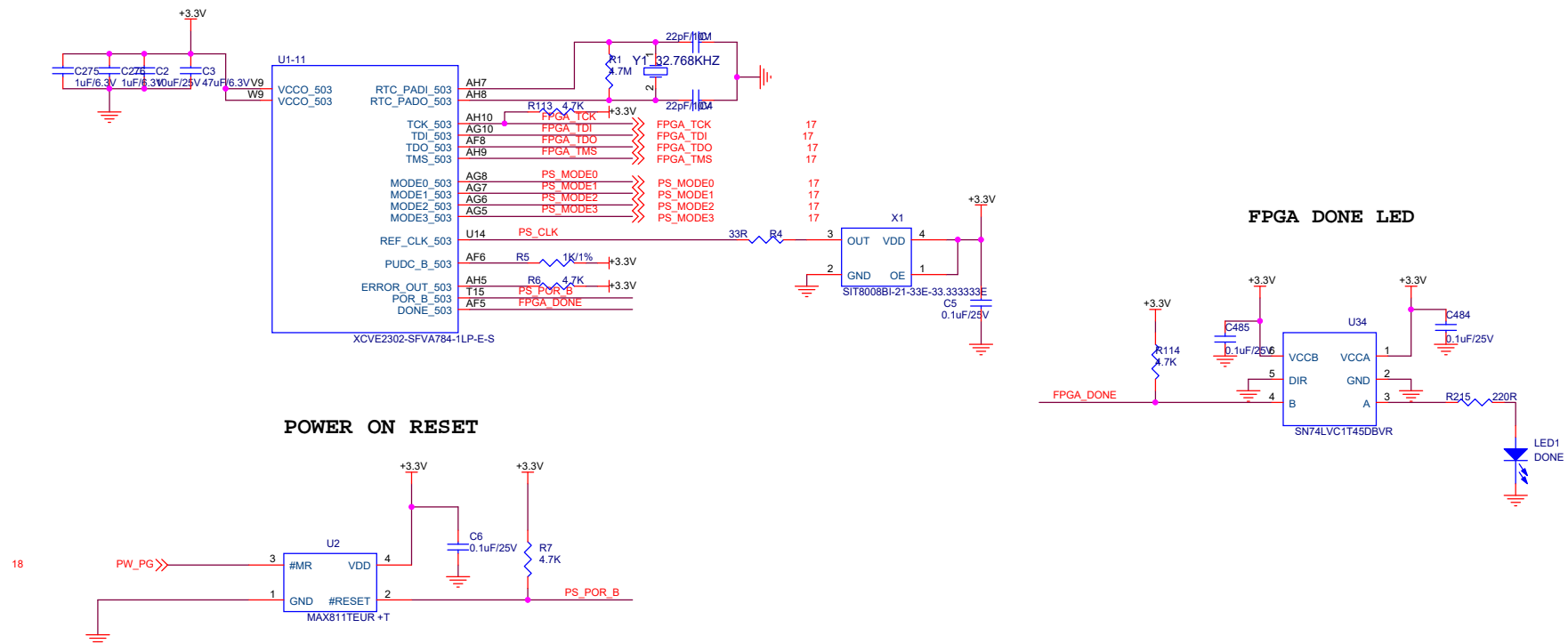
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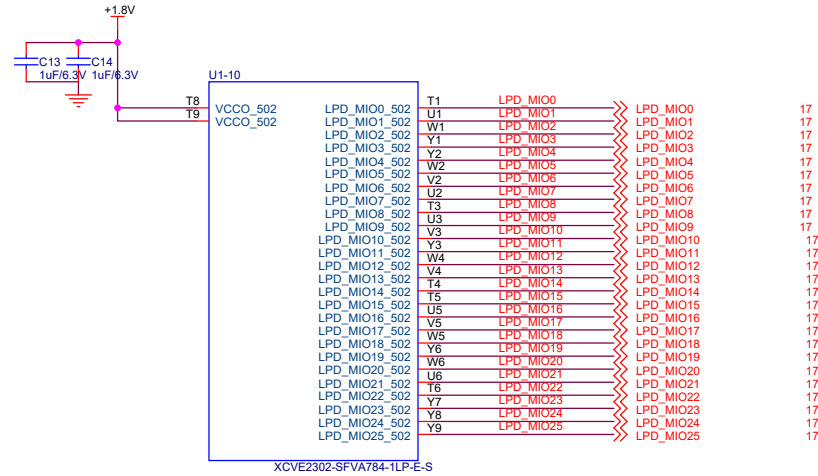
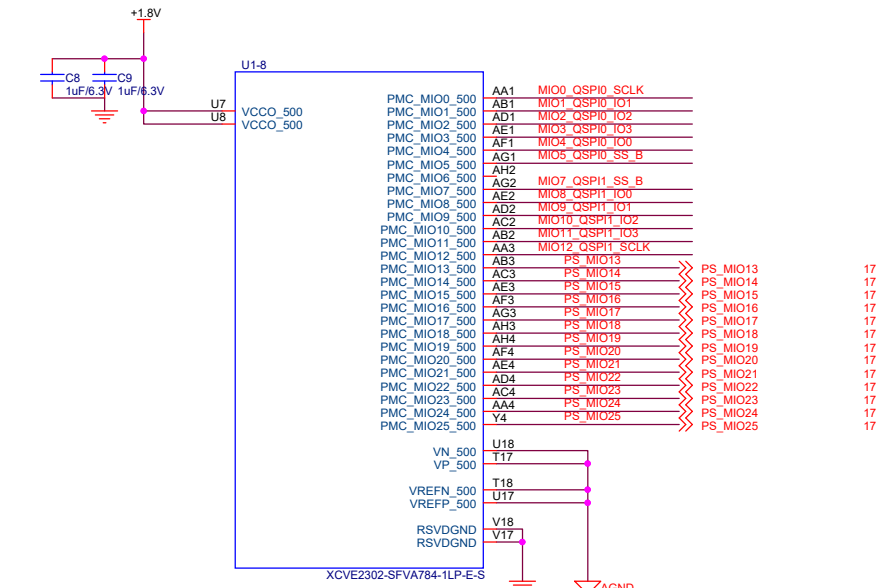
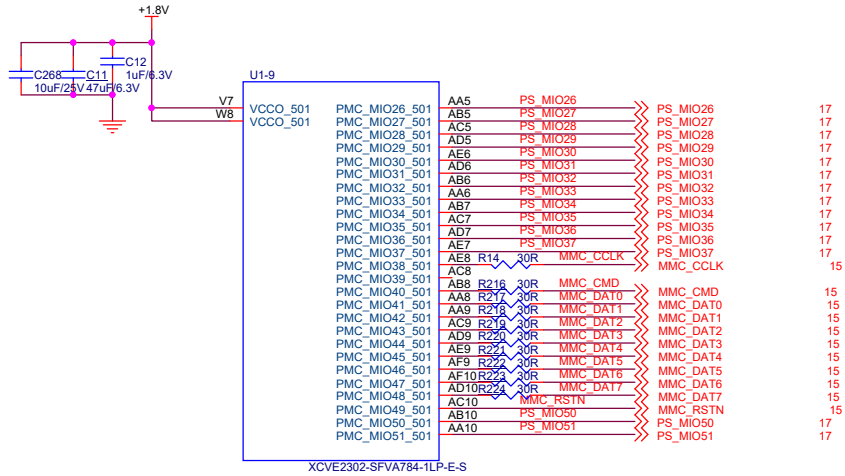
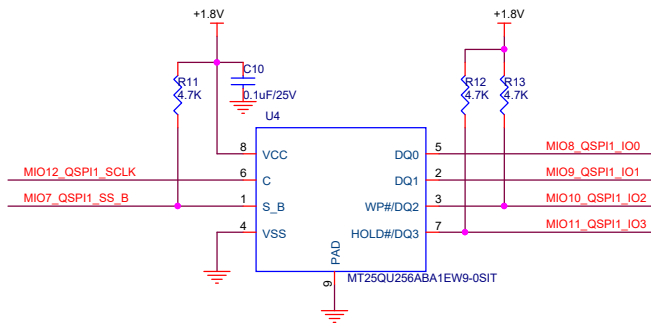
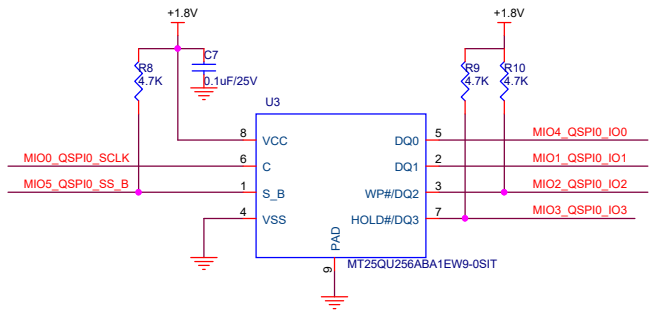
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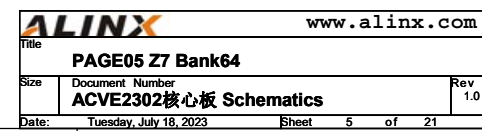
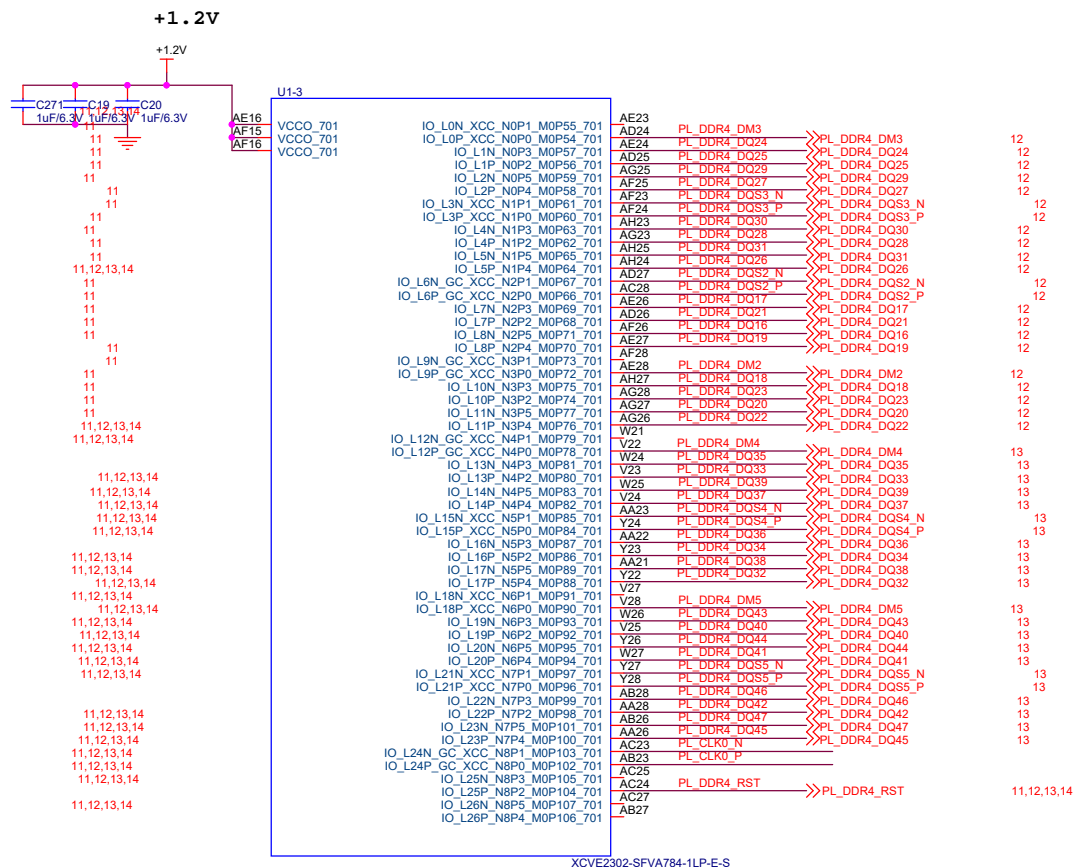
ALINX Confidential

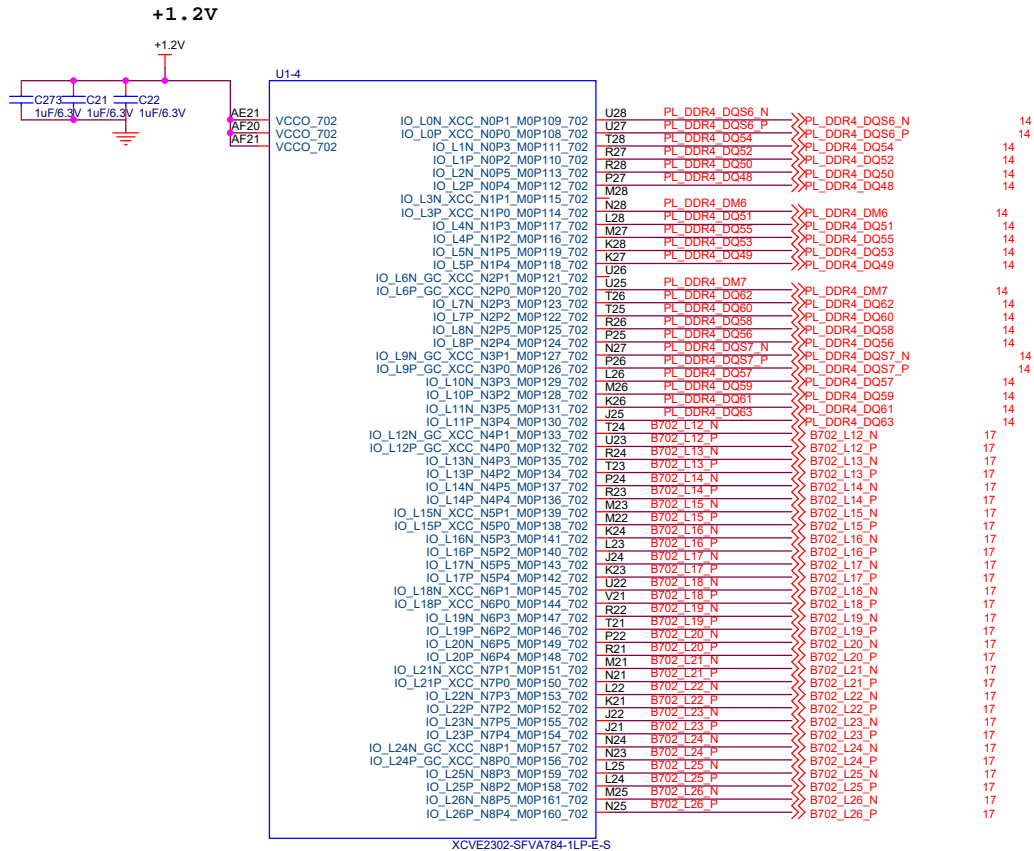
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Title			
PAGE01 Block diagram			
Size	Document Number		Rev
	ACU4EV核心板 Schematics		1.0
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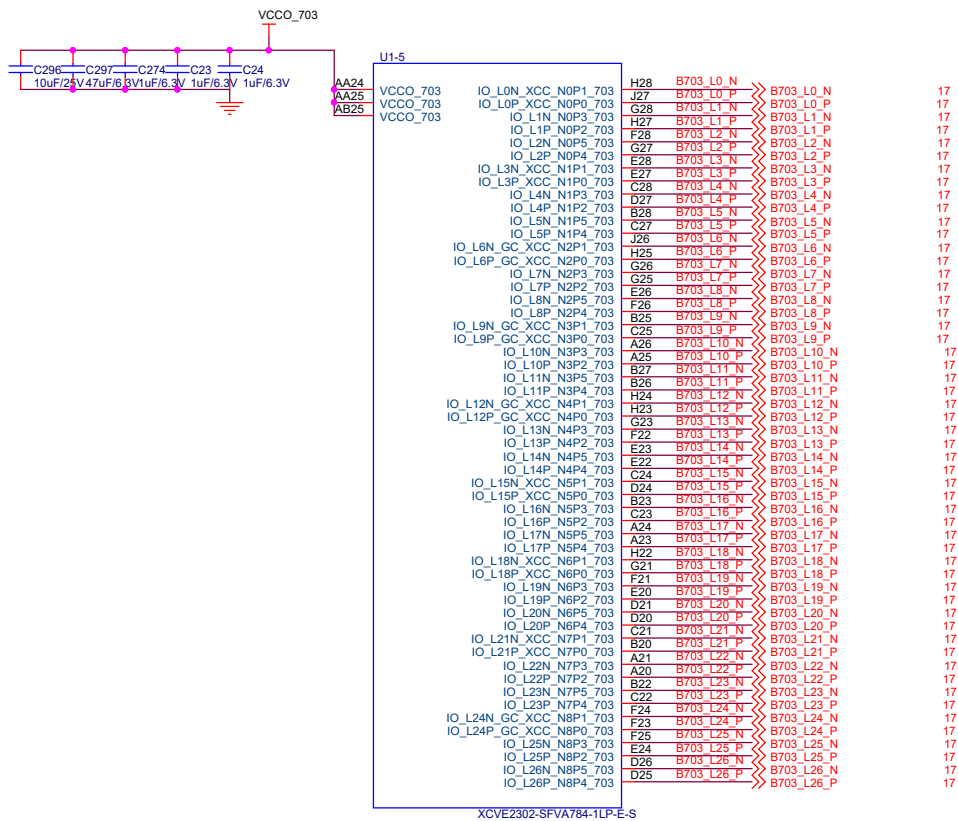
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0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI(24b)	24-Bit addresssing(QSPI24)
0010	Quad_SPI(32b)	32-Bit addresssing(QSPI32)
0011	SD0(2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1(2.0)	SD2.0
0110	eMMC(1.8V)	eMMC version 4.5 at 1.8V
0111	USB0(2.0)	USB 2.0 only
1000	PJTAG(MIO #0)	PJTAG connection 0 option
1001	PJTAG(MIO #1)	PJTAG connection 1 option
1110	SD1 LS(3.0)	SD 3.0

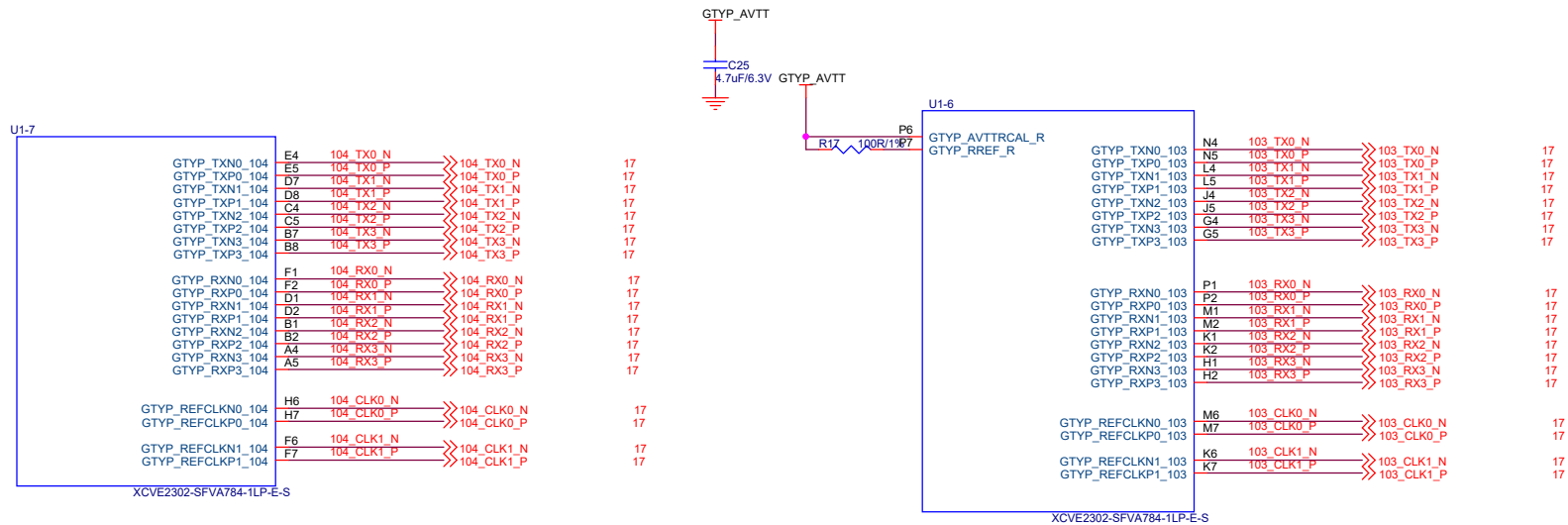


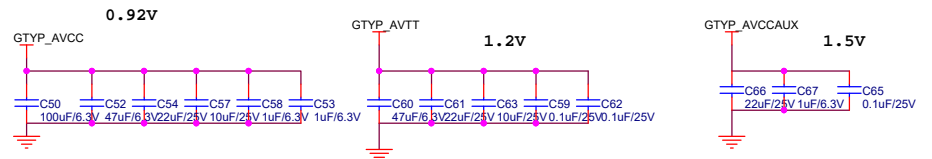
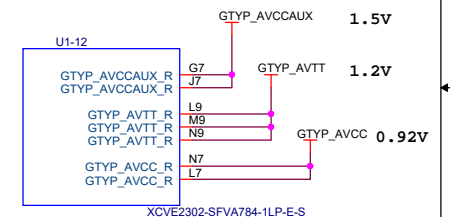
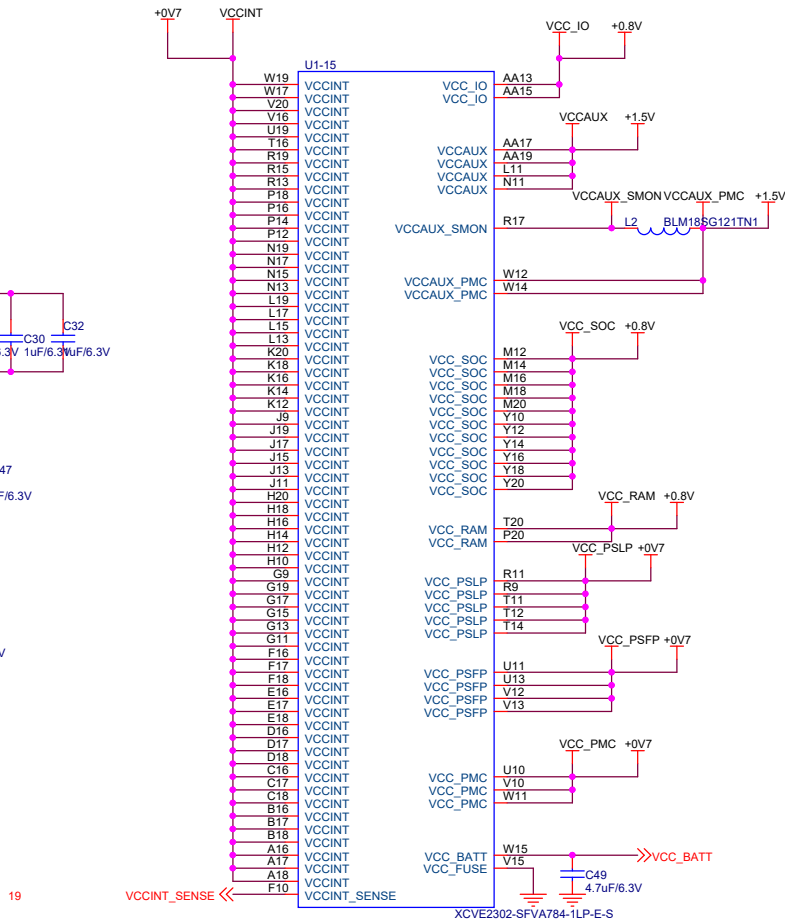
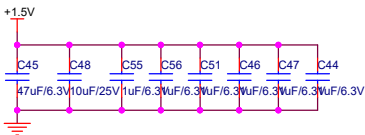
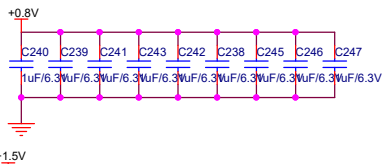
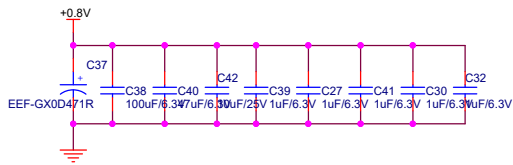
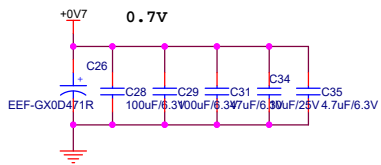
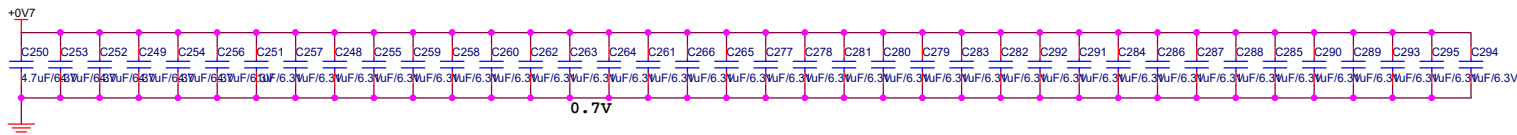


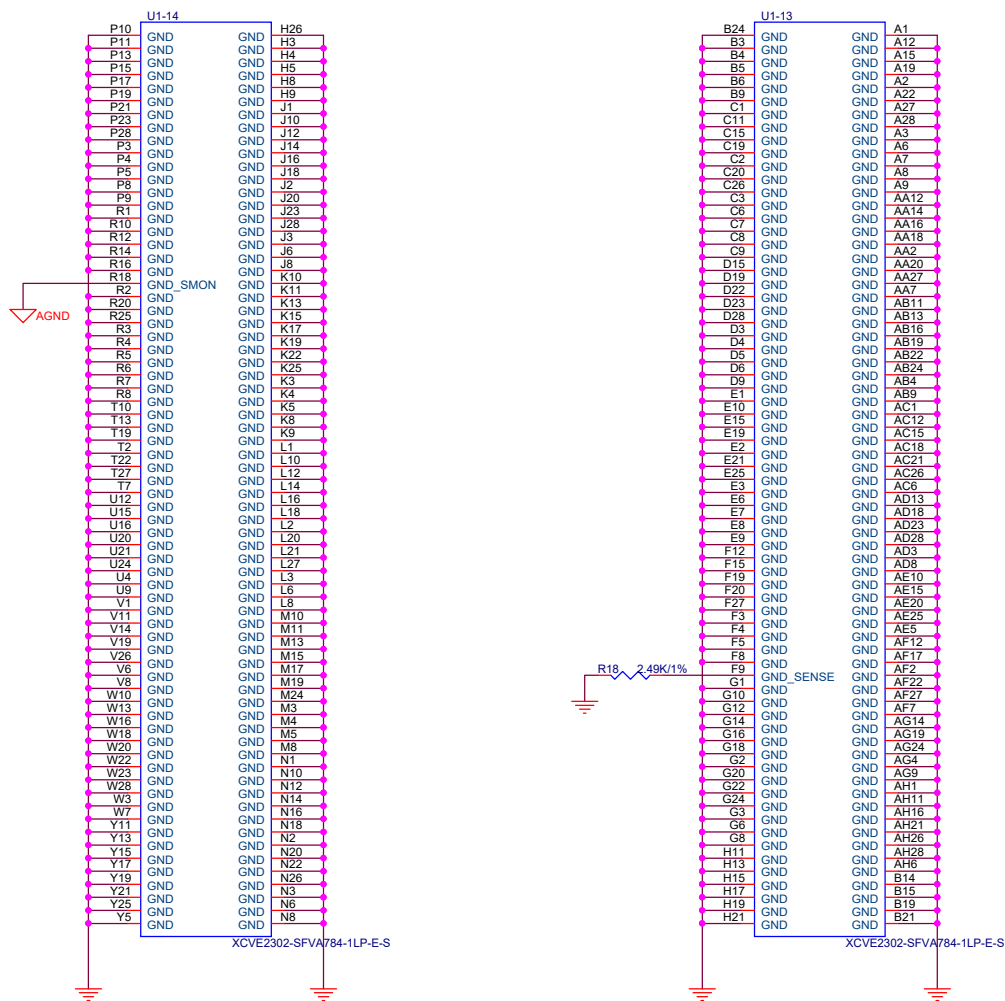


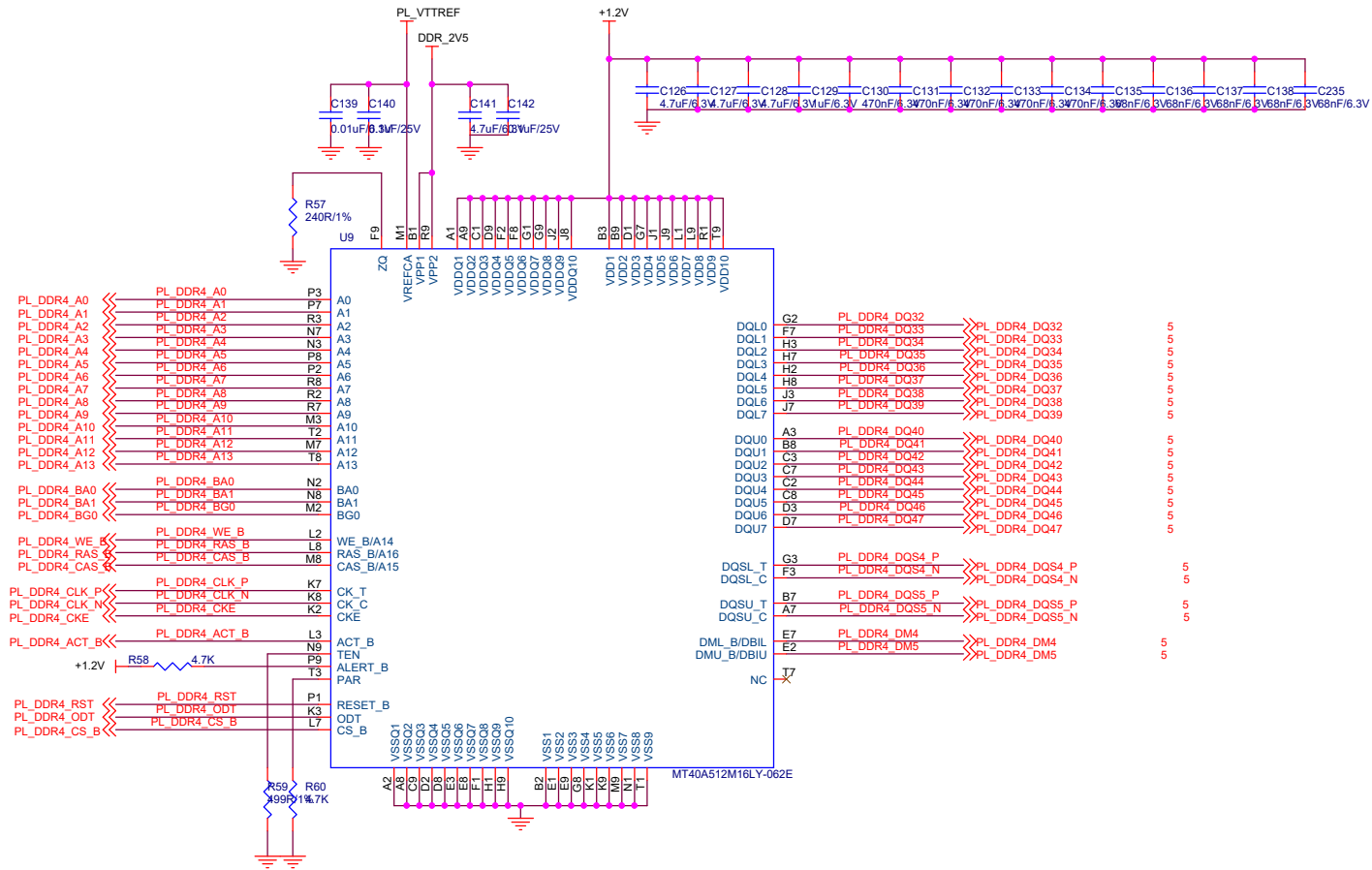


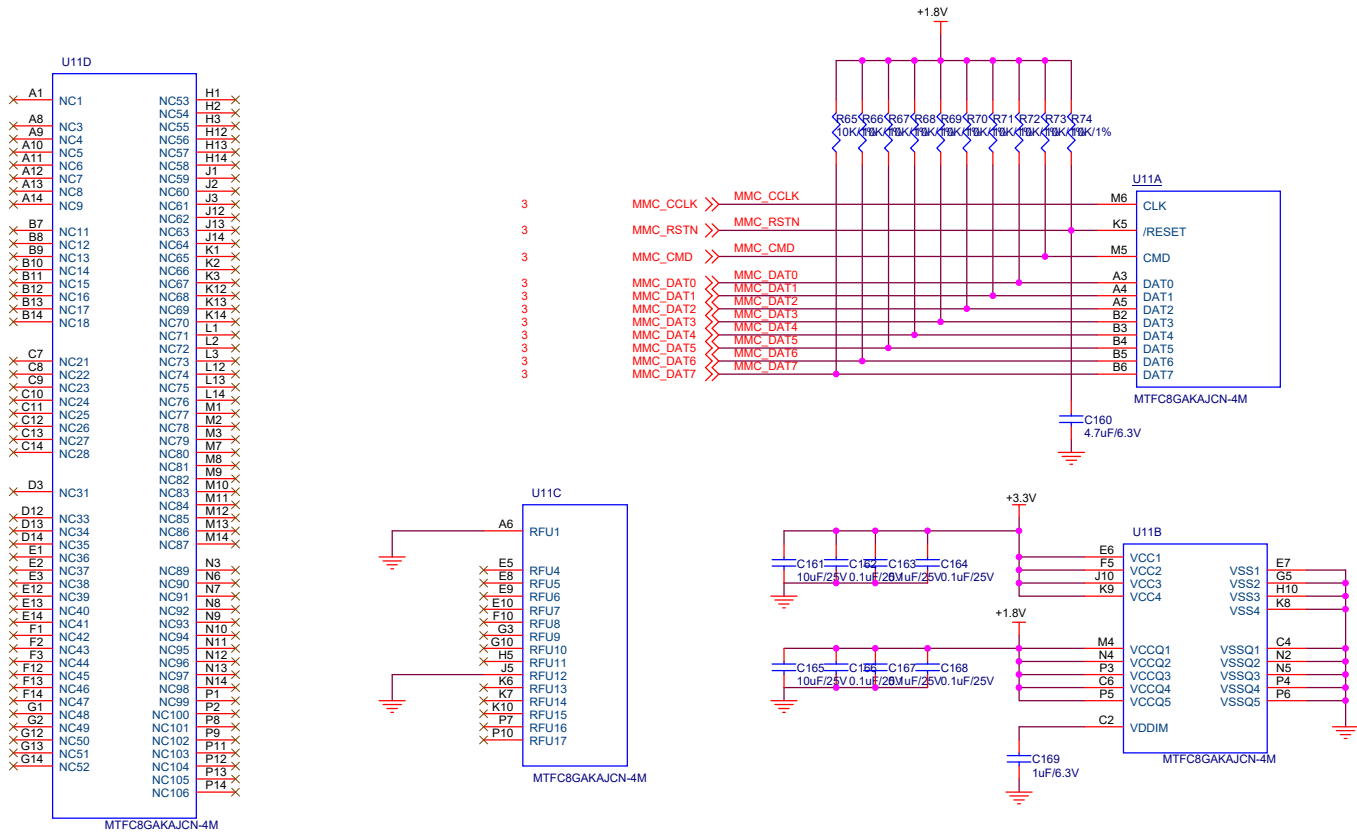






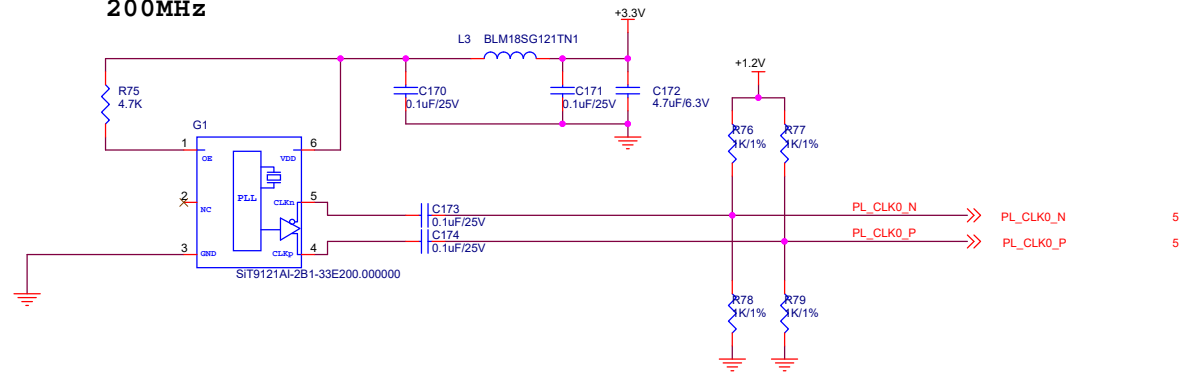


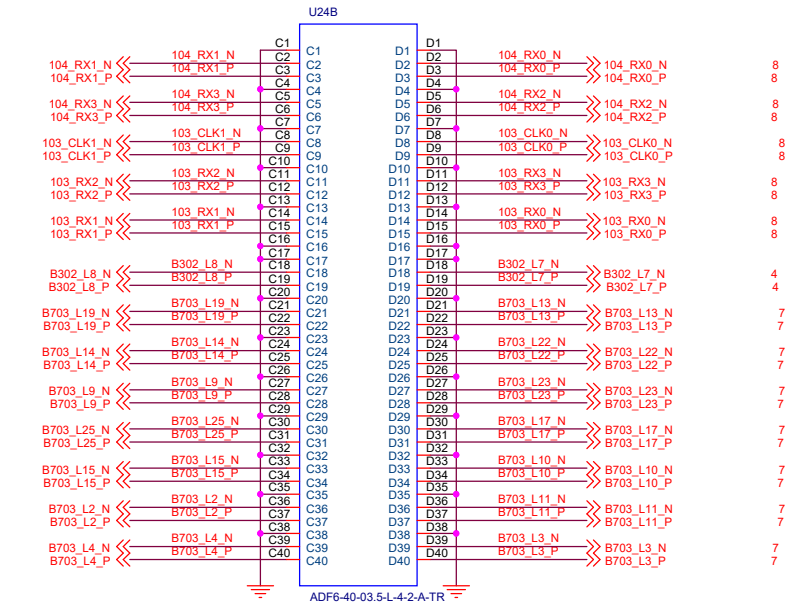
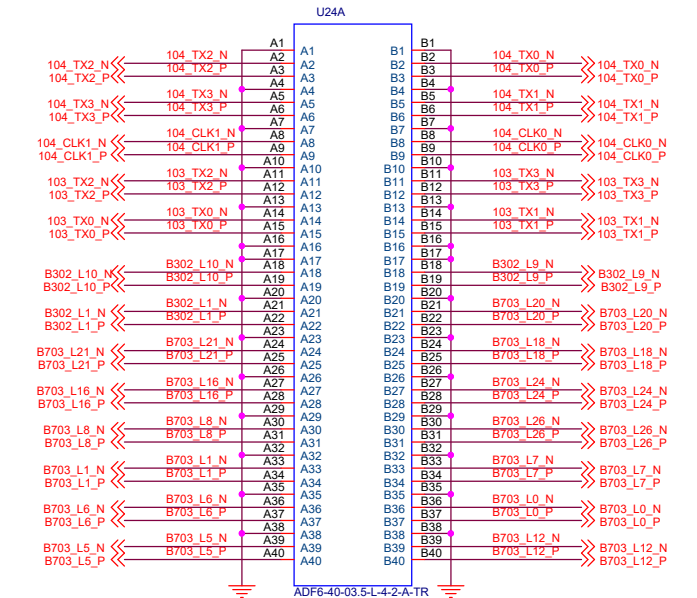
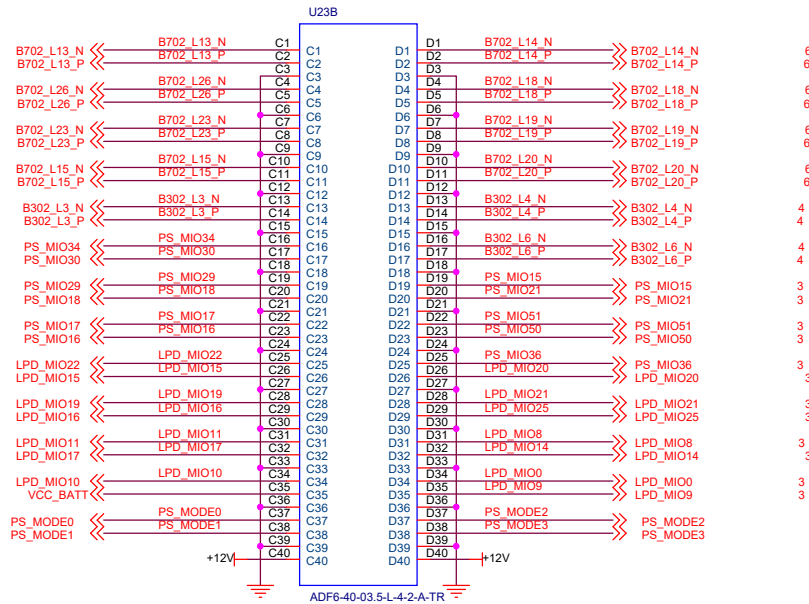
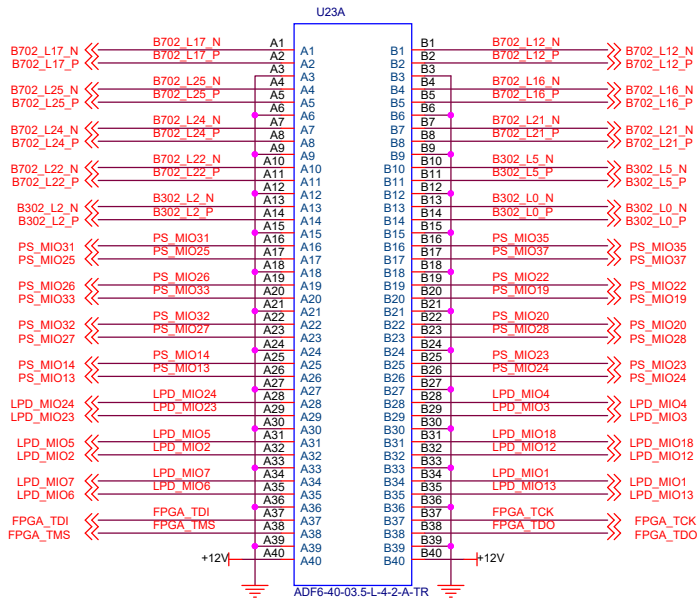
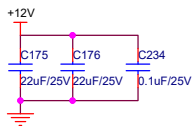


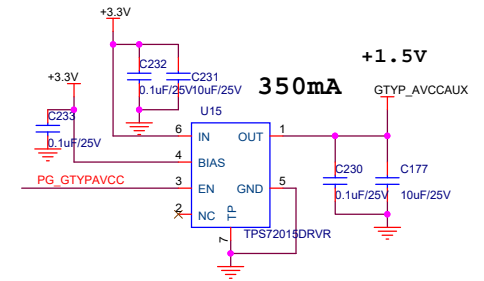
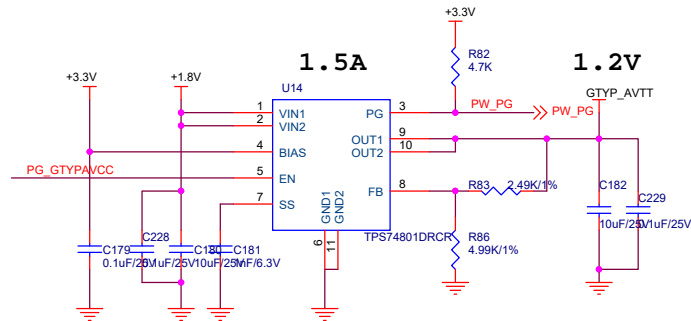
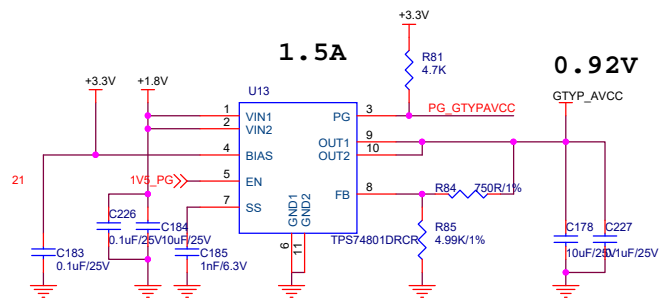
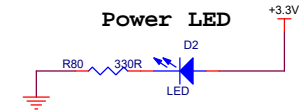
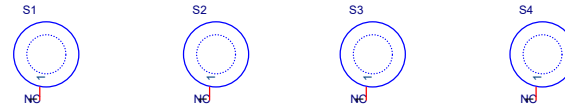


PL SYSTEM CLOCK

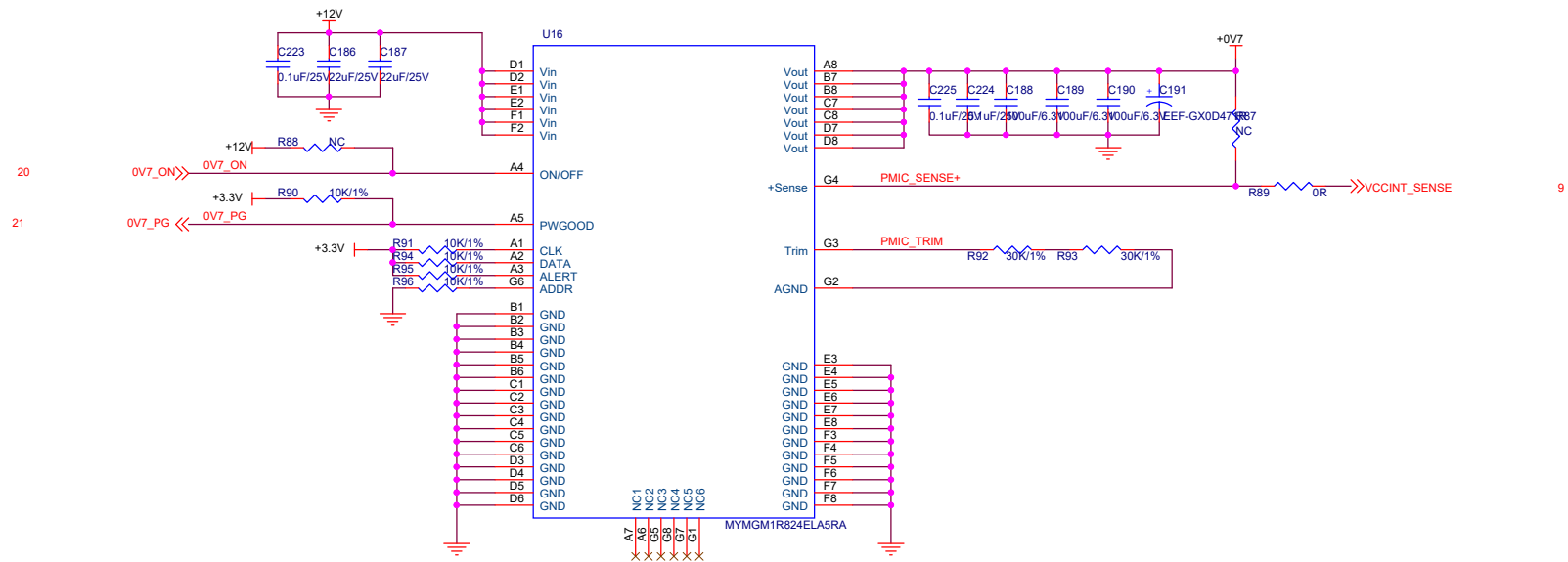
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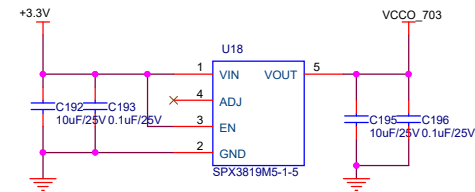
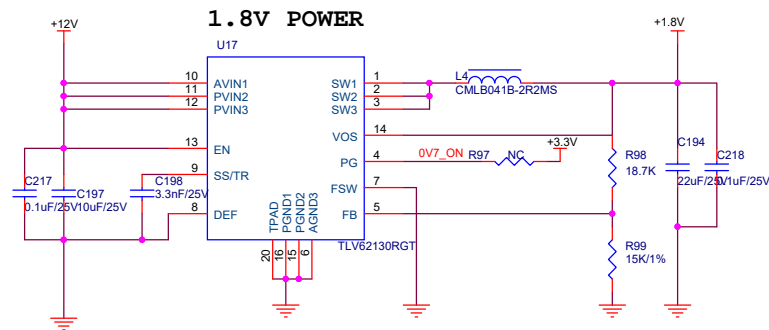






+0.7V 24A





POWER Sequence:

+3.3V(VCCO_503/VCCO_302) +1.8V(VCCIO_501/502/503) +1.2V(VCCIO700~702)



+0V7(VCCINT/VCC_PMC/VCC_PSFPP/VCC_PSLP)



+0.8V(VCC_RAM/VCC_SOC/VCC_IO)



+1.5V(VCCAUX/VCCAUX_PMC/VCCAUX_SMON)



GTYP_AVCC



GTYP_AVCCAUX



GTYP_AVTT

