The Hardware-in-the-loop Testbed for Microgrid

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WHY HIL?

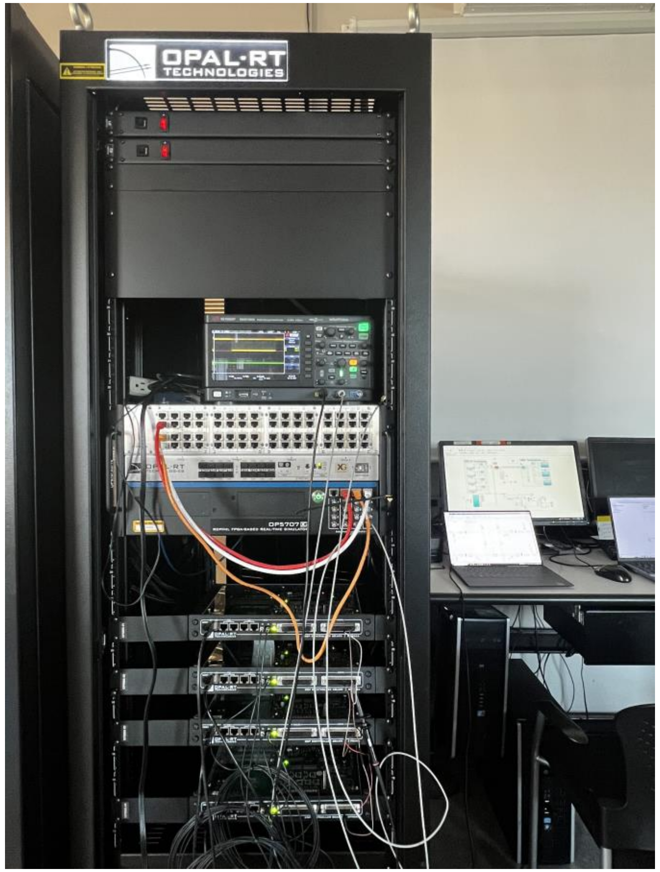
HIL Simulation: validate a control system's design by running the control on its actual hardware.

	HIL	Software Simulation
Synchronization	Not guarantee (fit reality)	Always guarantee
Communication	Real protocol with delay(fit reality)	No protocol and virtual delay
Measurement	Real sensors with bias, error and delay (fit reality)	Virtual sensor
Simulation speed	Real time (fit reality)	Virtual time (slow)
Cost-efficiency	Low	High

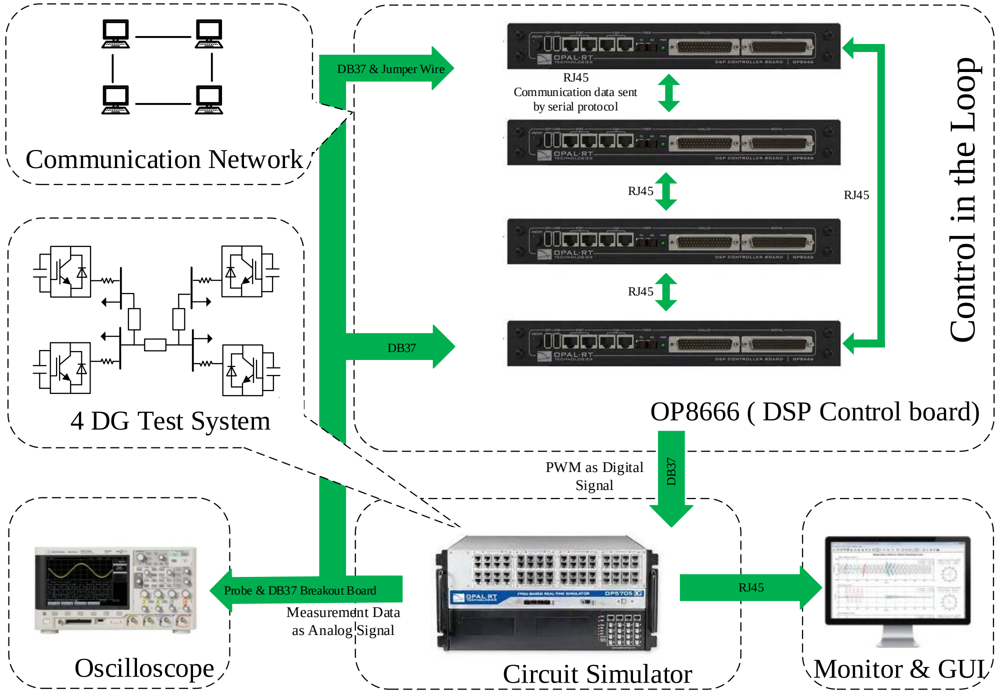
HIL is closer to reality

TESTBED STRUCTURE

- Testbed overview



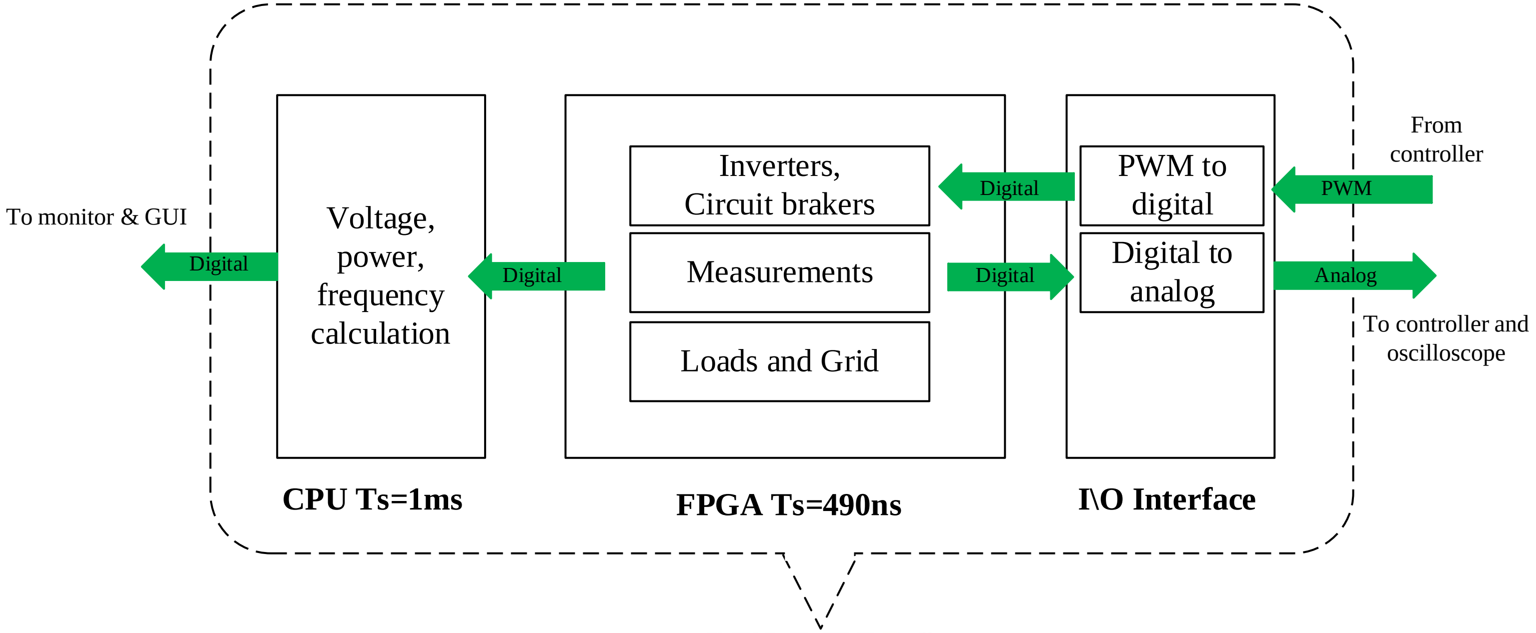
- System data flow



Simulator: model the inverters, measurements, and the power grid in real time
OP8666: DSP controller
Monitor and Oscilloscope: Data monitoring

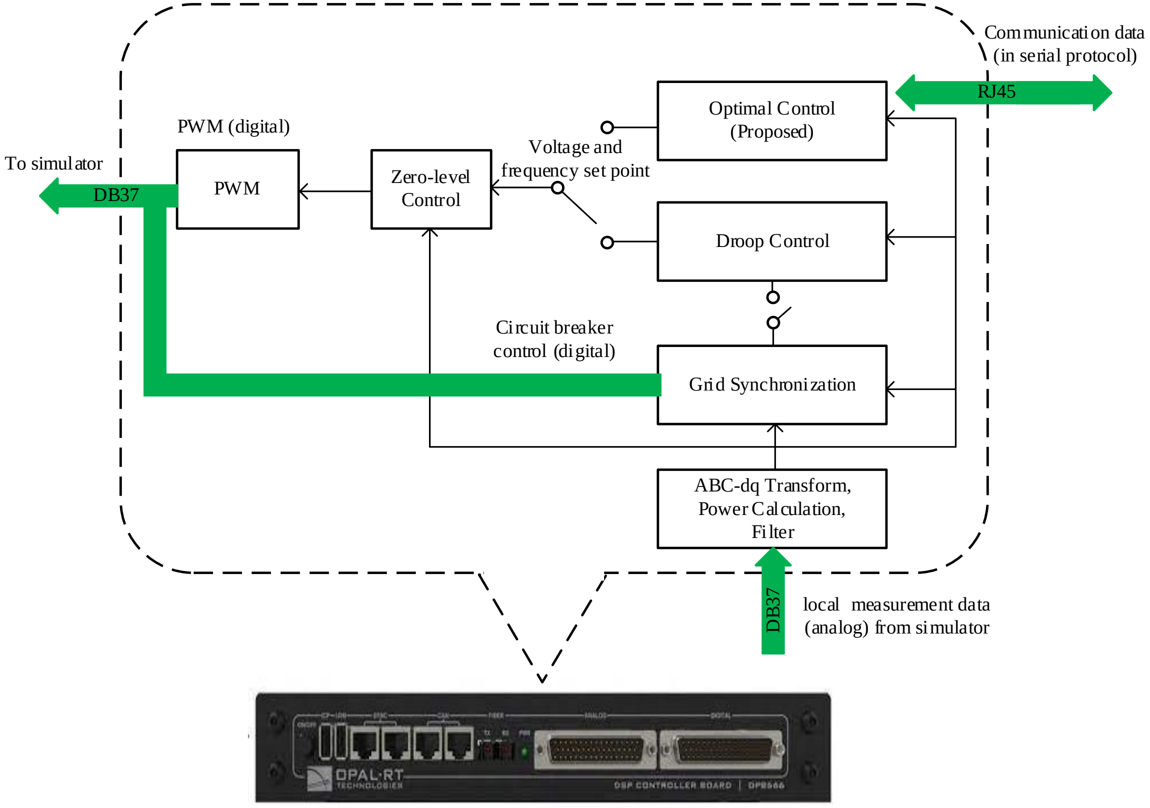
SIMULATOR STRUCTURE

- Blocks in DSP
  - **CPU**: calculate information for host PC
  - **FPGA**: simulate microgrid in small time step
  - **I\O**: converter the digital signal in FPGA to analog signal for controllers and converter the PWM from controllers to digital signal for FPGA



CONTROL STRUCTURE

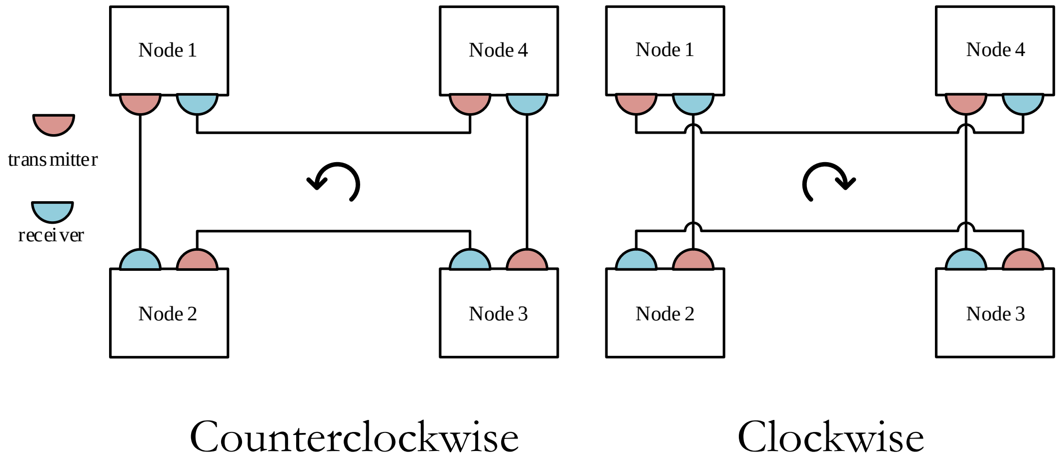
- Control blocks in DSP
  - **Zero-level control**: tracks the control set points
  - **Grid synchronization control**: mitigates the impulse current when an inverter is connected to the grid
  - **Droop control**: supports the grid voltage and frequency without communication (time step: 50 μs)
  - **Optimal secondary control**: optimizes the system's voltage and frequency, and achieves proportional power sharing (time step: 0.025 s)



OP8666 (DSP Control board)

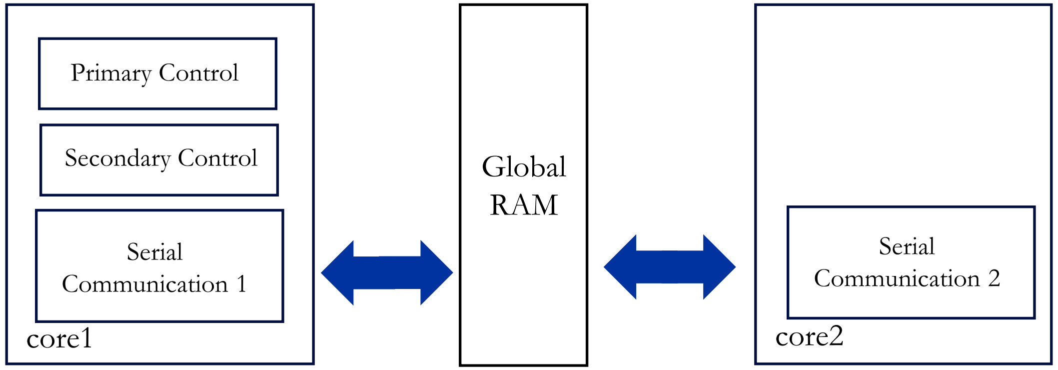
COMMUNICATION

- **Bidirected communication**: use two set of transmitter and receiver to have bidirected communication.
- **Protocol**: UART with baud rate of 115200
- **Communication time step**: 0.025s



CORES ASSIGNMENT

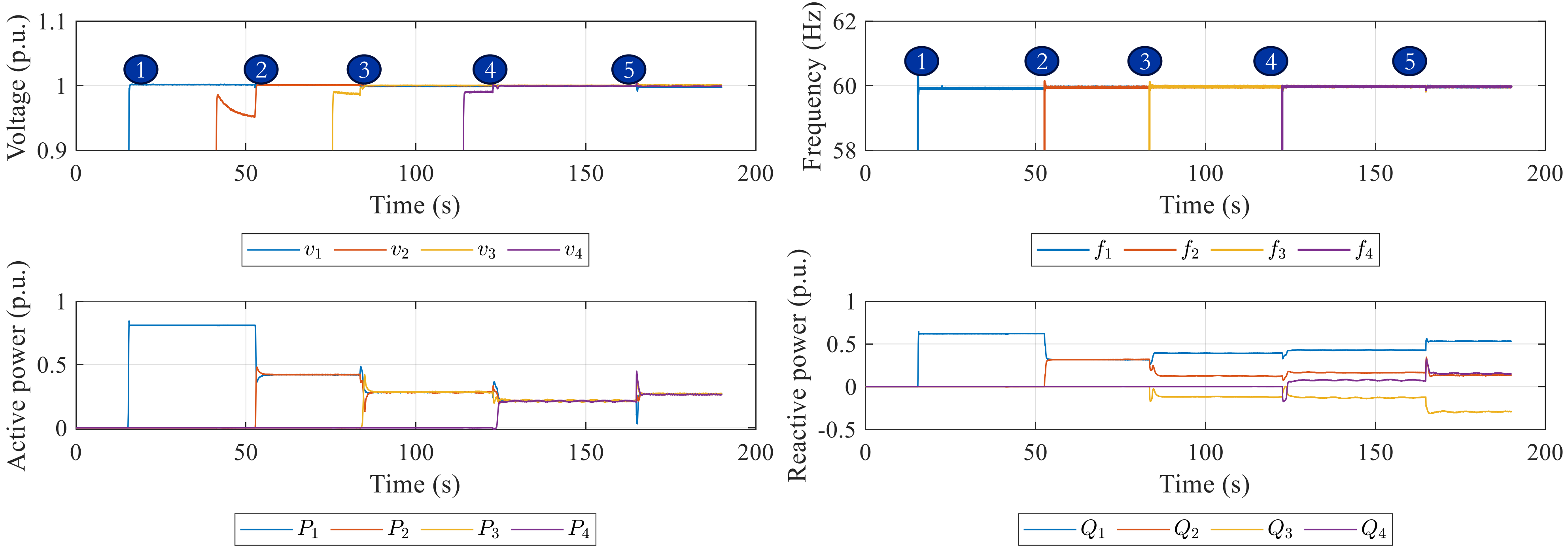
- **Limited computational resources**: DSP with one core cannot handle all the tasks in one time step.
- **Method:** Cores assignment
  - Core1: primary control, secondary control and clockwise communication
  - Core2: counterclockwise communication
  - Communication between core1 and core2 by global RAM



SIMULATION RESULT

- System under droop mode

1. Black start in droop mode: 1 Inverter 1 black starts 2 3 4 Inverters 2,3, and 4 plugin 5 Load changes

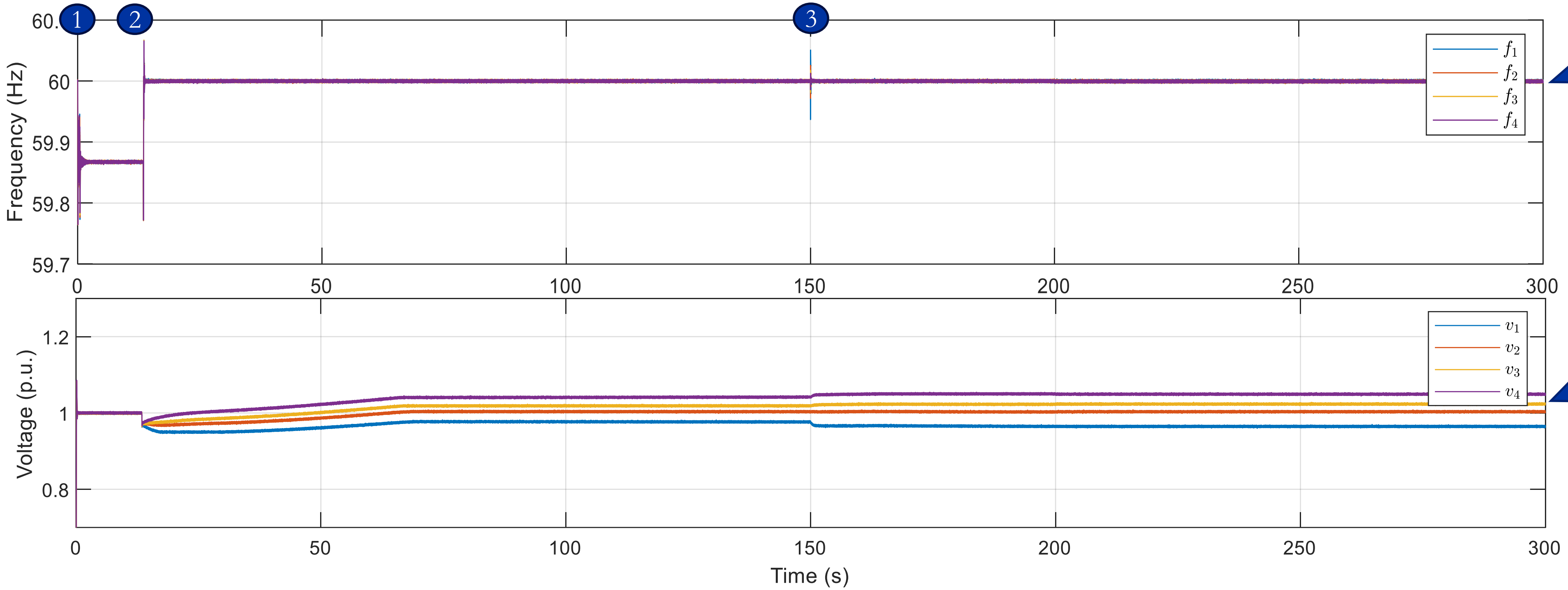


SIMULATION RESULT

- System under optimal control

2. Switch to optimal control:

1 Running in droop mode 2 Mode change 3 Load changes

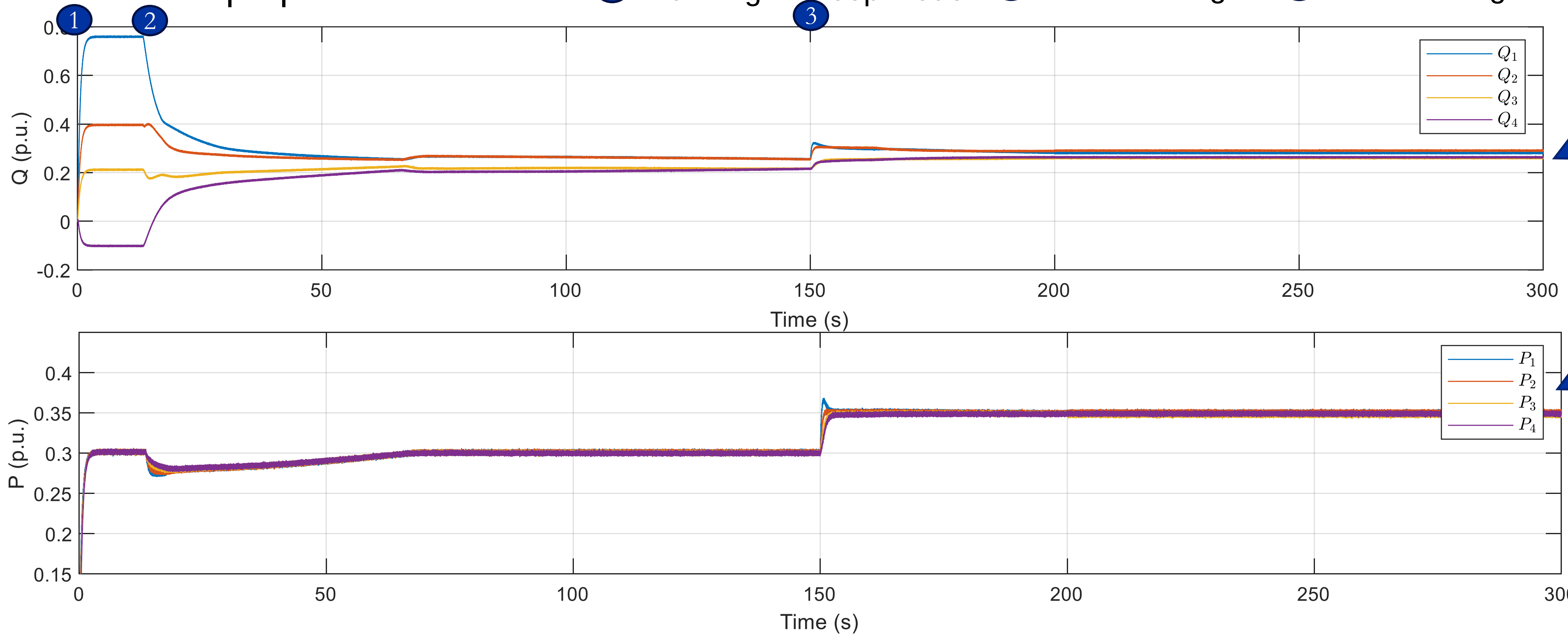


Restore the frequency to 60 Hz

Admissible voltage profile

SIMULATION RESULT

2.Shift to the proposed control: ① Running in droop mode ② Mode change ③ Load changes



Better reactive power sharing

Perfect active power sharing

Q & A

THANKS FOR YOUR LISTENING!