2DX4: Microprocessor System
PreLab 3

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is our own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Junbo Wang wangj430 400249823]**

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1.**What methods of analog to digital conversion does the MSP432E401Y ARM microcontroller use for its ADC? How many bits?**

The ADC of MSP432E401Y uses a Successive Approximation Register (SAR) architecture to deliver a 12-bit conversion value.

2.**Converting an analog signal to digital will result in quantization error - show the calculations and explain the MSP432E401Y's maximum quantization error.**

Max quantization error = (Vin_max - Vin_min)/2^12.
For instance, if the analogue signal is between 0 and 5 volts, the maximum quantization error is 5/212 = 1.22e-3 volts.

3.**Draw a flowchart outlining the steps to configure the ADC on the MSP432E401Y. Hint: there are 13 steps.**

1. Set bit 4 of SYSCTL RCGCGPIO R to enable clock for port E. Wait till the clock/port is ready/stable before proceeding.

2. Clear bit 4 of GPIO PORTE DIR R to make PE4 input.

3. Set bit 4 of GPIO PORT E AFSEL R to enable an alternate function on PE4.

4. Clear bit 4 of GPIO PORT E DEN R to disable digital I/O on PE4.

5. Set bit 4 of GPIO PORT E AMSEL R to enable analogue function on PE4.

6. Set bit 0 of SYSCTL RCGC ADC R to activate ADC0.

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7. By setting ADC0 PC R to 0x01, you can set the maximum speed to 125K samples/sec.

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8. Set ADC 0 SSPRI R to 0x0123 to give sequencer 3 the greatest priority. Clear bit 3 of ADC 0 ACTSS R to disable sample sequencer 3.

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9. Clear bit 15-12 in the ADC0 EMUX R register to set the sample sequencer's trigger event.

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10. In the ADC 0 SSMUX3 register, set the corresponding input source (in this case channel 9)

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11. Clear bit 0 and bit 3 in the ADC 0 SSCTL3 register and set bit 1 and bit 2 to configure the sample control bits in the corresponding nibble.

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12. Clear bit 3 in the ADC 0 IM R register to disable SS3 interrupts.

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13. By writing a 1 to the relevant ASEN3 register, sample sequencer 3 is enabled (bit 3).

4.Complete the table below assuming a 12-bit ADC (same as MSP432E401Y's ADC), assuming a full-scale voltage of 3.3V

Analog Voltage (Vh)	X-bit ADC (hex)
0.00	000
0.33	199
0.66	333
1.00	4D8
1.33	672

1.66	80B
2.00	9B1
2.33	B4B
2.66	CE4
3.00	E8A
3.30	FFF