YOUR Group Details:

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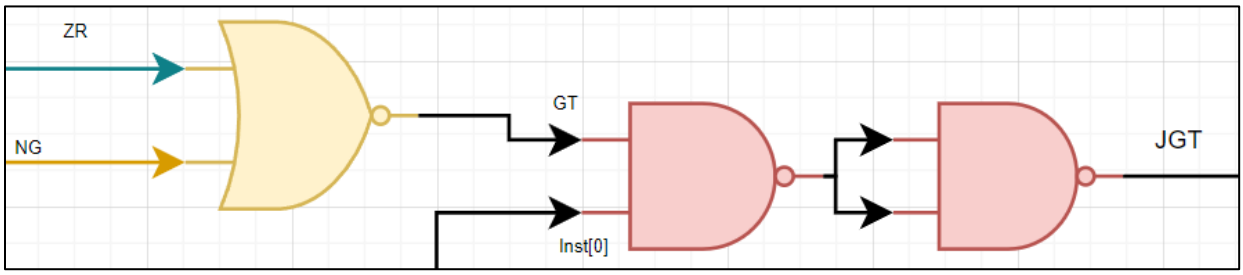
Justification of YOUR Circuitry Diagram Design:

(**NOTE**: No more than 300 words)

Figure 1.1

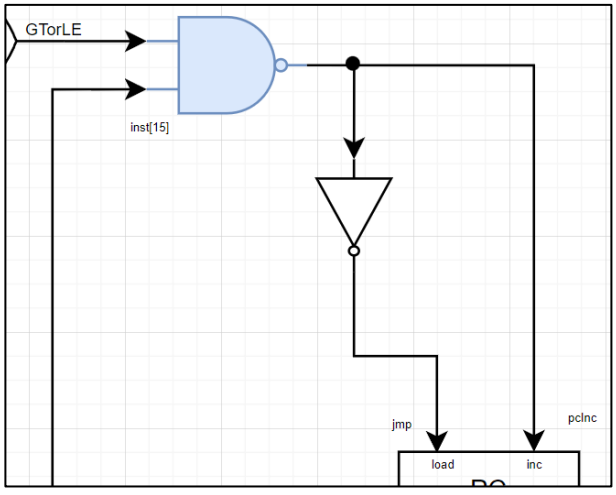
Producing JGT signal



JGT is 0 iff GT and inst[0] are both 1, where GT is 1 iff zr and ng are both 0. Thus in order to produce JGT, zr and ng from the ALU were first fed into a NOR gate which produces a 1 iff both inputs are 0. Then, the output was fed into a NAND gate along with [j3] which produces a 0 iff both inputs are 1. Nand2tetris does not have a built in NOR gate, so we optimised by directly using NOR instead of OR with NOT.

Figure 1.2

Producing jump and pcinc



Jump signal is 1 if either JGT or JLE is 1, so we feed JGT and JLE into an OR gate to produce jump. Inst[15] along with the jump signal were fed into a NAND gate to produce the load and

pcInc. Here, once again, Nand2tetris does not have a built in NAND gate, so we optimised by directly using NAND instead of OR with AND. The load is 1 iff both the jump signal and inst[15] is 1, thus we negate the output from the NAND gate.

We also utilised NAND gates (highlighted in red in circuit diagram) in place of every AND gate required. We did this with two NAND gates, where the output of the first NAND gate will be the two inputs of the second NAND gate. Using NAND gates allow better performance because NAND gates are faster and cheaper to produce than AND gates due to fewer transistor count and smaller overall size. However, we maintained the OR gates instead of replacing them with NOR gates because contradictory to NAND with AND gates, NOR gates are harder to produce than OR gates.

References

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4) Rattan, A. (2023, May 21). *The reason behind the inexpensive cost of NAND gates - Javascript*. CopyProgramming. https://copyprogramming.com/howto/why-are-nand-gates-cheap