Report

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Control unit

The input of the control unit is the 32-bit instruction. And there are 10 outputs of the control unit, the ports are RegDst, ALUSrc, MemtoReg, RegW, MemR, MemW, Branch, Bne, Bgtz and the 4-bit ALUCtr.

When RegDst outputs 0, the register destination number for the write register comes from the rt field. Otherwise it comes from the rd field.

When ALUSrc outputs 0, the second ALU operand comes from the second register file output. Otherwise, the second operand is the sign-extended.

When MemtoReg outputs 0, the value fed to the register Write data input comes from the ALU. Otherwise, the value comes from the memeory.

When RegW outputs 1, the register is written with the value on the Write data input.

When MemR outputs 1. Data memory contents designated by the address input are put on the Read data output.

When MemW outputs 1, Data memory contents designated by the address input are replaced by the value on the Write data input.

When Branch outputs 1, IF unit will check Zero flag to determine branch or not.

When Bne outputs 1, IF unit will check Zero flag to determine branch or not.

When Bgtz outputs 1, IF unit will check Zero flag and R[s]' MSB to determine branch or not.

And the control can be divided into 2 parts. One is the main control and another is the alu control.

Main control

The input of the main control 26-31 bit instruction. And the outputs are RegDst, ALUSrc, MemtoReg, RegW, MemR, MemW, Branch, Bne, Bgtz and 2-bit ALU_op which is used to control the alu control.

And table below is the truth table of the main control.

				ma	ain co	ntrol tr	uth tak	ole				
	ОР	RegDs t	ALUSr c	MemtoRe g	Reg W	Mem R	Mem W	V h E Z		BGT Z	ALU_op(1)	ALU_op(0)
R-typ e	00000 0	1	0	0	1	0	0	0	0	0	1	0

LW	10001 1	0	1	1	1	1	0	0	0	0	0	0
SW	10101 1	x	1	x	0	0	1	0	0	0	0	0
ADDI	00100 0	0	1	0	1	0	0	0	0	0	0	0
BEQ	00010 0	x	0	x	0	0	0	1	0	0	0	1
BNE	00010 1	x	0	x	0	0	0	0	1	0	0	1
BGT Z	00011 1	x	0	x	0	0	0	0	0	1	0	1

As we can see there are 7 different types of operations.

When the operation is R-type, the register destination number for the write register comes from the rd field. the second ALU operand comes from the second register file output. the value fed to the register Write data input comes from the ALU. And the register is written with the value on the Write data input. And R-type will not use the memory.

When the operation is LW, the register destination number for the write register comes from the rt field. And the second operand comes from the sign-extended. It will read the data from the memory and write into the register.

When the operation is SW, it do not need the register. And the second operand comes from the sign-extended. And write the output of the alu into memory.

When the operation is ADDI, the register destination number for the write register comes from the rt field. The second operand coms from the sign-extended. And need to write the output data of the alu into register.

When the operation is BEQ, only the IF unit and zero flag matter. If zero flag is set then pc = pc + 4 + offset * 4.

When the operation is BNE, if zero flag is not set then pc = pc + 4 + offset * 4.

When the operation is BGTZ, if zero flag is not set and [Rs] is greater than zero then pc = pc + 4 + offset * 4.

ALU control

The inputs of the ALU control are instruction of 0 to 5 bit, and the ALU_op. And the output of the ALU control is the 4 bits ALUCtr.

And table below is the truth table of the ALU control.

ALU _	ор	Func	ALUCtr	operation	
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00	xxxxxx	0011	add
00	xxxxxx	0011	add
01	xxxxxx	0111	sub
01	xxxxxx	0111	sub
01	xxxxxx	0111	sub
00	xxxxxx	0011	add
10	100000	0011	add
10	100001	0011	add
10	100010	0111	sub
10	100011	0111	sub
10	100100	0000	and
10	100101	0001	or
10	000000	1000	sll
10	101010	0100	slt
10	101011	0101	sltu

As we can see, the ALU_op data of the R-type operation is 10. And ALU_op of the SW,LW,ADDI are 00. The ALU_op of the BEQ,BNE,BGTZ are 01. The ALUCtr is just the signal that control the ALU. Then we just combine this two parts and get the whole control unit.

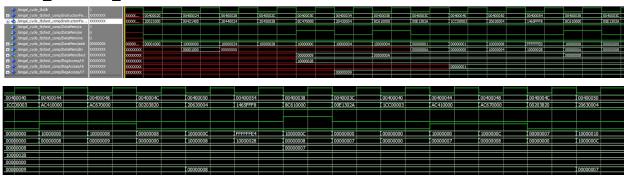
Problem in the Project

One problem is how to use the clock signal in Reg_file. Since we only write back at falling edge of the clock, we use a and gate to sync the write back and the clk.

Another problem is we need to add two more signals to the control unit to distinguish between beq, bne and bgtz. They are all branch but have different branch conditions.

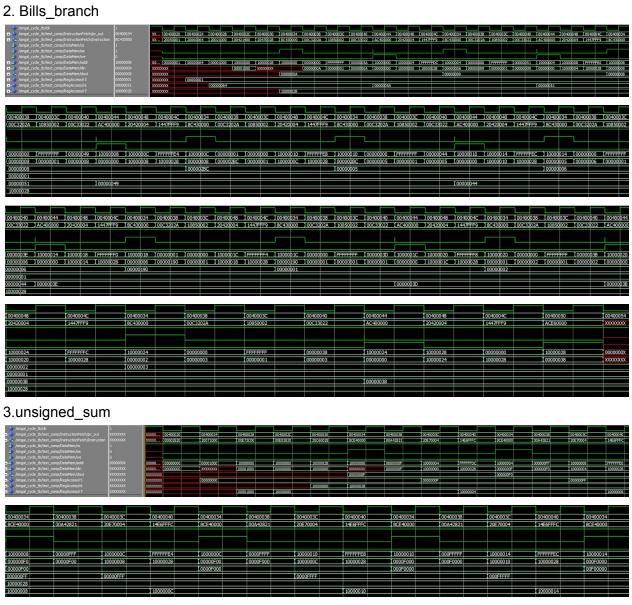
Trace

1. Sort_corrected_branch



(00400054 (1465FFF8	00400038 8C610000	(0040003C (00E1302A	(00400040 (1CC00003	(00400044 (AC410000	(00400048 (AC670000	(0040004C (00203820	(00400050 (20630004	00400054 146SFFF8	00400038 8C610000	0040003C 00E1302A	(00400040 (1000003	200400050 20630004
(FFFFFE8 (10000028 10007 10028 10000	10000010 10000007 10000005	(00000000	(0000000	10000000	10000010	(00000005	10000014 10000010	XFFFFFEC X 10000028	10000014 10000005 10000006	00000001 00000005	X0000001 X0000000 X0000001	10000018
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	X00400038 X0040003C X8C610000 X00€1302A											
10000028	X10000024 X00000001 X00000002 X00000003 X00000003	(00000001) 1000002 (00000000) 1000002	8	000000 (10000024	X1000004 X100000 X0000001 X100000 X000000A	08	0000000 X00000000 0000009 X00000000 X00000000	[10000004] 10000 [00000009] 10000	000A (00000000 (1000000C	4 X1000000C X0000 8 X00000009 X0000 X00000008	0000 (00000000) 0008 (00000000)
00400044 AC410000	(00400048	(0040050 (0040054 (20630004 (1465FF8	(00400038 (004000 (8C610000 (00E13	03C (0040040 (004 02A (1CC00003 (AC	000044 X00400048 X 410000 XAC670000 X	0040004C 10040055 00203820 120630004	0 (0040054 (0040 4 (1465FF8 (806)	00038 (0040003C) 10000 (00E1302A)	00400040 (00400044 1CC00003 (AC410000	(00400048 (00400 (AC670000 (00203	04C (00400050 (00- 820 (20630004)144	400054
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	X0000000 X1000004 X0000000 X0000005											
(20630004	X00400054 X00400038 X1465FFF8 X8C610000 XFFFFFFFC X10000024	X00E1302A X1CC00003) 20630004 1465F	FF8 20420004 14	44FF4 (8C470000	X20430004 X8C61000	00	C00003 (AC410000	XAC670000 X0020382	0 (20630004 (146)	5FFF8	00E1302A (1CC00003
X 10000020 00000002 10000028 00000000 X 00000002	(10000028 (00000002 (00000003	100000001 100000001) 10000024	028 10000004 10	000024 (00000002 (0000000A	(10000028 (1000000) (10000000) (10000000A	03 <u>(00000009 (000</u> 09	000000 (00000009	(2000000A (20000000	(00000009	00028 X0000009 X0	0000008 (0000000
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	00000005 100000000 1			1C X1000028 X000 X000						00000003 (00000		

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