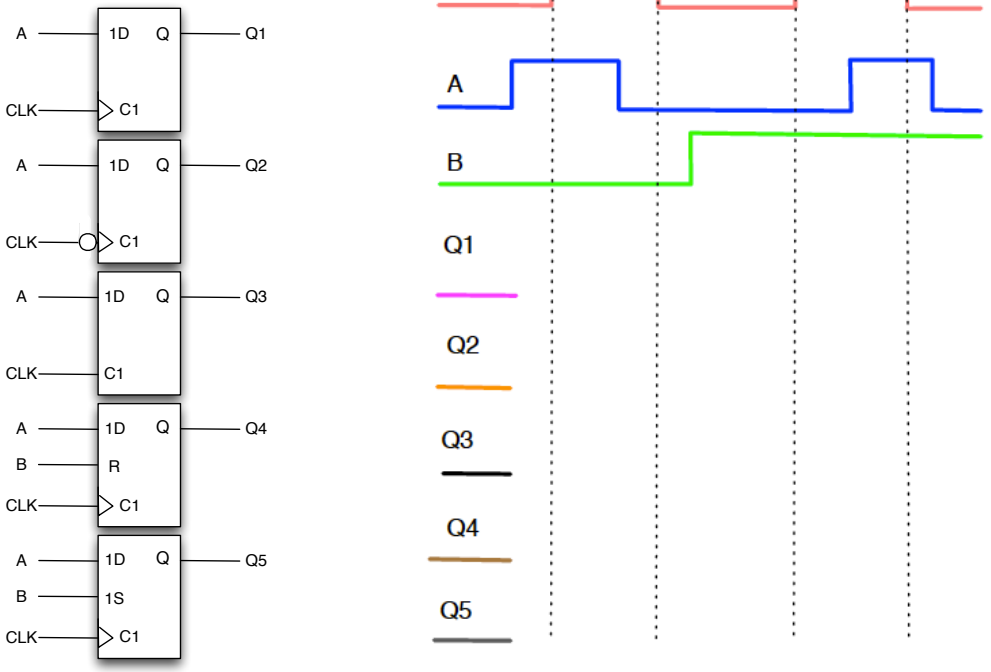
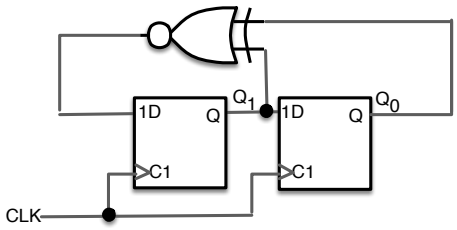
Preparação para Mini-testes 5

1.- Desenhe as formas de onda dos seguintes flip-flops e latches.



2.- Desenhe a forma de onda (4 ciclos de relogio) do seguinte circuito a partir de uma saida Q_1Q_0=10.



3.- Obtenha um flip-flop tipo D e outro tipo T usando flip-flops tipo JK.

J	K	Q
0	0	q
0	1	0
1	0	1
1	1	$\overline{q}$

4.- Qual das opções corresponde com o VHDL apresentado:

```
library ieee;
use ieee.std_logic_1164.all;
entity REG4 is port (
     CLK:  in std_logic;
     ST:  in std_logic;
     EN:  in std_logic;
     D:  in std_logic_vector(3 downto 0);
     Q: out std_logic_vector(3 downto 0)
          );
end REG4;
architecture behv of REG4 is
begin
     process (CLK,  ST, D, EN)
     begin
          if ST = '1' then
               Q <= '1111';
          elsif CLK'event and CLK = '1' then
                    if EN = '1' then
                         Q <= D;
                     end if;
          end if;
     end process;
end behv;
```