Intro to the Intel x64

Part 2

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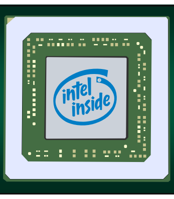

The Intel x64

It was simple at first…

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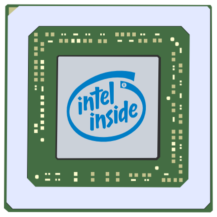
The Intel x64

- The Intel x64 is the main processor used by servers, laptops, and desktops
- It has evolved continuously over a 40+ year period



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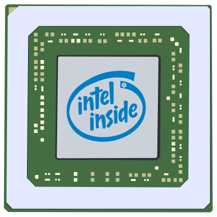
The Original x86

- First "x86" was the 8086
- Released in 1978
- Attributes:
  - 16-bit registers
  - 16 registers
  - could access of 1MB of RAM *(in 64KB blocks using a special "segment" register)*



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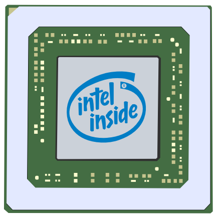
What to call the processor

- The classic term "x86" refers to the 32-bit and 16-bit processor family
- With move to 64-bit, the term "x64" is used to differentiate the newest design from the previous



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Original x86 Registers

It was simple at first…

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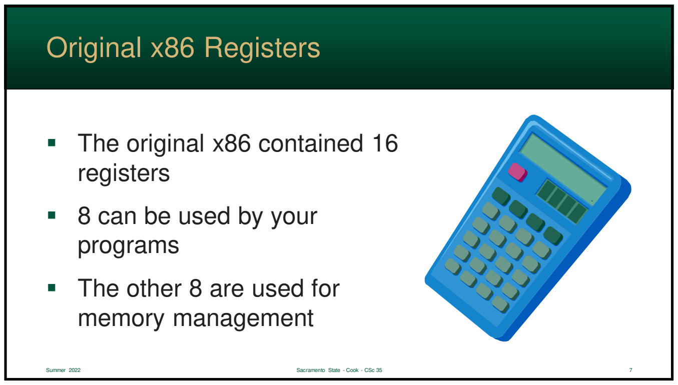

Original x86 Registers

- The original x86 contained 16 registers
- 8 can be used by your programs
- The other 8 are used for memory management

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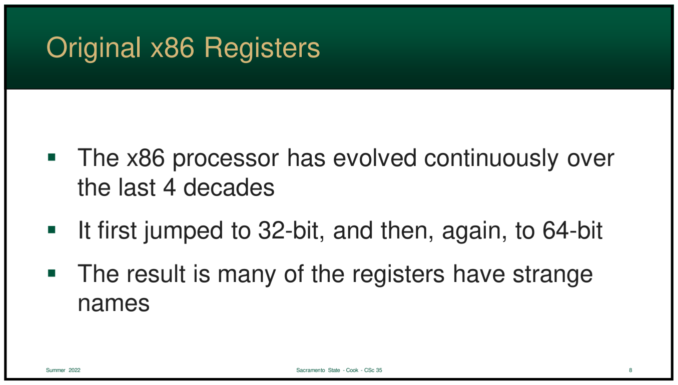

Original x86 Registers

- The x86 processor has evolved continuously over the last 4 decades
- It first jumped to 32-bit, and then, again, to 64-bit
- The result is many of the registers have strange names

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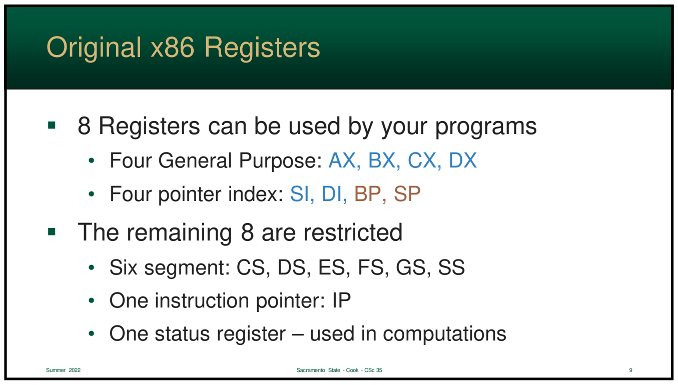

Original x86 Registers

- 8 Registers can be used by your programs
  - Four General Purpose: AX, BX, CX, DX
  - Four pointer index: SI, DI, BP, SP
- The remaining 8 are restricted
  - Six segment: CS, DS, ES, FS, GS, SS
  - One instruction pointer: IP
  - One status register – used in computations

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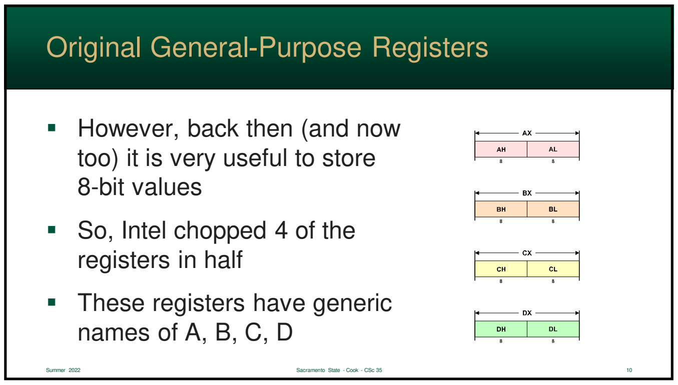
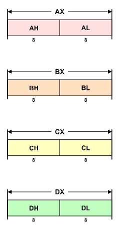


Original General-Purpose Registers

- However, back then (and now too) it is very useful to store 8-bit values
- So, Intel chopped 4 of the registers in half
- These registers have generic names of A, B, C, D



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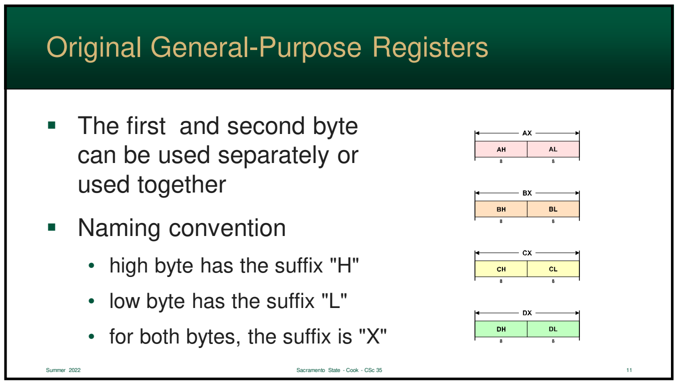
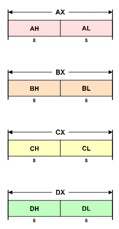


Original General-Purpose Registers

- The first and second byte can be used separately or used together
- Naming convention
  - high byte has the suffix "H"
  - low byte has the suffix "L"
  - for both bytes, the suffix is "X"



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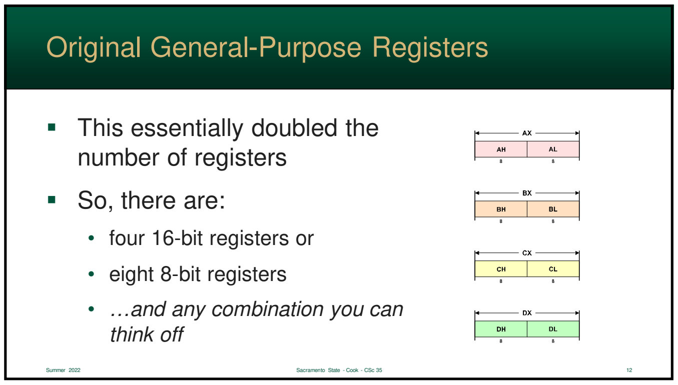
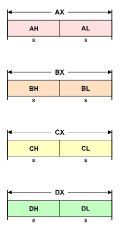


Original General-Purpose Registers

- This essentially doubled the number of registers
- So, there are:
  - four 16-bit registers or
  - eight 8-bit registers
  - *…and any combination you can think off*



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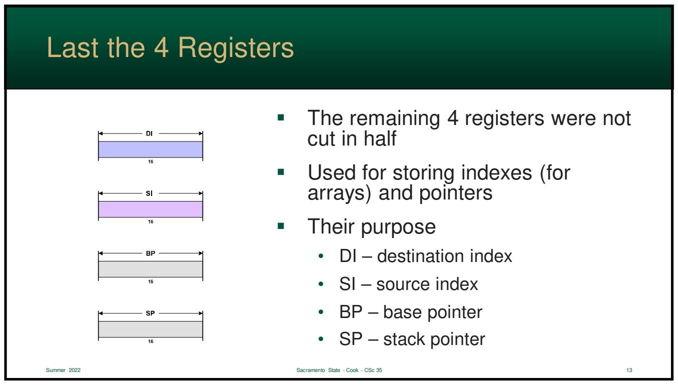

Last the 4 Registers

- The remaining 4 registers were not cut in half
- Used for storing indexes (for arrays) and pointers
- Their purpose
  - DI – destination index
  - SI – source index
  - BP – base pointer
  - SP – stack pointer

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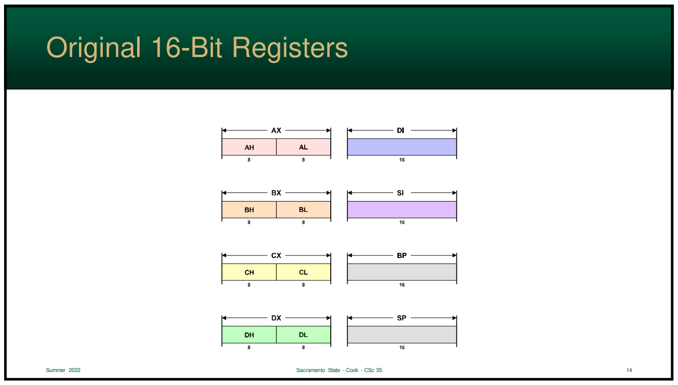

Original 16-Bit Registers

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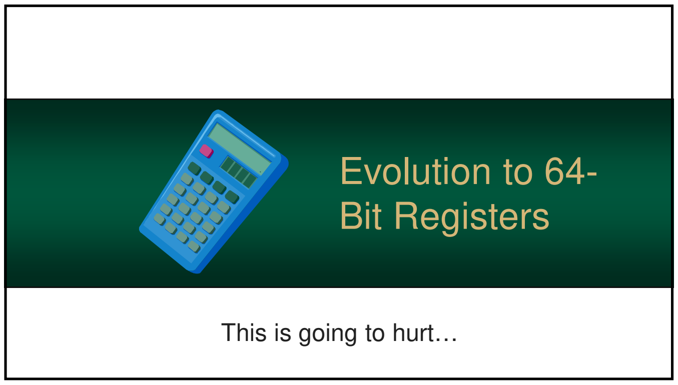

Evolution to 64-Bit Registers

This is going to hurt…

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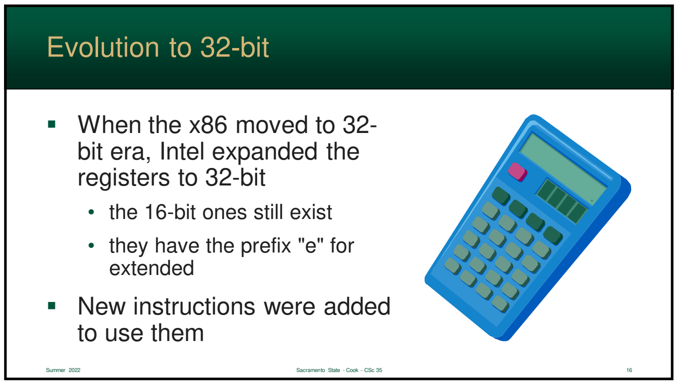

Evolution to 32-bit

- When the x86 moved to 32-bit era, Intel expanded the registers to 32-bit
  - the 16-bit ones still exist
  - they have the prefix "e" for extended
- New instructions were added to use them

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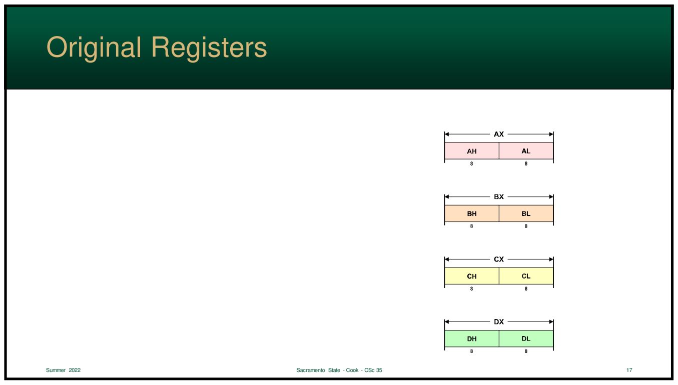

Original Registers

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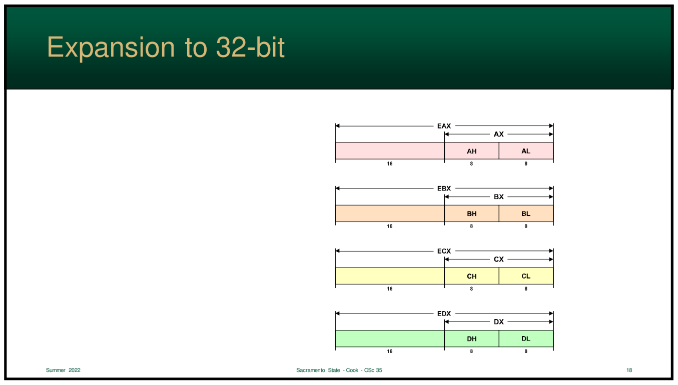

Expansion to 32-bit

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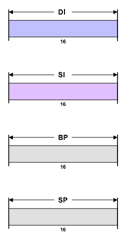
Original Registers



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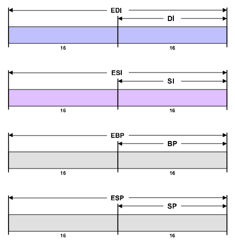
Expansion to 32-bit



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Evolution to 64-bit

- At this point, Intel had decided to abandon the x86 in lieu of their new Itanium Processor
- The Itanium was a radically different design and was completely incompatible
- Advanced Micro Devices (AMD), to Intel's chagrin, decided to – *once again* – extend the x86

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Evolution to 64-bit

- Registers were extended again
  - 64-bit registers have the prefix *"r"*
  - 8 additional registers were added
  - also, it is now possible to get 8-bit values from all registers (hardware is more consistent!)
- Some old, archaic, features were dropped

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Evolution to 64-bit

- The AMD-64 was a huge commercial *success*
- The Itanium was a commercial *failure*
- Intel, dropped the Itanium and started making 64-bit x86 using AMD's design

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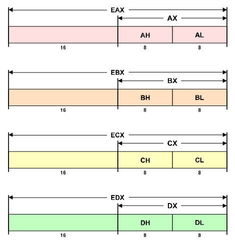
Expansion to 64-bit



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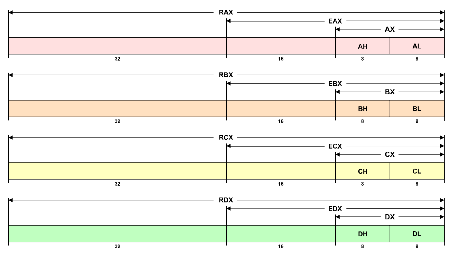
Expansion to 64-bit



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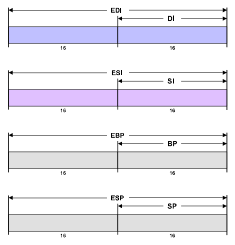
Expansion to 64-bit



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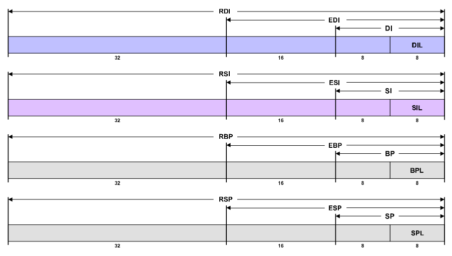
Expansion to 64-bit



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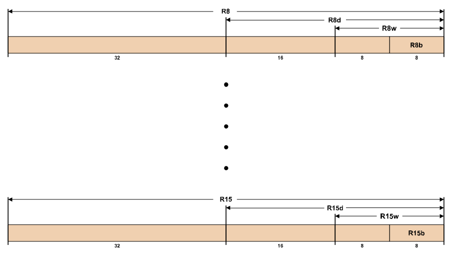
New 64-bit Registers: R8…R15



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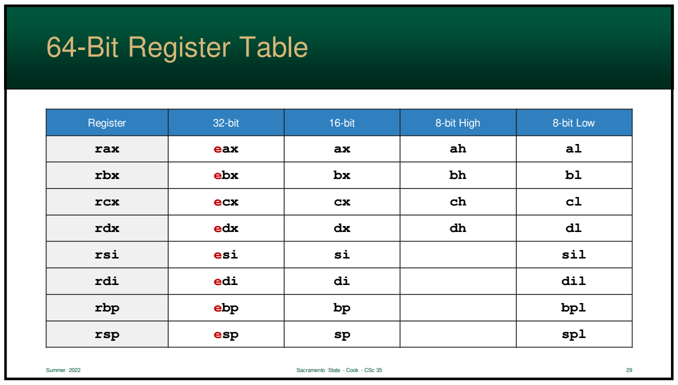
64-Bit Register Table



Register	32-bit	16-bit	8-bit High	8-bit Low
rax	eax	ax	ah	al
rbx	ebx	bx	bh	bl
rcx	ecx	cx	ch	cl
rdx	edx	dx	dh	dl
rsi	esi	si		sil
rdi	edi	di		dil
rbp	ebp	bp		bpl
rsp	esp	sp		spl

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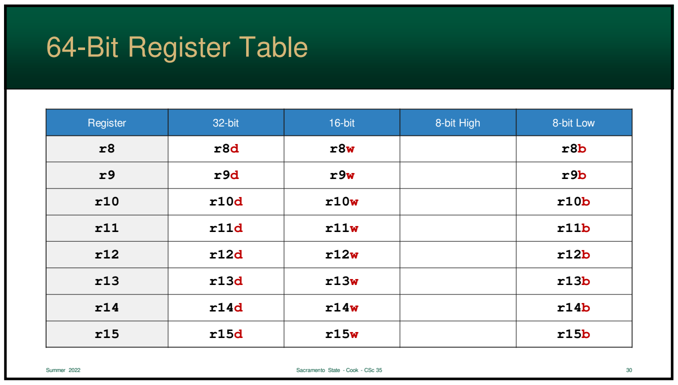
64-Bit Register Table



Register	32-bit	16-bit	8-bit High	8-bit Low
r8	r8d	r8w		r8b
r9	r9d	r9w		r9b
r10	r10d	r10w		r10b
r11	r11d	r11w		r11b
r12	r12d	r12w		r12b
r13	r13d	r13w		r13b
r14	r14d	r14w		r14b
r15	r15d	r15w		r15b

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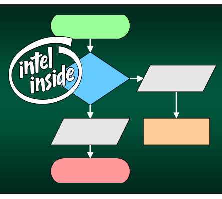

Basic Intel x86 Instructions

Feel the pow-wah of the x86!

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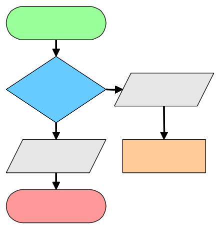
Basic Intel x86 Instructions

- Each x86 instruction can have up to 2 operands
- Operands in x86 instructions are very versatile
- Each operand can be either a memory address, register or an immediate value



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Types of Operands

- Registers
- Address in memory
- Register pointing to a memory address
- Immediate

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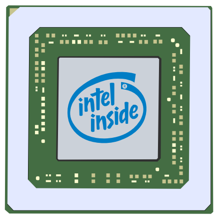
Intel x86 Instruction Limits

- There are some limitations…
- Some instructions must use an immediate
- Some instructions require a *specific* register to perform calculations



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Intel x86 Instruction Limits

- A register must always be involved
  - processors use registers for all activity
  - both operands cannot access memory at the same time
  - *the processor has to have it at some point!*
- Also, obviously, the receiving field cannot be an immediate value

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Instruction: Move

- The Intel *Move Instruction* combines transfer, load and store instructions under one name
- … well, that's something the assembler does for us – but, we'll cover that soon
- "Move" is a tad confusing – it copies data

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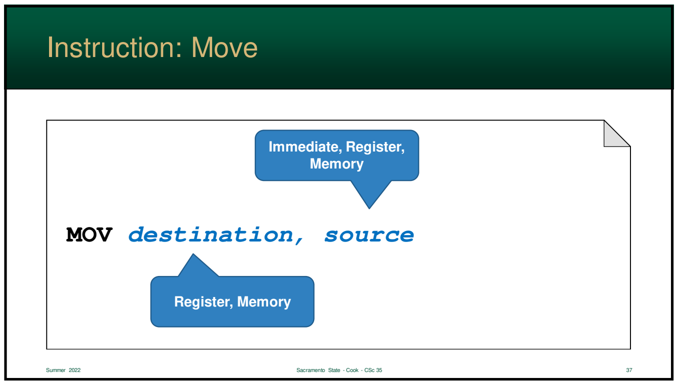

Instruction: Move

Immediate, Register, Memory

```
MOV destination, source
```

Register, Memory

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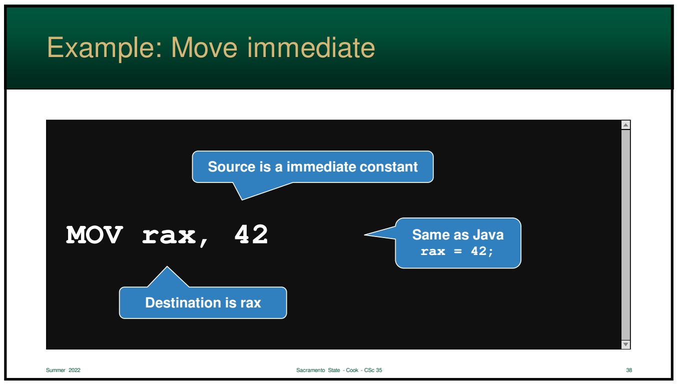

Example: Move immediate

Source is a immediate constant

```
MOV rax, 42
```

Same as Java `rax = 42;`

Destination is rax

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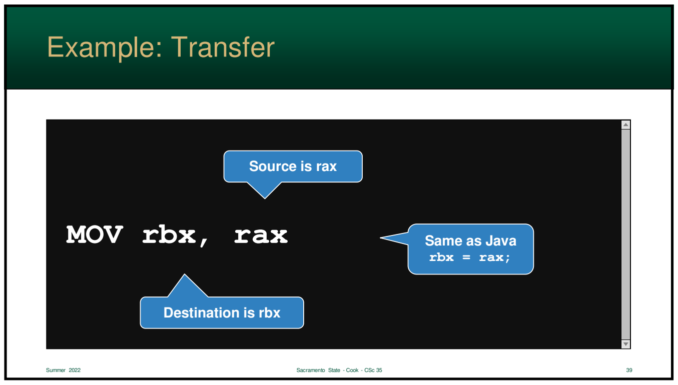

Example: Transfer

Source is rax

```
MOV rbx, rax
```

Same as Java `rbx = rax;`

Destination is rbx

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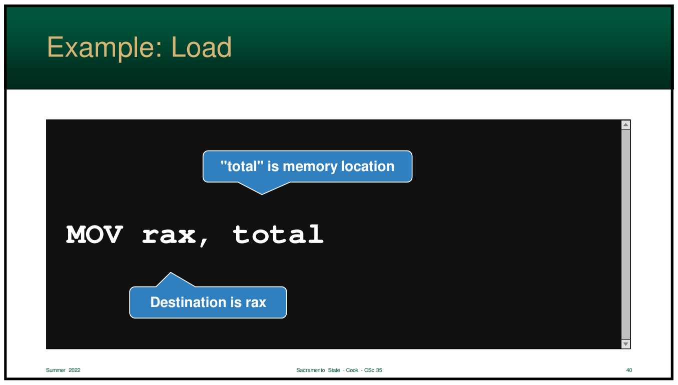

Example: Load

"total" is memory location

```
MOV rax, total
```

Destination is rax

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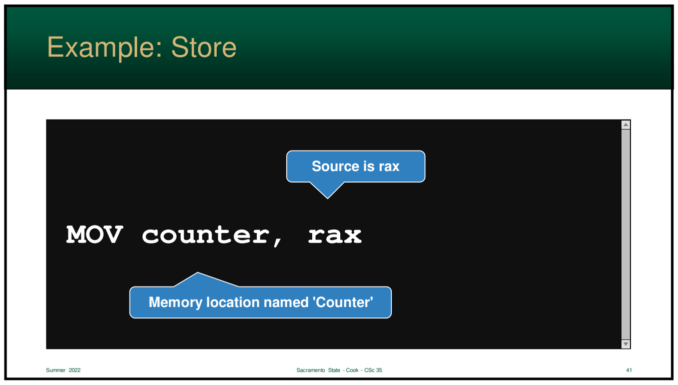

Example: Store

Source is rax

```
MOV counter, rax
```

Memory location named 'Counter'

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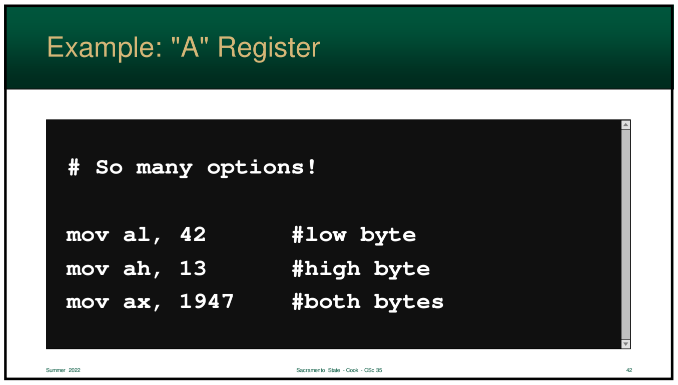

Example: "A" Register

```
# So many options!

mov al, 42      #low byte
mov ah, 13      #high byte
mov ax, 1947    #both bytes
```

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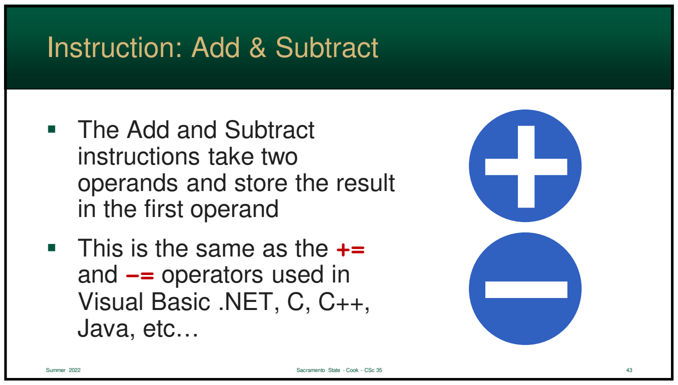

Instruction: Add & Subtract

- The Add and Subtract instructions take two operands and store the result in the first operand
- This is the same as the **+=** and **−=** operators used in Visual Basic .NET, C, C++, Java, etc…

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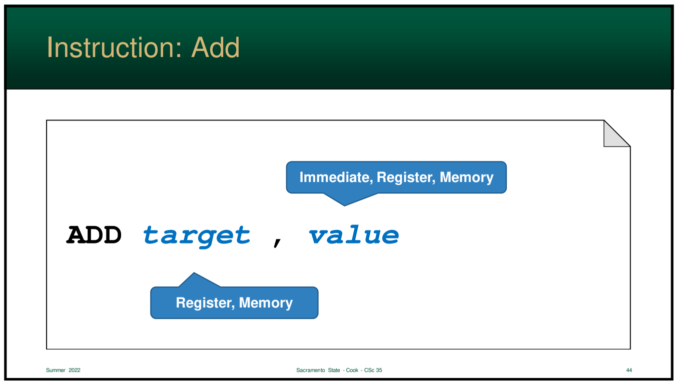

Instruction: Add

Immediate, Register, Memory

```
ADD target , value
```

Register, Memory

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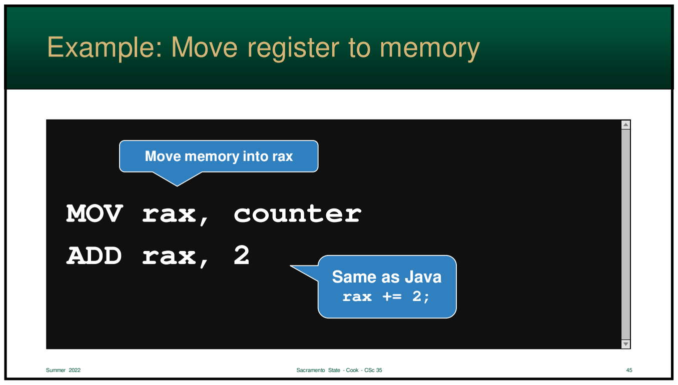

Example: Move register to memory

Move memory into rax

```
MOV rax, counter
ADD rax, 2
```

Same as Java
`rax += 2;`

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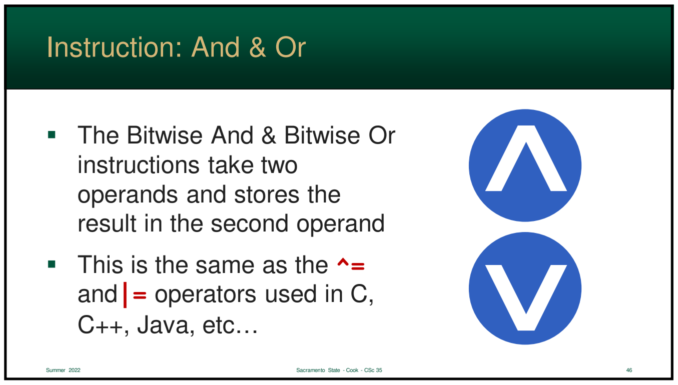

Instruction: And & Or

- The Bitwise And & Bitwise Or instructions take two operands and stores the result in the second operand
- This is the same as the **^=** and **|=** operators used in C, C++, Java, etc…

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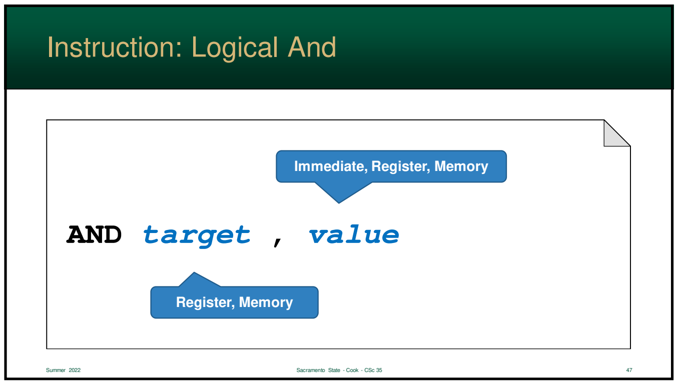

Instruction: Logical And

Immediate, Register, Memory

```
AND target , value
```

Register, Memory

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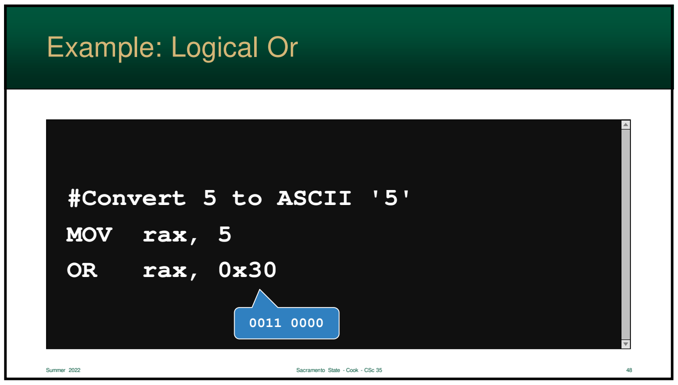

Example: Logical Or

```
#Convert 5 to ASCII '5'
MOV  rax, 5
OR   rax, 0x30
```

0011 0000

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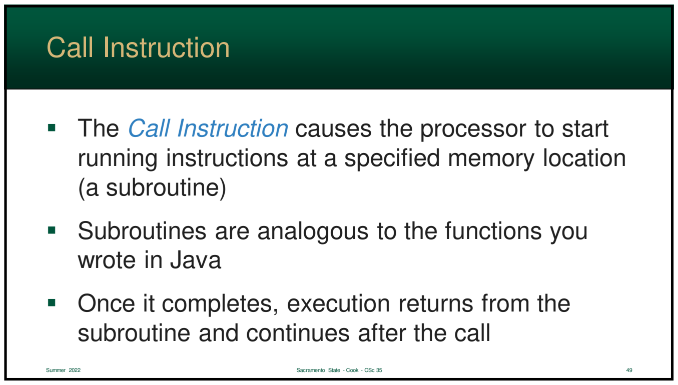

Call Instruction

- The *Call Instruction* causes the processor to start running instructions at a specified memory location (a subroutine)
- Subroutines are analogous to the functions you wrote in Java
- Once it completes, execution returns from the subroutine and continues after the call

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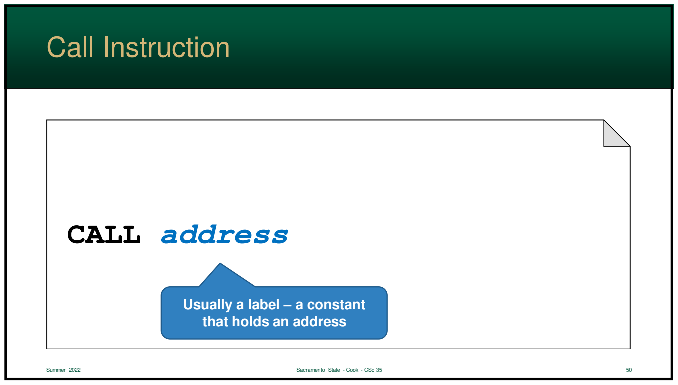

Call Instruction

```
CALL address
```

Usually a label – a constant that holds an address

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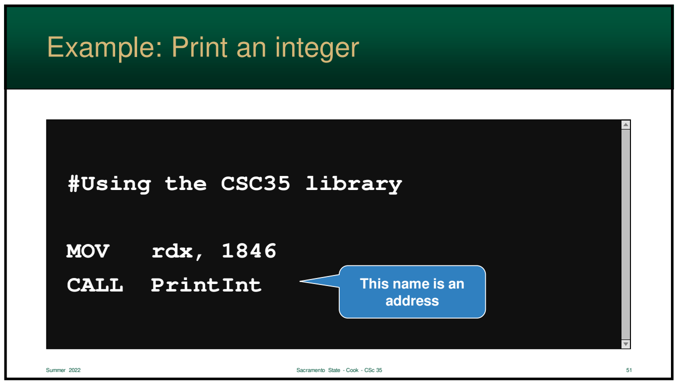

Example: Print an integer

```
#Using the CSC35 library

MOV   rdx, 1846
CALL  PrintInt
```

This name is an address

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