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HW#5
CSc 137

Problem I: Consider the sequential circuit in Figure 5.31 where the adder is a CLA. Its simplified circuit is shown in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, AND gate = 0.2 ns and EXOR = 0.3 ns determine the upper bound for its clock frequency. (10 pts)

1)

Longest Path Delay

$= \Delta AND + \Delta EXOR + \Delta AND + \Delta To_{Flip}$

$= 0.2ns + 0.3ns + 0.2ns + 0.3ns$

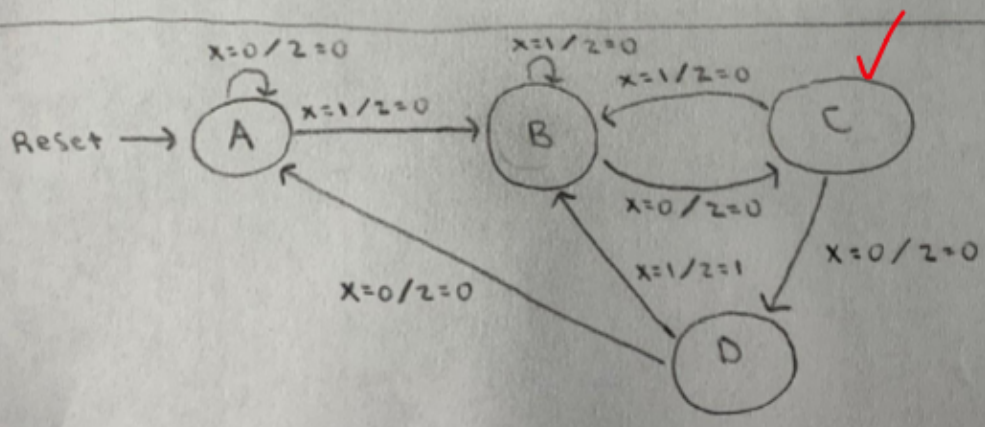
$= 1.0ns$

Upper Bound Frequency

For the first flip flop from right in figure 5.32 the clock-skew time will be (0.1+0.1) = 0.2 ns. Now adding the clock-to-Q time and register setting up time to this we get, 0.4 ns. So the clock frequency maximum should be $1/(0.4ns) = 2.5 * 10^9$ Hz

$\boxed{1/(0.4ns) = 2.5 * 10^9 Hz}$ -1

3)



Problem III: Textbook problem 5.11 (only FSD) (5 pts)