HW #1

CSc 137, Harvey

Total (12 pts)

Problems 1.3, 1.4 , 1.5, 1.14 (3 pts each)

Reading assignment: Section 1.1 to 1.4 (all sub-sections).

Advance reading assignment: Section 2.1 through 2.4 (all subsections)

1.3. What is the 16-bit FP number representation of −5.375 in hex with 1-bit sign, 4-bit biased exponent, and 11-bit fraction, where bias offset = 7?

−5.375

5 = 101

.375 = .011

−5.375 in binary is 101.011

$= 1.01011 \times 2^2$

(scientific notation)

Since the number is a negative one, Sign bit is also 1

Exponent = 2 + bias

= 2 + 7

= 9

8421 → 8+1

= 1001

fraction = 01011

The 16 bit FP number is

1 1001 01011000000

X

-1

1.4. What is the real number equivalent to FP number 0x3400 with 1-bit sign, 4-bit biased exponent, 11-bit fraction, and bias offset = 7?

0 x 3400 = 0011 0100 0000 0000

$Real = (-1)^S \times (1 + Fraction) \times 2^e$

$Real = (-1)^0 \times (1 + 0.25) \times 2^{-4}$

$Real = 1 \times 1.25 \times 2^{-4}$

$Real = \frac{1.25}{16}$

Real = 0.078125 ✓ X

1.5. What is the real number equivalent to FP number 0x3400 with 1-bit sign, 4-bit biased exponent, 11-bit fraction, and bias offset = 8?

0 x 3400 = 0011 0100 0000 0000

Sign bit = 0

biased exponent = 0110

fraction = 100 0000 0000

The given FP number is 0x3400, which is a 16-bit binary number. To convert this to its binary equivalent, we can write each hexadecimal digit as its 4-bit binary equivalent.

Thus, 0x34 can be written as 0011 0100 and 0x00 can be written as 0000 0000. Therefore, the binary equivalent of the given FP number is:

$100\ 0000\ 0000 = 1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} + \ldots + 0 \times 2^{-11} = 0.5$

$(-1)^{signbit} \times (1 + fraction) \times 2^{(biased\ exponent - bias\ offset)}$

Plugging in values, we get

$(-1)^0 \times (1 + 0.5) \times 2^{6-8}$

$= 1.5 \times 2^{-2} \rightarrow \boxed{0.375}$

1.14 What is a Von Neumann architecture bottleneck?

The Von Neumann architecture bottleneck is a limitation on throughput caused by the standard personal computer architecture. This architectural design consists of a Central Processing Unit and a single shared memory for both data and instructions.