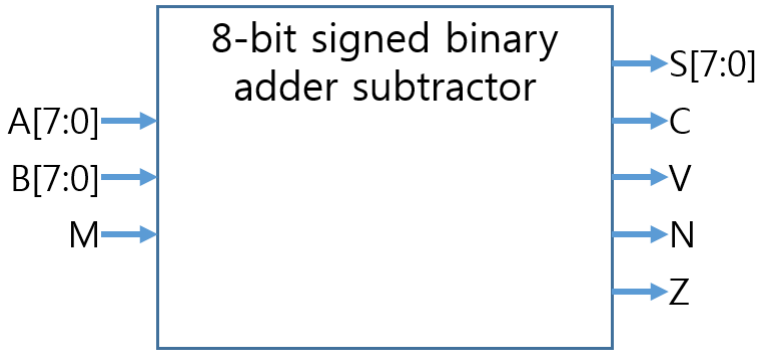
Project 1

(COSE221 Digital Logic Design, Spring 2016)

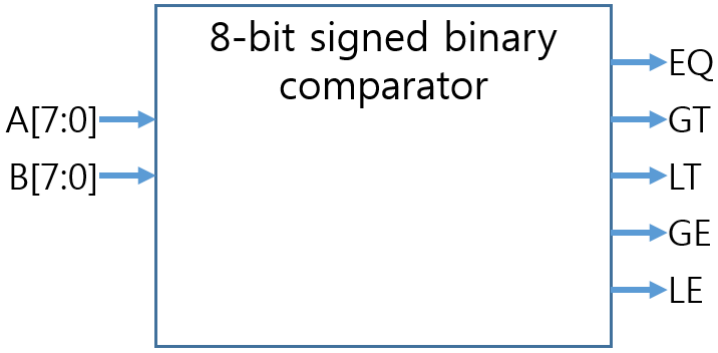
In this project, you should describe your designs ONLY with gate-level model, except for testbench.

1. Design the 8-bit signed binary adder-subtractor with following functionalities.



- input : A, B, M
- output : S, C, V, N, Z
- S : A + B
- C : carry
- V : overflow
- N : negative
- Z : zero

2. Design the 8-bit signed binary comparator with the adder-subtractor implemented in 1.



- EQ : A == B, Equal
- GT : A > B, Greater Than
- LT : A < B, Less Than
- GE : A >= B, Greater than or Equal
- LE : A <= B, Less than or Equal

※ Submission list

- Verilog files describing above modules
- Verilog files for testbench
  (testbench should cover all the combinations of inputs.)
- Images capturing simulation waveform