CSC258H1: Pre-lab Exercise for Lab 1

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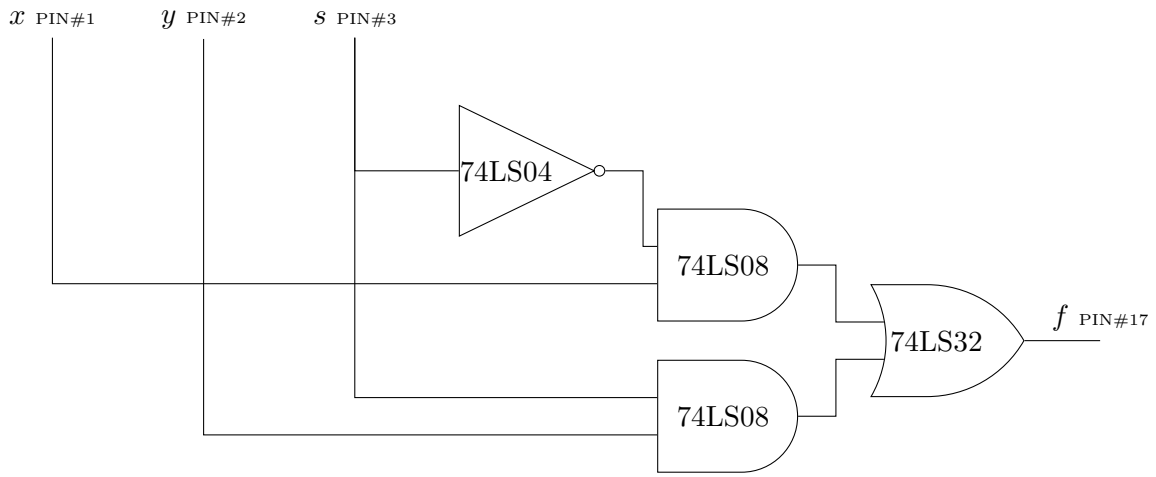
Due: January 14, 2018 before 12 a.m.

1 Part I

1. Draw a 2-to-1 multiplexer design using the gates specified above. Indicate pin numbers on the chips. You do not need to draw the entire chip, but you must specify which chip was used for which gate and which pins the inputs and outputs are connected to. Show this design to your TA as part of your pre-lab to verify that the design is correct before you start to implement it.

Solution.



Chips Used:

- 74LS04;
- 74LS08;
- 74LS32.

2. Write out the truth table for the design and show that to the TA as well as part of the pre-lab.

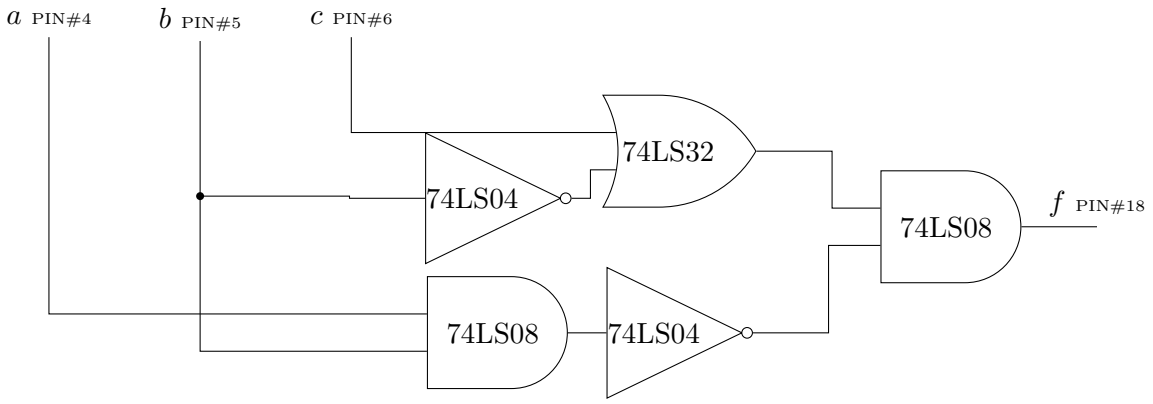
Solution. The truth table is as follows:

x	y	s	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

2 Part II

1. Draw the function shown above using the gates specified in the lab preparation. Indicate pin numbers on the chips. You do not need to draw the entire chip, but you must specify which chip was used for which gate and which pins the inputs and outputs are connected to. Show this design to your TA as part of your pre-lab to verify that the design is correct before you start to implement it.

Solution.



Chips Used:

- 74LS04;
- 74LS08;
- 74LS32.

2. Write out the truth table for your design and show it to the TA as another part of the pre-lab.

Solution. The truth table is as follows:

x	y	s	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

3. Is there a cheaper implementation for your design, assuming you are still limited to using the same three chip types? If yes, explain by rewriting the boolean function. For this question we consider a given implementation cheaper if it uses fewer gates or if it uses the same number of gates but fewer chips.

Solution.

$$\begin{aligned} f &= (a+b)' + cb' \\ &= a'b' + cb' \\ &= (a'+c)b' \end{aligned}$$