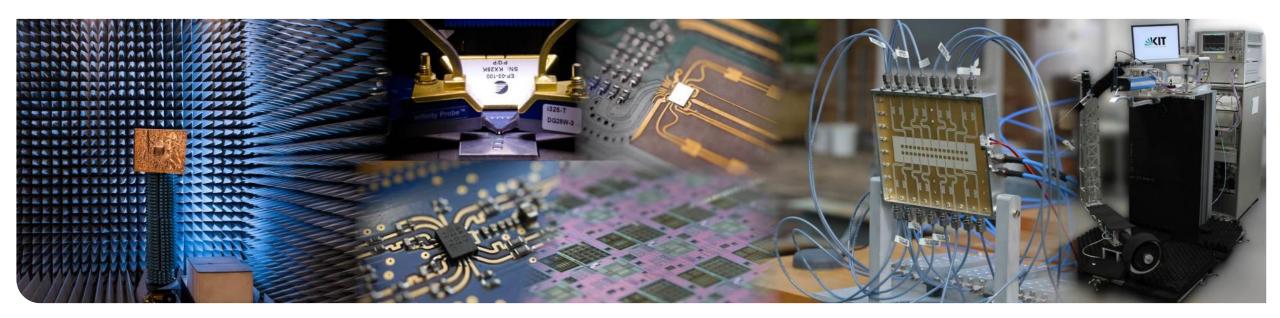




MMICDL – Up-conversion Mixer Design

2379568 Jiyun Kim



Contents



- Introduction
- Design Procedure
 - Schematic view and simulation
 - Layout view and simulation
- Conclusion
 - Application

Contents



- Introduction
 - MMIC
 - Advantages and disadvantages
 - RF transmitter
 - Up-conversion Mixer and Design goal

I. Introduction

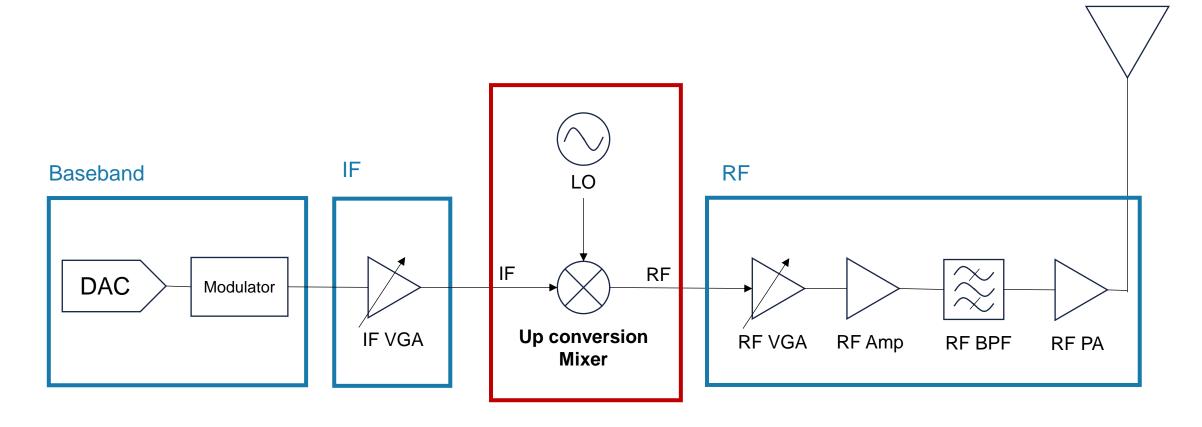


- MMIC (Monolithic microwave integrated circuits)
 - All circuits and components are fabricated directly on a single semiconductor
 - advantages
 - Compact size
 - low cost
 - Operates at high frequencies (K band and higher) reaching mmWave
 - challenges
 - waveguide effects have to be considered
 - Modelling and simulation have to be accurate to produce correctly
 - parasitics increases with frequency
 - Achievable output powers drop with frequency necessitating

I. Introduction



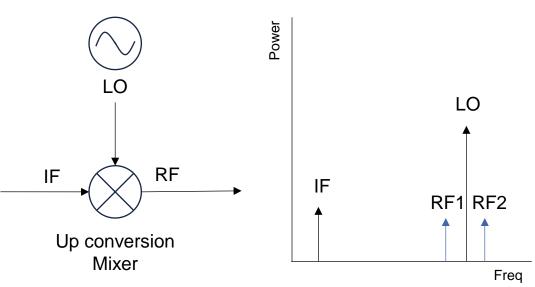
RF Transmitter



I. Introduction



Up-conversion Mixer



RF1 = LO – IF RF2 = LO + IF

Design Goals

- 1dB compression point > 0dBm
- Gain > 10dB
- IF Bandwidth > 200MHz
- S11 < -15dB
- S22 < -15dB

II. Design Procedure



- Schematic view and simulation
 - Single balance or Double balance
 - Core design (include transistor decision)
 - DC simulation
 - S-param simulation
 - output / input matching network
 - Design params check with HB simulation
- Layout view and simulation
 - Core Layout & EM simulation
 - S-param simulation
 - output / input matching network
 - Design params check with HB simulation
 - Inductor Layout design (Pcell) & EM simulation
 - Mixer Layout EM simulation
 - Design params check with HB simulation

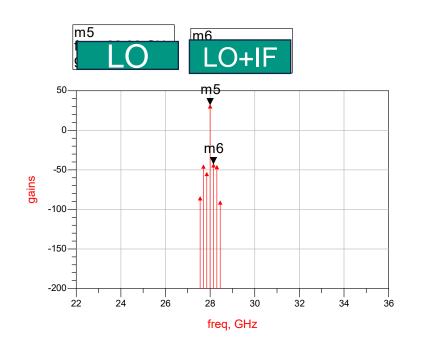
II. Design Procedure

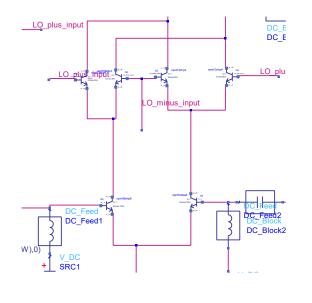


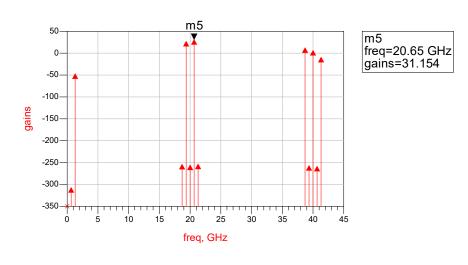
- Schematic view and simulation
 - Single balance or Double balance
 - Core design (include transistor decision)
 - DC simulation
 - S-param simulation
 - output / input matching network
 - Design params check with HB simulation



- Balance Mixer : improves isolation
- Single Balance vs Double Balance
 - Unwanted LO component in output in Single Balance

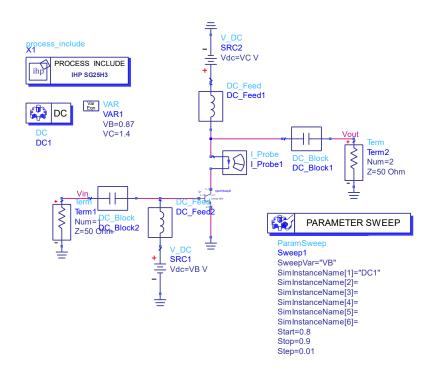


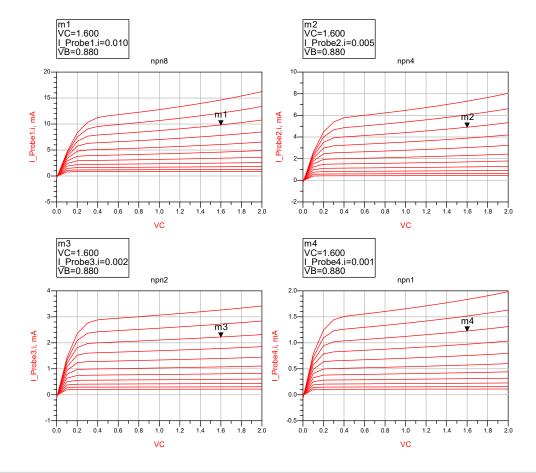






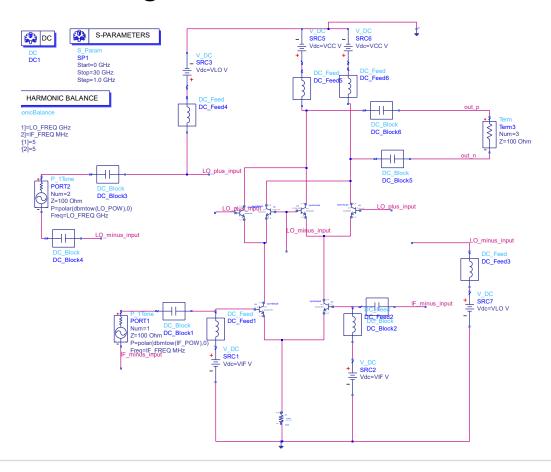
Core Design – transistor analysis







Core Design

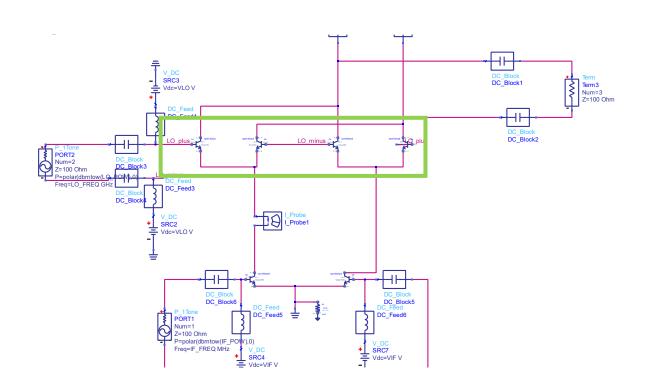


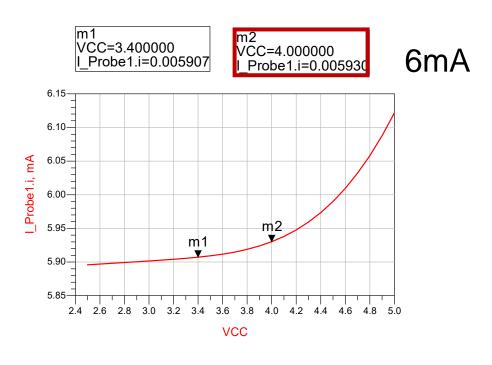
Fixed Parameters

- VCC=3.6 V,VLO= 2.4V,VIF=0.89V
- Q0, Q1, Q2, Q3: npnhp4 and Q4, Q5: npnhp8 from SG25_dev library from IHP
- Initial value LO_POW=0dBm, LO_FREQ=20GHz, IF POW=-30dBm, IF FREQ=100MHz



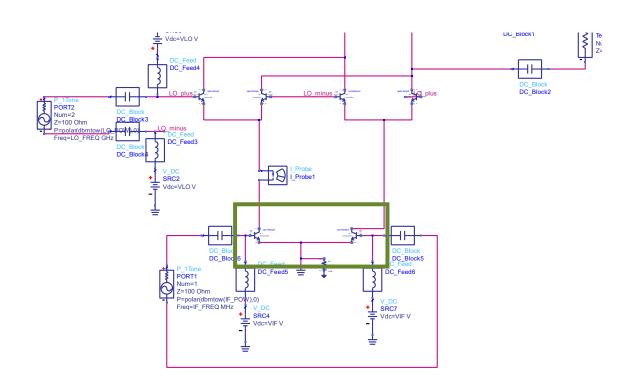
DC Simulation

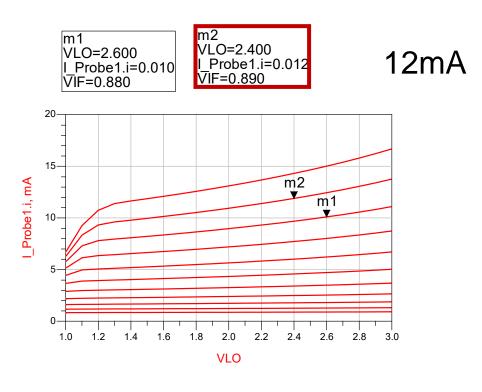






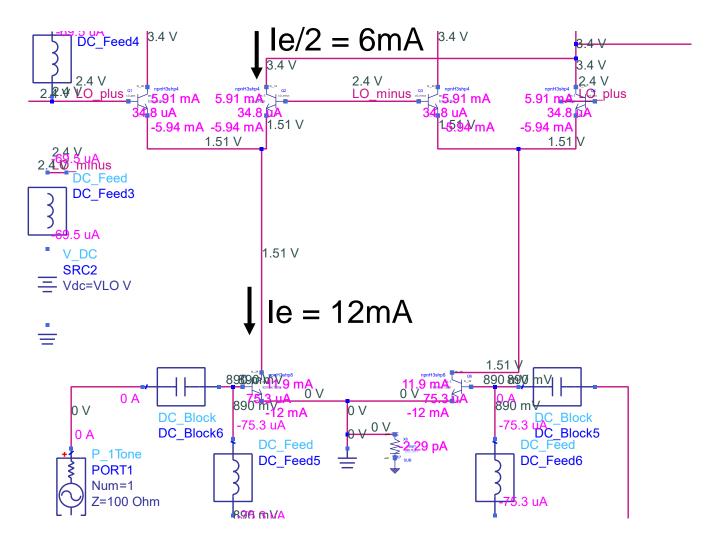
DC Simulation





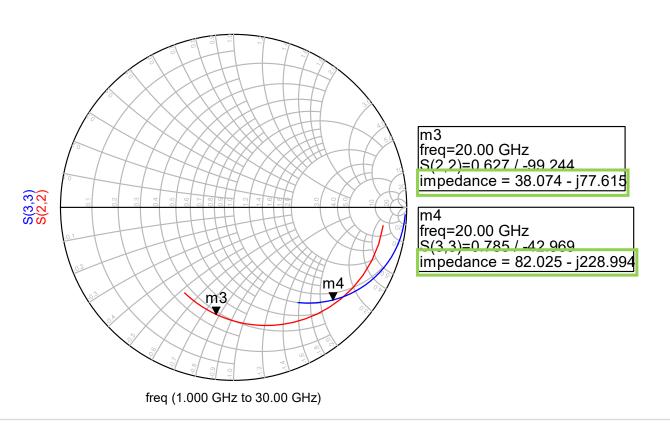


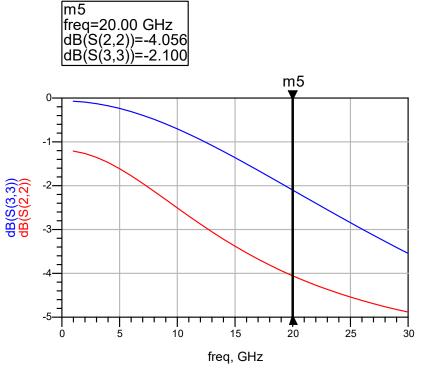
DC Simulation with annotation





■ S-parameter Simulation ($Z0 = 100\Omega$)

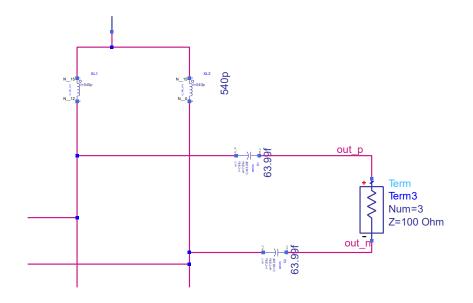






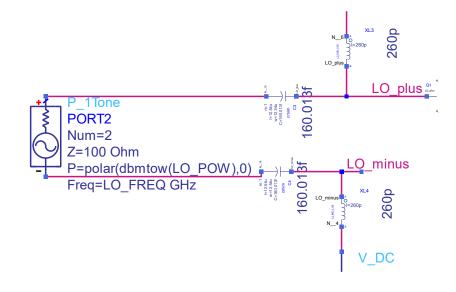
Output Matching

(L=540pH, C=64fF)



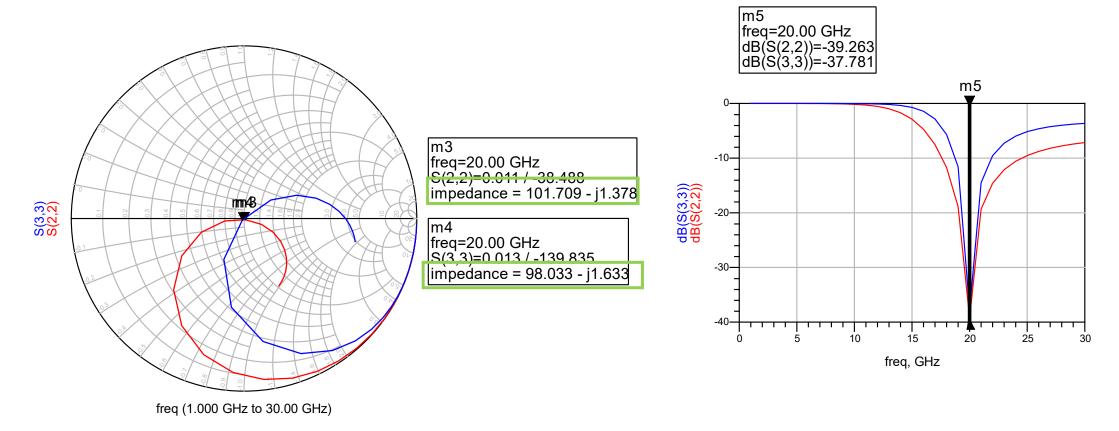
Input Matching

■ (L=260pH, C=160fF)



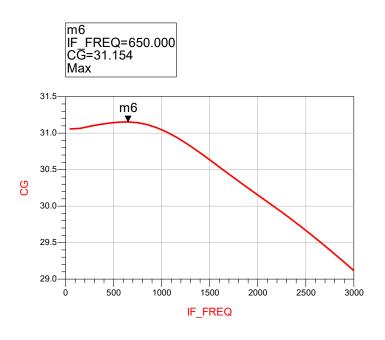


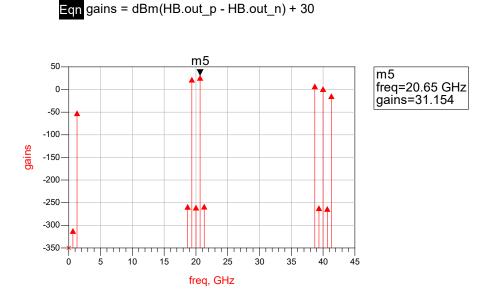
■ Matched S-parameter Simulation ($Z0 = 100\Omega$)





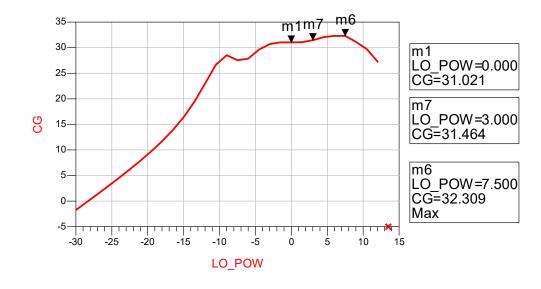
■ Harmonic Balance (HB) Simulation – conversion gain vs IF frequency







■ Harmonic Balance (HB) Simulation – conversion gain vs LO power





Design goals

- 1dB compression point > 0dBm
- Gain > 10dB
- IF Bandwidth > 200MHz
- S11 < -15dB
- S22 < -15dB

Simulation Result

- 1dB compression point
- Gain= 31.154dB
- IF Bandwidth = more than 3GHz
- S11= -39.263dB
- S22= -37.781dB

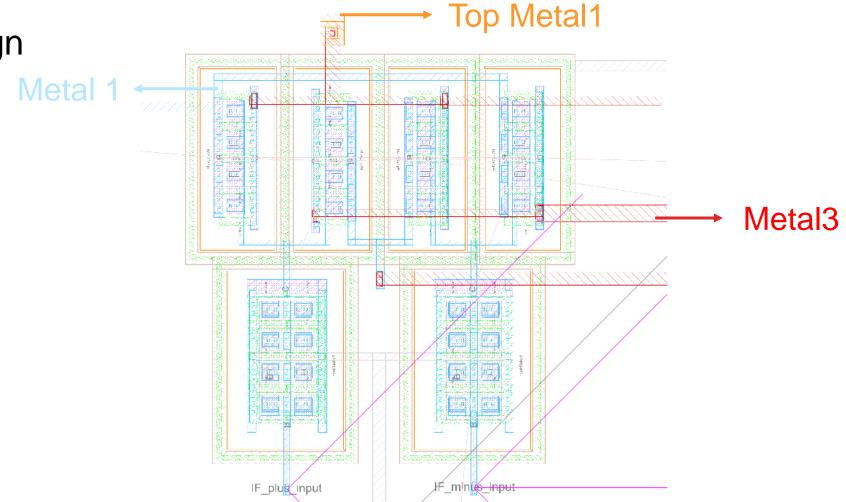
II. Design Procedure



- Layout view and simulation
 - Core design
 - Core Layout & EM simulation
 - S-param simulation
 - output / input matching network
 - Design params check with HB simulation
 - Inductor Layout design (Pcell) & EM simulation
 - Mixer Layout EM simulation
 - Design params check with HB simulation

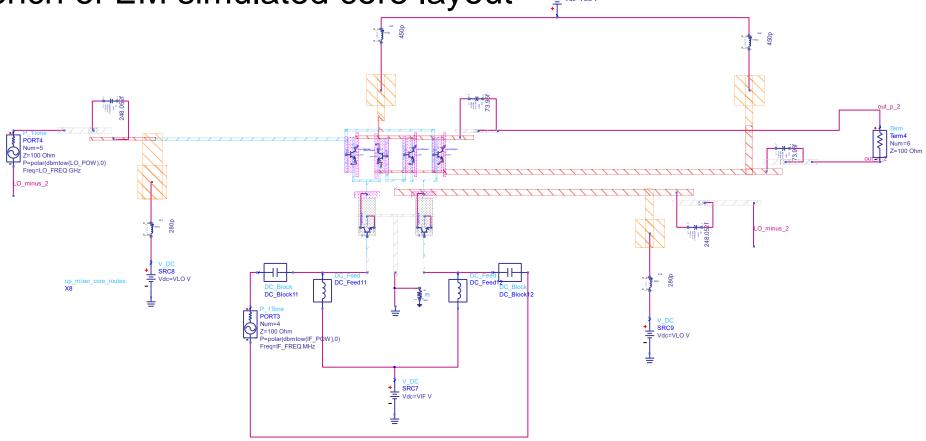


Core design



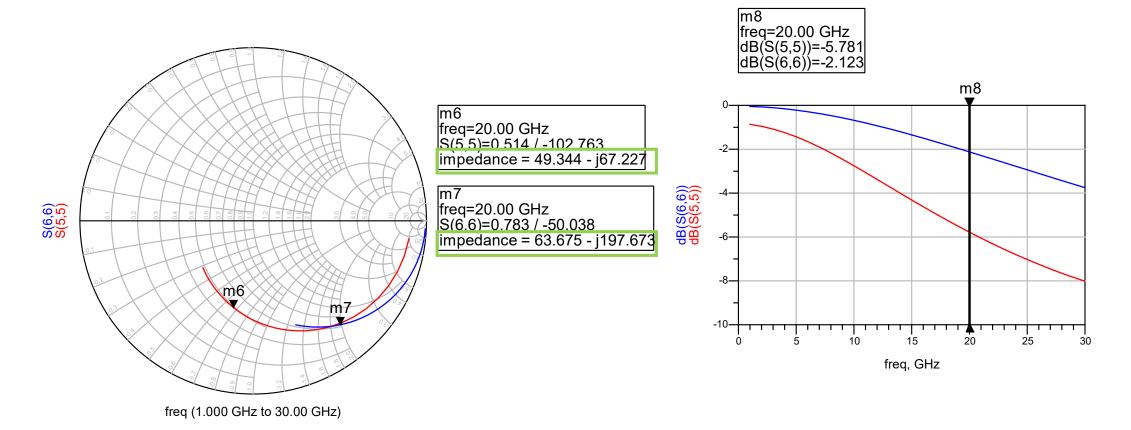


■ Test bench of EM simulated core layout





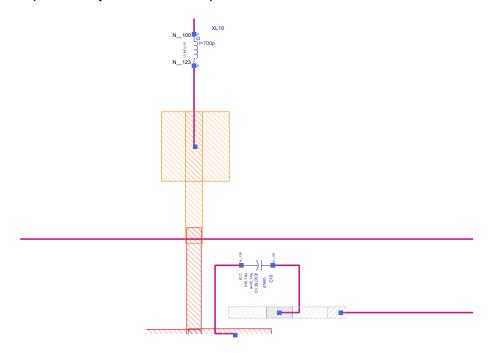
■ EM simulated core – S-parameter simulation





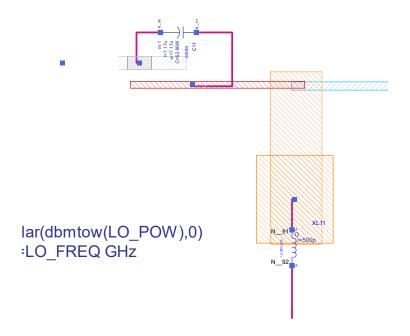
Output Matching

(L=450pH, C=74fF)



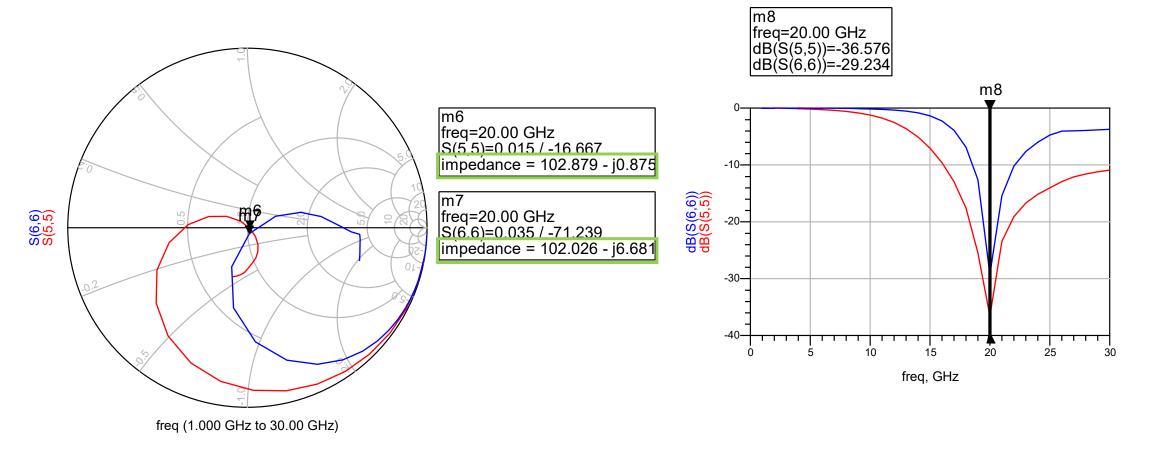
Input Matching

■ (L=280p, C=248fF)



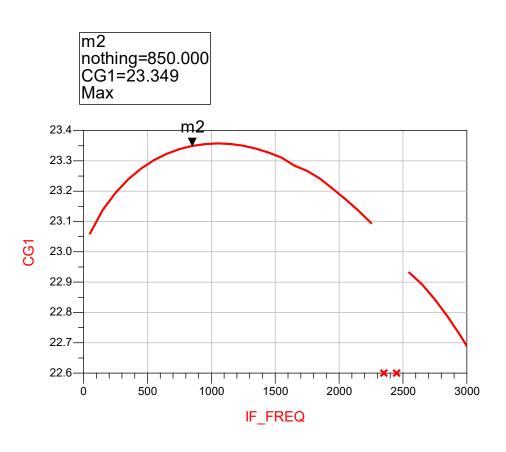


■ Matched S-parameter Simulation ($Z0 = 100\Omega$)





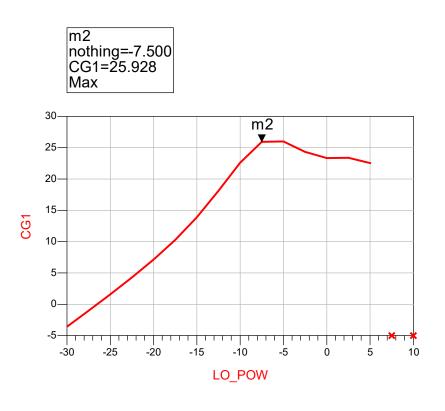
Harmonic Balance (HB)
Simulation – conversion gain vs IF frequency

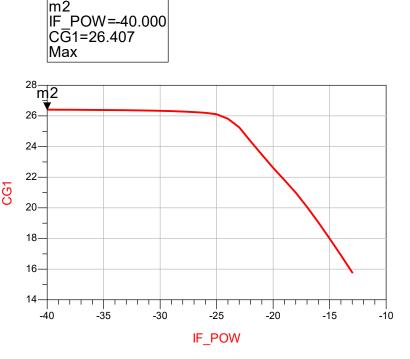




Conversion gain vs LO power

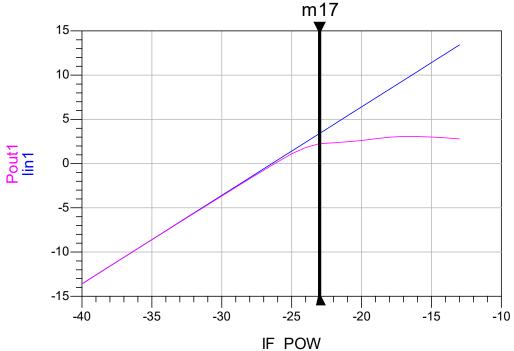
Conversion gain vs IF power







Harmonic Balance (HB)
Simulation – 1dB compression point



m17 IF_POW=-23.000 lin1=3.407 Pout1=2.252



Design goals

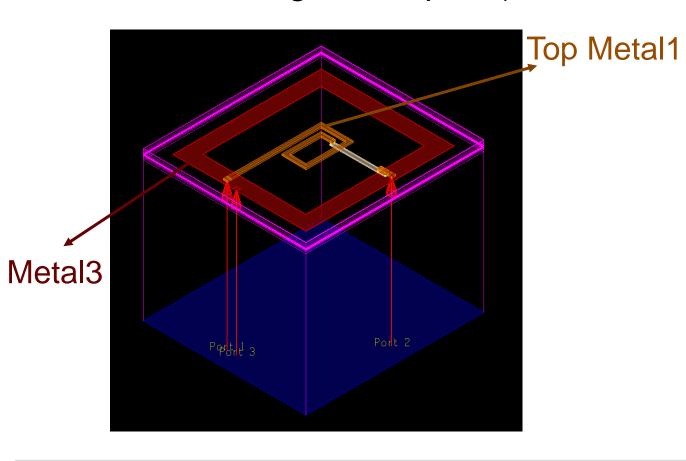
- 1dB compression point > 0dBm
- Gain > 10dB
- IF Bandwidth > 200MHz
- S11 < -15dB
- S22 < -15dB

Simulation Result

- 1dB compression point = 2.252dBm
- Gain = 23.349dB
- IF Bandwidth = more than 3GHz
- \blacksquare S11 = -36.576dB
- \blacksquare S22 = -29.234dB



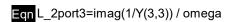
■ Inductor design — LO port (L= 280.1pH with Q-factor value 17.863)

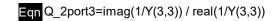


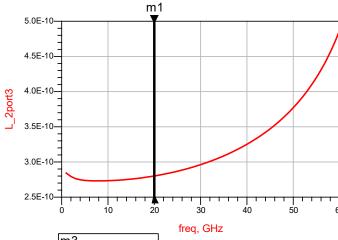
Pcell parameters defined in skill pcell IDE			
cond_width	TW(track width)	8.5u	
coil_length		87u	
width	ID(inner-turn diameter)	57u	
sep	D(Distance between tracks)	8.5u	
gnd_sep	GPS(Ground path side)	75u	
gnd_size	GPW(Ground path width)	30u	
turns	N (Number of turns)	1.5	
coil_exit		2	

Karlsruhe Institute of Technology

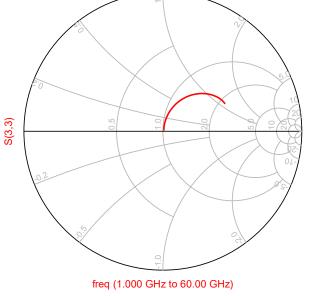
- Inductor design LO port
 - L= 280.1pH
 - Q-factor = 17.863

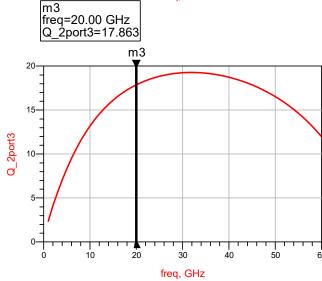






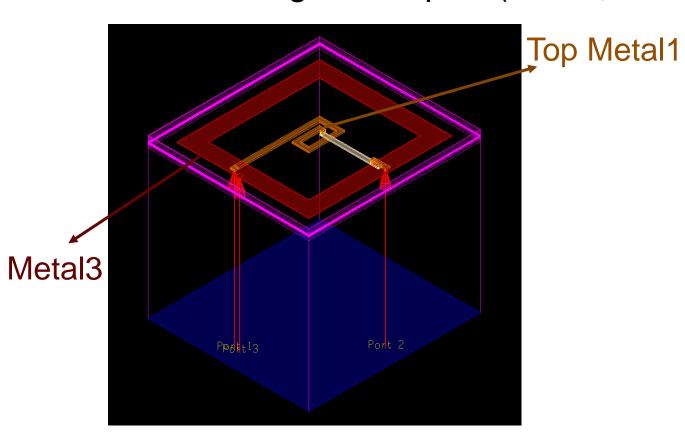
freq=20.00 GHz L_2port3=2.801E-10







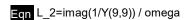
■ Inductor design — RF port (L = 422.1pH with Q-factor value 19.574)

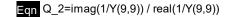


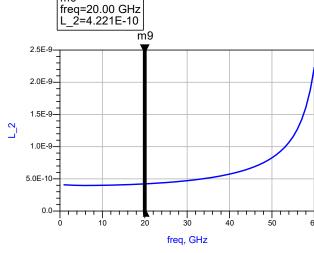
Pcell parameters defined in skill pcell IDE			
cond_width	TW(track width)	8u	
coil_length		60u	
width	ID(inner-turn diameter)	40u	
sep	D(Distance between tracks)	8u	
gnd_sep	GPS(Ground path side)	75u	
gnd_size	GPW(Ground path width)	30u	
turns	N (Number of turns)	1.5	
coil_exit		2	

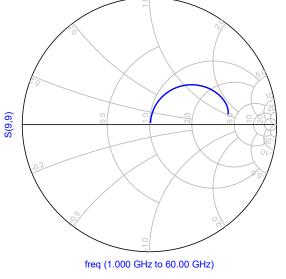


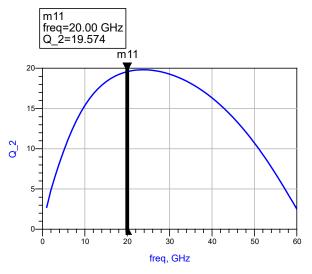
- Inductor design LO port
 - L= 422.1pH
 - Q-factor = 19.574





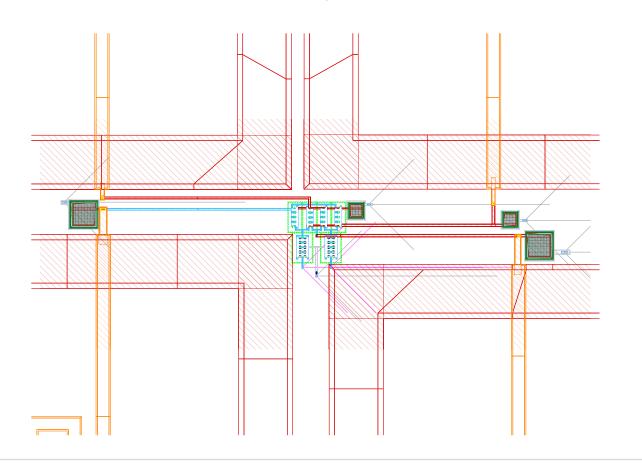


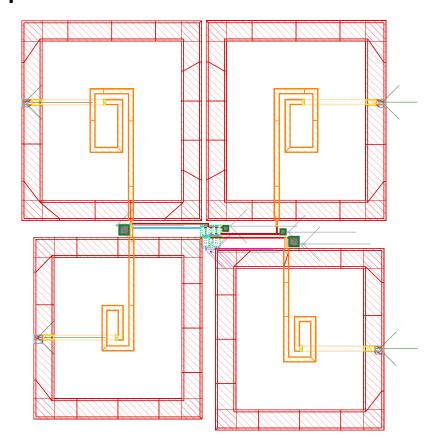






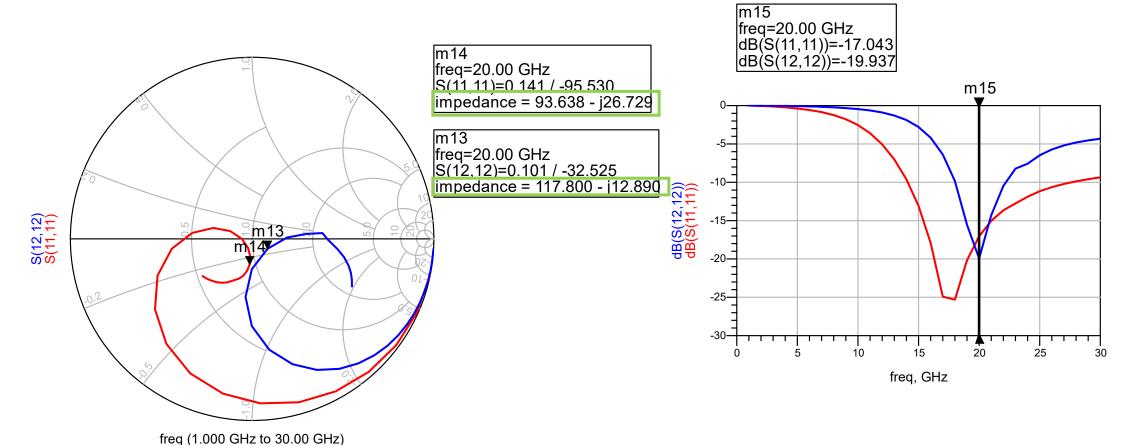
EM simulated final layout with inductors and capacitors





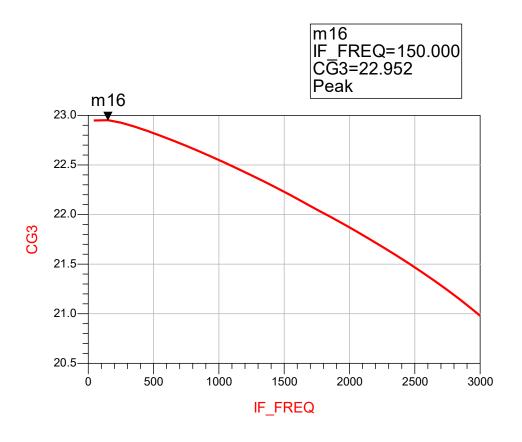


S-parameter simulation





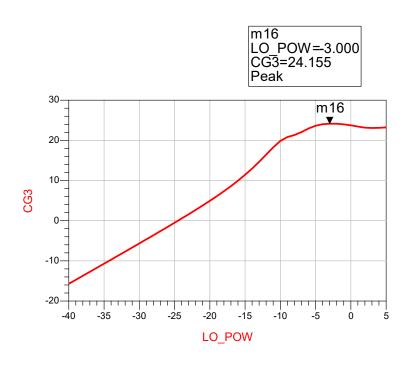
Harmonic Balance (HB)
Simulation – conversion gain vs IF frequency

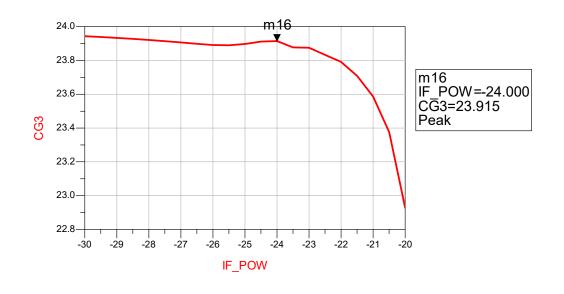




Conversion gain vs LO power

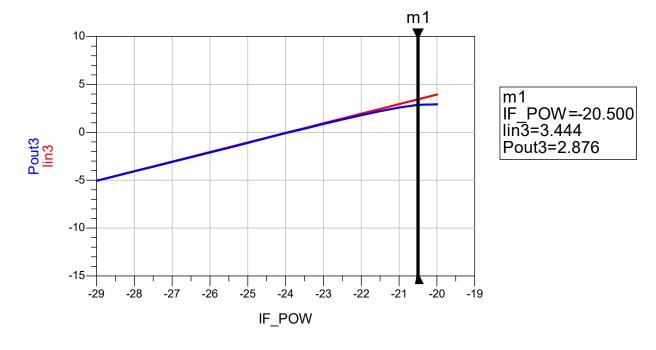
Conversion gain vs IF power







Harmonic Balance (HB)
Simulation – 1dB compression point





Design goals

- 1dB compression point > 0dBm
- Gain > 10dB
- IF Bandwidth > 200MHz
- S11 < -15dB
- S22 < -15dB

Simulation Result

- 1dB compression point = 2.876dBm
- Gain = 22.952dB
- IF Bandwidth = more than 3GHz
- \blacksquare S11 = -17.043dB
- \blacksquare S22 = -19.937dB

III. Conclusion



- IF frequency = 150MHz, LO frequency= 20GHz, RF frequency = 20.15GHz, BW > 3GHz
- Application
 - Broadband application
 - High quality
 - Large amount of data transmission

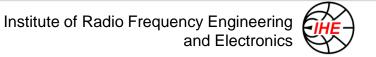
III. Conclusion



- RF frequency = 20.15GHz
- Application
 - SHF band
 - Modern communications technologies
 - modern radars
 - DTH services
 - 5GHz Wi-Fi channel
 - radio astronomy
 - mobile networks
 - TV broadcasting satellites
 - microwave devices
 - broadcasting satellites
 - amateur radio

Frequency Band	ITU band number	Frequency
Extremely low fre quency (ELF)	1	3 Hz-30 Hz
Super low freque ncy (SLF)	2	30 Hz-300 Hz
Ultra low frequen cy (ULF)	3	300 Hz-3 kHz
Very low frequen cy (VLF)	4	3–30 kHz
Low frequency (L F)	5	30–300 kHz
Medium frequen cy (MF)	6	300–3,000 kHz
High frequency (HF)	7	3–30 MHz
Very high freque ncy (VHF)	8	30–300 MHz
Ultra high freque ncy (UHF)	9	300–3,000 MHz
Super high freque ncy (SHF)	10	3–30 GHz
Extremely high fr equency (EHF)	11	30–300 GHz
Terahertz or trem endously high fre quency (THF)	12	300–3,000 GHz

ITU classification of frequency bands (https://resources.pcb.cadence.com/blog/2022-an-overview-of-frequency-bands-and-their-applications)



III. Conclusion



- RF frequency = 20.15GHz
- Application
 - K-band(Radar waves)
 - police radars operate in USA
 - short-range communication
 - automatic door openers
 - collision avoidance systems
 - blind spot monitoring systems in vehicles
 - K-band MMIC
 - local-multipoint distribution services (LMDS)
 - digital point-to-point radio services
 - fixed satellites

T
Band designation
HF
VHF
ULF
L
S
С
X
Ku
K
Ка
V
W
mm or G

IEEE classifications of frequency bands(https://resources.pcb.cadence.com/blog/2022-an-overview-of-frequency-bands-and-their-applications)