

SoC Robot Brain Board – FPGA

System Design Innovation & Application Research Center

- I. FPGA Device
- II. Altera Quartus Download & Setup
- III. SoC Robot Project
- IV. Compilation
- V. FPGA Download



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FPGA Device

- **Company Name:** Altera
- **Device Family:** Cyclone IV **Device:** EP4CE75U19I7
- **Package:** 324Pins
- **LEs:** 75408
- **User I/O:** 293
- **Generated Simulation Language:** Verilog HDL

FPGA PROM

- **Device Name:** EPCS64
- **Package:** 16pins SOIC
- **Configuration:** Serial

Design Software

- **Altera Quartus II**

Design Software

- **Altera USB Blaster**



- Altera 홈페이지 접속
=> <http://www.altera.com>
- Quartus II Web Edition Download Page 접속
=> <http://dl.altera.com/?edition=subscription>

Combined Files Individual Files DVD Files Additional Software Updates

Download and install instructions: [More](#)
[Read Altera Software v13.1 Installation FAQ](#)
[Quick Start Guide](#)

☒ Select All

☒ Quartus II Subscription Edition

☒ Quartus II Software (includes Nios II EDS)
Size: 1.6 GB MD5: BC38BCB26C7E6E11C7ADA56940DC9269

☒ ModelSim-Altera Edition (includes Starter Edition)
Size: 822.8 MB MD5: B97739CAD5FA9BE4156DFFC614AC9F26

☒ UPDATE

☒ Devices

You must install device support for at least one device family to use the Quartus II software.

☐ Arria II device support (includes all variations)
Size: 595.6 MB MD5: 675B2B6BDCD7C892A59F84D8B4A5B6AF

☐ Arria V device support
Size: 1.2 GB MD5: 5CA879C0AD3E8E4933700153907D490F

☐ Arria V GZ device support
Size: 1.4 GB MD5: C0B21B60D53BB8B6C8161A7B38005D0F

☒ Cyclone III, Cyclone IV device support (includes all variations)
Size: 548.4 MB MD5: 2252CD4F2CBA75018F9B1325929F69FF

☐ Cyclone V device support (includes all variations)
Size: 810.4 MB MD5: 075BC842C2379B8D9B2CC74F9CAEDCB7

☐ MAX II, MAX V device support
Size: 6.1 MB MD5: 253524637B52DA417107249344B7DF80

☐ Stratix III, Stratix IV device support (includes all variations)
Size: 633.7 MB MD5: 43AC8DF41B1A19087858A16716A39B96

☐ Stratix V device support (includes all variations)
Size: 1.9 GB MD5: B3975A8190C4C47C5C1C51528D949531



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- SoC 로봇워 홈페이지 => 소스자료 게시판
- 2014년 SoC 두뇌보드, FPGA 소스 첨부파일 다운로드

소스자료

> Home > 자료실 > 소스자료

2014년 SoC 두뇌보드, FPGA 소스

2014-06-19 15:49:59

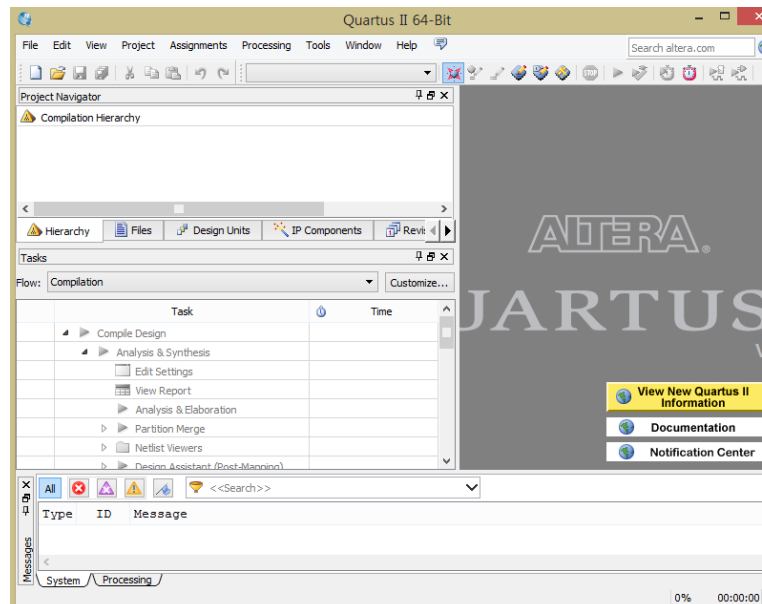
대회담당자 (143,248,146,153)

조회 : 4

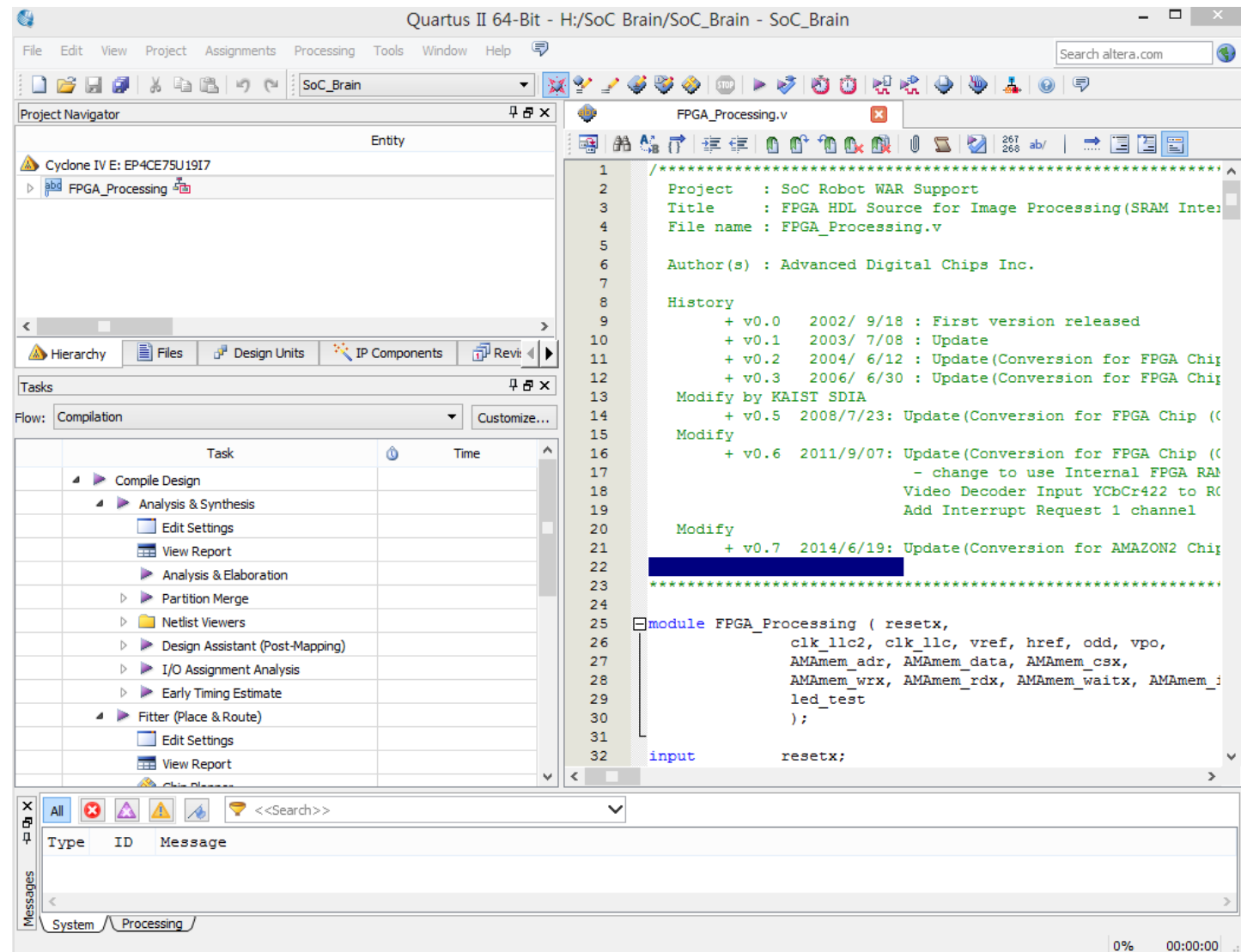
Download : SoC Brain.zip (7,6M), Down:1

Verilog로 작성된 FPGA 소스입니다.

- SoC Brain.zip 압축풀기
- Quatus 실행



- 프로젝트 Open
 - => File => Open Project
 - => SoC_Brain.qpf 파일 선택, Open



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ROBOTWAR

KIRIA 한국로봇산업진흥원
KOREA INSTITUTE FOR ROBOT INDUSTRY ADVANCEMENT

adc

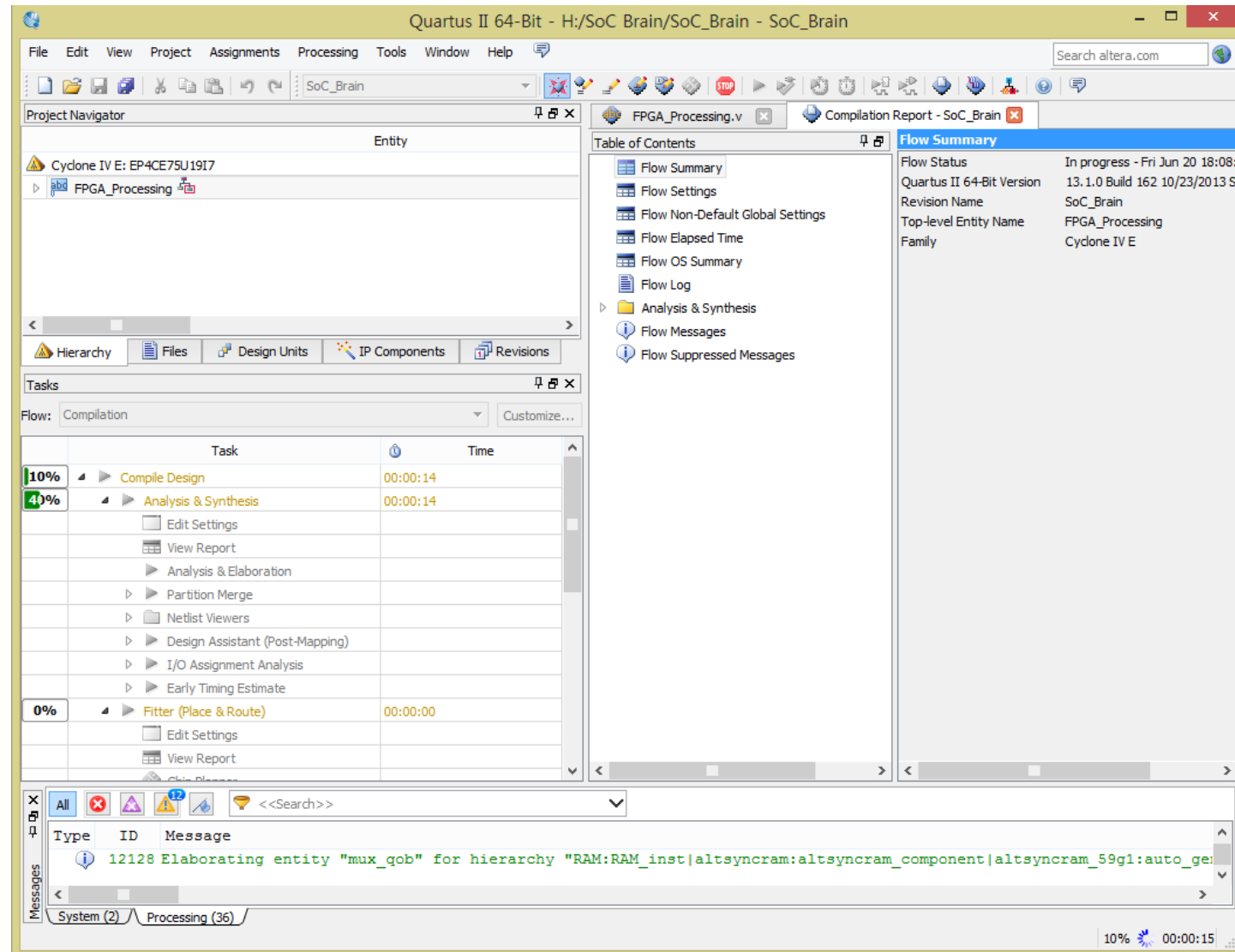
ALTERA

MINI (주)미니로봇
ROBOT

ROBOTIS

IDEG 반도체설계교육센터
IC DESIGN EDUCATION CENTER

- Compile
=> Processing => Start Compilation



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KOREA INSTITUTE FOR ROBOT INDUSTRY ADVANCEMENT

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ROBOT

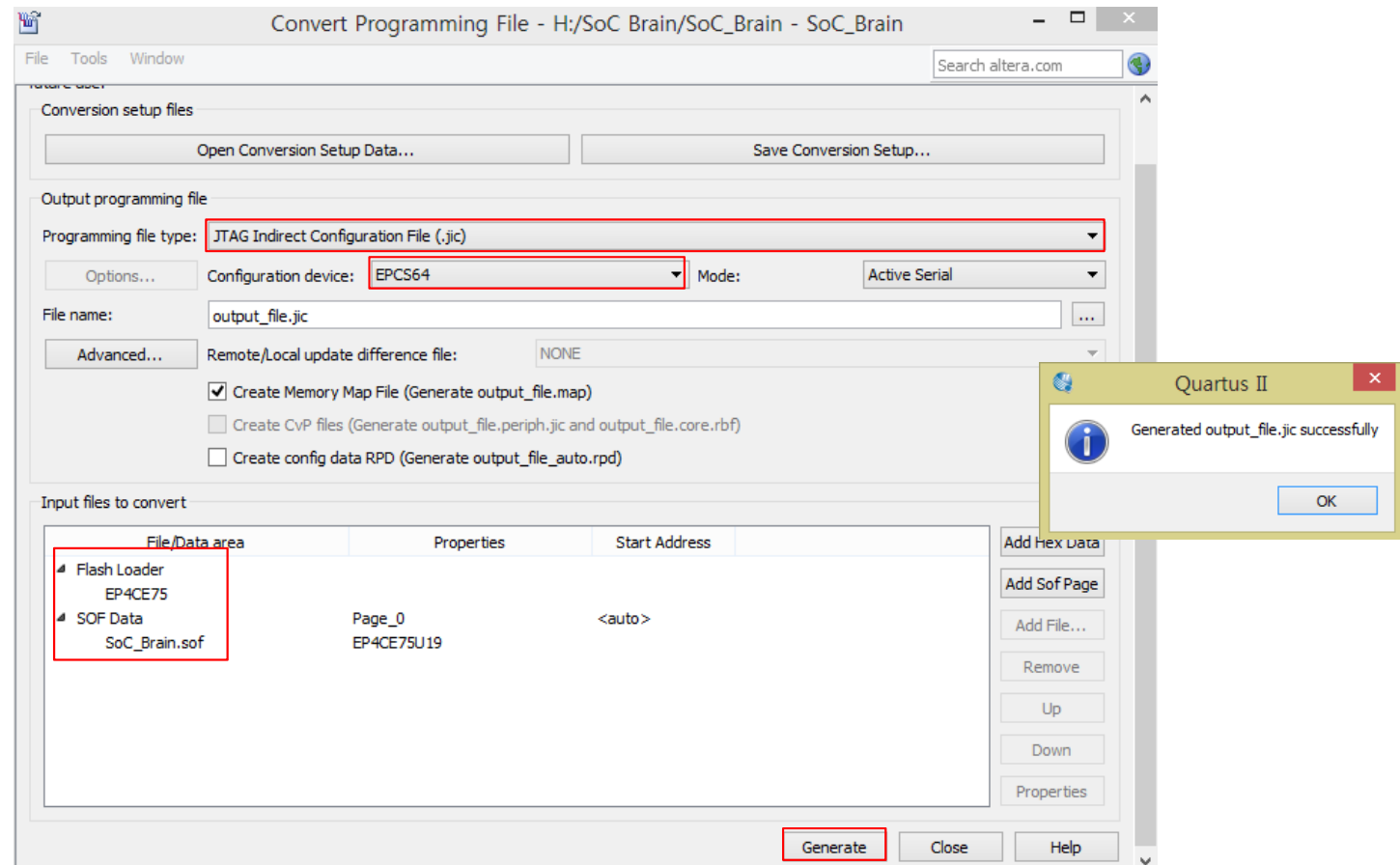
ROBOTIS

IDeC 반도체설계교육센터
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• JIC(JTAG indirect Configuration file) 파일 생성

=> File => Convert Programming Files

- Programming file type: JTAG Indirect Configuration File(.jic)
- Configuration device: EPCS64
- Flash Loader 선택 => Add Device... => Cyclone IV E / EP4CE75 체크
- SOF Data 선택 => Add File... => output_files 폴더 선택 => SoC_Brain.sof Open
- Generate 선택



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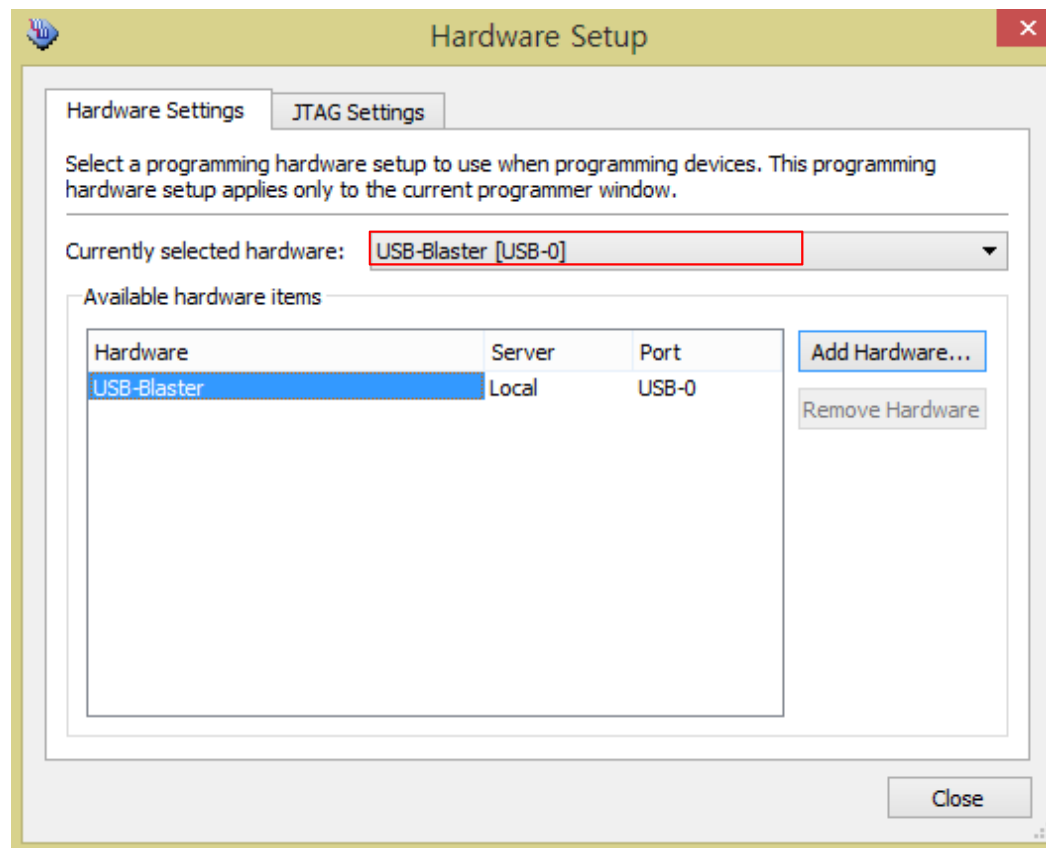


- FPGA Programming

=> tools => Programmer

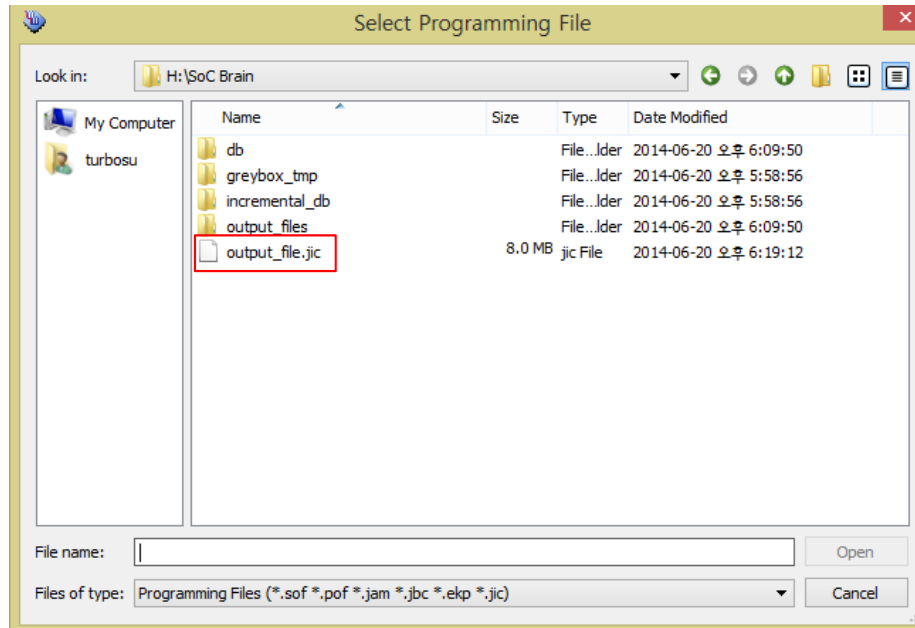
- Hardware Setup

=> USB Blaster 연결 후 드라이버 설치 => USB-Blaster 선택



• JIC 파일 추가

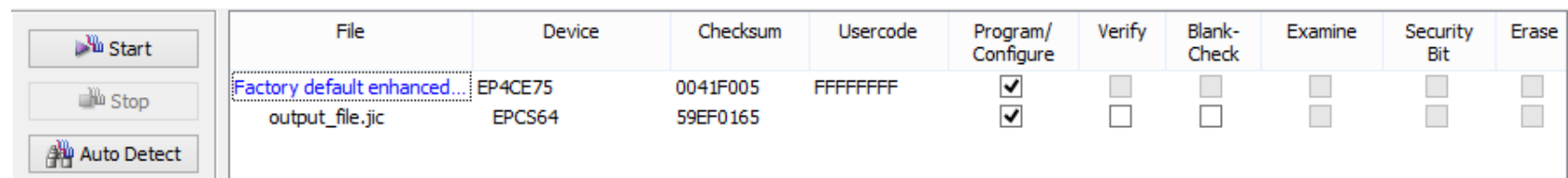
=> Add File... => Programmer => output_file.jic 선택



• Programming

=> Program/Configure 체크

=> SoC Brain Board 전원 ON => Start



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