Alveo U280 Data Center Accelerator Card

User Guide

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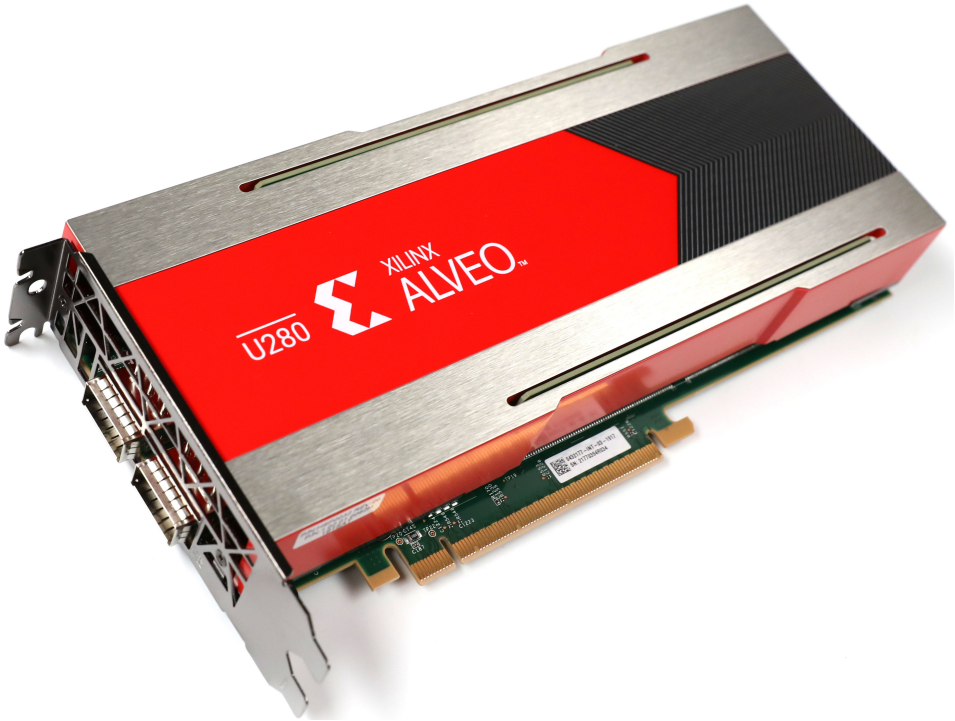
Introduction

The AMD Alveo™ U280 data center accelerator cards are Peripheral Component Interconnect express (PCIe®) Gen3 x16 compliant and Gen4 x8 compatible cards featuring the 16 nm AMD UltraScale+™ technology. The Alveo U280 card offers 8 GB of HBM2 at 460 GB/s bandwidth to provide high-performance, adaptable acceleration for memory-bound, compute-intensive applications including database, analytics, and machine learning inference.

The Alveo U280 data center accelerator cards are available in passive and active cooling configurations. Except where noted, this user guide applies to both the active and passive versions of the U280 card. The following figure shows a passively cooled Alveo U280 accelerator card.

Figure 1: **Alveo U280 Data Center Accelerator Card (Passive Cooling)**



> **CAUTION!** *The Alveo U280 accelerator card with passive cooling is designed to be installed into a data center server, where controlled air flow provides direct cooling. Due to the card enclosure, switches and LEDs are not accessible or visible. The card details in this user guide are provided to aid understanding of the card features. If the cooling enclosure is removed from the card and the card is powered-up, external fan cooling airflow MUST be applied to prevent over-temperature shut-down and possible damage to the card electronics. Removing the cooling enclosure voids the board warranty.*

For additional information about airflow requirements, see the *Alveo U280 Data Center Accelerator Cards Data Sheet* (DS963).

See Appendix A: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the Alveo U280 accelerator cards.

AMD

Chapter 2

Accelerator Card Overview

Card Features

Features of the AMD Alveo™ U280 data center accelerator cards are listed in the following table.

Table 1: **Alveo U280 Features**

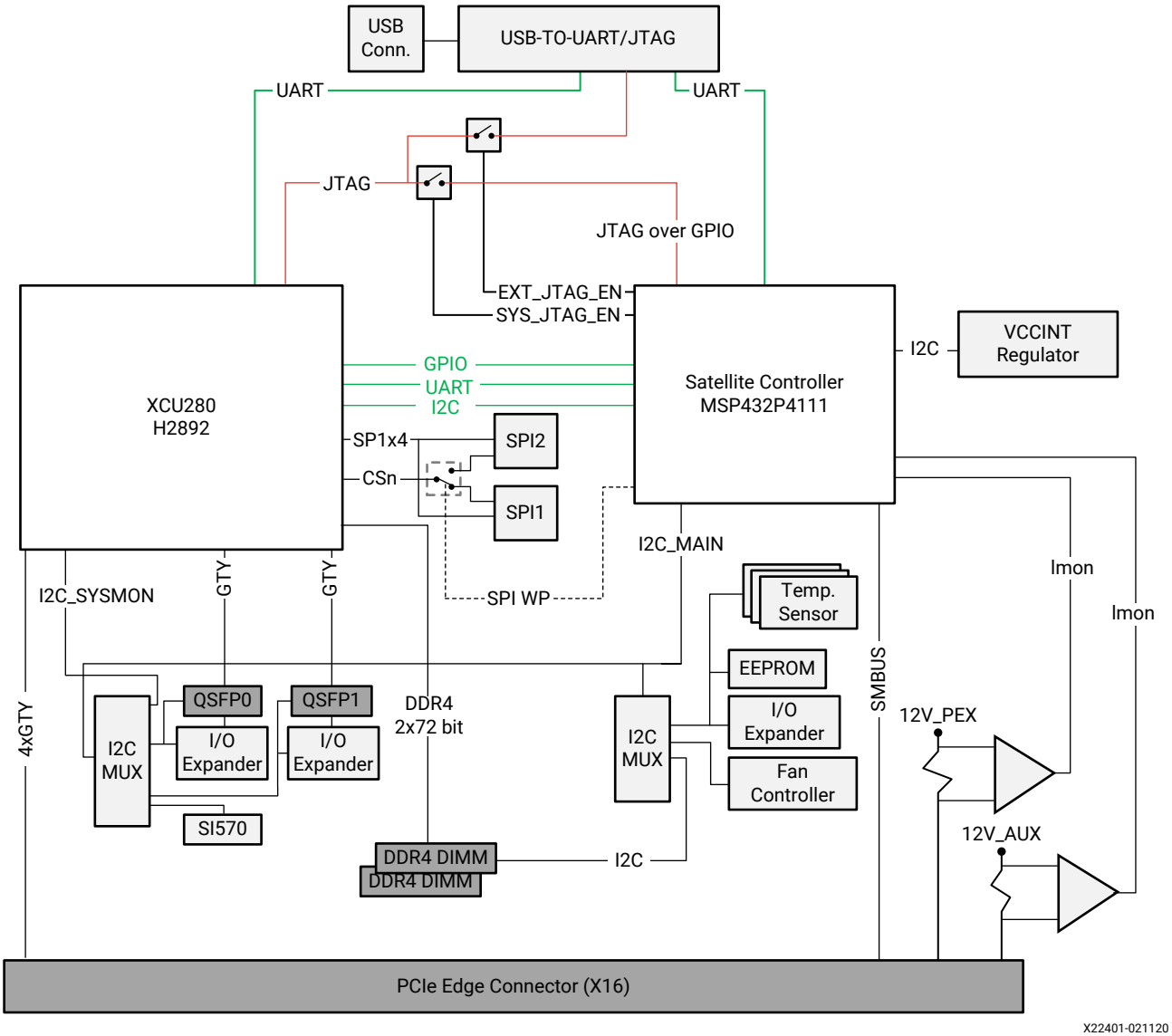
Card Component	U280
FPGA	UltraScale+ XCU280-L2FSVH2892E
DDR4	32 gigabyte (GB) 2x DDR4 16 GB
	2400 mega-transfers per second (MT/s), 64-bit with error correcting code (ECC) DIMM
	x4/x8 unregistered dual inline memory module (UDIMM) support
HBM	8 GB
Configuration Options	1 gigabit (Gb) Quad Serial Peripheral Interface (SPI) flash memory
	Micro-AB universal serial bus (USB) JTAG configuration port
PCIe	16-lane PCI Express
	PCIe Integrated Endpoint block connectivity
	Gen1, 2, or 3 up to x16, Gen4 x8
I2C Bus	✓
Status LEDs	✓
Power Management	Power management with system management bus (SMBus) voltage, current, and temperature monitoring
External Power Sources	65W PCIe slot functional with PCIe slot power only
	150 W PCIe slot functional with 110 A max V_{CCINT} current PCIe slot power and 6-pin PCIe AUX power cable connected
	225 W PCIe slot functional with 160 A max V_{CCINT} current PCIe slot power and 8-pin PCIe AUX power cable connected
Flash Memory	Onboard reprogrammable flash configuration memory
UART	Universal asynchronous receiver-transmitter (UART) access through the USB port
Configuration	UltraScale+ device configurable over USB/JTAG and Quad SPI configuration flash memory

For card specifications, see *Alveo U280 Data Center Accelerator Cards Data Sheet* (DS963).

Block Diagram

The block diagram of the Alveo U280 accelerator card is shown in the following figure.

Figure 2: **U280 Block Diagram**

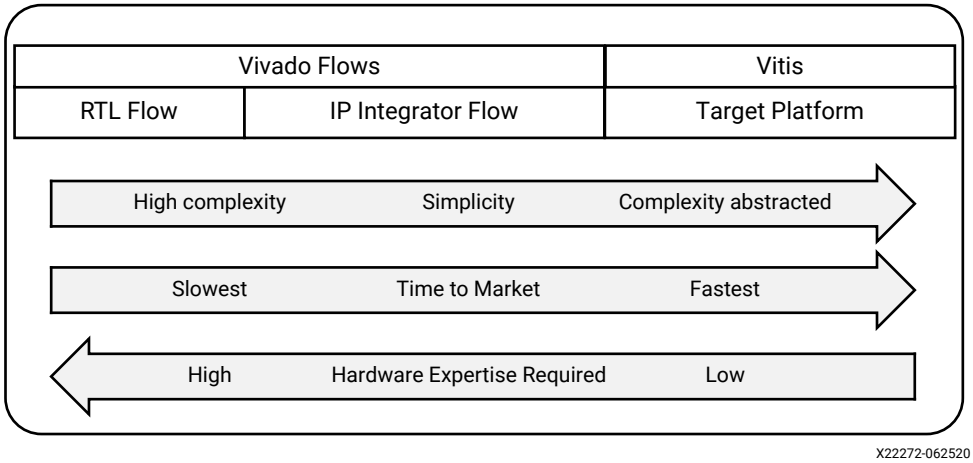


***Note*:** In the block diagram, QSFP1 is port 1, the upper port located on the card PCIe bracket and QSFP0 is port 2, the lower port on the PCIe bracket, closest to the PCIe card edge fingers.

Design Flows

The preferred optimal design flow for targeting the Alveo data center accelerator card uses the AMD Vitis™ unified software platform. However, traditional design flows, such as RTL or IP integrator are also supported using the AMD Vivado™ Design Suite. The following figure shows a summary of the design flows.

Figure 3: **Alveo Data Center Accelerator Card Design Flows**



Documents related to the different design flows are listed in the following table. Additional details on the Vivado design flow are given in Chapter 3: Vivado Design Flow.

For the Vitis design flow details, see *Vitis Unified Software Platform Documentation* (UG1416).

Table 2: **Documentation to Get Started with Alveo Data Center Accelerator Card Design Flows**

	RTL Flow	IP Integrator Flow	Vitis
Flow documentation	UG949[1]	UG994[2]	UG1416[3]
Vivado tools support	Board support XDC	Vivado Board File	N/A
Programming the FPGA	Vivado Hardware Manager	Vivado Hardware Manager	UG1377[4]

Notes:

1. *UltraFast Design Methodology Guide for FPGAs and SoCs* (UG949).
2. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994).
3. Vitis Accelerated Software Development Flow Documentation in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).
4. *Alveo Programming Cable User Guide* (UG1377).

Chapter 3

Vivado Design Flow

This section provides a starting point for expert HDL developers using the RTL and IP integrator flows using the Vivado™ tools.

Vivado Board Support and XDC Files Installation

Prior to creating a Vivado RTL project based on an Alveo™ card, download the Alveo Vivado board support and XDC files associated with your Alveo card from the **Getting Started** tab of the Alveo U280 Product Page.

1. Close all instances of Vivado tools.
2. Navigate to the desired Alveo product page, and download the Vivado board zip file.
3. Update the Vivado board support repository by extracting the Vivado Board ZIP file to the boards directory. For Vivado 2021.1 and greater, the boards directory is located within the AMD Vivado Design Suite installation path at:

   ```
   \data\xhub\boards\XilinxBoardStore\boards\Xilinx\
   ```

   For example, if your Vivado tools installation is located at:

   ```
   C:\Xilinx\Vivado\<version>
   ```

   where `<version>` is the Vivado tools version you are using, then for Vivado 2021.1 and greater extract the contents to:

   ```
   C:\Xilinx\Vivado\<version>\data\xhub\boards\XilinxBoardStore\boards
   \Xilinx\
   ```

   For Vivado releases prior to 2021.1, the boards directory is located within the AMD Vivado Design Suite installation path at:

   ```
   \data\boards\board_files
   ```

4. In addition to the Vivado board file, also download the Xilinx Design Constraints (XDC) file from the Alveo product page. The location of the XDC file on your system is not important.

After you install the Vivado board file and download the XDC file, you can create a Vivado RTL project.

Creating a Vivado RTL Project

There are two flows available for the RTL developer: board aware and XDC based flow. In either flow, you can add RTL files or block designs to your project. The steps necessary for creating a project for each flow are described in the following sections.

Board Aware Flow

Use the following steps to create a board aware Vivado RTL project using the Vivado board files downloaded from the Alveo product page. The Vivado board files associated with the card is used to configure IP and generate constraints for IP used in the block design.

1. Launch Vivado tools.
2. Create a new project by clicking on **File → Project → New**. Click **Next**.
3. Add a project name and click **Next**.
4. Select **RTL Project** as the Project Type and click **Next**.
5. Within the Default Part window, select **Boards**, in the search tab enter the card name you are designing for and click **Next → Finish**. This will create a new RTL project based on the selected accelerator card.

XDC Based Flow

Use the following steps to create an XDC based Vivado RTL project using the XDC downloaded from the Alveo product page. The XDC is a reference for the static pinout of the card.

Within the XDC based Vivado flow, the AMD Alveo™ parts are not visible in the Vivado part selection window. A project using a Vivado part can only be created using a Tcl command. Use the following steps:

1. Launch Vivado tools.
2. In the Tcl console, run the following command:

   ```
   create_project <project> <path> -part <part number>
   ```

   where,

   - `<project>` is the name of the project you want to create
   - `<path>` is the path where you want to create the project
   - `<part number>` is the Vivado part number as defined in the following table.

Table 3: **Vivado Part Number**

Alveo Card	Alveo Part	Vivado Part Number
A-U280	XCU280-L2FSVH2892E	XCU280-FSVH2892-2L-E

3. Add the card XDC file to the project by clicking on **File → Add Sources → Add or Create Constraints**. Click **Next**. Select **Add Files**. Navigate to the location of the XDC file and click **OK**.

UltraScale+ Device Configuration

The Alveo U280 accelerator card supports two AMD UltraScale+™ FPGA configuration modes:

- Quad SPI flash memory
- JTAG using USB JTAG configuration port

The FPGA bank 0 mode pins are hardwired to master SPI mode M[2:0] = `001` with pull-up/down resistors.

At power up, the FPGA is configured by the Quad SPI NOR flash device using the primary serial configuration mode. Refer to the XDC for recommended configuration parameters specified via the various `BITSTREAM.CONFIG` constraints.

If the JTAG cable is plugged in, QSPI configuration might not occur. JTAG mode is always available independent of the mode pin settings.

For complete details on configuring the FPGA, see the *UltraScale Architecture Configuration User Guide* (UG570).

Table 4: **Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable – JTAG overrides	x1	Not applicable

MCS File Generation and Alveo Card Programming

This section outlines the steps to generate and program the MCS file.

***Note*:** When creating a design for this card, it is necessary to drive the CATTRIP pin listed in the following table. This pin is monitored by the card's satellite controller (SC) and represents the HBM_CATTRIP (HBM catastrophic temperature failure). When instantiating the HBM IP in your design, the two HBM IP signals, DRAM_0_STAT_CATTRIP and DRAM_1_STAT_CATTRIP, must be ORed together and connected to this pin for proper card operation. If the pin is undefined it will be pulled High by the card causing the SC to infer a CATTRIP failure and shut power down to the card.

If you do not use the HBM IP in your design, you must drive the pin Low to avoid the SC shutting down the card. If the pin is undefined and the QSPI is programmed with the MCS file, there is a potential chance that the card will continuously power down and reset after the bitstream is loaded. This can result in the card being unusable.

MCS File Generation

The MCS file represents the PROM image which is loaded onto the Alveo accelerator card at power on. It is generated using the write_cfgmem tool. This section outlines the steps to generate and program the MCS file.

Prior to generating the MCS file, ensure your project XDC file sets the following properties.

- CONFIG_VOLTAGE
- BITSTREAM.CONFIG.CONFIGFALLBACK
- BITSTREAM.GENERAL.COMPRESS
- CONFIG_MODE
- BITSTREAM.CONFIG.SPI_BUSWIDTH
- BITSTREAM.CONFIG.CONFIGRATE
- BITSTREAM.CONFIG.EXTMASTERCCLK_EN
- BITSTREAM.CONFIG.SPI_FALL_EDGE
- BITSTREAM.CONFIG.UNUSEDPIN
- BITSTREAM.CONFIG.SPI_32BIT_ADDR

Use the following command with the parameters outlined in Table 5 to generate the MCS file.

```
write_cfgmem -force -format mcs -interface <interface_type> -size <size> -
loadbit "up <user_config_region_offset> <input_file.bit>" -file
"<output_file.mcs>"
```

Table 5: **write_cfgmem Parameter Settings**

write_cfgmem Parameter	Setting
interface_type	`spix4`
size	128
user_config_region_offset[1]	`0x01002000`
input_file.bit	Filename of the input .bit file

Table 5: **write_cfgmem Parameter Settings** *(cont'd)*

write_cfgmem Parameter	Setting
output_file.mcs	MCS output filename

Notes:

1. Address `0x00000000` through `0x01001FFF` is a write protected region which holds the card's golden recovery image and cannot be written to. The `user_config_region_offset` setting cannot be within this range.

For additional details on write_cfgmem, see the *UltraScale Architecture Configuration User Guide* (UG570).

Program the Alveo Data Center accelerator card

After the MCS file has been generated, use the following steps to flash the FPGA on the Alveo Data Center accelerator card using the Vivado hardware manager. Detailed steps for programming the FPGA are outlined in the chapter Programming the FPGA Device in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

RECOMMENDED: *Programming through JTAG maintenance port must be from a separate machine to avoid PCIe downlink causing the server to reboot during programming. Alternatively, the PCIe link can be manually disabled through software and rescanned after programming is complete.*

1. Connect to the Alveo U280 data center accelerator card using the Vivado hardware manager via the Micro-USB port.
2. Select **Add Configuration Device** and select the mt25qu01g-spi-x1_x2_x4 part.
3. Select OK when prompted "Do you want to program the configuration memory device now?" or right-click the target to select **Program the Configuration Memory Device**.
   a. Select the MCS file target.
   b. Select **Configuration File Only**.
   c. Click **OK**.
4. After programming has completed, disconnect the card in the hardware manager, and disconnect the JTAG programming cable from the Alveo accelerator card.
5. Perform a cold reboot on the host machine to complete the card update.

IMPORTANT! *When switching between an Alveo data center accelerator card target platform and a custom design, revert the card to the factory image before loading an alternate image into the PROM. See Answer Record 71757 for more information.*

Chapter 4

Card Installation

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

Installing Alveo Data Center Accelerator Cards in Server Chassis

For hardware installation procedures, see *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

Because each server or PC vendor's hardware is different, for physical board installation guidance, see the manufacturer's PCI Express® board installation instructions.

Card Component Description

This chapter provides a functional description of the components of the Alveo™ U280 data center accelerator card.

UltraScale+ Device

The Alveo U280 accelerator card is populated with the 16 nm UltraScale+™ XCU280-L2FSVH2892E device Vivado part number: XCU280-FSVH2892-2L-E.

DDR4 DIMM Memory

Two 288-pin DDR4 DIMM sockets are populated with single rank DIMMs capable of operating at data rates up to 2400 MegaTransfers per second (MT/s).

Table 6: **DDR4 Interfaces**

Alveo Card	Parameter	Description
A-U280-A32G-DEV-G A-U280-P32G-PQ-G	Manufacturer	Micron
	Part Number	MTA18ASF2G72PZ-2G3B1
	Description	16 GB 288-pin DDR4 RDIMM
		Configuration: 2 Gb x 72
		Single rank
		Supports ECC error detection and correction
		Supports 2400 MT/s

The detailed FPGA and DIMM pin connections are documented in the Alveo U280 accelerator card XDC file found in the **Getting Started** tab of the respective Alveo card landing page:

- Alveo U200 Product Page
- Alveo U250 Product Page

For more details about the Micron DDR4 DIMM, see the Micron MTA18ASF2G72PZ-2G3B1IG data sheet at the Micron website: http://www.micron.com.

HBM Memory

This device contains two 4 GB high-bandwidth memory (HBM) stacks for a total of 8 GB HBM memory. There are 32 AXI interfaces along with an internal switch that provides access to the 8 GB memory space. For detailed information, refer to the *AXI High Bandwidth Controller LogiCORE IP Product Guide* (PG276). The extensive connections between the device and HBM stacks help with floorplanning and timing closure.

***Note*:** When creating a design for this card, it is necessary to drive the CATTRIP pin listed in the following table. This pin is monitored by the card's satellite controller (SC) and represents the HBM_CATTRIP (HBM catastrophic temperature failure). When instantiating the HBM IP in your design, the two HBM IP signals, DRAM_0_STAT_CATTRIP and DRAM_1_STAT_CATTRIP, must be ORed together and connected to this pin for proper card operation. If the pin is undefined it will be pulled High by the card causing the SC to infer a CATTRIP failure and shut power down to the card.

If you do not use the HBM IP in your design, you must drive the pin Low to avoid the SC shutting down the card. If the pin is undefined and the QSPI is programmed with the MCS file, there is a potential chance that the card will continuously power down and reset after the bitstream is loaded. This can result in the card becoming unusable.

Table 7: **HBM CATTRIP Pin Connection**

Signal Name	Direction	Bank	I/O Reference	Pin	Description
HBM_CATTRIP_LS	Output	75	IO_L17P_T2U_N8_AD10P_75_D32	D32	Catastrophic temperature indicator to the SC (Active-High)

Quad SPI Flash Memory

The Quad SPI device provides 1 Gb of nonvolatile storage.

- Supply voltage: 1.8V
- Datapath width: 4 bits

For flash memory details, see the Micron data sheet at the Micron website.

For configuration details, see the *UltraScale Architecture Configuration User Guide* (UG570). The detailed FPGA and Flash pin connections for the feature described in this section are documented in the Alveo U280 accelerator card XDC file found in the **Getting Started** tab of the Alveo U280 Product Page.

FT4232HQ USB-JTAG/UART Interface

The USB connector for debug and development is located on the rear of the card and requires a micro-AB USB connection cable. The USB is connected to a FTDI FT4232HQ device, which has the following connectivity:

- ADBUS → JTAG connection to the UltraScale+ device JTAG through a level shifter that can be disabled by the satellite controller to prevent user tampering.

  ***Note*:** This port is also connected to the satellite controller through a level shifter that can be disabled by the satellite controller to prevent user tampering.

- ACBUS → RS232 serial port connection to the satellite controller.
  - Port connection needs to be configured for no parity, 8 data bits, 1 stop bit with a line rate of 115200.
- ABBUS → RS232 serial port connection to the UltraScale+ device.
  - Port connection needs to be configured by user and UltraScale+ device design.
  - USB_UART_TX connects to IO_L24N_T3U_N11_75 (pin A28) on the UltraScale+ device.
  - USB_UART_RX connects to IO_T3U_N12_75 (pin B33) on the UltraScale+ device.

The FTDI FT4232HQ data sheet is available on the FTDI website: https://www.ftdichip.com/.

PCI Express Endpoint

The Alveo U280 accelerator card implements a 16-lane PCI Express® edge connector that performs data transfers at the rate of 2.5 giga-transfers per second (GT/s) for Gen1, 5.0 GT/s for Gen2, 8.0 GT/s for Gen3 applications, and 16.0 GT/s for Gen4 applications.

The detailed UltraScale+ device and PCIe pin connections for the feature described in this section are documented in the accelerator card design constraints (XDC) file. The endpoint is compliant to the v3.0 specification, and compatible with the specification. For additional information about Gen4 compatible features, see *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213).

QSFP28 Module Connector

The Alveo accelerator cards host two 4-lane small form-factor pluggable (QSFP) connectors that accept an array of optical modules and copper cables. Each connector is housed within a single QSFP cage assembly. Note QSFP1 is port 1, the upper port located on the PCIe bracket and QSFP0 is port 2, the lower port located on the PCIe bracket, closest to the PCIe card edge fingers.

Refer to the section for the FPGA clock sources. The detailed device and QSFP pin connections for the feature described in this section are documented in the XDC file found in the **Getting Started** tab of the Alveo U280 Product Page.

The QSFP+ connectors sideband control signals (MODSELL, RESETL, MODPRSL, INTL, and LPMODE) are behind an I2C expander and are not accessible from the UltraScale+ device. The QSFP+ I2C interface and sideband control signals on the Alveo U280 accelerator card are only accessible through the satellite controller, and are currently not supported with the exception that the satellite controller does actively drive the LPMODE signal low so that an optical module is enabled when inserted. The MODSELL, RESETL, MODPRSL, INTL, and LPMODE sideband signals are defined in the following small form factor (SFF) specifications.

For additional information about the quad SFF pluggable (28 Gb/s QSFP+) module, see the SFF-8663 and SFF-8679 specifications for the 28 Gb/s QSFP+ at the SNIA Technology Affiliates website: https://www.snia.org/sff/specifications2.

QSFP0

The QSFP0 interface has the high-speed connections to the UltraScale+ device listed in the following table.

Table 8: **QSFP0 Interface High-Speed Connections**

Signal Name	Direction	Bank	I/O Reference	Pin	Description
MGT_SI570_CLOCK0_C_N	Input	134	MGTREFCLK0N_134	T43	REFCLK0 Negative LVDS Signal
MGT_SI570_CLOCK0_C_P	Input	134	MGTREFCLK0P_134	T42	REFCLK0 Positive LVDS Signal
QSFP0_CLOCK_N	Input	134	MGTREFCLK1N_134	R41	REFCLK1 Negative LVDS Signal
QSFP0_CLOCK_P	Input	134	MGTREFCLK1P_134	R40	REFCLK1 Positive LVDS Signal
QSFP0_RX1_N	Input	134	MGTYRXN0_134	L54	Negative Receive Lane 1 Input
QSFP0_RX2_N	Input	134	MGTYRXN1_134	K52	Negative Receive Lane 2 Input
QSFP0_RX3_N	Input	134	MGTYRXN2_134	J54	Negative Receive Lane 3 Input

Table 8: **QSFP0 Interface High-Speed Connections** *(cont'd)*

Signal Name	Direction	Bank	I/O Reference	Pin	Description
QSFP0_RX4_N	Input	134	MGTYRXN3_134	H52	Negative Receive Lane 4 Input
QSFP0_RX1_P		134	MGTYRXP0_134	L53	Positive Receive Lane 1 Input
QSFP0_RX2_P	Input	134	MGTYRXP1_134	K51	Positive Receive Lane 2 Input
QSFP0_RX3_P	Input	134	MGTYRXP2_134	J53	Positive Receive Lane 3 Input
QSFP0_RX4_P	Input	134	MGTYRXP3_134	H51	Positive Receive Lane 4 Input
QSFP0_TX1_N	Output	134	MGTYTXN0_134	L49	Negative Transmit Lane 1 Output
QSFP0_TX2_N	Output	134	MGTYTXN1_134	L45	Negative Transmit Lane 2 Output
QSFP0_TX3_N	Output	134	MGTYTXN2_134	K47	Negative Transmit Lane 3 Output
QSFP0_TX4_N	Output	134	MGTYTXN3_134	J49	Negative Transmit Lane 4 Output
QSFP0_TX1_P	Output	134	MGTYTXP0_134	L48	Positive Transmit Lane 1 Output
QSFP0_TX2_P	Output	134	MGTYTXP1_134	L44	Positive Transmit Lane 2 Output
QSFP0_TX3_P	Output	134	MGTYTXP2_134	K46	Positive Transmit Lane 3 Output
QSFP0_TX4_P	Output	134	MGTYTXP3_134	J48	Positive Transmit Lane 4 Output

QSFP1

The QSFP1 interface has the high-speed connections to the UltraScale+ device listed in the following table.

Table 9: **QSFP1 Interface High-Speed Connections**

Signal Name	Direction	Bank	I/O Reference	Pin	Description
MGT_SI570_CLOCK1_C_N	Input	135	MGTREFCLK0N_135	P43	REFCLK0 Negative LVDS Signal
MGT_SI570_CLOCK1_C_P	Input	135	MGTREFCLK0P_135	P42	REFCLK0 Positive LVDS Signal
QSFP1_CLOCK_N	Input	135	MGTREFCLK1N_135	M43	REFCLK1 Negative LVDS Signal
QSFP1_CLOCK_P	Input	135	MGTREFCLK1P_135	M42	REFCLK1 Positive LVDS Signal
QSFP1_RX1_N	Input	135	MGTYRXN0_135	G54	Negative Receive Lane 1 Input
QSFP1_RX2_N	Input	135	MGTYRXN1_135	F52	Negative Receive Lane 2 Input

Table 9: **QSFP1 Interface High-Speed Connections** *(cont'd)*

Signal Name	Direction	Bank	I/O Reference	Pin	Description
QSFP1_RX3_N	Input	135	MGTYRXN2_135	E54	Negative Receive Lane 3 Input
QSFP1_RX4_N		135	MGTYRXN3_135	D52	Negative Receive Lane 4 Input
QSFP1_RX1_P	Input	135	MGTYRXP0_135	G53	Positive Receive Lane 1 Input
QSFP1_RX2_P	Input	135	MGTYRXP1_135	F51	Positive Receive Lane 2 Input
QSFP1_RX3_P		135	MGTYRXP2_135	E53	Positive Receive Lane 3 Input
QSFP1_RX4_P	Input	135	MGTYRXP3_135	D51	Positive Receive Lane 4 Input
QSFP1_TX1_N	Output	135	MGTYTXN0_135	G49	Negative Transmit Lane 1 Output
QSFP1_TX2_N	Output	135	MGTYTXN1_135	E49	Negative Transmit Lane 2 Input
QSFP1_TX3_N	Output	135	MGTYTXN2_135	C49	Negative Transmit Lane 3 Input
QSFP1_TX4_N	Output	135	MGTYTXN3_135	A50	Negative Transmit Lane 4 Input
QSFP1_TX1_P	Output	135	MGTYTXP0_135	G48	Positive Transmit Lane 1 Input
QSFP1_TX2_P		135	MGTYTXP1_135	E48	Positive Transmit Lane 2 Input
QSFP1_TX3_P	Output	135	MGTYTXP2_135	C48	Positive Transmit Lane 3 Input
QSFP1_TX4_P	Output	135	MGTYTXP3_135	A49	Positive Transmit Lane 4 Input

I2C Bus

The Alveo U280 accelerator cards support the SMBus/I2C interface for out-of-band card management. The server Board Management Controller will communicate using SMBus to the satellite controller over the PCIe edge connector. For more information on out-band-card management, see Alveo Card Out-of-Band Management Specification for Server BMC.

Status LEDs

The Alveo card is designed to operate with the passive heat sink enclosure cover installed. LEDs DS1, DS2, DS3, and DS5 are visible through a cutout in the PCIe end bracket. The following table defines the card status LEDs.

Table 10: **Card Status LEDs**

Reference Designator	Description
DS1	BLUE: DONE When illuminated, the FPGA is successfully programmed.
DS2	RED: POWER_GOOD When illuminated solid red, power to the card is not within specification. During power ON, the LED might blink, which is expected behavior.
DS3	Not present
DS4	YELLOW: STATUS_LED0 (not defined)
DS5	GREEN: STATUS_LED2 (not defined)

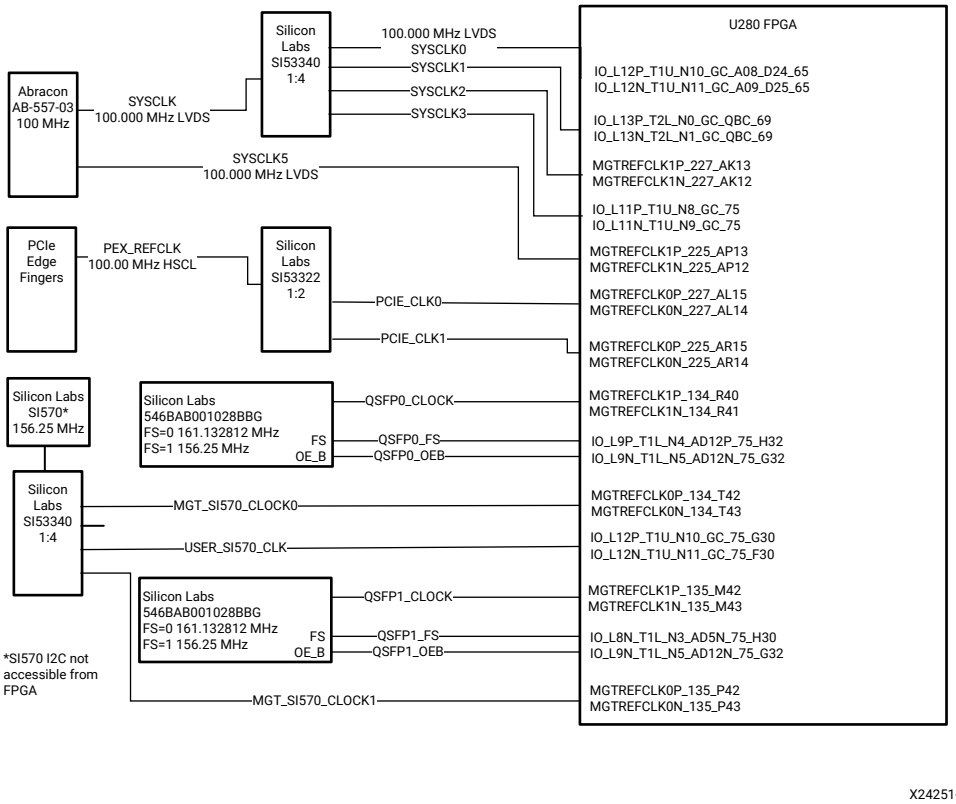
Card Power System

Limited power system telemetry is available through the card management system (CMS) I2C IP. See *Card Management Solution Subsystem Product Guide* (PG348) for information on how the I2C IP is instantiated in the UltraScale+ IP integrator flow. See Design Flows for more information.

Clocks

The following figure shows the clocks generated and connected to the FPGA. The detailed FPGA, clock pin connections, and frequencies for the feature described in this section are further documented in the U280 accelerator card XDC file.

Figure 4: **Alveo U280 Clocking**



Miscellaneous I/O

On the U280 card, the UltraScale+ device has a single bank with various inputs and outputs to communicate with the satellite controller and other devices on the card. See the XDC file for all of the signal connections. This section only references the signals that are usable in bank 75. Bank 75 is powered from a 1.8V source.

IMPORTANT! *The D32 pin must be connected appropriately or tied to logic 0. If D32 is pulled up, floated, or tied to 1, the U280 card might become unrecoverable after programming.*

Table 11: **Bank 75 SLR2 Miscellaneous I/O Descriptions**

Signal Name	Direction	Pin	I/O	Description
FPGA_RXD_MSP	Input	E28	IO_L18P_T2U_N10_AD2P_75	Satellite controller CMS UART receive (115200, no parity, 8 bits, 1 stop bit).
FPGA_TXD_MSP	Output	D29	IO_L18N_T2U_N11_AD2N_75	Satellite controller CMS UART transmit (115200, no parity, 8 bits, 1 stop bit).

Table 11: **Bank 75 SLR2 Miscellaneous I/O Descriptions** *(cont'd)*

Signal Name	Direction	Pin	I/O	Description
I2C_FPGA_SDA	Bi Dir	C33	IO_T2U_N12_75	Slave I2C data connection from satellite controller to FPGA.
I2C_FPGA_SCL	Bi Dir	C30	IO_L19P_T3L_N0_DBC_AD9P_75	Slave I2C clock connection from satellite controller to FPGA.
I2C_MAIN_INT_B	Output	B31	IO_L19N_T3L_N1_DBC_AD9N_75	Slave I2C active-Low system interrupt output from FPGA to satellite controller.
I2C_MUX0_INTB_FPGA	Input	D31	IO_L16N_T2U_N7_QBC_AD3N_75	Slave I2C active-Low interrupt output from FPGA to satellite controller.
PEX_PWRBRKN	Input	C32	IO_L17N_T2U_N9_AD10N_75	PEX_PWRBRKN active-Low input from PCIe connector signaling PCIe card to shut down card power in server failing condition.
PCIE_PERST	Input	BH26	IO_L13P_T2L_N0_GC_QBC_67	PCIe_PERSTN active-Low input from PCIe connector to FPGA to detect presence.
HBM_CATTRIP	Output	D32	IO_L17P_T2U_N8_AD10P_75	HBM_CATTRIP active-High indicator to satellite controller to indicate the HBM has exceeded its maximum allowable temperature. This signal is not a dedicated FPGA output and is a derived signal in RTL. Making this signal active shuts off the FPGA power rails.
DDR4_RESET_GATE	Output	H33	IO_L7P_T1L_N0_QBC_AD13P_75	DDR4_RESET_GATE active-High output from FPGA to hold all external DDR4 interfaces in self-refresh. This output disconnects the memory interface reset and holds it in active and pulls the clock enable signal on the memory interfaces.
USER_SI570_CLOCK_P	Input	G30	IO_L12P_T1U_N10_GC_75	General purpose LVDS 156.250 MHz clock input from SI570 programmable clock. The I2C interface is not accessible from the UltraScale+ device.
USER_SI570_CLOCK_N	Input	F30	IO_L12N_T1U_N11_GC_75	General purpose LVDS 156.250 MHz clock input from SI570 programmable clock. The I2C interface is not accessible from the UltraScale+ device.
SYS_CLK3_P	Input	G31	IO_L11P_T1U_N8_GC_75	General purpose LVDS 100.000 MHz clock reference derived from an onboard free running oscillator.
SYS_CLK3_N	Input	F31	IO_L11N_T1U_N9_GC_75	General purpose LVDS 100.000 MHz clock reference derived from an onboard free running oscillator.

Chapter 6

Known Issues and Limitations

Refer to Answer Record 71752 for known issues with Alveo data center accelerator cards. For card installation support, debugging information, and known issues, see the *Alveo Card Debug Guide* (XD027). For Technical Support, open a Support Service Request.

Appendix A

Additional Resources and Legal Notices

Finding Additional Documentation

Documentation Portal

The AMD Adaptive Computing Documentation Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Documentation Portal, go to https://docs.xilinx.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help → Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the Design Hubs webpage.

***Note*:** For more information on DocNav, see the Documentation Navigator webpage.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

These documents provide supplemental material useful with this guide:

Product Websites

The most up-to-date information related to the AMD Alveo™ U280 card and documentation is available on the Alveo U280 Data Center Accelerator Card.

Supplemental Documents

The following AMD document provide supplemental material useful with this guide.

- *Alveo U280 Data Center Accelerator Cards Data Sheet* (DS963)
- *Vitis Unified Software Platform Documentation* (UG1416)
- *UltraFast Design Methodology Guide for FPGAs and SoCs* (UG949)
- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Getting Started with Alveo Data Center Accelerator Cards* (UG1301)
- *Alveo Data Center Accelerator Card Platforms User Guide* (UG1120)
- *UltraScale Architecture Configuration User Guide* (UG570)
- *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
- *AXI High Bandwidth Controller LogiCORE IP Product Guide* (PG276)
- *UltraScale+ Devices Integrated Block for PCI Express LogiCORE IP Product Guide* (PG213)
- *Card Management Solution Subsystem Product Guide* (PG348)
- *Alveo Card Debug Guide* (XD027)

Additional Links

The following links provide supplemental material useful with this guide.

- Xilinx, Inc: https://www.xilinx.com
- Answer Record 71757
- Answer Record 71752

- Micron Technology: http://www.micron.com

  (MTA18ASF2G72PZ-2G3B1IG, MT25QU01GBB8E12-OAAT)
- *Si53322 Data Sheet*: https://www.silabs.com/documents/public/data-sheets/si5332x-datasheet.pdf
- *AB-557-03 Data Sheet*: https://abracon.com/Oscillators/AB-557-03.pdf
- *Si546 Data Sheet*: https://www.silabs.com/documents/public/data-sheets/si546-datasheet.pdf
- Future Technology Devices International, Ltd.: http://www.ftdichip.com

  (FT4232HQ)
- QSFP+ module: https://members.snia.org/document/dl/25969

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
06/15/2023 Version 1.1	
MCS File Generation and Alveo Card Programming	• Added step to address configuration of the memory device. • Corrected write_cfgmem Parameter Settings size.
05/05/2023 Version 1.0	
Initial release.	N/A

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